

To our customers,

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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**Phase-out/Discontinued**

**384-OUTPUT TFT-LCD SOURCE DRIVER  
(COMPATIBLE WITH 256-GRAY SCALES)**

The  $\mu$  PD16740 is a source driver for TFT-LCDs capable of dealing with displays with 256 gray scales. Data input is based on digital input configured as 8 bits by 6 dots (2 pixels), which can realize a full-color display of 16,700,000 colors by output of 256 values  $\gamma$ -corrected by an internal D/A converter and 11 external power modules. Because the output dynamic range is as large as  $V_{SS2} + 0.1\text{ V}$  to  $V_{ref} - 0.1\text{ V}$ , level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 8-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. The D/A converter, which incorporates a digital offset circuit, is suitable for an LCD panel in which liquid crystal transmittance in positive and negative polarities is different. Assuring a maximum clock frequency of 40 MHz when driving at 3.0 V, this driver is applicable to SXGA and XGA-standard TFT-LCD panels.

**FEATURES**

- CMOS level input
- 384-output channel
- Input of 8 bits (gradation data) by 6 dots
- Capable of outputting 256 values by means of 11 external power modules and a D/A converter (C-DAC)
- Logic Part Power Supply Voltage ( $V_{DD1}$ ) :  $3.3 \pm 0.3\text{ V}$
- Driver Part Power Supply Voltage ( $V_{DD2}$ ) :  $8.5 \pm 0.5\text{ V}$
- High-speed data transfer:  $f_{MAX.} = 40\text{ MHz}$  (internal data transfer speed when operating at  $V_{DD1} = 3.0\text{ V}$ )
- Output dynamic range  $V_{SS2} + 0.1\text{ V}$  to  $V_{ref} - 0.1\text{ V}$
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity reverse is possible (POLA)
- Input data reverse function is incorporated (POLB)

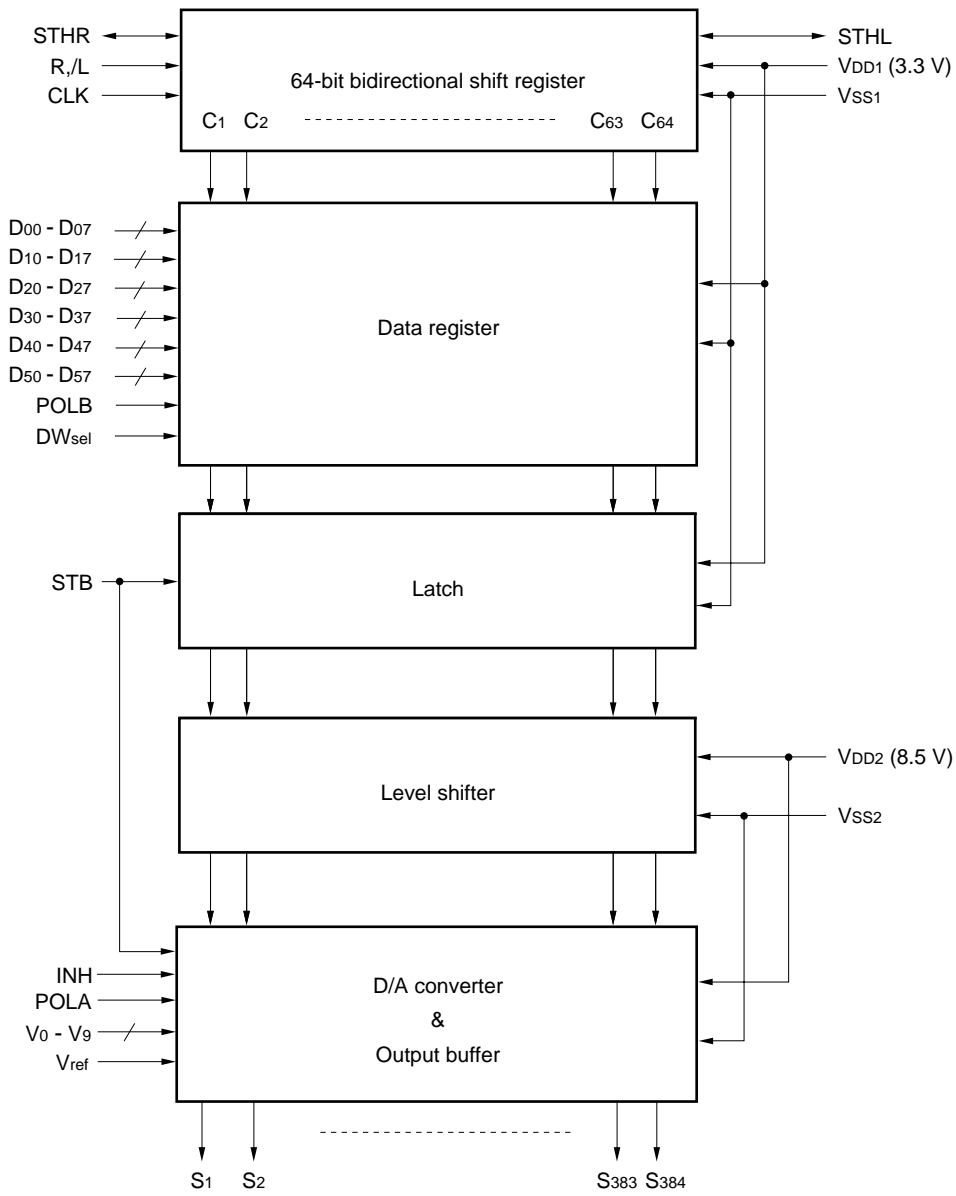
**ORDERING INFORMATION**

Part Number	Package
$\mu$ PD16740N-xxx	TCP (TAB package)

**Remark** The TCP's external shape is custom-order item. Users are requested to consult with a NEC sales representative.

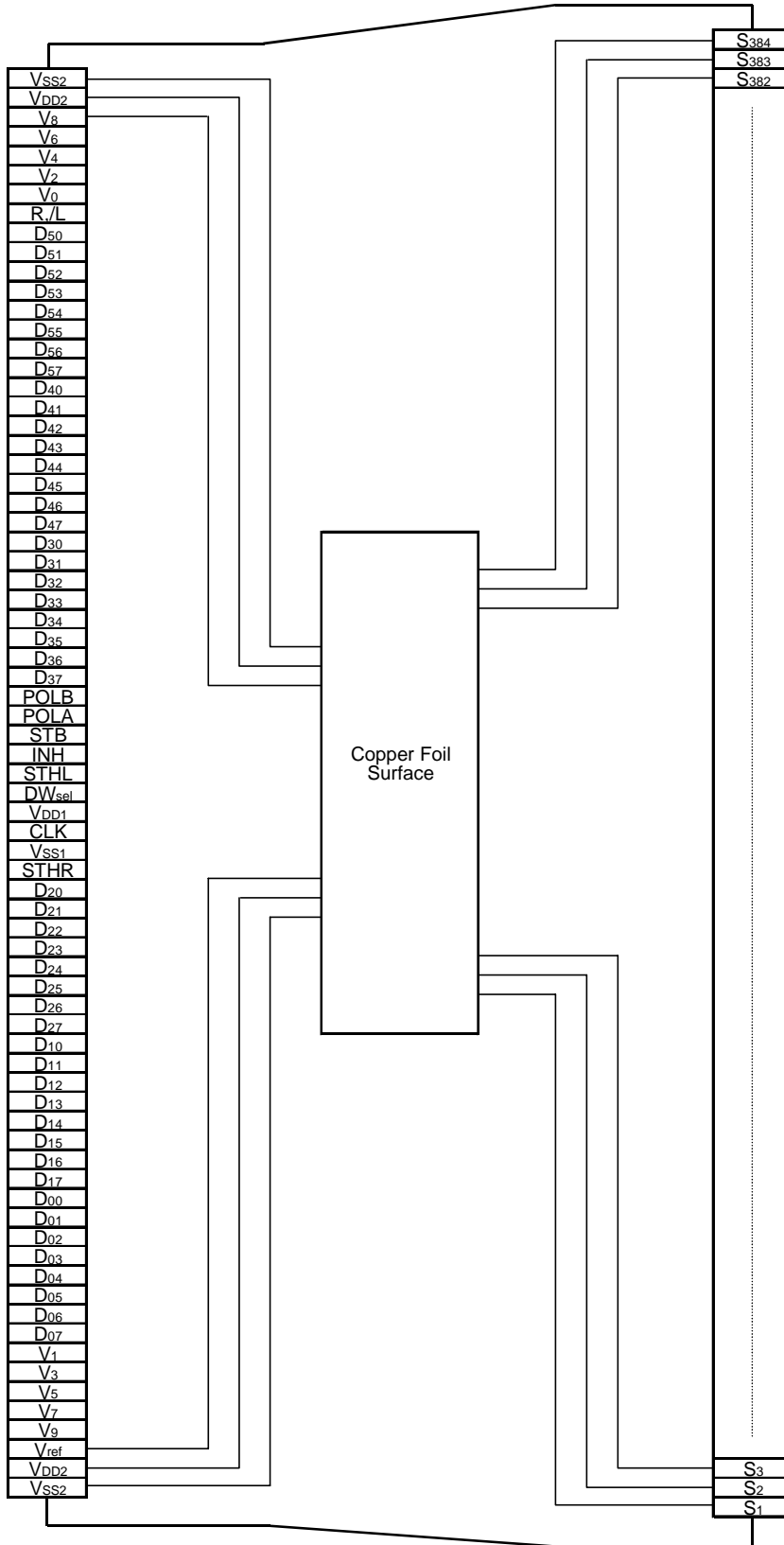
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1. BLOCK DIAGRAM



**Remark** /xxx indicates active low signal.

2. PIN CONFIGURATION (μ PD16740N-xxx)



**Remark** This figure does not specify the TCP package.

3. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S <sub>1</sub> to S <sub>384</sub>	Driver output	The D/A converted 64/256-gray-scale analog voltage is output.
D <sub>00</sub> to D <sub>07</sub>	Display data	The display data is input in either a 48-bit width of 8-bit gray-scale data × 6 dots (2 pixels) or in a 36-bit width of 6-bit gray-scale data × 6 dots (2 pixels). In 8-bit input: D <sub>x7</sub> : MSB, D <sub>x0</sub> : LSB In 6-bit input: D <sub>x7</sub> : MSB, D <sub>x2</sub> : LSB In 6-bit input (DW <sub>sel</sub> = L), the D <sub>n0</sub> and D <sub>n1</sub> pins are fixed to low in the IC. Therefore, be sure to leave them open on TCP.
D <sub>10</sub> to D <sub>17</sub>		
D <sub>20</sub> to D <sub>27</sub>		
D <sub>30</sub> to D <sub>37</sub>		
D <sub>40</sub> to D <sub>47</sub>		
D <sub>50</sub> to D <sub>57</sub>		
DW <sub>sel</sub>	6-/8-bit input control	This pin switches the bit width of the display data between 6 bits and 8 bits. DW <sub>sel</sub> = H: 8-bit input DW <sub>sel</sub> = L: 6-bit input This pin is pulled down internally.
R <sub>/</sub> L	Shift direction control input	These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R <sub>/</sub> L = H(Right shift) : STHR (input) → S <sub>1</sub> → S <sub>384</sub> → STHL (output) R <sub>/</sub> L = L (Left shift) : STHL (input) → S <sub>384</sub> → S <sub>1</sub> → STHR (output)
STHR	Right shift start pulse input/output	Start pulse I/O pin at cascade connection. The display data is acquired when the high level is read at the rising edge of CLK. Right shift : STHR is input. STHL is output. Left shift : STHL is input. STHR is output.
STHL	Left shift start pulse input/output	
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. Start pulse high level is read at rising edge of CLK, start to load the display data from next rising edge of CLK. Also, after start pulse input and CLK input 66 pulses, it stops to load the display data and it makes contents of shift register clear at rising edge of STB.
STB	Latch input	After the contents of data register is transferred to a latch at a rising edge and is cleared, operation of analog output voltage for output voltage is started.
INH	Inhibit input	At the falling edge complete calculation of analog output voltage, and output the voltage appointed by display data.
POLA	Polarity input	This signal is read at the rising edge of latch signal and determines the output voltage polarity to reference voltage of each output pin. POLA = L : Pins with even number are negative output. Pins with odd number are positive output. POLA = H : Pins with even number are positive output. Pins with odd number are negative output.
POLB	Data inversion	By inputting a switching signal to this pin, this pin enables the data whose polarity is reversed to be read. POLB = H : Acquires with displayed data reversed POLB = L : Acquires raw displayed data
V <sub>ref</sub>	Reference power supply	This terminal is the input reference power supply need to calculation output. Please refer to <b>4. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE.</b>
V <sub>0</sub> to V <sub>9</sub>	γ-corrected power supplies	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. $V_{ref} - 0.1\text{ V} \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_6 \geq V_7 \geq V_8 \geq V_9 \geq V_{SS2} + 0.1\text{ V}$ $V_{ref} - 0.1\text{ V} \geq V_9 \geq V_8 \geq V_7 \geq V_6 \geq V_5 \geq V_4 \geq V_3 \geq V_2 \geq V_1 \geq V_0 \geq V_{SS2} + 0.1\text{ V}$ During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level.
V <sub>DD1</sub>	Logic power supply	3.3 V ± 0.3 V
V <sub>DD2</sub>	Driver power supply	8.5 V ± 0.5 V
V <sub>SS1</sub>	Logic ground	Grounding
V <sub>SS2</sub>	Driver ground	Grounding

- Cautions**
1. The power start sequence must be  $V_{DD1} \rightarrow$  logic input  $\rightarrow V_{DD2} \rightarrow V_{ref} \rightarrow V_0$  to  $V_9$  in that order. Reverse this sequence to shut down. Be sure to observe this power sequence even during a transition period.
  2. To stabilize the supply voltage, please be sure to insert each  $0.1 \mu F$ ,  $0.47 \mu F$  bypass capacitor between  $V_{DD1}$ - $V_{SS1}$  and  $V_{DD2}$ - $V_{SS2}$ . Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about  $0.01 \mu F$  is also advised between the  $\gamma$ -corrected power supply terminals ( $V_0, V_1, V_2, \dots, V_9$ ) and  $V_{SS2}$ .
  3. This IC employs the C-DAC circuit to control gray-scale generation. The  $\gamma$ -corrected voltage is sampled between the rising of the STB signal and the rising of the INH signal, and the  $\gamma$ -corrected voltage is output from the driver output pin two or three clocks after the INH signal falls. That is, each gray-scale voltage is determined by sampling  $\gamma$ -corrected voltage. At this time, a large transient current flows instantly into the  $\gamma$ -corrected power supply pin. Therefore, when inputting  $\gamma$ -corrected voltage and  $\gamma$ -corrected reference voltage, an operational amplifier is recommended to reduce the input impedance of this pin. In addition to this, the voltage to be input to this pin needs to be stabilized.  
When a switching signal with high frequency is input to the  $\gamma$ -corrected power supply pin, the application voltage becomes unstable and display may be abnormal. For details of the output timing, refer to 9. SWITCHING CHARACTERISTICS WAVEFORM.
  4. When this product is used as a 6-bit driver ( $DWsel = L$ ), the wiring for the  $D_{n1}$  and  $D_{n2}$  (lower 2 bits of display data) pins must be left open on the TCP, since they are forcibly short-circuited to  $V_{SS1}$  in the IC.

**4. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE**

**4.1 Calculation of output voltage in 8-bit input**

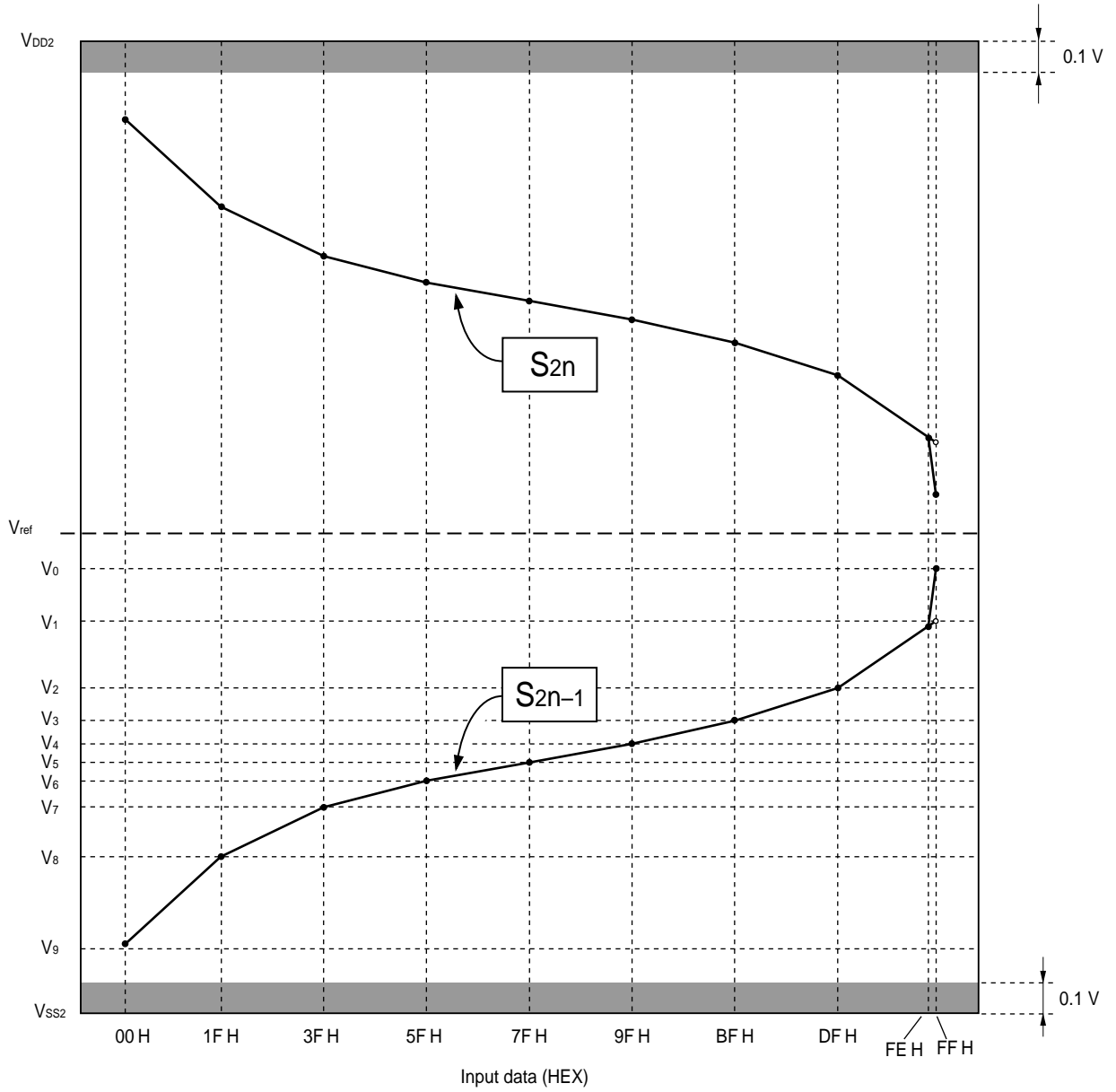
$$(DW_{sel} = H, V_{ref} - 0.1 V \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_6 \geq V_7 \geq V_8 \geq V_9 \geq V_{SS2} + 0.1 V)$$

Gray Scale	Binary	Input Data								Output Voltage	
		Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	S <sub>2n-1</sub> (POLA=H), S <sub>2n</sub> (POLA=L)	S <sub>2n</sub> (POLA=H),S <sub>2n-1</sub> (POLA=L)
0	00H	0	0	0	0	0	0	0	0	$2V_{ref} - \{V_8+(V_9 - V_8) \times 31/32\}$	$V_8+(V_9-V_8) \times 31/32$
1	01H	0	0	0	0	0	0	1	1	$2V_{ref} - \{V_8+(V_9 - V_8) \times 30/32\}$	$V_8+(V_9-V_8) \times 30/32$
⋮	⋮									⋮	⋮
30	1EH	0	0	0	1	1	1	1	0	$2V_{ref} - \{V_8+(V_9 - V_8) \times 1/32\}$	$V_8+(V_9-V_8) \times 1/32$
31	1FH	0	0	0	1	1	1	1	1	$2V_{ref} - V_8$	$V_8$
32	20H	0	0	1	0	0	0	0	0	$2V_{ref} - \{V_7+(V_8 - V_7) \times 31/32\}$	$V_7+(V_8-V_7) \times 31/32$
33	21H	0	0	1	0	0	0	1	1	$2V_{ref} - \{V_7+(V_8 - V_7) \times 30/32\}$	$V_7+(V_8-V_7) \times 30/32$
⋮	⋮									⋮	⋮
62	3EH	0	0	1	1	1	1	1	0	$2V_{ref} - \{V_7+(V_8 - V_7) \times 1/32\}$	$V_7+(V_8-V_7) \times 1/32$
63	3FH	0	0	1	1	1	1	1	1	$2V_{ref} - V_7$	$V_7$
64	40H	0	1	0	0	0	0	0	0	$2V_{ref} - \{V_6+(V_7 - V_6) \times 31/32\}$	$V_6+(V_7-V_6) \times 31/32$
65	41H	0	1	0	0	0	0	1	1	$2V_{ref} - \{V_6+(V_7 - V_6) \times 30/32\}$	$V_6+(V_7-V_6) \times 30/32$
⋮	⋮									⋮	⋮
94	5EH	0	1	0	1	1	1	1	0	$2V_{ref} - \{V_6+(V_7 - V_6) \times 1/32\}$	$V_6+(V_7-V_6) \times 1/32$
95	5FH	0	1	0	1	1	1	1	1	$2V_{ref} - V_6$	$V_6$
96	60H	0	1	1	0	0	0	0	0	$2V_{ref} - \{V_5+(V_6 - V_5) \times 31/32\}$	$V_5+(V_6-V_5) \times 31/32$
97	61H	0	1	1	0	0	0	1	1	$2V_{ref} - \{V_5+(V_6 - V_5) \times 30/32\}$	$V_5+(V_6-V_5) \times 30/32$
⋮	⋮									⋮	⋮
126	7EH	0	1	1	1	1	1	1	0	$2V_{ref} - \{V_5+(V_6 - V_5) \times 1/32\}$	$V_5+(V_6-V_5) \times 1/32$
127	7FH	0	1	1	1	1	1	1	1	$2V_{ref} - V_5$	$V_5$
128	80H	1	0	0	0	0	0	0	0	$2V_{ref} - \{V_4+(V_5 - V_4) \times 31/32\}$	$V_4+(V_5-V_4) \times 31/32$
129	81H	1	0	0	0	0	0	1	1	$2V_{ref} - \{V_4+(V_5 - V_4) \times 30/32\}$	$V_4+(V_5-V_4) \times 30/32$
⋮	⋮									⋮	⋮
158	9EH	1	0	0	1	1	1	1	0	$2V_{ref} - \{V_4+(V_5 - V_4) \times 1/32\}$	$V_4+(V_5-V_4) \times 1/32$
159	9FH	1	0	0	1	1	1	1	1	$2V_{ref} - V_4$	$V_4$
160	A0H	1	0	1	0	0	0	0	0	$2V_{ref} - \{V_3+(V_4 - V_3) \times 31/32\}$	$V_3+(V_4-V_3) \times 31/32$
161	A1H	1	0	1	0	0	0	1	1	$2V_{ref} - \{V_3+(V_4 - V_3) \times 30/32\}$	$V_3+(V_4-V_3) \times 30/32$
⋮	⋮									⋮	⋮
190	BEH	1	0	1	1	1	1	1	0	$2V_{ref} - \{V_3+(V_4 - V_3) \times 1/32\}$	$V_3+(V_4-V_3) \times 1/32$
191	BFH	1	0	1	1	1	1	1	1	$2V_{ref} - V_3$	$V_3$
192	C0H	1	1	0	0	0	0	0	0	$2V_{ref} - \{V_2+(V_3 - V_2) \times 31/32\}$	$V_2+(V_3-V_2) \times 31/32$
193	C1H	1	1	0	0	0	0	1	1	$2V_{ref} - \{V_2+(V_3 - V_2) \times 30/32\}$	$V_2+(V_3-V_2) \times 30/32$
⋮	⋮									⋮	⋮
222	DEH	1	1	0	1	1	1	1	0	$2V_{ref} - \{V_2+(V_3 - V_2) \times 1/32\}$	$V_2+(V_3-V_2) \times 1/32$
223	DFH	1	1	0	1	1	1	1	1	$2V_{ref} - V_2$	$V_2$
224	E0H	1	1	1	0	0	0	0	0	$2V_{ref} - \{V_1+(V_2 - V_1) \times 31/32\}$	$V_1+(V_2-V_1) \times 31/32$
225	E1H	1	1	1	0	0	0	1	1	$2V_{ref} - \{V_1+(V_2 - V_1) \times 30/32\}$	$V_1+(V_2-V_1) \times 30/32$
⋮	⋮									⋮	⋮
254	FEH	1	1	1	1	1	1	1	0	$2V_{ref} - \{V_1+(V_2 - V_1) \times 1/32\}$	$V_1+(V_2-V_1) \times 1/32$
255	FFH	1	1	1	1	1	1	1	1	$2V_{ref} - V_1$	$V_1$



**4.2 Curved line of output voltage in 8-bit input**

( $DW_{sel} = H, POLA = H, V_{ref} - 0.1 V \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_6 \geq V_7 \geq V_8 \geq V_9 \geq V_{SS2} + 0.1 V$ )



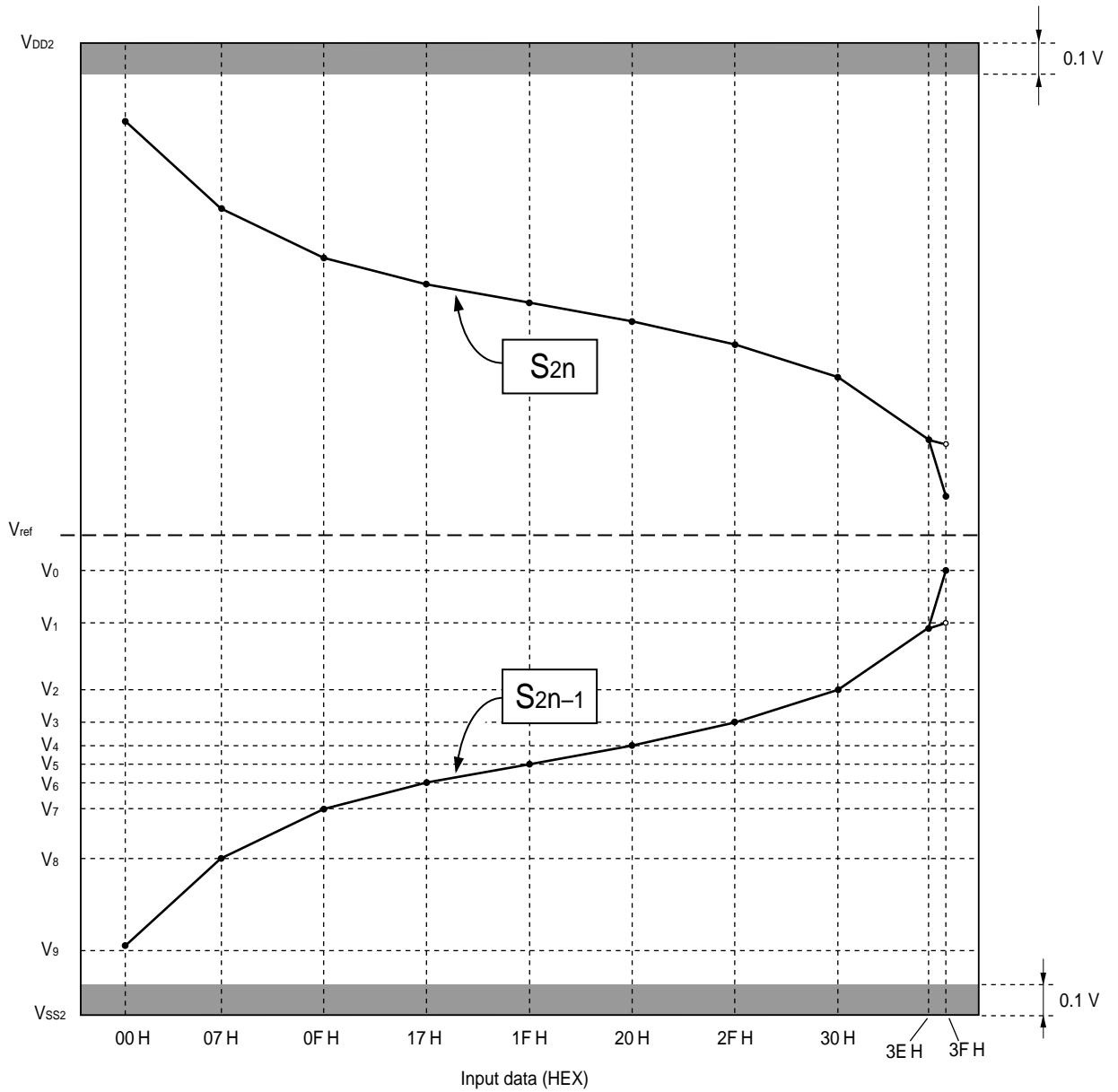
**4.3 Calculation of output voltage in 6-bit input**

( $DW_{sel} = L, V_{ref} - 0.1 V \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_6 \geq V_7 \geq V_8 \geq V_9 \geq V_{SS2} + 0.1 V$ )

Gray Scale	Binary	Input Data								Output Voltage	
		D <sub>X7</sub>	D <sub>X6</sub>	D <sub>X5</sub>	D <sub>X4</sub>	D <sub>X3</sub>	D <sub>X2</sub>	D <sub>X1</sub>	D <sub>X0</sub>	S <sub>2n-1</sub> (POLA=H), S <sub>2n</sub> (POLA=L)	S <sub>2n</sub> (POLA=H),S <sub>2n-1</sub> (POLA=L)
0	00H	0	0	0	0	0	0	0	0	$2V_{ref} - \{V_8+(V_9 - V_8) \times 7/8\}$	$V_8+(V_9-V_8) \times 7/8$
1	01H	0	0	0	0	0	0	1	0	$2V_{ref} - \{V_8+(V_9 - V_8) \times 6/8\}$	$V_8+(V_9-V_8) \times 6/8$
⋮	⋮									⋮	⋮
6	06H	0	0	0	1	1	0	0	0	$2V_{ref} - \{V_8+(V_9 - V_8) \times 1/8\}$	$V_8+(V_9-V_8) \times 1/8$
7	07H	0	0	0	1	1	1	0	0	$2V_{ref} - V_8$	$V_8$
8	08H	0	0	1	0	0	0	0	0	$2V_{ref} - \{V_7+(V_8 - V_7) \times 7/8\}$	$V_7+(V_8-V_7) \times 7/8$
9	09H	0	0	1	0	0	0	1	0	$2V_{ref} - \{V_7+(V_8 - V_7) \times 6/8\}$	$V_7+(V_8-V_7) \times 6/8$
⋮	⋮									⋮	⋮
14	0EH	0	0	1	1	1	0	0	0	$2V_{ref} - \{V_7+(V_8 - V_7) \times 1/8\}$	$V_7+(V_8-V_7) \times 1/8$
15	0FH	0	0	1	1	1	1	0	0	$2V_{ref} - V_7$	$V_7$
16	10H	0	1	0	0	0	0	0	0	$2V_{ref} - \{V_6+(V_7 - V_6) \times 7/8\}$	$V_6+(V_7-V_6) \times 7/8$
17	11H	0	1	0	0	0	0	1	0	$2V_{ref} - \{V_6+(V_7 - V_6) \times 6/8\}$	$V_6+(V_7-V_6) \times 6/8$
⋮	⋮									⋮	⋮
22	16H	0	1	0	1	1	0	0	0	$2V_{ref} - \{V_6+(V_7 - V_6) \times 1/8\}$	$V_6+(V_7-V_6) \times 1/8$
23	17H	0	1	0	1	1	1	0	0	$2V_{ref} - V_6$	$V_6$
24	18H	0	1	1	0	0	0	0	0	$2V_{ref} - \{V_5+(V_6 - V_5) \times 7/8\}$	$V_5+(V_6-V_5) \times 7/8$
25	19H	0	1	1	0	0	0	1	0	$2V_{ref} - \{V_5+(V_6 - V_5) \times 6/8\}$	$V_5+(V_6-V_5) \times 6/8$
⋮	⋮									⋮	⋮
30	1EH	0	1	1	1	1	0	0	0	$2V_{ref} - \{V_5+(V_6 - V_5) \times 1/8\}$	$V_5+(V_6-V_5) \times 1/8$
31	1FH	0	1	1	1	1	1	0	0	$2V_{ref} - V_5$	$V_5$
32	20H	1	0	0	0	0	0	0	0	$2V_{ref} - \{V_4+(V_5 - V_4) \times 7/8\}$	$V_4+(V_5-V_4) \times 7/8$
33	21H	1	0	0	0	0	0	1	0	$2V_{ref} - \{V_4+(V_5 - V_4) \times 6/8\}$	$V_4+(V_5-V_4) \times 6/8$
⋮	⋮									⋮	⋮
38	26H	1	0	0	1	1	0	0	0	$2V_{ref} - \{V_4+(V_5 - V_4) \times 1/8\}$	$V_4+(V_5-V_4) \times 1/8$
39	27H	1	0	0	1	1	1	0	0	$2V_{ref} - V_4$	$V_4$
40	28H	1	0	1	0	0	0	0	0	$2V_{ref} - \{V_3+(V_4 - V_3) \times 7/8\}$	$V_3+(V_4-V_3) \times 7/8$
41	29H	1	0	1	0	0	0	1	0	$2V_{ref} - \{V_3+(V_4 - V_3) \times 6/8\}$	$V_3+(V_4-V_3) \times 6/8$
⋮	⋮									⋮	⋮
46	2EH	1	0	1	1	1	0	0	0	$2V_{ref} - \{V_3+(V_4 - V_3) \times 1/8\}$	$V_3+(V_4-V_3) \times 1/8$
47	2FH	1	0	1	1	1	1	0	0	$2V_{ref} - V_3$	$V_3$
48	30H	1	1	0	0	0	0	0	0	$2V_{ref} - \{V_2+(V_3 - V_2) \times 7/8\}$	$V_2+(V_3-V_2) \times 7/8$
49	31H	1	1	0	0	0	0	1	0	$2V_{ref} - \{V_2+(V_3 - V_2) \times 6/8\}$	$V_2+(V_3-V_2) \times 6/8$
⋮	⋮									⋮	⋮
54	36H	1	1	0	1	1	0	0	0	$2V_{ref} - \{V_2+(V_3 - V_2) \times 1/8\}$	$V_2+(V_3-V_2) \times 1/8$
55	37H	1	1	0	1	1	1	0	0	$2V_{ref} - V_2$	$V_2$
56	38H	1	1	1	0	0	0	0	0	$2V_{ref} - \{V_1+(V_2 - V_1) \times 7/8\}$	$V_1+(V_2-V_1) \times 7/8$
57	39H	1	1	1	0	0	0	1	0	$2V_{ref} - \{V_1+(V_2 - V_1) \times 6/8\}$	$V_1+(V_2-V_1) \times 6/8$
⋮	⋮									⋮	⋮
63	3EH	1	1	1	1	1	0	0	0	$2V_{ref} - \{V_1+(V_2 - V_1) \times 1/8\}$	$V_1+(V_2-V_1) \times 1/8$
64	3FH	1	1	1	1	1	1	0	0	$2V_{ref} - V_1$	$V_1$

**4.4 Curved line of output voltage in 6-bit input**

( $DW_{sel} = L, POLA = H, V_{ref} - 0.1\text{ V} \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_6 \geq V_7 \geq V_8 \geq V_9 \geq V_{SS2} + 0.1\text{ V}$ )



**5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN**

The reference power supply of the D/A converter is made up of a capacitance ladder circuit, which minimizes current flow into the  $\gamma$ -corrected power supply pins. However, in the LCD driver of previous R-DAC systems the resistance ratio between the  $\gamma$ -corrected power supply pins was set to be identical to the  $\gamma$ -corrected voltage ratio used for an actual LCD panel. Such a function is not available in this product. Therefore,  $\gamma$ -corrected voltage directly becomes D/A converter reference power voltage in the IC. Determine  $\gamma$ -corrected voltage based on the data of  $\gamma$  characteristics of a LCD panel described in **4. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE.**

**6. INPUT FORMAT OF DISPLAY DATA**

Data format : 8/6 bits × 2 RGBs (6 dots)  
 Input width : 48/36 bits (2-pixel data)

**(1) R,/L = H (Right shift)**

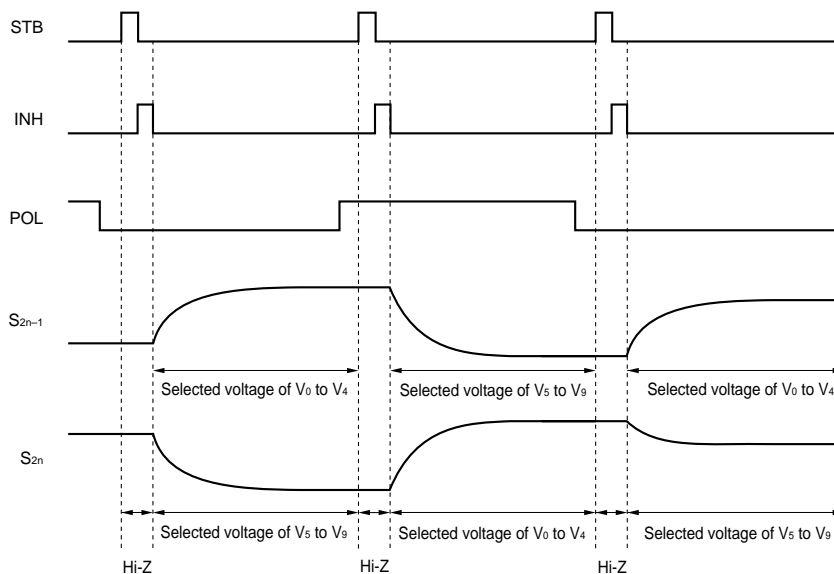
Output	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	...	S <sub>383</sub>	S <sub>384</sub>
Data	D <sub>00</sub> to D <sub>05/07</sub>	D <sub>10</sub> to D <sub>15/17</sub>	D <sub>20</sub> to D <sub>25/27</sub>	D <sub>30</sub> to D <sub>35/37</sub>	...	D <sub>40</sub> to D <sub>45/47</sub>	D <sub>50</sub> to D <sub>55/57</sub>

**(2) R,/L = L (Left shift)**

Output	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	...	S <sub>383</sub>	S <sub>384</sub>
Data	D <sub>00</sub> to D <sub>05/07</sub>	D <sub>10</sub> to D <sub>15/17</sub>	D <sub>20</sub> to D <sub>25/27</sub>	D <sub>30</sub> to D <sub>35/37</sub>	...	D <sub>40</sub> to D <sub>45/47</sub>	D <sub>50</sub> to D <sub>55/57</sub>

**7. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM**

The output buffer consists of an operational amplifier circuit that does not perform recharge operation. Therefore, driver output current I<sub>VOH</sub> is the charging current to the LCD, and I<sub>VOL</sub> is the discharging current.



**8. ELECTRICAL SPECIFICATIONS**

**Absolute Maximum Ratings (T<sub>A</sub> = +25°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Ratings	Unit
Logic Part Power Supply Voltage	V <sub>DD1</sub>	-0.5 to + 5.0	V
Driver Part power Supply Voltage	V <sub>DD2</sub>	-0.5 to + 10.0	V
Logic Part Input Voltage	V <sub>I1</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Driver Part Input Voltage	V <sub>I2</sub>	-0.5 to V <sub>DD2</sub> + 0.5	V
Logic Part Output Voltage	V <sub>O1</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Driver Part Output Voltage	V <sub>O2</sub>	-0.5 to V <sub>DD2</sub> + 0.5	V
Operating Temperature Range	T <sub>A</sub>	-10 to +75	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +125	°C

**Caution** If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

**Recommended Operating Range (T<sub>A</sub> = -10 to +75°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V <sub>DD1</sub>	3.0	3.3	3.6	V
Driver Part Supply Voltage	V <sub>DD2</sub>	8.0	8.5	9.0	V
Driver Part Output Voltage Range	V <sub>O</sub>	V <sub>SS2</sub> + 0.1		V <sub>DD2</sub> - 0.1	V
γ-Corrected Voltage	V <sub>0</sub> to V <sub>9</sub>	V <sub>SS2</sub> + 0.1		V <sub>ref</sub> - 0.1	V
γ-Corrected Reference Power Supply	V <sub>ref</sub>		0.5 V <sub>DD2</sub>	5.0	V
Maximum Clock Frequency	f <sub>MAX.</sub>	40			MHz

**Electrical Characteristics (T<sub>A</sub> = -10 to +75°C, V<sub>DD1</sub> = 3.3 V ± 0.3 V, V<sub>DD2</sub> = 8.5 V ± 0.5 V, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V <sub>IH</sub>	CLK,STB,R,/L,INH,POLA,POLB,	0.7 V <sub>DD2</sub>		V <sub>DD2</sub>	V
Low-level Input Voltage	V <sub>IL</sub>	D <sub>00</sub> to D <sub>07</sub> , D <sub>10</sub> to D <sub>17</sub> , D <sub>20</sub> to D <sub>27</sub> ,	V <sub>SS2</sub>		0.3 V <sub>DD2</sub>	V
Input Leak Current	I <sub>IL</sub>	D <sub>30</sub> to D <sub>37</sub> , D <sub>40</sub> to D <sub>47</sub> , D <sub>50</sub> to D <sub>57</sub>	-1.0		+1.0	μA
High-Level Output Voltage	V <sub>OH</sub>	STHR (STHL), I <sub>OH</sub> = -1.0 mA	V <sub>DD1</sub> - 0.5			V
Low-level Output Voltage	V <sub>OL</sub>	STHR (STHL), I <sub>OL</sub> = +1.0 mA			V <sub>SS1</sub> + 0.5	V
Driver Output Current (V <sub>DD2</sub> = 8.5 V)	I <sub>VOH</sub>	V <sub>DD1</sub> = 3.3 V, INH = 0 V, V <sub>OUT</sub> = 7.9 V, V <sub>O</sub> = 8.4 V <sup>Note</sup>		-90	-40	mA
	I <sub>VOL</sub>	V <sub>DD1</sub> = 3.3 V, INH = 0 V, V <sub>OUT</sub> = 0.6 V, V <sub>O</sub> = 0.1 V <sup>Note</sup>	40	90		mA
Output Voltage Deviation	ΔV <sub>O</sub>	V <sub>DD1</sub> = 3.3 V, V <sub>DD2</sub> = 8.5 V, V <sub>OUT</sub> = 0.5 / 3.0 / 5.0 / 8.0 V <sup>Note</sup>		±18	±25	mV
Logic Part Dynamic Current Consumption	I <sub>DD1</sub>	V <sub>DD1</sub> = 3.3 V, with no load		1.2	4.0	mA
Driver Part Dynamic Current Consumption	I <sub>DD2</sub>	V <sub>DD2</sub> = 8.5 V, with no load		4.0	12.0	mA

**Note** V<sub>OUT</sub> indicates application voltage to output pins. V<sub>O</sub> indicates output voltage to output pins.

**Caution** For logic part dynamic current consumption, the TYP. value is based on the condition while the screen is displayed in entirely dark or entirely light and the MAX. value is based on the condition while the screen is displayed in chess board pattern.

**Switching Characteristics (T<sub>A</sub> = -10 to +75°C, V<sub>DD1</sub> = 3.3 V ± 0.3 V, V<sub>DD2</sub> = 8.5 V ± 0.5 V, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

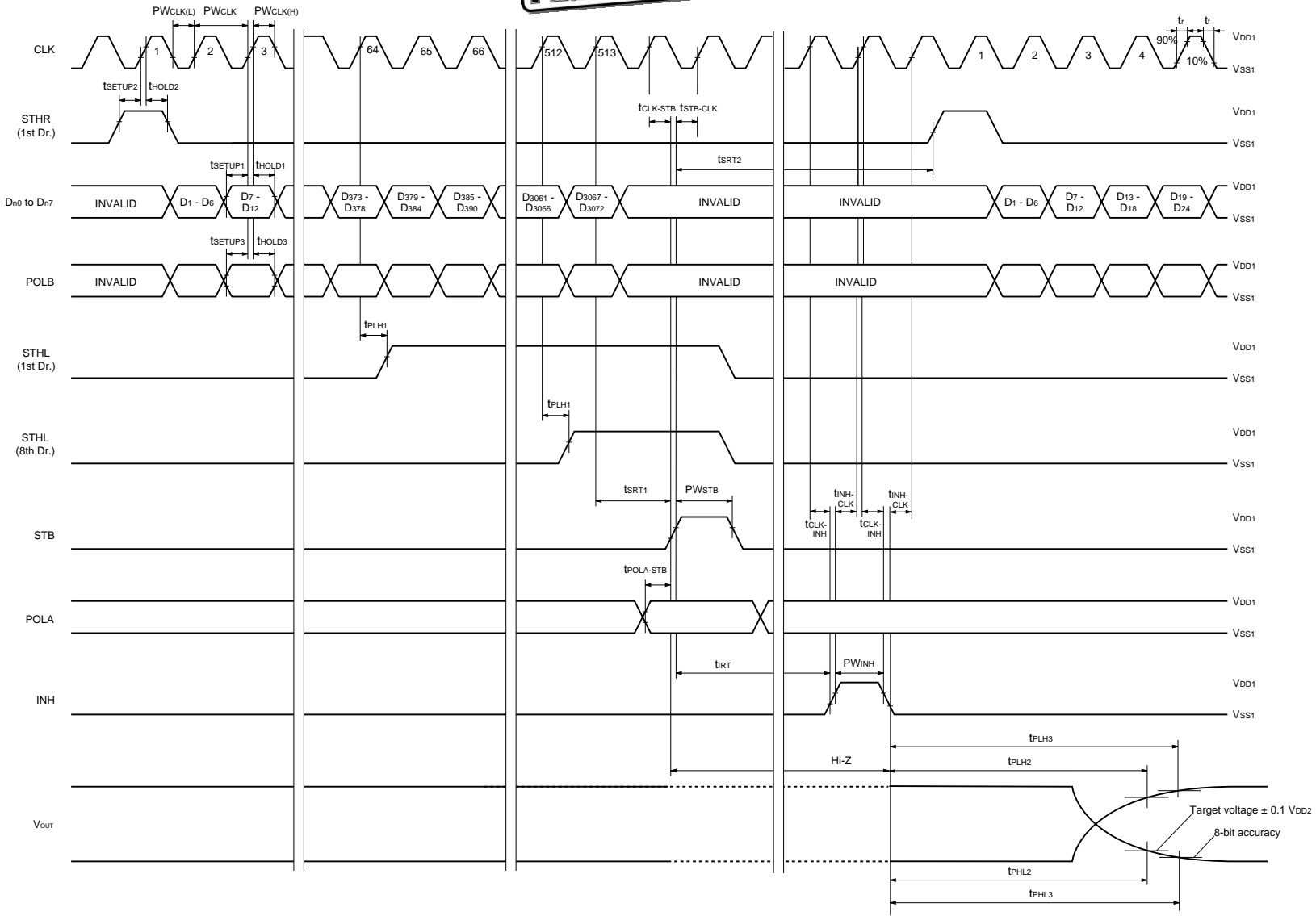
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Start Pulse Delay Time	t <sub>PLH1</sub>	C <sub>L</sub> = 10 pF, CLK → STHL (STHR)	2	4.3	20	ns	
Driver Output Delay Time	t <sub>PLH2</sub>	V <sub>DD2</sub> = 8.5 V, R <sub>L</sub> = 5.0 kΩ,			2.8	6.0	μs
	t <sub>PLH3</sub>						
	t <sub>PHL2</sub>	C <sub>L</sub> = 35 pF x 2			1.6	6.0	μs
	t <sub>PHL3</sub>						
Input Capacitance	C <sub>I1</sub>	T <sub>A</sub> = +25°C, STHR (STHL), V <sub>O</sub> to V <sub>9</sub> , V <sub>ref</sub>		8	15	pF	
	C <sub>I2</sub>	T <sub>A</sub> = +25°C, STHR(STHL), V <sub>O</sub> to V <sub>9</sub> , Except V <sub>ref</sub>		6	10	pF	

Timing Requirement ( $T_A = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD1} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS1} = V_{SS2} = 0\text{ V}$ )

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW <sub>CLK</sub>		25			ns
Clock Pulse High Period	PW <sub>CLK(H)</sub>		8			ns
Clock Pulse Low Period	PW <sub>CLK(L)</sub>		8			ns
STB Pulse Width	PW <sub>STB</sub>		1			CLK
INH Pulse Width	PW <sub>INH</sub>		1			CLK
Data Setup Time	t <sub>SETUP1</sub>		4			ns
Data Hold Time	t <sub>HOLD1</sub>		0			ns
Start Pulse Setup Time	t <sub>SETUP2</sub>		4			ns
Start Pulse Hold Time	t <sub>HOLD2</sub>		0			ns
POLB Setup Time	t <sub>SETUP3</sub>		4			ns
POLB Hold Time	t <sub>HOLD3</sub>		0			ns
STB Pulse Rise Timing	t <sub>SRT1</sub>		1			CLK
Start Pulse Rise Timing	t <sub>SRT2</sub>		1			CLK
INH Rise Timing	t <sub>IRT</sub>		1			$\mu\text{s}$
CLK-INH Time	t <sub>CLK-INH</sub>	CLK $\uparrow$ $\rightarrow$ INH $\downarrow$	4			ns
INH-CLK Time	t <sub>INH-CLK</sub>	INH $\uparrow$ $\rightarrow$ CLK $\uparrow$	4			ns
POLA-STB Time	t <sub>POLA-STB</sub>	POLA $\uparrow$ or $\downarrow$ $\rightarrow$ STB $\uparrow$	4			ns
CLK-STB Time	t <sub>CLK-STB</sub>	CLK $\uparrow$ $\rightarrow$ STB $\uparrow$	4			ns
STB-CLK Time	t <sub>STB-CLK</sub>	STB $\uparrow$ $\rightarrow$ CLK $\uparrow$	4			ns

**9. SWITCHING CHARACTERISTICS WAVEFORM (In case of XGA drive)**  
 (Unless otherwise specified, the input level is defined to be  $V_{IH} = 0.7 V_{DD1}$ ,  $V_{IL} = 0.3 V_{DD1}$ .)

**Phase-out/Discontinued**





**10. RECOMMENDED SOLDERING CONDITIONS**

The following conditions must be met for soldering conditions of the μ PD16740.

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

**μ PD16740N-xxx : TCP (TAB package)**

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C: heating for 2 to 3 seconds: pressure 100 g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm <sup>2</sup> : time 3 to 5 secs. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm <sup>2</sup> : time 30 to 40 secs. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

**Caution** To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

[MEMO]

[MEMO]

[MEMO]

## NOTES FOR CMOS DEVICES

**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**Reference Documents**

**NEC Semiconductor Device Reliability / Quality Control System (C10983E)  
Quality Grades to NEC's Semiconductor Devices (C11531E)**

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