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April 1st, 2010
Renesas Electronics Corporation

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DATA SHEET

RENESAS

Phase-out/Discontinued

MOS INTEGRATED CIRCUIT

μPD16738

384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

DESCRIPTION

The μPD16738 is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as V_{SS2}+0.1 V to V_{DD2}–0.1 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 45 MHz when driving at 2.7 V, this driver is applicable to XGA-standard TFT-LCD panels.

FEATURES

- CMOS level input
- 384 Outputs
- Input of 6 bits (gradation data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter
- Logic power supply voltage (V_{DD1}) : 3.3 V $^{+0.3}_{-0.6}$ V
- Driver power supply voltage (V_{DD2}) : 8.5 V $^{+0.5}_{-1.0}$ V
- ★ High-speed data transfer : f_{CLK} = 45 MHz MAX. (internal data transfer speed when operating at V_{DD1} = 2.7 V)
- Output dynamic range : V_{SS2} + 0.1 V to V_{DD2} – 0.1 V
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output Voltage polarity inversion function (POL)
- Display data inversion function (POL2)
- Single bank arrangement is possible (Loaded with slim or bending TCP)

ORDERING INFORMATION

Part Number	Package
μPD16738N -×××	TCP (TAB package)

Remark The TCP's external shape is customized. To order your TCP's external shape, please contact a NEC salesperson.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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The mark ★ shows major revised points.

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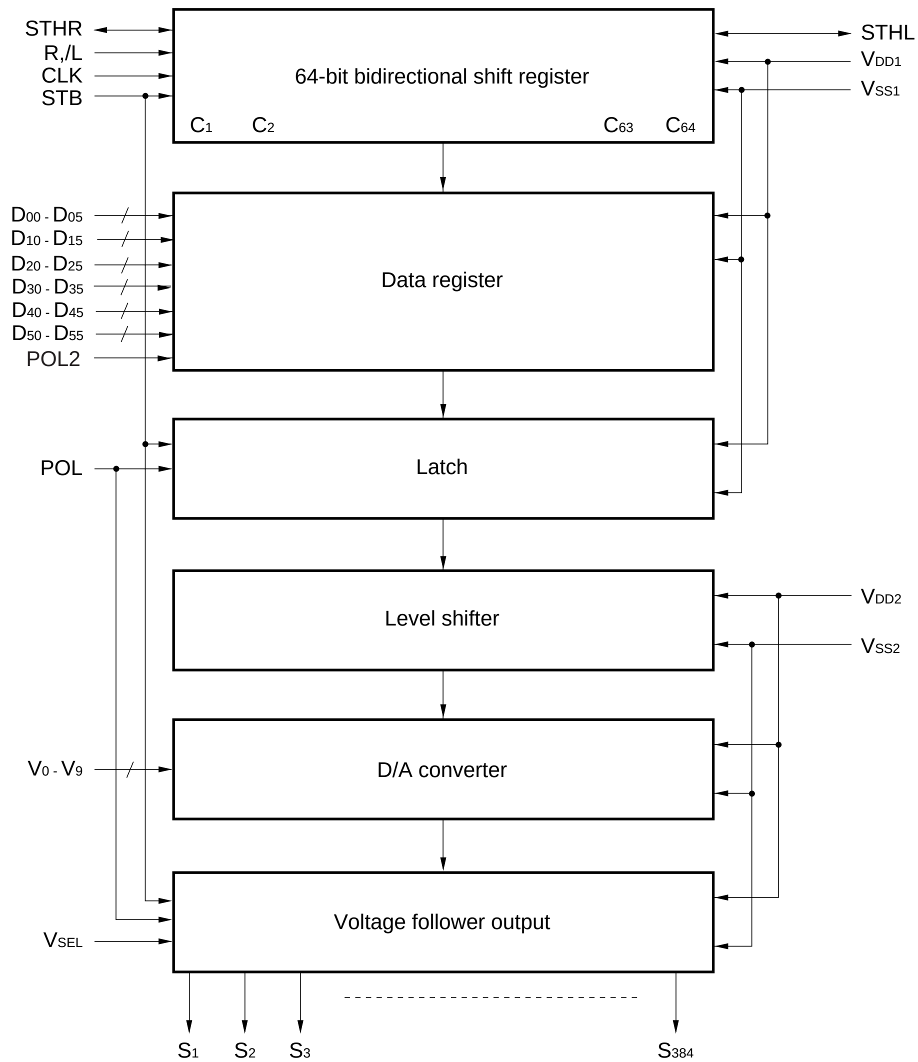
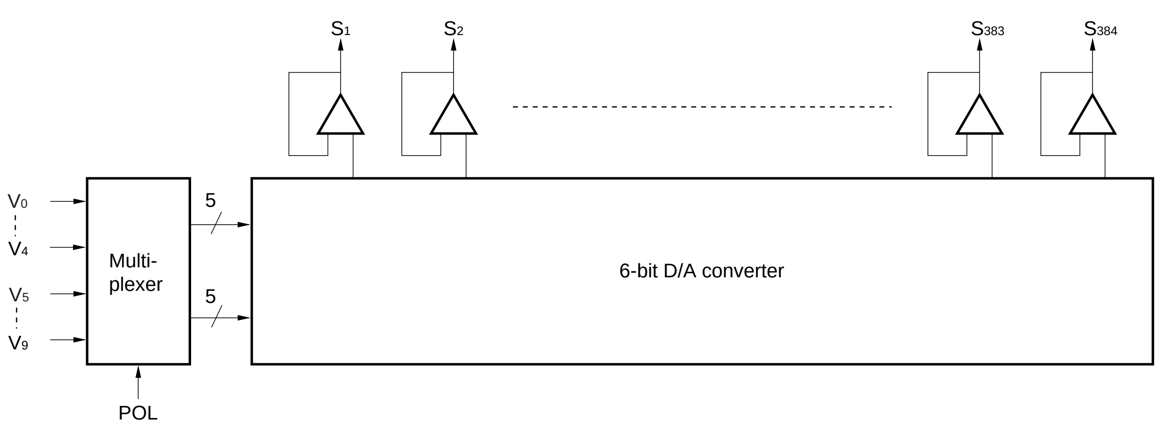
Phase-out/Discontinued

BLOCK DIAGRAM

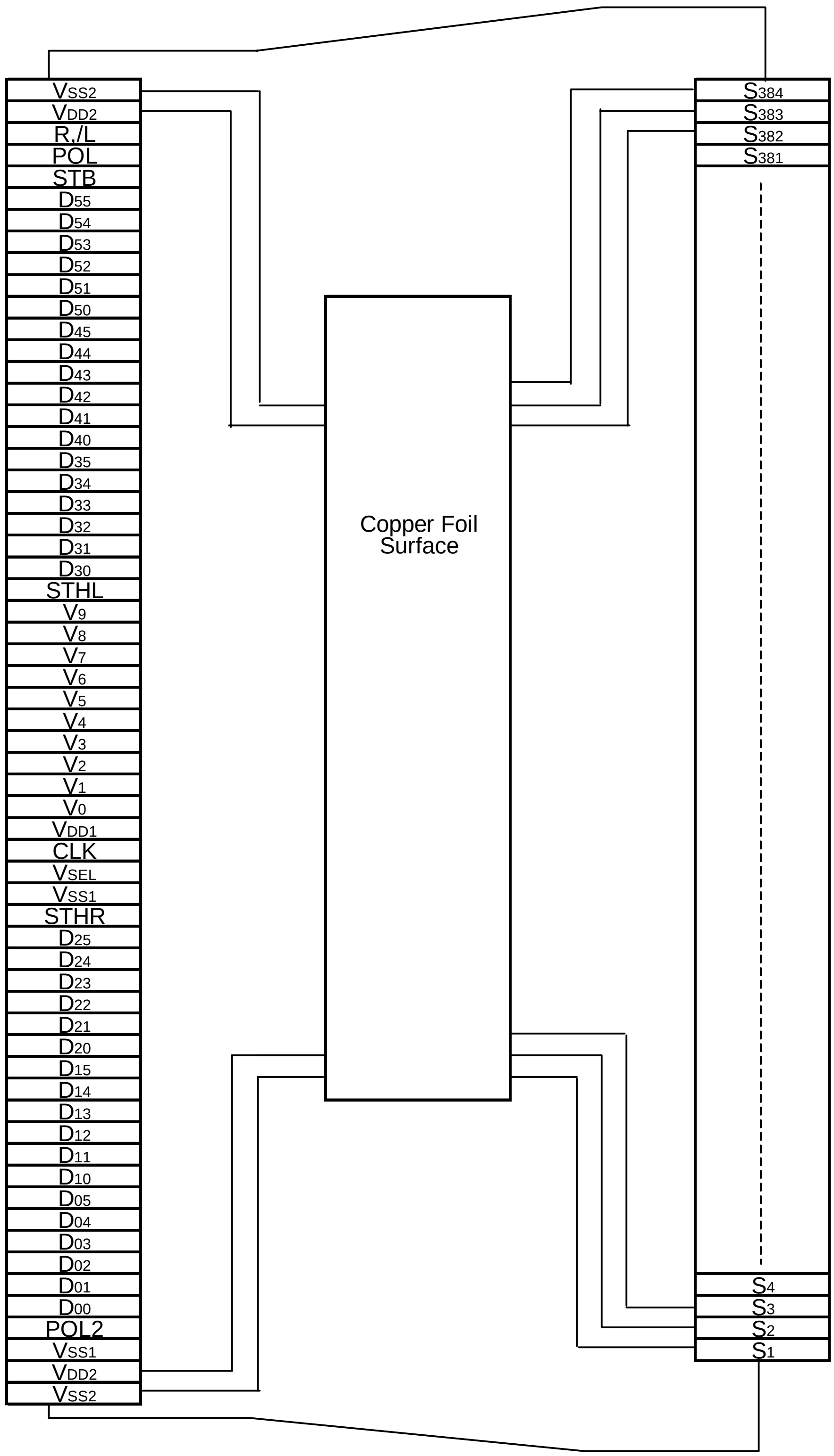


Remark /xxx indicates active low signal.

RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



PIN CONFIGURATION (μPD16738N-××× : TCP (TAB package))



Remark This figure does not specify the TCP package.

1. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	Description
S_1 to S_{384}	Driver output	The D/A converted 64-gray scale analog voltage is output.
D_{00} to D_{05}	Display data input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D_{X0} : LSB, D_{X5}: MSB
D_{10} to D_{15}		
D_{20} to D_{25}		
D_{30} to D_{35}		
D_{40} to D_{45}		
D_{50} to D_{55}		
R,/L	Shift direction control input	These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R,/L = H : STHR input, $S_1 \rightarrow S_{384}$, STHL output R,/L = L : STHL input, $S_{384} \rightarrow S_1$, STHR output
STHR	Right shift start pulse input/output	R,/L = H : Becomes the start pulse input pin. R,/L = L : Becomes the start pulse output pin.
STHL	Left shift start pulse input/output	R,/L = H : Becomes the start pulse output pin. R,/L = L : Becomes the start pulse input pin.
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver.
STB	Latch input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	POL = L : The S_{2n-1} output uses V_0 to V_4 as the reference supply. The S_{2n} output uses V_5 to V_9 as the reference supply. POL = H: The S_{2n-1} output uses V_5 to V_9 as the reference supply. The S_{2n} output uses V_0 to V_4 as the reference supply. S_{2n-1} indicates the odd output: and S_{2n} indicates the even output. Input of the POL signal is allowed the setup time ($t_{POL-STB}$) with respect to STB's rising edge.
POL2	Data inversion	POL2 = H : Display data is inverted. POL2 = L : Display data is not inverted
V_{SEL}	Driver voltage selection	Selects driver voltage. V_{SEL} = H or open : V_{DD2} = 8.5 V (TYP.) ★ V_{SEL} = L : V_{DD2} = 7.5 V ± 0.5 V

(2/2)

Pin Symbol	Pin Name	Description
V_0 to V_9	γ-corrected power supplies	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.1\ V > V_0 > V_1 > V_2 > V_3 > V_4 > 0.5\ V_{DD2}$ $0.5\ V_{DD2} - 0.3\ V > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1\ V$
V_{DD1}	Logic power supply	$3.3\ V\ ^{+0.3}_{-0.6}\ V$
V_{DD2}	Driver power supply	$8.5\ V\ ^{+0.5}_{-1.0}\ V$
V_{SS1}	Logic ground	Grounding
V_{SS2}	Driver ground	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_9 in that order. Reverse this sequence to shut down. (Simultaneous power application to V_{DD2} and V_0 to V_9 is possible.)

2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals (V_0, V_1, V_2, ⋯, V_9) and V_{SS2}.

2. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors (r0 to r62) are designed so that the ratio of LCD panel γ-compensated voltages to V_0' to V_{63}' and V_0" to V_{63}" is almost equivalent. For the 2 sets of five γ-compensated power supplies, V_0 to V_4 and V_5 to V_9, respectively, input gray scale voltages of the same polarity with respect to the common voltage. When fine-gray scale voltage precision is not necessary, there is no need to connect a voltage follower circuit to the γ-compensated power supplies V_1 to V_3 and V_6 to V_8.

Figure 2–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential VCOM, and γ-corrected voltages V0 to V9 and the input data. Be sure to maintain the voltage relationships of

$$V_{DD2} – 0.1\ V > V_0 > V_1 > V_2 > V_3 > V_4 > 0.5\ V_{DD2}$$
$$0.5\ V_{DD2} – 0.3\ V > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1\ V$$

Figures 2–2 and 2–3 show the relationship between the input data and the output data and the resistance values of the resistor strings.

This driver IC is designed for only single-sided mounting. Therefore, please do not use it for γ-corrected power supply level inversion in double-sided mounting.

Figure 2–1. Relationship Between Input Data and γ- corrected Power Supply

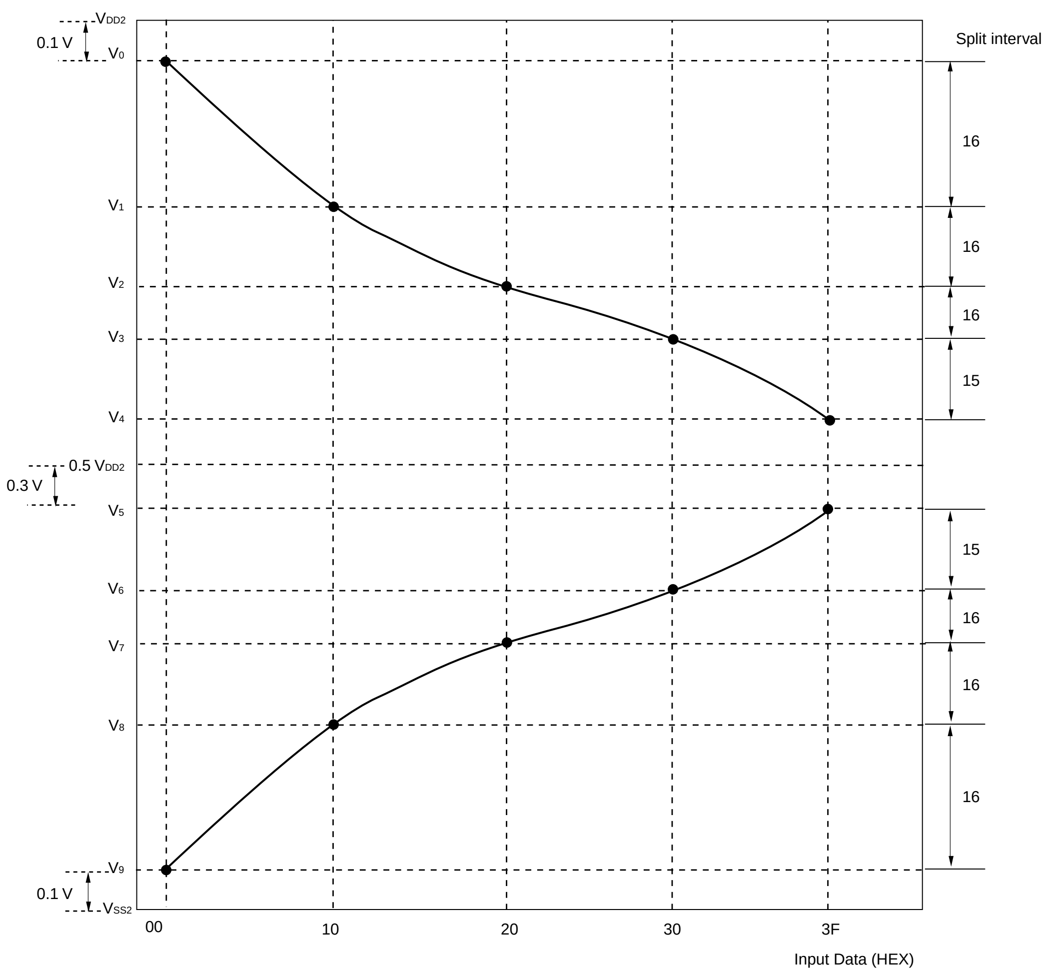
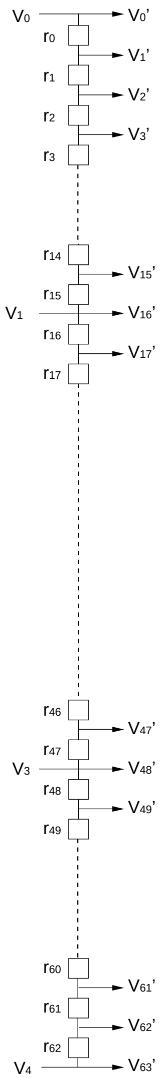


Figure 2–2. Relationship between Input Data and Output Voltage (1/2)

V_{DD2} – 0.1 V > V_0 > V_1 > V_2 > V_3 > V_4 > 0.5 V_{DD2}

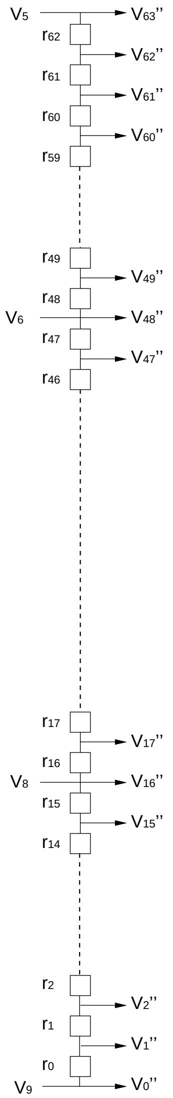


Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage		r n	(Ω)
00H	0	0	0	0	0	0	$V_{0'}$	V_0	r0	500
01H	0	0	0	0	0	1	$V_{1'}$	$V_1+(V_0-V_1)\times$ 7170 / 7670	r1	500
02H	0	0	0	0	1	0	$V_{2'}$	$V_1+(V_0-V_1)\times$ 6670 / 7670	r2	500
03H	0	0	0	0	1	1	$V_{3'}$	$V_1+(V_0-V_1)\times$ 6170 / 7670	r3	500
04H	0	0	0	1	0	0	$V_{4'}$	$V_1+(V_0-V_1)\times$ 5670 / 7670	r4	500
05H	0	0	0	1	0	1	$V_{5'}$	$V_1+(V_0-V_1)\times$ 5170 / 7670	r5	500
06H	0	0	0	1	1	0	$V_{6'}$	$V_1+(V_0-V_1)\times$ 4670 / 7670	r6	500
07H	0	0	0	1	1	1	$V_{7'}$	$V_1+(V_0-V_1)\times$ 4170 / 7670	r7	500
08H	0	0	1	0	0	0	$V_{8'}$	$V_1+(V_0-V_1)\times$ 3670 / 7670	r8	500
09H	0	0	1	0	0	1	$V_{9'}$	$V_1+(V_0-V_1)\times$ 3170 / 7670	r9	500
0AH	0	0	1	0	1	0	$V_{10'}$	$V_1+(V_0-V_1)\times$ 2670 / 7670	r10	500
0BH	0	0	1	0	1	1	$V_{11'}$	$V_1+(V_0-V_1)\times$ 2170 / 7670	r11	500
0CH	0	0	1	1	0	0	$V_{12'}$	$V_1+(V_0-V_1)\times$ 1670 / 7670	r12	450
0DH	0	0	1	1	0	1	$V_{13'}$	$V_1+(V_0-V_1)\times$ 1220 / 7670	r13	450
0EH	0	0	1	1	1	0	$V_{14'}$	$V_1+(V_0-V_1)\times$ 770 / 7670	r14	400
0FH	0	0	1	1	1	1	$V_{15'}$	$V_1+(V_0-V_1)\times$ 370 / 7670	r15	370
10H	0	1	0	0	0	0	$V_{16'}$	V_1	r16	330
11H	0	1	0	0	0	1	$V_{17'}$	$V_2+(V_1-V_2)\times$ 3810 / 4140	r17	330
12H	0	1	0	0	1	0	$V_{18'}$	$V_2+(V_1-V_2)\times$ 3480 / 4140	r18	330
13H	0	1	0	0	1	1	$V_{19'}$	$V_2+(V_1-V_2)\times$ 3150 / 4140	r19	320
14H	0	1	0	1	0	0	$V_{20'}$	$V_2+(V_1-V_2)\times$ 2830 / 4140	r20	300
15H	0	1	0	1	0	1	$V_{21'}$	$V_2+(V_1-V_2)\times$ 2530 / 4140	r21	280
16H	0	1	0	1	1	0	$V_{22'}$	$V_2+(V_1-V_2)\times$ 2250 / 4140	r22	270
17H	0	1	0	1	1	1	$V_{23'}$	$V_2+(V_1-V_2)\times$ 1980 / 4140	r23	260
18H	0	1	1	0	0	0	$V_{24'}$	$V_2+(V_1-V_2)\times$ 1720 / 4140	r24	250
19H	0	1	1	0	0	1	$V_{25'}$	$V_2+(V_1-V_2)\times$ 1470 / 4140	r25	240
1AH	0	1	1	0	1	0	$V_{26'}$	$V_2+(V_1-V_2)\times$ 1230 / 4140	r26	230
1BH	0	1	1	0	1	1	$V_{27'}$	$V_2+(V_1-V_2)\times$ 1000 / 4140	r27	220
1CH	0	1	1	1	0	0	$V_{28'}$	$V_2+(V_1-V_2)\times$ 780 / 4140	r28	210
1DH	0	1	1	1	0	1	$V_{29'}$	$V_2+(V_1-V_2)\times$ 570 / 4140	r29	200
1EH	0	1	1	1	1	0	$V_{30'}$	$V_2+(V_1-V_2)\times$ 370 / 4140	r30	190
1FH	0	1	1	1	1	1	$V_{31'}$	$V_2+(V_1-V_2)\times$ 180 / 4140	r31	180
20H	1	0	0	0	0	0	$V_{32'}$	V_2	r32	175
21H	1	0	0	0	0	1	$V_{33'}$	$V_3+(V_2-V_3)\times$ 2590 / 2765	r33	175
22H	1	0	0	0	1	0	$V_{34'}$	$V_3+(V_2-V_3)\times$ 2415 / 2765	r34	170
23H	1	0	0	0	1	1	$V_{35'}$	$V_3+(V_2-V_3)\times$ 2245 / 2765	r35	170
24H	1	0	0	1	0	0	$V_{36'}$	$V_3+(V_2-V_3)\times$ 2075 / 2765	r36	165
25H	1	0	0	1	0	1	$V_{37'}$	$V_3+(V_2-V_3)\times$ 1910 / 2765	r37	165
26H	1	0	0	1	1	0	$V_{38'}$	$V_3+(V_2-V_3)\times$ 1745 / 2765	r38	165
27H	1	0	0	1	1	1	$V_{39'}$	$V_3+(V_2-V_3)\times$ 1580 / 2765	r39	165
28H	1	0	1	0	0	0	$V_{40'}$	$V_3+(V_2-V_3)\times$ 1415 / 2765	r40	170
29H	1	0	1	0	0	1	$V_{41'}$	$V_3+(V_2-V_3)\times$ 1245 / 2765	r41	170
2AH	1	0	1	0	1	0	$V_{42'}$	$V_3+(V_2-V_3)\times$ 1075 / 2765	r42	170
2BH	1	0	1	0	1	1	$V_{43'}$	$V_3+(V_2-V_3)\times$ 905 / 2765	r43	175
2CH	1	0	1	1	0	0	$V_{44'}$	$V_3+(V_2-V_3)\times$ 730 / 2765	r44	175
2DH	1	0	1	1	0	1	$V_{45'}$	$V_3+(V_2-V_3)\times$ 555 / 2765	r45	175
2EH	1	0	1	1	1	0	$V_{46'}$	$V_3+(V_2-V_3)\times$ 380 / 2765	r46	180
2FH	1	0	1	1	1	1	$V_{47'}$	$V_3+(V_2-V_3)\times$ 200 / 2765	r47	200
30H	1	1	0	0	0	0	$V_{48'}$	V_3	r48	210
31H	1	1	0	0	0	1	$V_{49'}$	$V_5+(V_3-V_4)\times$ 4050 / 4260	r49	220
32H	1	1	0	0	1	0	$V_{50'}$	$V_5+(V_3-V_4)\times$ 3830 / 4260	r50	230
33H	1	1	0	0	1	1	$V_{51'}$	$V_5+(V_3-V_4)\times$ 3600 / 4260	r51	240
34H	1	1	0	1	0	0	$V_{52'}$	$V_5+(V_3-V_4)\times$ 3360 / 4260	r52	250
35H	1	1	0	1	0	1	$V_{53'}$	$V_5+(V_3-V_4)\times$ 3110 / 4260	r53	260
36H	1	1	0	1	1	0	$V_{54'}$	$V_5+(V_3-V_4)\times$ 2850 / 4260	r54	270
37H	1	1	0	1	1	1	$V_{55'}$	$V_5+(V_3-V_4)\times$ 2580 / 4260	r55	290
38H	1	1	1	0	0	0	$V_{56'}$	$V_5+(V_3-V_4)\times$ 2290 / 4260	r56	300
39H	1	1	1	0	0	1	$V_{57'}$	$V_5+(V_3-V_4)\times$ 1990 / 4260	r57	310
3AH	1	1	1	0	1	0	$V_{58'}$	$V_5+(V_3-V_4)\times$ 1680 / 4260	r58	320
3BH	1	1	1	0	1	1	$V_{59'}$	$V_5+(V_3-V_4)\times$ 1360 / 4260	r59	340
3CH	1	1	1	1	0	0	$V_{60'}$	$V_5+(V_3-V_4)\times$ 1020 / 4260	r60	340
3DH	1	1	1	1	0	1	$V_{61'}$	$V_5+(V_3-V_4)\times$ 680 / 4260	r61	340
3EH	1	1	1	1	1	0	$V_{62'}$	$V_5+(V_3-V_4)\times$ 340 / 4260	r62	340
3FH	1	1	1	1	1	1	$V_{63'}$	V_4	r total	18835

Caution Between V_4 and V_5 terminal is not connected in the chip.

Figure 2–3. Relationship between Input Data and Output Voltage (2/2)

$0.5\ V_{DD2} - 0.3\ V > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1\ V$



Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage	
00H	0	0	0	0	0	0	$V_{0''}$	V_9
01H	0	0	0	0	0	1	$V_{1''}$	$V_9+(V_8-V_9)$ × 500 / 7670
02H	0	0	0	0	1	0	$V_{2''}$	$V_9+(V_8-V_9)$ × 1000 / 7670
03H	0	0	0	0	1	1	$V_{3''}$	$V_9+(V_8-V_9)$ × 1500 / 7670
04H	0	0	0	1	0	0	$V_{4''}$	$V_9+(V_8-V_9)$ × 2000 / 7670
05H	0	0	0	1	0	1	$V_{5''}$	$V_9+(V_8-V_9)$ × 2500 / 7670
06H	0	0	0	1	1	0	$V_{6''}$	$V_9+(V_8-V_9)$ × 3000 / 7670
07H	0	0	0	1	1	1	$V_{7''}$	$V_9+(V_8-V_9)$ × 3500 / 7670
08H	0	0	1	0	0	0	$V_{8''}$	$V_9+(V_8-V_9)$ × 4000 / 7670
09H	0	0	1	0	0	1	$V_{9''}$	$V_9+(V_8-V_9)$ × 4500 / 7670
0AH	0	0	1	0	1	0	$V_{10''}$	$V_9+(V_8-V_9)$ × 5000 / 7670
0BH	0	0	1	0	1	1	$V_{11''}$	$V_9+(V_8-V_9)$ × 5500 / 7670
0CH	0	0	1	1	0	0	$V_{12''}$	$V_9+(V_8-V_9)$ × 6000 / 7670
0DH	0	0	1	1	0	1	$V_{13''}$	$V_9+(V_8-V_9)$ × 6450 / 7670
0EH	0	0	1	1	1	0	$V_{14''}$	$V_9+(V_8-V_9)$ × 6900 / 7670
0FH	0	0	1	1	1	1	$V_{15''}$	$V_9+(V_8-V_9)$ × 7300 7670
10H	0	1	0	0	0	0	$V_{16''}$	V_8
11H	0	1	0	0	0	1	$V_{17''}$	$V_8+(V_7-V_8)$ × 330 / 4140
12H	0	1	0	0	1	0	$V_{18''}$	$V_8+(V_7-V_8)$ × 660 / 4140
13H	0	1	0	0	1	1	$V_{19''}$	$V_8+(V_7-V_8)$ × 990 / 4140
14H	0	1	0	1	0	0	$V_{20''}$	$V_8+(V_7-V_8)$ × 1310 / 4140
15H	0	1	0	1	0	1	$V_{21''}$	$V_8+(V_7-V_8)$ × 1610 / 4140
16H	0	1	0	1	1	0	$V_{22''}$	$V_8+(V_7-V_8)$ × 1890 / 4140
17H	0	1	0	1	1	1	$V_{23''}$	$V_8+(V_7-V_8)$ × 2160 / 4140
18H	0	1	1	0	0	0	$V_{24''}$	$V_8+(V_7-V_8)$ × 2420 / 4140
19H	0	1	1	0	0	1	$V_{25''}$	$V_8+(V_7-V_8)$ × 2670 / 4140
1AH	0	1	1	0	1	0	$V_{26''}$	$V_8+(V_7-V_8)$ × 2910 / 4140
1BH	0	1	1	0	1	1	$V_{27''}$	$V_8+(V_7-V_8)$ × 3140 / 4140
1CH	0	1	1	1	0	0	$V_{28''}$	$V_8+(V_7-V_8)$ × 3360 / 4140
1DH	0	1	1	1	0	1	$V_{29''}$	$V_8+(V_7-V_8)$ × 3570 / 4140
1EH	0	1	1	1	1	0	$V_{30''}$	$V_8+(V_7-V_8)$ × 3770 / 4140
1FH	0	1	1	1	1	1	$V_{31''}$	$V_8+(V_7-V_8)$ × 3960 4140
20H	1	0	0	0	0	0	$V_{32''}$	V_7
21H	1	0	0	0	0	1	$V_{33''}$	$V_7+(V_6-V_7)$ × 175 / 2765
22H	1	0	0	0	1	0	$V_{34''}$	$V_7+(V_6-V_7)$ × 350 / 2765
23H	1	0	0	0	1	1	$V_{35''}$	$V_7+(V_6-V_7)$ × 520 / 2765
24H	1	0	0	1	0	0	$V_{36''}$	$V_7+(V_6-V_7)$ × 690 / 2765
25H	1	0	0	1	0	1	$V_{37''}$	$V_7+(V_6-V_7)$ × 855 / 2765
26H	1	0	0	1	1	0	$V_{38''}$	$V_7+(V_6-V_7)$ × 1020 / 2765
27H	1	0	0	1	1	1	$V_{39''}$	$V_7+(V_6-V_7)$ × 1185 / 2765
28H	1	0	1	0	0	0	$V_{40''}$	$V_7+(V_6-V_7)$ × 1350 / 2765
29H	1	0	1	0	0	1	$V_{41''}$	$V_7+(V_6-V_7)$ × 1520 / 2765
2AH	1	0	1	0	1	0	$V_{42''}$	$V_7+(V_6-V_7)$ × 1690 / 2765
2BH	1	0	1	0	1	1	$V_{43''}$	$V_7+(V_6-V_7)$ × 1860 / 2765
2CH	1	0	1	1	0	0	$V_{44''}$	$V_7+(V_6-V_7)$ × 2035 / 2765
2DH	1	0	1	1	0	1	$V_{45''}$	$V_7+(V_6-V_7)$ × 2210 / 2765
2EH	1	0	1	1	1	0	$V_{46''}$	$V_7+(V_6-V_7)$ × 2385 / 2765
2FH	1	0	1	1	1	1	$V_{47''}$	$V_7+(V_6-V_7)$ × 2565 / 2765
30H	1	1	0	0	0	0	$V_{48''}$	V_6
31H	1	1	0	0	0	1	$V_{49''}$	$V_6+(V_5-V_6)$ × 210 / 4260
32H	1	1	0	0	1	0	$V_{50''}$	$V_6+(V_5-V_6)$ × 430 / 4260
33H	1	1	0	0	1	1	$V_{51''}$	$V_6+(V_5-V_6)$ × 660 / 4260
34H	1	1	0	1	0	0	$V_{52''}$	$V_6+(V_5-V_6)$ × 900 / 4260
35H	1	1	0	1	0	1	$V_{53''}$	$V_6+(V_5-V_6)$ × 1150 / 4260
36H	1	1	0	1	1	0	$V_{54''}$	$V_6+(V_5-V_6)$ × 1410 / 4260
37H	1	1	0	1	1	1	$V_{55''}$	$V_6+(V_5-V_6)$ × 1680 / 4260
38H	1	1	1	0	0	0	$V_{56''}$	$V_6+(V_5-V_6)$ × 1970 / 4260
39H	1	1	1	0	0	1	$V_{57''}$	$V_6+(V_5-V_6)$ × 2270 / 4260
3AH	1	1	1	0	1	0	$V_{58''}$	$V_6+(V_5-V_6)$ × 2580 / 4260
3BH	1	1	1	0	1	1	$V_{59''}$	$V_6+(V_5-V_6)$ × 2900 / 4260
3CH	1	1	1	1	0	0	$V_{60''}$	$V_6+(V_5-V_6)$ × 3240 / 4260
3DH	1	1	1	1	0	1	$V_{61''}$	$V_6+(V_5-V_6)$ × 3580 / 4260
3EH	1	1	1	1	1	0	$V_{62''}$	$V_6+(V_5-V_6)$ × 3920 / 4260
3FH	1	1	1	1	1	1	$V_{63''}$	V_5

r n	(Ω)
r0	500
r1	500
r2	500
r3	500
r4	500
r5	500
r6	500
r7	500
r8	500
r9	500
r10	500
r11	500
r12	450
r13	450
r14	400
r15	370
r16	330
r17	330
r18	330
r19	320
r20	300
r21	280
r22	270
r23	260
r24	250
r25	240
r26	230
r27	220
r28	210
r29	200
r30	190
r31	180
r32	175
r33	175
r34	170
r35	170
r36	165
r37	165
r38	165
r39	165
r40	170
r41	170
r42	170
r43	175
r44	175
r45	175
r46	180
r47	200
r48	210
r49	220
r50	230
r51	240
r52	250
r53	260
r54	270
r55	290
r56	300
r57	310
r58	320
r59	340
r60	340
r61	340
r62	340
r total	18835

Caution   Between V_4 and V_5 terminal is not connected in the chip.

3. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 6 bits × 2 RGBs (6 dots)
Input width: 36 bits (2-pixel data)

R,/L = H (Right shift)

Output	S_1	S_2	S_3	S_4	···	S_{383}	S_{384}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	···	D_{40} to D_{45}	D_{50} to D_{55}

R,/L = L (Left shift)

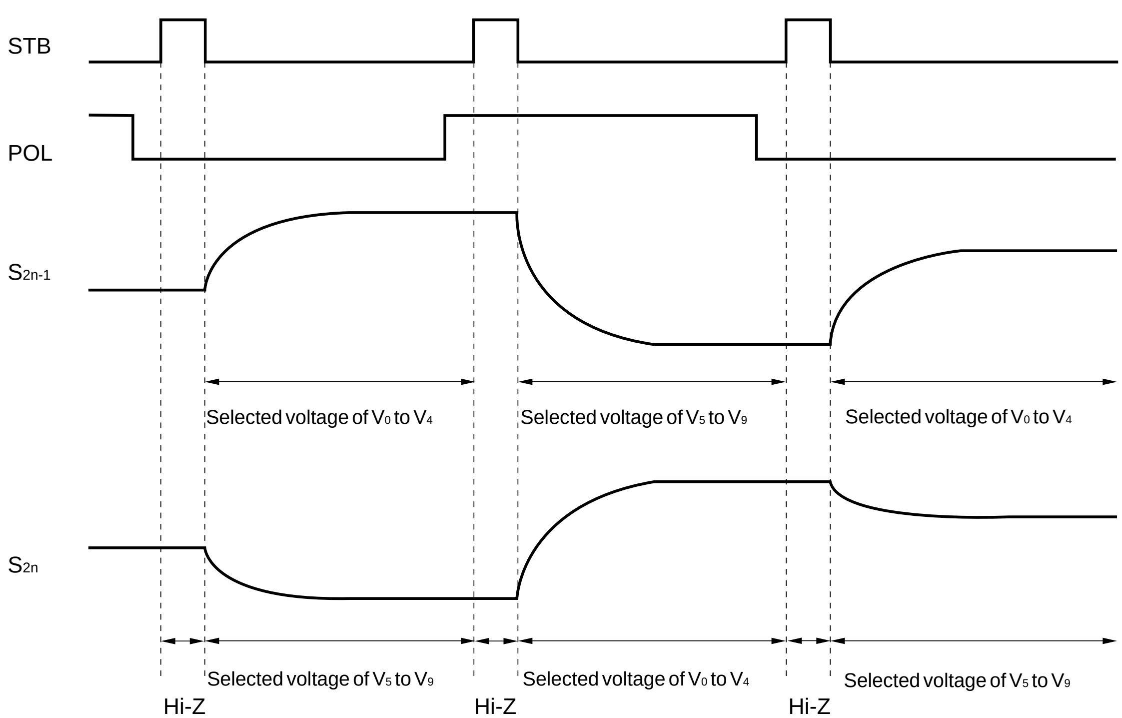
Output	S_1	S_2	S_3	S_4	···	S_{383}	S_{384}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	···	D_{40} to D_{45}	D_{50} to D_{55}

POL	S_{2n-1} Note	S_{2n} Note
L	V_0 to V_4	V_5 to V_9
H	V_5 to V_9	V_0 to V_4

Note S_{2n-1} (Odd output), S_{2n} (Even output)

4. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +4.0	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +10.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} + 0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Operating Ambient Temperature	T_A	–10 to +75	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range (T_A = –10 to +75 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}		2.7	3.3	3.6	V
Driver Part Supply Voltage	V_{DD2}	V_{SEL} = H or open	7.5	8.5	9.0	V
★		V_{SEL} = L	7.0	7.5	8.0	V
High-Level Input Voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}		0		0.3 V_{DD1}	V
γ-Corrected Voltage	V_0 to V_4		0.5 V_{DD2}		V_{DD2} – 0.1	V
	V_5 to V_9		V_{SS2} + 0.1		0.5 V_{DD2} – 0.3	V
Driver Part Output Voltage	V_O		V_{SS2} + 0.1		V_{DD2} – 0.1	V
Clock Frequency	f_{CLK}				45	MHz

Electrical Characteristics (T_A = –10 to +75 °C, V_{DD1} = 3.3 V $^{+0.3}_{-0.6}$ V, V_{DD2} = 8.5 V $^{+0.5}_{-1.0}$ V (V_{SEL} = H or open), V_{SS1} = V_{SS2} = 0 V)

	Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
	Input Leak Current	I_{IL}					±1.0	μA
	High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = 0 mA		V_{DD1} – 0.1		V_{DD1}	V
	Low-Level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = 0 mA		0		0.1	V
★	γ-Corrected Supply Current	I_γ	V_0 to V_4 = V_5 to V_9 = 3.0 V	V_0 pin, V_5 pin	80	160	320	μA
				V_4 pin, V_9 pin	–320	–160	–80	μA
★	Driver Output Current	I_{VOH}	V_X = 7.5 V, V_{OUT} = 7.0 V Note, V_{DD2} = 8.0 V			–0.17	–0.1	mA
		I_{VOL}	V_X = 0.5 V, V_{OUT} = 1.0 V Note, V_{DD2} = 8.0 V		0.1	0.23		mA
	Output Voltage Deviation	ΔV_O	Input data	V_0 = 0.1 V to 1.2 V, V_0 = V_{DD2} – 1.2 V to V_{DD2} – 0.1 V		±20	±30	mV
				V_0 = 1.2 V to 0.5 V_{DD2} – 0.3 V, V_0 = 0.5 V_{DD2} to V_{DD2} – 1.2 V		±10	±20	mV
	Output Swing Voltage Difference Deviation	ΔV_{p-p1}		V_0 = 0.1 V to 0.8 V, V_0 = V_{DD2} – 0.8 V to V_{DD2} – 0.1 V		±20	±30	mV
		ΔV_{p-p2}		V_0 = 0.8 V to 1.2 V, V_0 = V_{DD2} – 1.2 V to V_{DD2} – 0.8 V		±10	±20	mV
		ΔV_{p-p3}		V_0 = 1.2 V to 0.5 V_{DD2} – 0.3 V , V_0 = 0.5 V_{DD2} to V_{DD2} –1.2 V		± 3	±10	mV
	Output Voltage Range	V_O	All Input data		0.1		V_{DD2} – 0.1	V
★	Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1}, with no load			0.8	4.5	mA
★	Driver Part Dynamic Current Consumption	I_{DD2}	V_{DD2} = 9.0 V, with no load			5.5	12	mA

Note V_X refers to the output voltage of analog output pins S_1 to S_{384}. V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{384}.

Cautions 1. The STB cycle is defined to be 20 μs at f_{CLK} = 45 MHz.

2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

3. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).

Switching Characteristics (T_A = –10 to +75 °C, V_{DD1} = 3.3 V $^{+0.3}_{-0.6}$ V, V_{DD2} = 8.5 V $^{+0.5}_{-1.0}$ V (V_{SEL} = H or open), V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 25 pF		8	20	ns
Driver Output Delay Time	t_{PLH2}	V_{DD2} = 8.5 V ± 0.5 V		4	8	μs
	t_{PLH3}	R_L = 10 kΩ, C_L = 80 pF		5.5	11	μs
	t_{PHL2}			4	8	μs
	t_{PHL3}			5.5	11	μs
Input Capacitance	C_{I1}	STHR (STHL) excluded, T_A = 25°C		4.8	10	pF
	C_{I2}	STHR (STHL), T_A = 25°C		8.6	15	pF

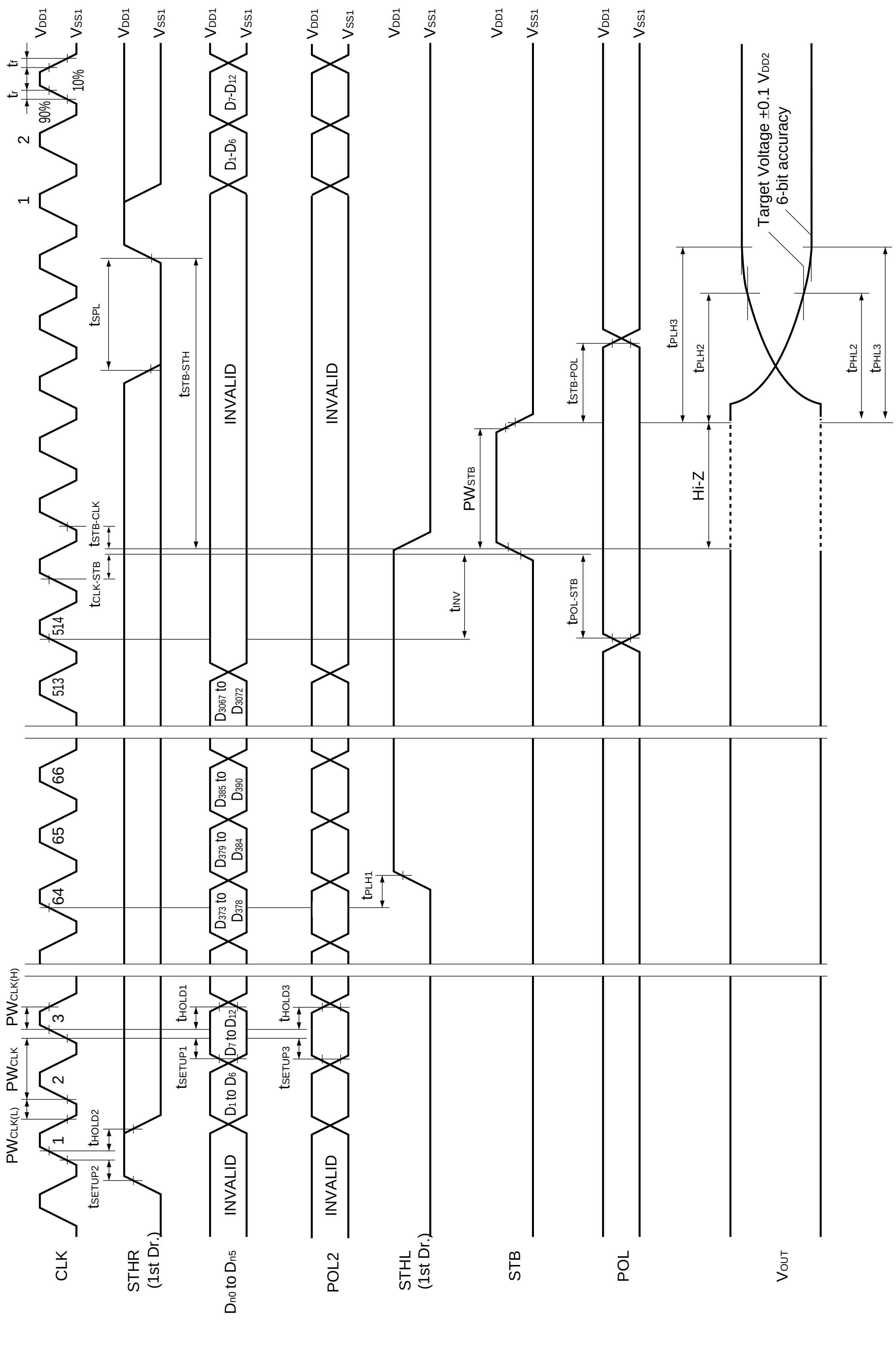
Timing Requirement (T_A = –10 to +75 °C, V_{DD1} = 3.3 V $^{+0.3}_{-0.6}$ V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 8.0 ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		22			ns
Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		4			ns
Data Setup Time	t_{SETUP1}		0			ns
Data Hold Time	t_{HOLD1}		4			ns
Start Pulse Setup Time	t_{SETUP2}		2			ns
Start Pulse Hold Time	t_{HOLD2}		2			ns
★ POL2 Setup Time	t_{SETUP3}		0			ns
★ POL2 Hold Time	t_{HOLD3}		4			ns
Start Pulse Low Period	t_{SPL}		1			CLK
STB Pulse Width	PW_{STB}		3			CLK
Data Invalid Period	t_{INV}		1			CLK
★ CLK-STB Time	$t_{CLK-STB}$	CLK ↑ → STB ↑	0			ns
★ STB-CLK Time	$t_{STB-CLK}$	STB ↑ → CLK ↑	10			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	STB ↑ → STHR(STHL) ↑	3			CLK
POL-STB Time	$t_{POL-STB}$	POL ↑ or ↓ → STB ↑	6			ns
STB-POL Time	$t_{STB-POL}$	STB ↓ → POL ↓ or ↑	3			CLK

★ **Remark** Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

★ 6. SWITCHING CHARACTERISTICS WAVEFORM (R,/L = H)

Unless otherwise specified, the input level is defined to be $V_{IH} = 0.7\ V_{DD1}$, $V_{IL} = 0.3\ V_{DD1}$.



7. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μPD16738.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Type of Surface Mount Device

μPD16738N-××× : TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds: pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm^2 : time 3 to 5 seconds. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm^2 : time 30 to 40 seconds. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability / Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)

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