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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

μPD16721

384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 256-GRAY SCALES)

DESCRIPTION

The μPD16721 is a source driver for TFT-LCDs capable of dealing with displays with 256-gray scales. Data input is based on digital input configured as 8 bits by 6 dots (2 pixels), which can realize a full-color display of 16,777,216 colors by output of 256 values γ-corrected by an internal D/A converter and 8-by-2 external power modules.

Because the output dynamic range is as large as V_{SS2} + 0.2 V to V_{DD2} – 0.2 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 8-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. The maximum clock frequency is 70 MHz when driving at 3.0 V.

FEATURES

- CMOS level input
- 384 outputs
- Input of 8 bits (gray scale data) by 6 dots
- Capable of outputting 256 values by means of 8-by-2 external power modules (16 units) and a D/A converter
- ★ • Logic power supply voltage (V_{DD1}): 2.5 to 3.4 V
- ★ • Driver power supply voltage (V_{DD2}): 13.0 ± 0.5 V or 15.0 ± 0.5 V (switchable, V_{SEL})
- ★ • High-speed data transfer: $f_{CLK.}$ = 70 MHz MAX. (internal data transfer speed when operating at V_{DD1} = 3.0 V)
  = 55 MHz MAX. (internal data transfer speed when operating at V_{DD1} = 2.5 V)
- Output dynamic range: V_{SS2} + 0.2 V to V_{DD2} – 0.2 V
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity inversion function (POL)
- Output inversion function (POL21/22)
- ★ • Output reset control is possible (MODE)
- ★ • Slew-rate control is possible (SRC)
- ★ • Output resistance control is possible (ORC)
- Single bank arrangement is possible (Loaded with slim TCP)

ORDERING INFORMATION

Part Number	Package
μPD16721N-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, so please contact one of our sales representatives.

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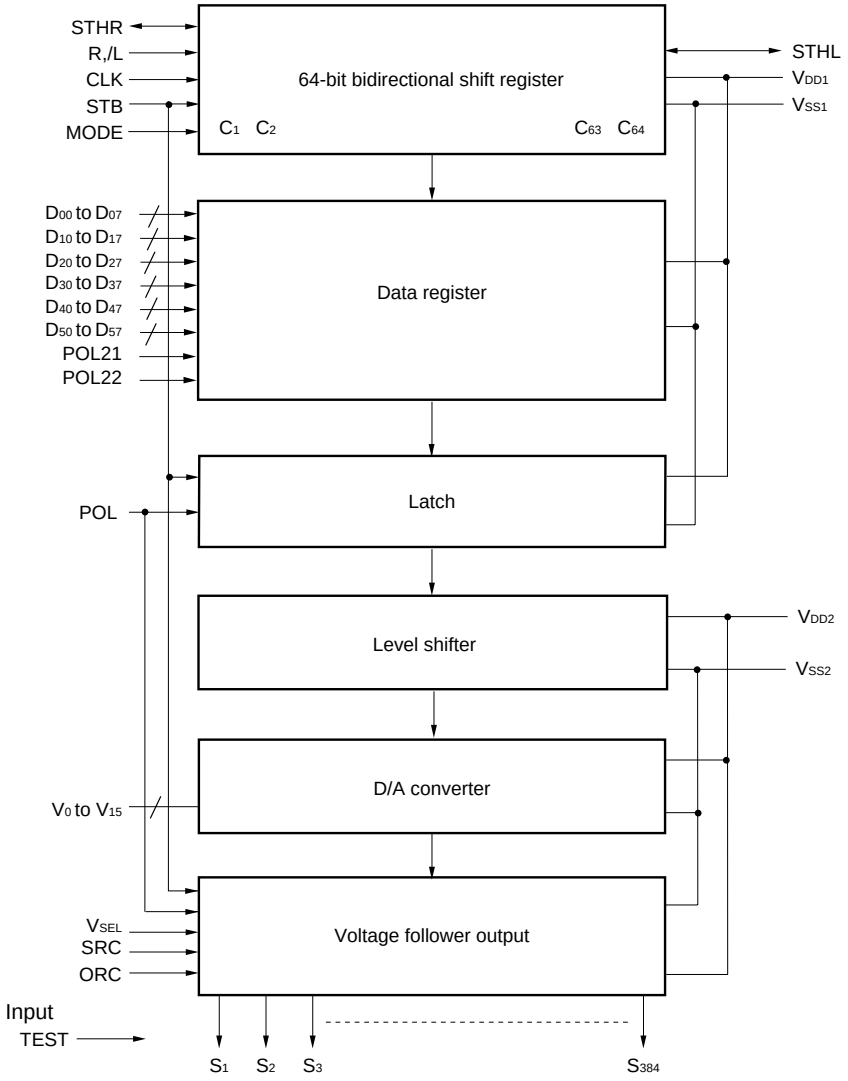
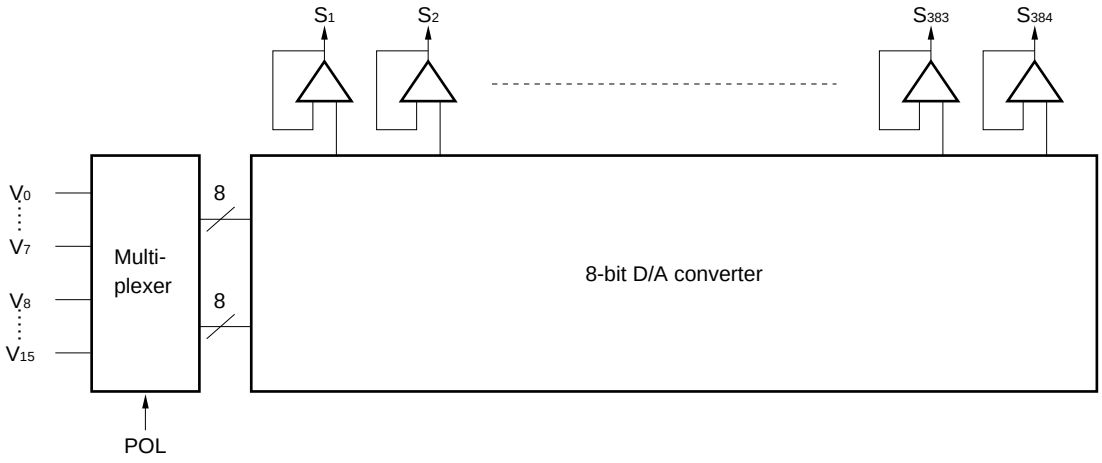
The mark ★ shows major revised points.

★1. BLOCK DIAGRAM

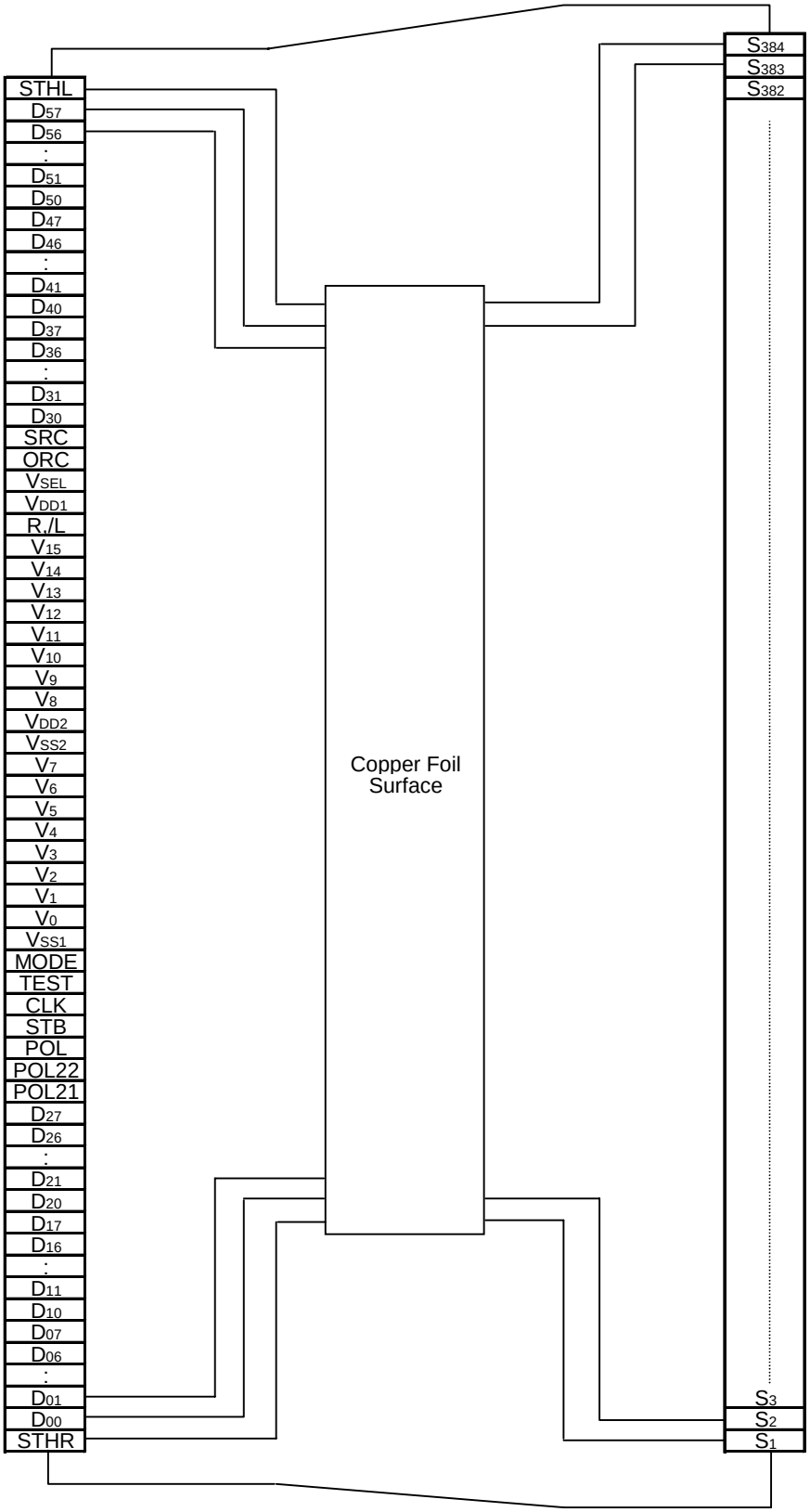


Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD16721N-xxx) (Copper Foil Surface, Face-up)



Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	I/O	Description
S_1 to S_{384}	Driver	O	The D/A converted 256-gray-scale analog voltage is output.
D_{00} to D_{07}	Port 1 display data	I	The display data is input with a width of 48 bits, viz., the gray scale data (8 bits) by 6 dots (2 pixels). D_{X0}: LSB, D_{X7}: MSB
D_{10} to D_{17}			
D_{20} to D_{27}			
D_{30} to D_{37}	Port 2 display data	I	
D_{40} to D_{47}			
D_{50} to D_{57}			
R,/L	Shift direction control	I	The shift direction control pin of shift register. The shift directions of the shift registers are as follows. R,/L = H (right shift): STHR input, $S_1 \rightarrow S_{384}$, STHL output R,/L = L (left shift) : STHL input, $S_{384} \rightarrow S_1$, STHR output
STHR	Right shift start pulse	I/O	This is the start pulse input/output pin when connected in cascade. Loading of display data starts when a high level is read at the rising edge of CLK. At the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. For right shift, STHR is input and STHL is output. For left shift, STHL is input and STHR is output.
STHL	Left shift start pulse	I/O	
CLK	Shift clock	I	The shift clock input pin of shift register. The display data is loaded into the data register at the rising edge. If 66 clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch	I	The contents of the data register are transferred to the latch circuit at the rising edge. In addition, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
SRC	Slew-rate control	I	SRC = H: High-slew-rate mode (large current consumption) SRC = L: Low-slew-rate mode (small current consumption) SRC is pulled up to the V_{DD1} in the LSI.
ORC	Output resistance control	I	ORC = H: Low output resistance mode ORC = L: High output resistance mode ORC is pulled up to the V_{DD1} in the LSI.
POL	Polarity input	I	POL = L: The S_{2n-1} output uses V_0 to V_7 as the reference supply. The S_{2n} output uses V_8 to V_{15} as the reference supply. POL = H: The S_{2n-1} output uses V_8 to V_{15} as the reference supply. The S_{2n} output uses V_0 to V_7 as the reference supply. S_{2n-1} indicates the odd output and S_{2n} indicates the even output. Input of the POL signal is allowed the setup time ($t_{POL-STB}$) with respect to STB's rising edge. When it switches such as POL = H→L or L→H, all output pins are output reset during STB = H. When it does not switch, all output pins become Hi-Z during STB = H. Refer to **7. RELATIONSHIP BETWEEN MODE, STB, SRC, ORC, POL, AND OUTPUT WAVEFORM** for details.

(2/2)

Pin Symbol	Pin Name	I/O	Description
MODE	Output reset control	I	MODE = H or open: Output reset MODE = L: No output reset MODE is pulled up to the V_{DD1} in the LSI.
POL21, POL22	Data inversion	I	Select of inversion or no inversion for input data. POL21: Data inversion or no inversion of Port1. POL22: Data inversion or no inversion of Port2 POL21/22 = H: Data are inverted in the LSI. POL21/22 = L: Data are not inverted in the LSI.
V_{SEL}	Driver voltage select	I	The driver voltage can be switched by controlling the stationary bias current of the output amplifier via V_{SEL}. V_{SEL} = H: V_{DD2} = 13.0 V (large bias current) V_{SEL} = L or open: V_{DD2} = 15.0 V (small bias current) LPC is pulled down to the V_{SS1} in the LSI.
★ V_0 to V_{15}	γ-corrected power supplies	–	Input the γ-corrected power supplies from outside by using operational amplifier. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. Make sure to maintain the following relationships. V_{DD2}–0.2 V ≥ V_0 > V_1 > V_2 > ..... > V_6 > V_7 ≥ 0.5 V_{DD2} + 0.5 V 0.5 V_{DD2}–0.5 V ≥ V_8 > V_9 > V_{10} > ..... V_{14} > V_{15} ≥ V_{SS2} + 0.2 V
TEST	Test	I	Normally, set the TEST pin to high level or leave open. This pin is pulled up to V_{DD1} in the LSI.
★ V_{DD1}	Logic power supply	–	2.5 to 3.4 V
V_{DD2}	Driver power supply	–	13.0 ± 0.5 V or 15.0 ± 0.5 V
V_{SS1}	Logic ground	–	Grounding
V_{SS2}	Driver ground	–	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_{15} in that order. Reverse this sequence to shut down.

2. To stabilize the supply voltage, please be sure to insert a 0.47 μF bypass capacitor between V_{DD1} to V_{SS1} and V_{DD2} to V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.1 μF is also advised between the γ-corrected power supply terminals (V_0, V_1, V_2,....., V_{15}) and V_{SS2}.

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The μPD16721 incorporates a 8-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors (r0 to r253) are designed so that the ratio of LCD panel (γ-compensated voltages to V_0' to V_{255}' and V_0" to V_{255}" is almost equivalent as shown in Figure 5-2 and 5-3. For the 2 sets of eight γ-compensated power supplies, V_0 to V_7 and V_8 to V_{15}, respectively, input gray scale voltages of the same polarity with respect to the 0.5 V_{DD2}.

Figure 5-1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2}, V_{SS2} and 0.5 V_{DD2}, and γ-corrected voltages V_0 to V_{15} and the input data. Be sure to maintain the voltage relationships below.

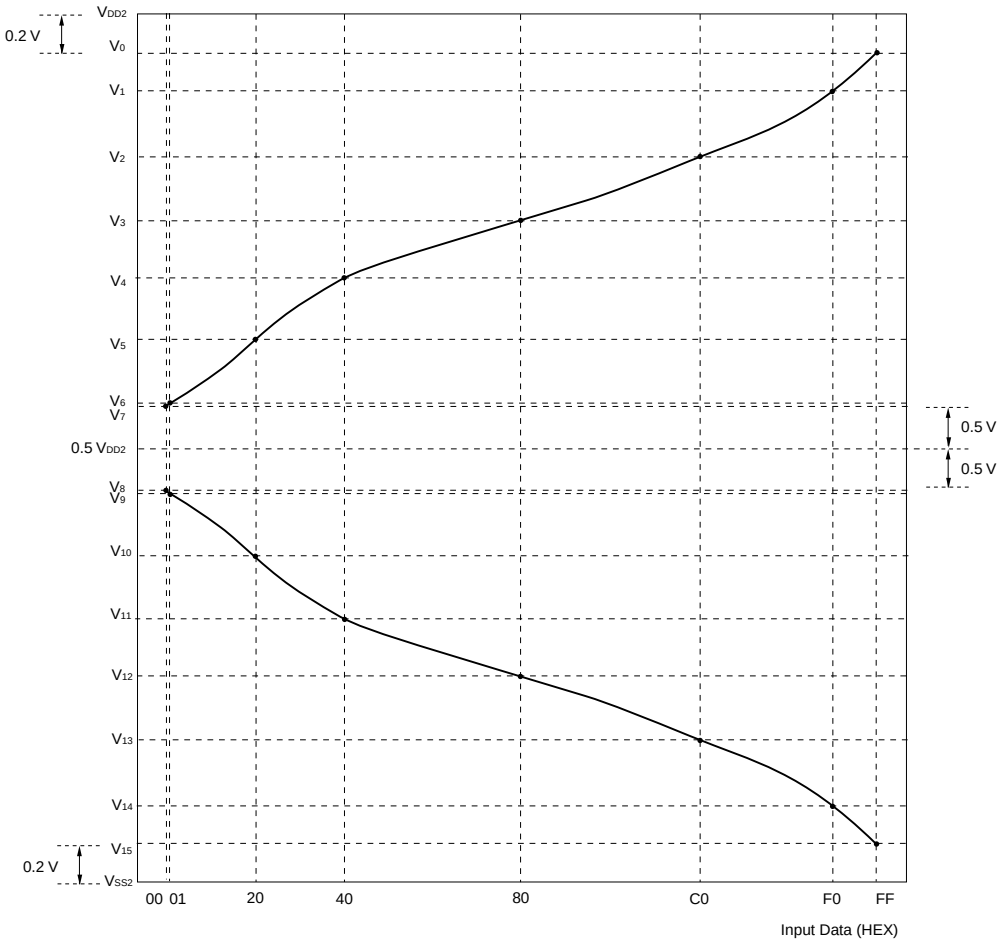
★ V_{DD2}–0.2 V ≥ V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 ≥ 0.5 V_{DD2}+0.5 V

0.5 V_{DD2}–0.5 V ≥ V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} ≥ 0.5 V_{SS2}+0.2 V

Also, V_6 to V_7 and V_8 to V_9 are left open in the LSI. Be sure to input the gray scale level power supply at a constant level to the all pins, as V_0 to V_{15}.

Figures 5-2 and 5-3 show the relationship between the input data and the output voltage and the resistance values of the resistor strings.

Figure 5-1. Relationship between Input Data and γ-corrected Power Supplies



★

Figure 5-2. Relationship between Input Data and Output Voltage (1/4)

V_{DD2}–0.2 V ≥ V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 ≥ 0.5 V_{DD2} + 0.5 V, POL21/22 = L

Input data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage					rn	(Ω)
00H	0	0	0	0	0	0	0	0	V_0'	V7					
01H	0	0	0	0	0	0	0	1	V_1'	V6				r0	86
02H	0	0	0	0	0	0	1	0	V_2'	V6+(V5-V6) X	86	/	2206	r1	86
03H	0	0	0	0	0	0	1	1	V_3'	V6+(V5-V6) X	172	/	2206	r2	86
04H	0	0	0	0	0	1	0	0	V_4'	V6+(V5-V6) X	258	/	2206	r3	86
05H	0	0	0	0	0	1	0	1	V_5'	V6+(V5-V6) X	344	/	2206	r4	86
06H	0	0	0	0	0	1	1	0	V_6'	V6+(V5-V6) X	430	/	2206	r5	84
07H	0	0	0	0	0	1	1	1	V_7'	V6+(V5-V6) X	514	/	2206	r6	84
08H	0	0	0	0	1	0	0	0	V_8'	V6+(V5-V6) X	598	/	2206	r7	82
09H	0	0	0	0	1	0	0	1	V_9'	V6+(V5-V6) X	680	/	2206	r8	82
0AH	0	0	0	0	1	0	1	0	V_{10}'	V6+(V5-V6) X	762	/	2206	r9	80
0BH	0	0	0	0	1	0	1	1	V_{11}'	V6+(V5-V6) X	842	/	2206	r10	78
0CH	0	0	0	0	1	1	0	0	V_{12}'	V6+(V5-V6) X	920	/	2206	r11	78
0DH	0	0	0	0	1	1	0	1	V_{13}'	V6+(V5-V6) X	998	/	2206	r12	76
0EH	0	0	0	0	1	1	1	0	V_{14}'	V6+(V5-V6) X	1074	/	2206	r13	74
0FH	0	0	0	0	1	1	1	1	V_{15}'	V6+(V5-V6) X	1148	/	2206	r14	74
10H	0	0	0	1	0	0	0	0	V_{16}'	V6+(V5-V6) X	1222	/	2206	r15	72
11H	0	0	0	1	0	0	0	1	V_{17}'	V6+(V5-V6) X	1294	/	2206	r16	70
12H	0	0	0	1	0	0	1	0	V_{18}'	V6+(V5-V6) X	1364	/	2206	r17	68
13H	0	0	0	1	0	0	1	1	V_{19}'	V6+(V5-V6) X	1432	/	2206	r18	68
14H	0	0	0	1	0	1	0	0	V_{20}'	V6+(V5-V6) X	1500	/	2206	r19	66
15H	0	0	0	1	0	1	0	1	V_{21}'	V6+(V5-V6) X	1566	/	2206	r20	64
16H	0	0	0	1	0	1	1	0	V_{22}'	V6+(V5-V6) X	1630	/	2206	r21	64
17H	0	0	0	1	0	1	1	1	V_{23}'	V6+(V5-V6) X	1694	/	2206	r22	62
18H	0	0	0	1	1	0	0	0	V_{24}'	V6+(V5-V6) X	1756	/	2206	r23	60
19H	0	0	0	1	1	0	0	1	V_{25}'	V6+(V5-V6) X	1816	/	2206	r24	60
1AH	0	0	0	1	1	0	1	0	V_{26}'	V6+(V5-V6) X	1876	/	2206	r25	58
1BH	0	0	0	1	1	0	1	1	V_{27}'	V6+(V5-V6) X	1934	/	2206	r26	56
1CH	0	0	0	1	1	1	0	0	V_{28}'	V6+(V5-V6) X	1990	/	2206	r27	56
1DH	0	0	0	1	1	1	0	1	V_{29}'	V6+(V5-V6) X	2046	/	2206	r28	54
1EH	0	0	0	1	1	1	1	0	V_{30}'	V6+(V5-V6) X	2100	/	2206	r29	54
1FH	0	0	0	1	1	1	1	1	V_{31}'	V6+(V5-V6) X	2154	/	2206	r30	52
20H	0	0	1	0	0	0	0	0	V_{32}'	V5				r31	52
21H	0	0	1	0	0	0	0	1	V_{33}'	V5+(V4-V5) X	52	/	1304	r32	50
22H	0	0	1	0	0	0	1	0	V_{34}'	V5+(V4-V5) X	102	/	1304	r33	50
23H	0	0	1	0	0	0	1	1	V_{35}'	V5+(V4-V5) X	152	/	1304	r34	48
24H	0	0	1	0	0	1	0	0	V_{36}'	V5+(V4-V5) X	200	/	1304	r35	48
25H	0	0	1	0	0	1	0	1	V_{37}'	V5+(V4-V5) X	248	/	1304	r36	46
26H	0	0	1	0	0	1	1	0	V_{38}'	V5+(V4-V5) X	294	/	1304	r37	46
27H	0	0	1	0	0	1	1	1	V_{39}'	V5+(V4-V5) X	340	/	1304	r38	46
28H	0	0	1	0	1	0	0	0	V_{40}'	V5+(V4-V5) X	386	/	1304	r39	44
29H	0	0	1	0	1	0	0	1	V_{41}'	V5+(V4-V5) X	430	/	1304	r40	44
2AH	0	0	1	0	1	0	1	0	V_{42}'	V5+(V4-V5) X	474	/	1304	r41	44
2BH	0	0	1	0	1	0	1	1	V_{43}'	V5+(V4-V5) X	518	/	1304	r42	42
2CH	0	0	1	0	1	1	0	0	V_{44}'	V5+(V4-V5) X	560	/	1304	r43	42
2DH	0	0	1	0	1	1	0	1	V_{45}'	V5+(V4-V5) X	602	/	1304	r44	42
2EH	0	0	1	0	1	1	1	0	V_{46}'	V5+(V4-V5) X	644	/	1304	r45	40
2FH	0	0	1	0	1	1	1	1	V_{47}'	V5+(V4-V5) X	684	/	1304	r46	40
30H	0	0	1	1	0	0	0	0	V_{48}'	V5+(V4-V5) X	724	/	1304	r47	40
31H	0	0	1	1	0	0	0	1	V_{49}'	V5+(V4-V5) X	764	/	1304	r48	40
32H	0	0	1	1	0	0	1	0	V_{50}'	V5+(V4-V5) X	804	/	1304	r49	38
33H	0	0	1	1	0	0	1	1	V_{51}'	V5+(V4-V5) X	842	/	1304	r50	38
34H	0	0	1	1	0	1	0	0	V_{52}'	V5+(V4-V5) X	880	/	1304	r51	38
35H	0	0	1	1	0	1	0	1	V_{53}'	V5+(V4-V5) X	918	/	1304	r52	38
36H	0	0	1	1	0	1	1	0	V_{54}'	V5+(V4-V5) X	956	/	1304	r53	36
37H	0	0	1	1	0	1	1	1	V_{55}'	V5+(V4-V5) X	992	/	1304	r54	36
38H	0	0	1	1	1	0	0	0	V_{56}'	V5+(V4-V5) X	1028	/	1304	r55	36
39H	0	0	1	1	1	0	0	1	V_{57}'	V5+(V4-V5) X	1064	/	1304	r56	36
3AH	0	0	1	1	1	0	1	0	V_{58}'	V5+(V4-V5) X	1100	/	1304	r57	34
3BH	0	0	1	1	1	0	1	1	V_{59}'	V5+(V4-V5) X	1134	/	1304	r58	34
3CH	0	0	1	1	1	1	0	0	V_{60}'	V5+(V4-V5) X	1168	/	1304	r59	34
3DH	0	0	1	1	1	1	0	1	V_{61}'	V5+(V4-V5) X	1202	/	1304	r60	34
3EH	0	0	1	1	1	1	1	0	V_{62}'	V5+(V4-V5) X	1236	/	1304	r61	34
3FH	0	0	1	1	1	1	1	1	V_{63}'	V5+(V4-V5) X	1270	/	1304	r62	34

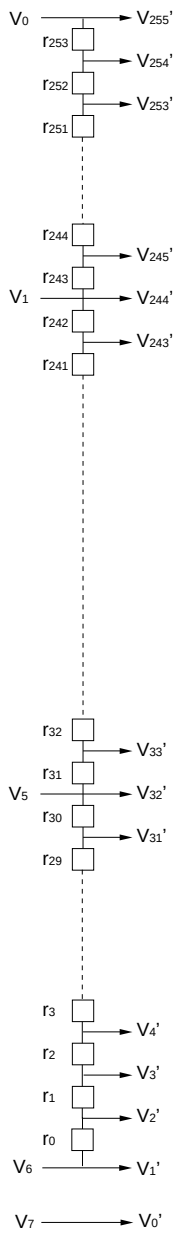
★ **Figure 5-2. Relationship between Input Data and Output Voltage (2/4)**

V_{DD2}–0.2 V ≥ V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 ≥ 0.5 V_{DD2} + 0.5 V, POL21/22 = L

Input data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage		rn	(Ω)
40H	0	1	0	0	0	0	0	0	V_{64}'	V4	r63	32
41H	0	1	0	0	0	0	0	1	V_{65}'	V4+(V3-V4) X 32 / 1772	r64	32
42H	0	1	0	0	0	0	1	0	V_{66}'	V4+(V3-V4) X 64 / 1772	r65	32
43H	0	1	0	0	0	0	1	1	V_{67}'	V4+(V3-V4) X 96 / 1772	r66	32
44H	0	1	0	0	0	1	0	0	V_{68}'	V4+(V3-V4) X 128 / 1772	r67	32
45H	0	1	0	0	0	1	0	1	V_{69}'	V4+(V3-V4) X 160 / 1772	r68	32
46H	0	1	0	0	0	1	1	0	V_{70}'	V4+(V3-V4) X 192 / 1772	r69	32
47H	0	1	0	0	0	1	1	1	V_{71}'	V4+(V3-V4) X 224 / 1772	r70	30
48H	0	1	0	0	1	0	0	0	V_{72}'	V4+(V3-V4) X 254 / 1772	r71	30
49H	0	1	0	0	1	0	0	1	V_{73}'	V4+(V3-V4) X 284 / 1772	r72	30
4AH	0	1	0	0	1	0	1	0	V_{74}'	V4+(V3-V4) X 314 / 1772	r73	30
4BH	0	1	0	0	1	0	1	1	V_{75}'	V4+(V3-V4) X 344 / 1772	r74	30
4CH	0	1	0	0	1	1	0	0	V_{76}'	V4+(V3-V4) X 374 / 1772	r75	30
4DH	0	1	0	0	1	1	0	1	V_{77}'	V4+(V3-V4) X 404 / 1772	r76	30
4EH	0	1	0	0	1	1	1	0	V_{78}'	V4+(V3-V4) X 434 / 1772	r77	30
4FH	0	1	0	0	1	1	1	1	V_{79}'	V4+(V3-V4) X 464 / 1772	r78	30
50H	0	1	0	1	0	0	0	0	V_{80}'	V4+(V3-V4) X 494 / 1772	r79	30
51H	0	1	0	1	0	0	0	1	V_{81}'	V4+(V3-V4) X 524 / 1772	r80	28
52H	0	1	0	1	0	0	1	0	V_{82}'	V4+(V3-V4) X 552 / 1772	r81	28
53H	0	1	0	1	0	0	1	1	V_{83}'	V4+(V3-V4) X 580 / 1772	r82	28
54H	0	1	0	1	0	1	0	0	V_{84}'	V4+(V3-V4) X 608 / 1772	r83	28
55H	0	1	0	1	0	1	0	1	V_{85}'	V4+(V3-V4) X 636 / 1772	r84	28
56H	0	1	0	1	0	1	1	0	V_{86}'	V4+(V3-V4) X 664 / 1772	r85	28
57H	0	1	0	1	0	1	1	1	V_{87}'	V4+(V3-V4) X 692 / 1772	r86	28
58H	0	1	0	1	1	0	0	0	V_{88}'	V4+(V3-V4) X 720 / 1772	r87	28
59H	0	1	0	1	1	0	0	1	V_{89}'	V4+(V3-V4) X 748 / 1772	r88	28
5AH	0	1	0	1	1	0	1	0	V_{90}'	V4+(V3-V4) X 776 / 1772	r89	28
5BH	0	1	0	1	1	0	1	1	V_{91}'	V4+(V3-V4) X 804 / 1772	r90	28
5CH	0	1	0	1	1	1	0	0	V_{92}'	V4+(V3-V4) X 832 / 1772	r91	28
5DH	0	1	0	1	1	1	0	1	V_{93}'	V4+(V3-V4) X 860 / 1772	r92	28
5EH	0	1	0	1	1	1	1	0	V_{94}'	V4+(V3-V4) X 888 / 1772	r93	26
5FH	0	1	0	1	1	1	1	1	V_{95}'	V4+(V3-V4) X 914 / 1772	r94	26
60H	0	1	1	0	0	0	0	0	V_{96}'	V4+(V3-V4) X 940 / 1772	r95	26
61H	0	1	1	0	0	0	0	1	V_{97}'	V4+(V3-V4) X 966 / 1772	r96	26
62H	0	1	1	0	0	0	1	0	V_{98}'	V4+(V3-V4) X 992 / 1772	r97	26
63H	0	1	1	0	0	0	1	1	V_{99}'	V4+(V3-V4) X 1018 / 1772	r98	26
64H	0	1	1	0	0	1	0	0	V_{100}'	V4+(V3-V4) X 1044 / 1772	r99	26
65H	0	1	1	0	0	1	0	1	V_{101}'	V4+(V3-V4) X 1070 / 1772	r100	26
66H	0	1	1	0	0	1	1	0	V_{102}'	V4+(V3-V4) X 1096 / 1772	r101	26
67H	0	1	1	0	0	1	1	1	V_{103}'	V4+(V3-V4) X 1122 / 1772	r102	26
68H	0	1	1	0	1	0	0	0	V_{104}'	V4+(V3-V4) X 1148 / 1772	r103	26
69H	0	1	1	0	1	0	0	1	V_{105}'	V4+(V3-V4) X 1174 / 1772	r104	26
6AH	0	1	1	0	1	0	1	0	V_{106}'	V4+(V3-V4) X 1200 / 1772	r105	26
6BH	0	1	1	0	1	0	1	1	V_{107}'	V4+(V3-V4) X 1226 / 1772	r106	26
6CH	0	1	1	0	1	1	0	0	V_{108}'	V4+(V3-V4) X 1252 / 1772	r107	26
6DH	0	1	1	0	1	1	0	1	V_{109}'	V4+(V3-V4) X 1278 / 1772	r108	26
6EH	0	1	1	0	1	1	1	0	V_{110}'	V4+(V3-V4) X 1304 / 1772	r109	26
6FH	0	1	1	0	1	1	1	1	V_{111}'	V4+(V3-V4) X 1330 / 1772	r110	26
70H	0	1	1	1	0	0	0	0	V_{112}'	V4+(V3-V4) X 1356 / 1772	r111	26
71H	0	1	1	1	0	0	0	1	V_{113}'	V4+(V3-V4) X 1382 / 1772	r112	26
72H	0	1	1	1	0	0	1	0	V_{114}'	V4+(V3-V4) X 1408 / 1772	r113	26
73H	0	1	1	1	0	0	1	1	V_{115}'	V4+(V3-V4) X 1434 / 1772	r114	26
74H	0	1	1	1	0	1	0	0	V_{116}'	V4+(V3-V4) X 1460 / 1772	r115	26
75H	0	1	1	1	0	1	0	1	V_{117}'	V4+(V3-V4) X 1486 / 1772	r116	26
76H	0	1	1	1	0	1	1	0	V_{118}'	V4+(V3-V4) X 1512 / 1772	r117	26
77H	0	1	1	1	0	1	1	1	V_{119}'	V4+(V3-V4) X 1538 / 1772	r118	26
78H	0	1	1	1	1	0	0	0	V_{120}'	V4+(V3-V4) X 1564 / 1772	r119	26
79H	0	1	1	1	1	0	0	1	V_{121}'	V4+(V3-V4) X 1590 / 1772	r120	26
7AH	0	1	1	1	1	0	1	0	V_{122}'	V4+(V3-V4) X 1616 / 1772	r121	26
7BH	0	1	1	1	1	0	1	1	V_{123}'	V4+(V3-V4) X 1642 / 1772	r122	26
7CH	0	1	1	1	1	1	0	0	V_{124}'	V4+(V3-V4) X 1668 / 1772	r123	26
7DH	0	1	1	1	1	1	0	1	V_{125}'	V4+(V3-V4) X 1694 / 1772	r124	26
7EH	0	1	1	1	1	1	1	0	V_{126}'	V4+(V3-V4) X 1720 / 1772	r125	26
7FH	0	1	1	1	1	1	1	1	V_{127}'	V4+(V3-V4) X 1746 / 1772	r126	26

★ **Figure 5-2. Relationship between Input Data and Output Voltage (3/4)**

V_{DD2}–0.2 V ≥ V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 ≥ 0.5 V_{DD2} + 0.5 V, POL21/22 = L



Input data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage		rn	(Ω)
80H	1	0	0	0	0	0	0	0	V_{128}'	V3	r127	26
81H	1	0	0	0	0	0	0	1	V_{129}'	V3+(V2-V3) X 26 / 1710	r128	24
82H	1	0	0	0	0	0	1	0	V_{130}'	V3+(V2-V3) X 50 / 1710	r129	26
83H	1	0	0	0	0	0	1	1	V_{131}'	V3+(V2-V3) X 76 / 1710	r130	24
84H	1	0	0	0	0	1	0	0	V_{132}'	V3+(V2-V3) X 100 / 1710	r131	24
85H	1	0	0	0	0	1	0	1	V_{133}'	V3+(V2-V3) X 124 / 1710	r132	24
86H	1	0	0	0	0	1	1	0	V_{134}'	V3+(V2-V3) X 148 / 1710	r133	24
87H	1	0	0	0	0	1	1	1	V_{135}'	V3+(V2-V3) X 172 / 1710	r134	26
88H	1	0	0	0	1	0	0	0	V_{136}'	V3+(V2-V3) X 198 / 1710	r135	26
89H	1	0	0	0	1	0	0	1	V_{137}'	V3+(V2-V3) X 224 / 1710	r136	26
8AH	1	0	0	0	1	0	1	0	V_{138}'	V3+(V2-V3) X 250 / 1710	r137	26
8BH	1	0	0	0	1	0	1	1	V_{139}'	V3+(V2-V3) X 276 / 1710	r138	26
8CH	1	0	0	0	1	1	0	0	V_{140}'	V3+(V2-V3) X 302 / 1710	r139	26
8DH	1	0	0	0	1	1	0	1	V_{141}'	V3+(V2-V3) X 328 / 1710	r140	26
8EH	1	0	0	0	1	1	1	0	V_{142}'	V3+(V2-V3) X 354 / 1710	r141	26
8FH	1	0	0	0	1	1	1	1	V_{143}'	V3+(V2-V3) X 380 / 1710	r142	26
90H	1	0	0	1	0	0	0	0	V_{144}'	V3+(V2-V3) X 406 / 1710	r143	26
91H	1	0	0	1	0	0	0	1	V_{145}'	V3+(V2-V3) X 432 / 1710	r144	26
92H	1	0	0	1	0	0	1	0	V_{146}'	V3+(V2-V3) X 458 / 1710	r145	26
93H	1	0	0	1	0	0	1	1	V_{147}'	V3+(V2-V3) X 484 / 1710	r146	26
94H	1	0	0	1	0	1	0	0	V_{148}'	V3+(V2-V3) X 510 / 1710	r147	26
95H	1	0	0	1	0	1	0	1	V_{149}'	V3+(V2-V3) X 536 / 1710	r148	26
96H	1	0	0	1	0	1	1	0	V_{150}'	V3+(V2-V3) X 562 / 1710	r149	26
97H	1	0	0	1	0	1	1	1	V_{151}'	V3+(V2-V3) X 588 / 1710	r150	26
98H	1	0	0	1	1	0	0	0	V_{152}'	V3+(V2-V3) X 614 / 1710	r151	26
99H	1	0	0	1	1	0	0	1	V_{153}'	V3+(V2-V3) X 640 / 1710	r152	26
9AH	1	0	0	1	1	0	1	0	V_{154}'	V3+(V2-V3) X 666 / 1710	r153	26
9BH	1	0	0	1	1	0	1	1	V_{155}'	V3+(V2-V3) X 692 / 1710	r154	26
9CH	1	0	0	1	1	1	0	0	V_{156}'	V3+(V2-V3) X 718 / 1710	r155	26
9DH	1	0	0	1	1	1	0	1	V_{157}'	V3+(V2-V3) X 744 / 1710	r156	26
9EH	1	0	0	1	1	1	1	0	V_{158}'	V3+(V2-V3) X 770 / 1710	r157	26
9FH	1	0	0	1	1	1	1	1	V_{159}'	V3+(V2-V3) X 796 / 1710	r158	26
A0H	1	0	1	0	0	0	0	0	V_{160}'	V3+(V2-V3) X 822 / 1710	r159	26
A1H	1	0	1	0	0	0	0	1	V_{161}'	V3+(V2-V3) X 848 / 1710	r160	26
A2H	1	0	1	0	0	0	1	0	V_{162}'	V3+(V2-V3) X 874 / 1710	r161	26
A3H	1	0	1	0	0	0	1	1	V_{163}'	V3+(V2-V3) X 900 / 1710	r162	26
A4H	1	0	1	0	0	1	0	0	V_{164}'	V3+(V2-V3) X 926 / 1710	r163	26
A5H	1	0	1	0	0	1	0	1	V_{165}'	V3+(V2-V3) X 952 / 1710	r164	26
A6H	1	0	1	0	0	1	1	0	V_{166}'	V3+(V2-V3) X 978 / 1710	r165	26
A7H	1	0	1	0	0	1	1	1	V_{167}'	V3+(V2-V3) X 1004 / 1710	r166	26
A8H	1	0	1	0	1	0	0	0	V_{168}'	V3+(V2-V3) X 1030 / 1710	r167	26
A9H	1	0	1	0	1	0	0	1	V_{169}'	V3+(V2-V3) X 1056 / 1710	r168	26
AAH	1	0	1	0	1	0	1	0	V_{170}'	V3+(V2-V3) X 1082 / 1710	r169	26
ABH	1	0	1	0	1	0	1	1	V_{171}'	V3+(V2-V3) X 1108 / 1710	r170	28
ACH	1	0	1	0	1	1	0	0	V_{172}'	V3+(V2-V3) X 1136 / 1710	r171	28
ADH	1	0	1	0	1	1	0	1	V_{173}'	V3+(V2-V3) X 1164 / 1710	r172	28
AEH	1	0	1	0	1	1	1	0	V_{174}'	V3+(V2-V3) X 1192 / 1710	r173	28
AFH	1	0	1	0	1	1	1	1	V_{175}'	V3+(V2-V3) X 1220 / 1710	r174	28
B0H	1	0	1	1	0	0	0	0	V_{176}'	V3+(V2-V3) X 1248 / 1710	r175	28
B1H	1	0	1	1	0	0	0	1	V_{177}'	V3+(V2-V3) X 1276 / 1710	r176	28
B2H	1	0	1	1	0	0	1	0	V_{178}'	V3+(V2-V3) X 1304 / 1710	r177	28
B3H	1	0	1	1	0	0	1	1	V_{179}'	V3+(V2-V3) X 1332 / 1710	r178	28
B4H	1	0	1	1	0	1	0	0	V_{180}'	V3+(V2-V3) X 1360 / 1710	r179	28
B5H	1	0	1	1	0	1	0	1	V_{181}'	V3+(V2-V3) X 1388 / 1710	r180	28
B6H	1	0	1	1	0	1	1	0	V_{182}'	V3+(V2-V3) X 1416 / 1710	r181	28
B7H	1	0	1	1	0	1	1	1	V_{183}'	V3+(V2-V3) X 1444 / 1710	r182	28
B8H	1	0	1	1	1	0	0	0	V_{184}'	V3+(V2-V3) X 1472 / 1710	r183	28
B9H	1	0	1	1	1	0	0	1	V_{185}'	V3+(V2-V3) X 1500 / 1710	r184	30
BAH	1	0	1	1	1	0	1	0	V_{186}'	V3+(V2-V3) X 1530 / 1710	r185	30
BBH	1	0	1	1	1	0	1	1	V_{187}'	V3+(V2-V3) X 1560 / 1710	r186	30
BCH	1	0	1	1	1	1	0	0	V_{188}'	V3+(V2-V3) X 1590 / 1710	r187	30
BDH	1	0	1	1	1	1	0	1	V_{189}'	V3+(V2-V3) X 1620 / 1710	r188	30
BEH	1	0	1	1	1	1	1	0	V_{190}'	V3+(V2-V3) X 1650 / 1710	r189	30
BFH	1	0	1	1	1	1	1	1	V_{191}'	V3+(V2-V3) X 1680 / 1710	r190	30

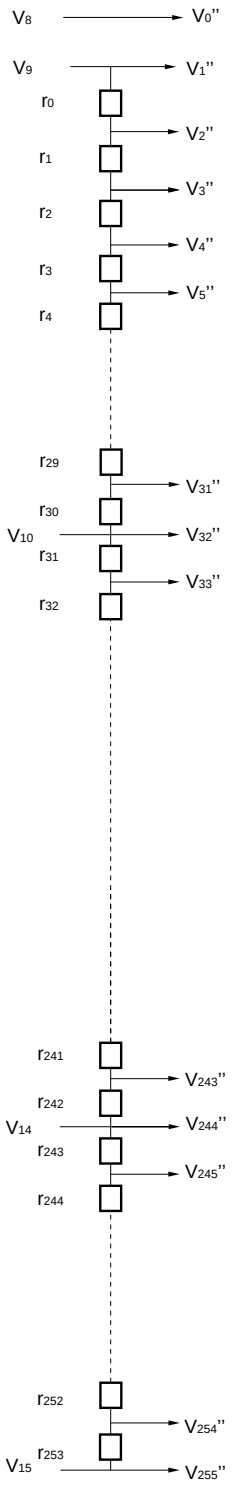
★ **Figure 5-2. Relationship between Input Data and Output Voltage (4/4)**

V_{DD2}–0.2 V ≥ V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 ≥ 0.5 V_{DD2} + 0.5 V, POL21/22 = L

Input data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage					rn	(Ω)
C0H	1	1	0	0	0	0	0	0	V_{192}'	V2				r191	30
C1H	1	1	0	0	0	0	0	1	V_{193}'	V2+(V1-V2) X	30	/	1966	r192	30
C2H	1	1	0	0	0	0	1	0	V_{194}'	V2+(V1-V2) X	60	/	1966	r193	30
C3H	1	1	0	0	0	0	1	1	V_{195}'	V2+(V1-V2) X	90	/	1966	r194	32
C4H	1	1	0	0	0	1	0	0	V_{196}'	V2+(V1-V2) X	122	/	1966	r195	32
C5H	1	1	0	0	0	1	0	1	V_{197}'	V2+(V1-V2) X	154	/	1966	r196	32
C6H	1	1	0	0	0	1	1	0	V_{198}'	V2+(V1-V2) X	186	/	1966	r197	32
C7H	1	1	0	0	0	1	1	1	V_{199}'	V2+(V1-V2) X	218	/	1966	r198	32
C8H	1	1	0	0	1	0	0	0	V_{200}'	V2+(V1-V2) X	250	/	1966	r199	32
C9H	1	1	0	0	1	0	0	1	V_{201}'	V2+(V1-V2) X	282	/	1966	r200	32
CAH	1	1	0	0	1	0	1	0	V_{202}'	V2+(V1-V2) X	314	/	1966	r201	34
CBH	1	1	0	0	1	0	1	1	V_{203}'	V2+(V1-V2) X	348	/	1966	r202	34
CCH	1	1	0	0	1	1	0	0	V_{204}'	V2+(V1-V2) X	382	/	1966	r203	34
CDH	1	1	0	0	1	1	0	1	V_{205}'	V2+(V1-V2) X	416	/	1966	r204	34
CEH	1	1	0	0	1	1	1	0	V_{206}'	V2+(V1-V2) X	450	/	1966	r205	34
CFH	1	1	0	0	1	1	1	1	V_{207}'	V2+(V1-V2) X	484	/	1966	r206	34
D0H	1	1	0	1	0	0	0	0	V_{208}'	V2+(V1-V2) X	518	/	1966	r207	36
D1H	1	1	0	1	0	0	0	1	V_{209}'	V2+(V1-V2) X	554	/	1966	r208	36
D2H	1	1	0	1	0	0	1	0	V_{210}'	V2+(V1-V2) X	590	/	1966	r209	36
D3H	1	1	0	1	0	0	1	1	V_{211}'	V2+(V1-V2) X	626	/	1966	r210	36
D4H	1	1	0	1	0	1	0	0	V_{212}'	V2+(V1-V2) X	662	/	1966	r211	36
D5H	1	1	0	1	0	1	0	1	V_{213}'	V2+(V1-V2) X	698	/	1966	r212	38
D6H	1	1	0	1	0	1	1	0	V_{214}'	V2+(V1-V2) X	736	/	1966	r213	38
D7H	1	1	0	1	0	1	1	1	V_{215}'	V2+(V1-V2) X	774	/	1966	r214	38
D8H	1	1	0	1	1	0	0	0	V_{216}'	V2+(V1-V2) X	812	/	1966	r215	38
D9H	1	1	0	1	1	0	0	1	V_{217}'	V2+(V1-V2) X	850	/	1966	r216	40
DAH	1	1	0	1	1	0	1	0	V_{218}'	V2+(V1-V2) X	890	/	1966	r217	40
DBH	1	1	0	1	1	0	1	1	V_{219}'	V2+(V1-V2) X	930	/	1966	r218	40
DCH	1	1	0	1	1	1	0	0	V_{220}'	V2+(V1-V2) X	970	/	1966	r219	42
DDH	1	1	0	1	1	1	0	1	V_{221}'	V2+(V1-V2) X	1012	/	1966	r220	42
DEH	1	1	0	1	1	1	1	0	V_{222}'	V2+(V1-V2) X	1054	/	1966	r221	42
DFH	1	1	0	1	1	1	1	1	V_{223}'	V2+(V1-V2) X	1096	/	1966	r222	44
E0H	1	1	1	0	0	0	0	0	V_{224}'	V2+(V1-V2) X	1140	/	1966	r223	44
E1H	1	1	1	0	0	0	0	1	V_{225}'	V2+(V1-V2) X	1184	/	1966	r224	44
E2H	1	1	1	0	0	0	1	0	V_{226}'	V2+(V1-V2) X	1228	/	1966	r225	46
E3H	1	1	1	0	0	0	1	1	V_{227}'	V2+(V1-V2) X	1274	/	1966	r226	46
E4H	1	1	1	0	0	1	0	0	V_{228}'	V2+(V1-V2) X	1320	/	1966	r227	48
E5H	1	1	1	0	0	1	0	1	V_{229}'	V2+(V1-V2) X	1368	/	1966	r228	48
E6H	1	1	1	0	0	1	1	0	V_{230}'	V2+(V1-V2) X	1416	/	1966	r229	50
E7H	1	1	1	0	0	1	1	1	V_{231}'	V2+(V1-V2) X	1466	/	1966	r230	50
E8H	1	1	1	0	1	0	0	0	V_{232}'	V2+(V1-V2) X	1516	/	1966	r231	52
E9H	1	1	1	0	1	0	0	1	V_{233}'	V2+(V1-V2) X	1568	/	1966	r232	52
EAH	1	1	1	0	1	0	1	0	V_{234}'	V2+(V1-V2) X	1620	/	1966	r233	54
EBH	1	1	1	0	1	0	1	1	V_{235}'	V2+(V1-V2) X	1674	/	1966	r234	56
ECH	1	1	1	0	1	1	0	0	V_{236}'	V2+(V1-V2) X	1730	/	1966	r235	56
EDH	1	1	1	0	1	1	0	1	V_{237}'	V2+(V1-V2) X	1786	/	1966	r236	58
EEH	1	1	1	0	1	1	1	0	V_{238}'	V2+(V1-V2) X	1844	/	1966	r237	60
EFH	1	1	1	0	1	1	1	1	V_{239}'	V2+(V1-V2) X	1904	/	1966	r238	62
F0H	1	1	1	1	0	0	0	0	V_{240}'	V1				r239	64
F1H	1	1	1	1	0	0	0	1	V_{241}'	V1+(V0-V1) X	64	/	1322	r240	66
F2H	1	1	1	1	0	0	1	0	V_{242}'	V1+(V0-V1) X	130	/	1322	r241	68
F3H	1	1	1	1	0	0	1	1	V_{243}'	V1+(V0-V1) X	198	/	1322	r242	70
F4H	1	1	1	1	0	1	0	0	V_{244}'	V1+(V0-V1) X	268	/	1322	r243	72
F5H	1	1	1	1	0	1	0	1	V_{245}'	V1+(V0-V1) X	340	/	1322	r244	76
F6H	1	1	1	1	0	1	1	0	V_{246}'	V1+(V0-V1) X	416	/	1322	r245	80
F7H	1	1	1	1	0	1	1	1	V_{247}'	V1+(V0-V1) X	496	/	1322	r246	82
F8H	1	1	1	1	1	0	0	0	V_{248}'	V1+(V0-V1) X	578	/	1322	r247	86
F9H	1	1	1	1	1	0	0	1	V_{249}'	V1+(V0-V1) X	664	/	1322	r248	92
FAH	1	1	1	1	1	0	1	0	V_{250}'	V1+(V0-V1) X	756	/	1322	r249	98
FBH	1	1	1	1	1	0	1	1	V_{251}'	V1+(V0-V1) X	854	/	1322	r250	104
FCH	1	1	1	1	1	1	0	0	V_{252}'	V1+(V0-V1) X	958	/	1322	r251	112
FDH	1	1	1	1	1	1	0	1	V_{253}'	V1+(V0-V1) X	1070	/	1322	r252	120
FEH	1	1	1	1	1	1	1	0	V_{254}'	V1+(V0-V1) X	1190	/	1322	r253	132
FFH	1	1	1	1	1	1	1	1	V_{255}'	V0				TOTAL	10280

★ **Figure 5-3. Relationship between Input Data and Output Voltage (1/4)**

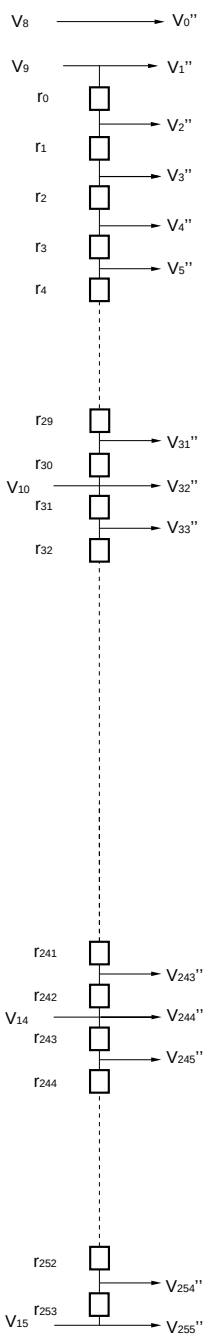
0.5 V_{DD2}–0.5 V ≥ V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} ≥ V_{SS2}+0.2 V, POL21/22 = L



Input data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage		rn	(Ω)
00H	0	0	0	0	0	0	0	0	V_0"	V8		
01H	0	0	0	0	0	0	0	1	V_1"	V9	r0	86
02H	0	0	0	0	0	0	1	0	V_2"	V10+(V9-V10) X 2120 / 2206	r1	86
03H	0	0	0	0	0	0	1	1	V_3"	V10+(V9-V10) X 2034 / 2206	r2	86
04H	0	0	0	0	0	1	0	0	V_4"	V10+(V9-V10) X 1948 / 2206	r3	86
05H	0	0	0	0	0	1	0	1	V_5"	V10+(V9-V10) X 1862 / 2206	r4	86
06H	0	0	0	0	0	1	1	0	V_6"	V10+(V9-V10) X 1776 / 2206	r5	84
07H	0	0	0	0	0	1	1	1	V_7"	V10+(V9-V10) X 1692 / 2206	r6	84
08H	0	0	0	0	1	0	0	0	V_8"	V10+(V9-V10) X 1608 / 2206	r7	82
09H	0	0	0	0	1	0	0	1	V_9"	V10+(V9-V10) X 1526 / 2206	r8	82
0AH	0	0	0	0	1	0	1	0	V_{10}"	V10+(V9-V10) X 1444 / 2206	r9	80
0BH	0	0	0	0	1	0	1	1	V_{11}"	V10+(V9-V10) X 1364 / 2206	r10	78
0CH	0	0	0	0	1	1	0	0	V_{12}"	V10+(V9-V10) X 1286 / 2206	r11	78
0DH	0	0	0	0	1	1	0	1	V_{13}"	V10+(V9-V10) X 1208 / 2206	r12	76
0EH	0	0	0	0	1	1	1	0	V_{14}"	V10+(V9-V10) X 1132 / 2206	r13	74
0FH	0	0	0	0	1	1	1	1	V_{15}"	V10+(V9-V10) X 1058 / 2206	r14	74
10H	0	0	0	1	0	0	0	0	V_{16}"	V10+(V9-V10) X 984 / 2206	r15	72
11H	0	0	0	1	0	0	0	1	V_{17}"	V10+(V9-V10) X 912 / 2206	r16	70
12H	0	0	0	1	0	0	1	0	V_{18}"	V10+(V9-V10) X 842 / 2206	r17	68
13H	0	0	0	1	0	0	1	1	V_{19}"	V10+(V9-V10) X 774 / 2206	r18	68
14H	0	0	0	1	0	1	0	0	V_{20}"	V10+(V9-V10) X 706 / 2206	r19	66
15H	0	0	0	1	0	1	0	1	V_{21}"	V10+(V9-V10) X 640 / 2206	r20	64
16H	0	0	0	1	0	1	1	0	V_{22}"	V10+(V9-V10) X 576 / 2206	r21	64
17H	0	0	0	1	0	1	1	1	V_{23}"	V10+(V9-V10) X 512 / 2206	r22	62
18H	0	0	0	1	1	0	0	0	V_{24}"	V10+(V9-V10) X 450 / 2206	r23	60
19H	0	0	0	1	1	0	0	1	V_{25}"	V10+(V9-V10) X 390 / 2206	r24	60
1AH	0	0	0	1	1	0	1	0	V_{26}"	V10+(V9-V10) X 330 / 2206	r25	58
1BH	0	0	0	1	1	0	1	1	V_{27}"	V10+(V9-V10) X 272 / 2206	r26	56
1CH	0	0	0	1	1	1	0	0	V_{28}"	V10+(V9-V10) X 216 / 2206	r27	56
1DH	0	0	0	1	1	1	0	1	V_{29}"	V10+(V9-V10) X 160 / 2206	r28	54
1EH	0	0	0	1	1	1	1	0	V_{30}"	V10+(V9-V10) X 106 / 2206	r29	54
1FH	0	0	0	1	1	1	1	1	V_{31}"	V10+(V9-V10) X 52 / 2206	r30	52
20H	0	0	1	0	0	0	0	0	V_{32}"	V10	r31	52
21H	0	0	1	0	0	0	0	1	V_{33}"	V11+(V10-V11) X 1252 / 1304	r32	50
22H	0	0	1	0	0	0	1	0	V_{34}"	V11+(V10-V11) X 1202 / 1304	r33	50
23H	0	0	1	0	0	0	1	1	V_{35}"	V11+(V10-V11) X 1152 / 1304	r34	48
24H	0	0	1	0	0	1	0	0	V_{36}"	V11+(V10-V11) X 1104 / 1304	r35	48
25H	0	0	1	0	0	1	0	1	V_{37}"	V11+(V10-V11) X 1056 / 1304	r36	46
26H	0	0	1	0	0	1	1	0	V_{38}"	V11+(V10-V11) X 1010 / 1304	r37	46
27H	0	0	1	0	0	1	1	1	V_{39}"	V11+(V10-V11) X 964 / 1304	r38	46
28H	0	0	1	0	1	0	0	0	V_{40}"	V11+(V10-V11) X 918 / 1304	r39	44
29H	0	0	1	0	1	0	0	1	V_{41}"	V11+(V10-V11) X 874 / 1304	r40	44
2AH	0	0	1	0	1	0	1	0	V_{42}"	V11+(V10-V11) X 830 / 1304	r41	44
2BH	0	0	1	0	1	0	1	1	V_{43}"	V11+(V10-V11) X 786 / 1304	r42	42
2CH	0	0	1	0	1	1	0	0	V_{44}"	V11+(V10-V11) X 744 / 1304	r43	42
2DH	0	0	1	0	1	1	0	1	V_{45}"	V11+(V10-V11) X 702 / 1304	r44	42
2EH	0	0	1	0	1	1	1	0	V_{46}"	V11+(V10-V11) X 660 / 1304	r45	40
2FH	0	0	1	0	1	1	1	1	V_{47}"	V11+(V10-V11) X 620 / 1304	r46	40
30H	0	0	1	1	0	0	0	0	V_{48}"	V11+(V10-V11) X 580 / 1304	r47	40
31H	0	0	1	1	0	0	0	1	V_{49}"	V11+(V10-V11) X 540 / 1304	r48	40
32H	0	0	1	1	0	0	1	0	V_{50}"	V11+(V10-V11) X 500 / 1304	r49	38
33H	0	0	1	1	0	0	1	1	V_{51}"	V11+(V10-V11) X 462 / 1304	r50	38
34H	0	0	1	1	0	1	0	0	V_{52}"	V11+(V10-V11) X 424 / 1304	r51	38
35H	0	0	1	1	0	1	0	1	V_{53}"	V11+(V10-V11) X 386 / 1304	r52	38
36H	0	0	1	1	0	1	1	0	V_{54}"	V11+(V10-V11) X 348 / 1304	r53	36
37H	0	0	1	1	0	1	1	1	V_{55}"	V11+(V10-V11) X 312 / 1304	r54	36
38H	0	0	1	1	1	0	0	0	V_{56}"	V11+(V10-V11) X 276 / 1304	r55	36
39H	0	0	1	1	1	0	0	1	V_{57}"	V11+(V10-V11) X 240 / 1304	r56	36
3AH	0	0	1	1	1	0	1	0	V_{58}"	V11+(V10-V11) X 204 / 1304	r57	34
3BH	0	0	1	1	1	0	1	1	V_{59}"	V11+(V10-V11) X 170 / 1304	r58	34
3CH	0	0	1	1	1	1	0	0	V_{60}"	V11+(V10-V11) X 136 / 1304	r59	34
3DH	0	0	1	1	1	1	0	1	V_{61}"	V11+(V10-V11) X 102 / 1304	r60	34
3EH	0	0	1	1	1	1	1	0	V_{62}"	V11+(V10-V11) X 68 / 1304	r61	34
3FH	0	0	1	1	1	1	1	1	V_{63}"	V11+(V10-V11) X 34 / 1304	r62	34

★ **Figure 5-3. Relationship between Input Data and Output Voltage (2/4)**

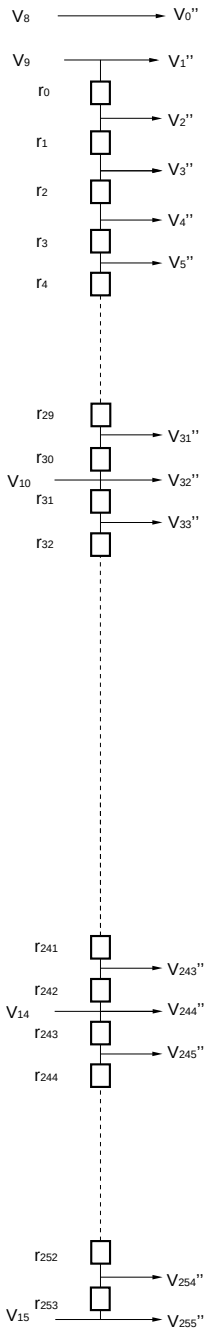
0.5 V_{DD2}–0.5 V ≥ V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} ≥ V_{SS2}+0.2 V, POL21/22 = L



Input data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage		rn	(Ω)
40H	0	1	0	0	0	0	0	0	V_{64}"	V11	r63	32
41H	0	1	0	0	0	0	0	1	V_{65}"	V12+(V11-V12) X 1740 / 1772	r64	32
42H	0	1	0	0	0	0	1	0	V_{66}"	V12+(V11-V12) X 1708 / 1772	r65	32
43H	0	1	0	0	0	0	1	1	V_{67}"	V12+(V11-V12) X 1676 / 1772	r66	32
44H	0	1	0	0	0	1	0	0	V_{68}"	V12+(V11-V12) X 1644 / 1772	r67	32
45H	0	1	0	0	0	1	0	1	V_{69}"	V12+(V11-V12) X 1612 / 1772	r68	32
46H	0	1	0	0	0	1	1	0	V_{70}"	V12+(V11-V12) X 1580 / 1772	r69	32
47H	0	1	0	0	0	1	1	1	V_{71}"	V12+(V11-V12) X 1548 / 1772	r70	30
48H	0	1	0	0	1	0	0	0	V_{72}"	V12+(V11-V12) X 1518 / 1772	r71	30
49H	0	1	0	0	1	0	0	1	V_{73}"	V12+(V11-V12) X 1488 / 1772	r72	30
4AH	0	1	0	0	1	0	1	0	V_{74}"	V12+(V11-V12) X 1458 / 1772	r73	30
4BH	0	1	0	0	1	0	1	1	V_{75}"	V12+(V11-V12) X 1428 / 1772	r74	30
4CH	0	1	0	0	1	1	0	0	V_{76}"	V12+(V11-V12) X 1398 / 1772	r75	30
4DH	0	1	0	0	1	1	0	1	V_{77}"	V12+(V11-V12) X 1368 / 1772	r76	30
4EH	0	1	0	0	1	1	1	0	V_{78}"	V12+(V11-V12) X 1338 / 1772	r77	30
4FH	0	1	0	0	1	1	1	1	V_{79}"	V12+(V11-V12) X 1308 / 1772	r78	30
50H	0	1	0	1	0	0	0	0	V_{80}"	V12+(V11-V12) X 1278 / 1772	r79	30
51H	0	1	0	1	0	0	0	1	V_{81}"	V12+(V11-V12) X 1248 / 1772	r80	28
52H	0	1	0	1	0	0	1	0	V_{82}"	V12+(V11-V12) X 1220 / 1772	r81	28
53H	0	1	0	1	0	0	1	1	V_{83}"	V12+(V11-V12) X 1192 / 1772	r82	28
54H	0	1	0	1	0	1	0	0	V_{84}"	V12+(V11-V12) X 1164 / 1772	r83	28
55H	0	1	0	1	0	1	0	1	V_{85}"	V12+(V11-V12) X 1136 / 1772	r84	28
56H	0	1	0	1	0	1	1	0	V_{86}"	V12+(V11-V12) X 1108 / 1772	r85	28
57H	0	1	0	1	0	1	1	1	V_{87}"	V12+(V11-V12) X 1080 / 1772	r86	28
58H	0	1	0	1	1	0	0	0	V_{88}"	V12+(V11-V12) X 1052 / 1772	r87	28
59H	0	1	0	1	1	0	0	1	V_{89}"	V12+(V11-V12) X 1024 / 1772	r88	28
5AH	0	1	0	1	1	0	1	0	V_{90}"	V12+(V11-V12) X 996 / 1772	r89	28
5BH	0	1	0	1	1	0	1	1	V_{91}"	V12+(V11-V12) X 968 / 1772	r90	28
5CH	0	1	0	1	1	1	0	0	V_{92}"	V12+(V11-V12) X 940 / 1772	r91	28
5DH	0	1	0	1	1	1	0	1	V_{93}"	V12+(V11-V12) X 912 / 1772	r92	28
5EH	0	1	0	1	1	1	1	0	V_{94}"	V12+(V11-V12) X 884 / 1772	r93	26
5FH	0	1	0	1	1	1	1	1	V_{95}"	V12+(V11-V12) X 858 / 1772	r94	26
60H	0	1	1	0	0	0	0	0	V_{96}"	V12+(V11-V12) X 832 / 1772	r95	26
61H	0	1	1	0	0	0	0	1	V_{97}"	V12+(V11-V12) X 806 / 1772	r96	26
62H	0	1	1	0	0	0	1	0	V_{98}"	V12+(V11-V12) X 780 / 1772	r97	26
63H	0	1	1	0	0	0	1	1	V_{99}"	V12+(V11-V12) X 754 / 1772	r98	26
64H	0	1	1	0	0	1	0	0	V_{100}"	V12+(V11-V12) X 728 / 1772	r99	26
65H	0	1	1	0	0	1	0	1	V_{101}"	V12+(V11-V12) X 702 / 1772	r100	26
66H	0	1	1	0	0	1	1	0	V_{102}"	V12+(V11-V12) X 676 / 1772	r101	26
67H	0	1	1	0	0	1	1	1	V_{103}"	V12+(V11-V12) X 650 / 1772	r102	26
68H	0	1	1	0	1	0	0	0	V_{104}"	V12+(V11-V12) X 624 / 1772	r103	26
69H	0	1	1	0	1	0	0	1	V_{105}"	V12+(V11-V12) X 598 / 1772	r104	26
6AH	0	1	1	0	1	0	1	0	V_{106}"	V12+(V11-V12) X 572 / 1772	r105	26
6BH	0	1	1	0	1	0	1	1	V_{107}"	V12+(V11-V12) X 546 / 1772	r106	26
6CH	0	1	1	0	1	1	0	0	V_{108}"	V12+(V11-V12) X 520 / 1772	r107	26
6DH	0	1	1	0	1	1	0	1	V_{109}"	V12+(V11-V12) X 494 / 1772	r108	26
6EH	0	1	1	0	1	1	1	0	V_{110}"	V12+(V11-V12) X 468 / 1772	r109	26
6FH	0	1	1	0	1	1	1	1	V_{111}"	V12+(V11-V12) X 442 / 1772	r110	26
70H	0	1	1	1	0	0	0	0	V_{112}"	V12+(V11-V12) X 416 / 1772	r111	26
71H	0	1	1	1	0	0	0	1	V_{113}"	V12+(V11-V12) X 390 / 1772	r112	26
72H	0	1	1	1	0	0	1	0	V_{114}"	V12+(V11-V12) X 364 / 1772	r113	26
73H	0	1	1	1	0	0	1	1	V_{115}"	V12+(V11-V12) X 338 / 1772	r114	26
74H	0	1	1	1	0	1	0	0	V_{116}"	V12+(V11-V12) X 312 / 1772	r115	26
75H	0	1	1	1	0	1	0	1	V_{117}"	V12+(V11-V12) X 286 / 1772	r116	26
76H	0	1	1	1	0	1	1	0	V_{118}"	V12+(V11-V12) X 260 / 1772	r117	26
77H	0	1	1	1	0	1	1	1	V_{119}"	V12+(V11-V12) X 234 / 1772	r118	26
78H	0	1	1	1	1	0	0	0	V_{120}"	V12+(V11-V12) X 208 / 1772	r119	26
79H	0	1	1	1	1	0	0	1	V_{121}"	V12+(V11-V12) X 182 / 1772	r120	26
7AH	0	1	1	1	1	0	1	0	V_{122}"	V12+(V11-V12) X 156 / 1772	r121	26
7BH	0	1	1	1	1	0	1	1	V_{123}"	V12+(V11-V12) X 130 / 1772	r122	26
7CH	0	1	1	1	1	1	0	0	V_{124}"	V12+(V11-V12) X 104 / 1772	r123	26
7DH	0	1	1	1	1	1	0	1	V_{125}"	V12+(V11-V12) X 78 / 1772	r124	26
7EH	0	1	1	1	1	1	1	0	V_{126}"	V12+(V11-V12) X 52 / 1772	r125	26
7FH	0	1	1	1	1	1	1	1	V_{127}"	V12+(V11-V12) X 26 / 1772	r126	26

★ **Figure 5-3. Relationship between Input Data and Output Voltage (3/4)**

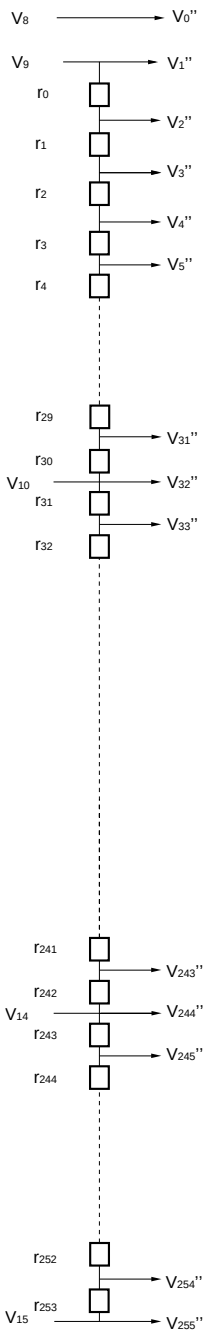
0.5 V_{DD2}–0.5 V ≥ V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} ≥ V_{SS2}+0.2 V, POL21/22 = L



Input data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage					rn	(Ω)
80H	1	0	0	0	0	0	0	0	V_{128}"	V12				r127	26
81H	1	0	0	0	0	0	0	1	V_{129}"	V13+(V12-V13) X	1684	/	1710	r128	24
82H	1	0	0	0	0	0	1	0	V_{130}"	V13+(V12-V13) X	1660	/	1710	r129	26
83H	1	0	0	0	0	0	1	1	V_{131}"	V13+(V12-V13) X	1634	/	1710	r130	24
84H	1	0	0	0	0	1	0	0	V_{132}"	V13+(V12-V13) X	1610	/	1710	r131	24
85H	1	0	0	0	0	1	0	1	V_{133}"	V13+(V12-V13) X	1586	/	1710	r132	24
86H	1	0	0	0	0	1	1	0	V_{134}"	V13+(V12-V13) X	1562	/	1710	r133	24
87H	1	0	0	0	0	1	1	1	V_{135}"	V13+(V12-V13) X	1538	/	1710	r134	26
88H	1	0	0	0	1	0	0	0	V_{136}"	V13+(V12-V13) X	1512	/	1710	r135	26
89H	1	0	0	0	1	0	0	1	V_{137}"	V13+(V12-V13) X	1486	/	1710	r136	26
8AH	1	0	0	0	1	0	1	0	V_{138}"	V13+(V12-V13) X	1460	/	1710	r137	26
8BH	1	0	0	0	1	0	1	1	V_{139}"	V13+(V12-V13) X	1434	/	1710	r138	26
8CH	1	0	0	0	1	1	0	0	V_{140}"	V13+(V12-V13) X	1408	/	1710	r139	26
8DH	1	0	0	0	1	1	0	1	V_{141}"	V13+(V12-V13) X	1382	/	1710	r140	26
8EH	1	0	0	0	1	1	1	0	V_{142}"	V13+(V12-V13) X	1356	/	1710	r141	26
8FH	1	0	0	0	1	1	1	1	V_{143}"	V13+(V12-V13) X	1330	/	1710	r142	26
90H	1	0	0	1	0	0	0	0	V_{144}"	V13+(V12-V13) X	1304	/	1710	r143	26
91H	1	0	0	1	0	0	0	1	V_{145}"	V13+(V12-V13) X	1278	/	1710	r144	26
92H	1	0	0	1	0	0	1	0	V_{146}"	V13+(V12-V13) X	1252	/	1710	r145	26
93H	1	0	0	1	0	0	1	1	V_{147}"	V13+(V12-V13) X	1226	/	1710	r146	26
94H	1	0	0	1	0	1	0	0	V_{148}"	V13+(V12-V13) X	1200	/	1710	r147	26
95H	1	0	0	1	0	1	0	1	V_{149}"	V13+(V12-V13) X	1174	/	1710	r148	26
96H	1	0	0	1	0	1	1	0	V_{150}"	V13+(V12-V13) X	1148	/	1710	r149	26
97H	1	0	0	1	0	1	1	1	V_{151}"	V13+(V12-V13) X	1122	/	1710	r150	26
98H	1	0	0	1	1	0	0	0	V_{152}"	V13+(V12-V13) X	1096	/	1710	r151	26
99H	1	0	0	1	1	0	0	1	V_{153}"	V13+(V12-V13) X	1070	/	1710	r152	26
9AH	1	0	0	1	1	0	1	0	V_{154}"	V13+(V12-V13) X	1044	/	1710	r153	26
9BH	1	0	0	1	1	0	1	1	V_{155}"	V13+(V12-V13) X	1018	/	1710	r154	26
9CH	1	0	0	1	1	1	0	0	V_{156}"	V13+(V12-V13) X	992	/	1710	r155	26
9DH	1	0	0	1	1	1	0	1	V_{157}"	V13+(V12-V13) X	966	/	1710	r156	26
9EH	1	0	0	1	1	1	1	0	V_{158}"	V13+(V12-V13) X	940	/	1710	r157	26
9FH	1	0	0	1	1	1	1	1	V_{159}"	V13+(V12-V13) X	914	/	1710	r158	26
A0H	1	0	1	0	0	0	0	0	V_{160}"	V13+(V12-V13) X	888	/	1710	r159	26
A1H	1	0	1	0	0	0	0	1	V_{161}"	V13+(V12-V13) X	862	/	1710	r160	26
A2H	1	0	1	0	0	0	1	0	V_{162}"	V13+(V12-V13) X	836	/	1710	r161	26
A3H	1	0	1	0	0	0	1	1	V_{163}"	V13+(V12-V13) X	810	/	1710	r162	26
A4H	1	0	1	0	0	1	0	0	V_{164}"	V13+(V12-V13) X	784	/	1710	r163	26
A5H	1	0	1	0	0	1	0	1	V_{165}"	V13+(V12-V13) X	758	/	1710	r164	26
A6H	1	0	1	0	0	1	1	0	V_{166}"	V13+(V12-V13) X	732	/	1710	r165	26
A7H	1	0	1	0	0	1	1	1	V_{167}"	V13+(V12-V13) X	706	/	1710	r166	26
A8H	1	0	1	0	1	0	0	0	V_{168}"	V13+(V12-V13) X	680	/	1710	r167	26
A9H	1	0	1	0	1	0	0	1	V_{169}"	V13+(V12-V13) X	654	/	1710	r168	26
AAH	1	0	1	0	1	0	1	0	V_{170}"	V13+(V12-V13) X	628	/	1710	r169	26
ABH	1	0	1	0	1	0	1	1	V_{171}"	V13+(V12-V13) X	602	/	1710	r170	28
ACH	1	0	1	0	1	1	0	0	V_{172}"	V13+(V12-V13) X	574	/	1710	r171	28
ADH	1	0	1	0	1	1	0	1	V_{173}"	V13+(V12-V13) X	546	/	1710	r172	28
AEH	1	0	1	0	1	1	1	0	V_{174}"	V13+(V12-V13) X	518	/	1710	r173	28
AFH	1	0	1	0	1	1	1	1	V_{175}"	V13+(V12-V13) X	490	/	1710	r174	28
B0H	1	0	1	1	0	0	0	0	V_{176}"	V13+(V12-V13) X	462	/	1710	r175	28
B1H	1	0	1	1	0	0	0	1	V_{177}"	V13+(V12-V13) X	434	/	1710	r176	28
B2H	1	0	1	1	0	0	1	0	V_{178}"	V13+(V12-V13) X	406	/	1710	r177	28
B3H	1	0	1	1	0	0	1	1	V_{179}"	V13+(V12-V13) X	378	/	1710	r178	28
B4H	1	0	1	1	0	1	0	0	V_{180}"	V13+(V12-V13) X	350	/	1710	r179	28
B5H	1	0	1	1	0	1	0	1	V_{181}"	V13+(V12-V13) X	322	/	1710	r180	28
B6H	1	0	1	1	0	1	1	0	V_{182}"	V13+(V12-V13) X	294	/	1710	r181	28
B7H	1	0	1	1	0	1	1	1	V_{183}"	V13+(V12-V13) X	266	/	1710	r182	28
B8H	1	0	1	1	1	0	0	0	V_{184}"	V13+(V12-V13) X	238	/	1710	r183	28
B9H	1	0	1	1	1	0	0	1	V_{185}"	V13+(V12-V13) X	210	/	1710	r184	30
BAH	1	0	1	1	1	0	1	0	V_{186}"	V13+(V12-V13) X	180	/	1710	r185	30
BBH	1	0	1	1	1	0	1	1	V_{187}"	V13+(V12-V13) X	150	/	1710	r186	30
BCH	1	0	1	1	1	1	0	0	V_{188}"	V13+(V12-V13) X	120	/	1710	r187	30
BDH	1	0	1	1	1	1	0	1	V_{189}"	V13+(V12-V13) X	90	/	1710	r188	30
BEH	1	0	1	1	1	1	1	0	V_{190}"	V13+(V12-V13) X	60	/	1710	r189	30
BFH	1	0	1	1	1	1	1	1	V_{191}"	V13+(V12-V13) X	30	/	1710	r190	30

★ **Figure 5-3. Relationship between Input Data and Output Voltage (4/4)**

0.5 V_{DD2}–0.5 V ≥ V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} ≥ V_{SS2}+0.2 V, POL21/22 = L



Input data	D_{X7}	D_{X6}	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output voltage					rn	(Ω)
C0H	1	1	0	0	0	0	0	0	V_{192}"	V13				r191	30
C1H	1	1	0	0	0	0	0	1	V_{193}"	V14+(V13-V14) X	1936	/	1966	r192	30
C2H	1	1	0	0	0	0	1	0	V_{194}"	V14+(V13-V14) X	1906	/	1966	r193	30
C3H	1	1	0	0	0	0	1	1	V_{195}"	V14+(V13-V14) X	1876	/	1966	r194	32
C4H	1	1	0	0	0	1	0	0	V_{196}"	V14+(V13-V14) X	1844	/	1966	r195	32
C5H	1	1	0	0	0	1	0	1	V_{197}"	V14+(V13-V14) X	1812	/	1966	r196	32
C6H	1	1	0	0	0	1	1	0	V_{198}"	V14+(V13-V14) X	1780	/	1966	r197	32
C7H	1	1	0	0	0	1	1	1	V_{199}"	V14+(V13-V14) X	1748	/	1966	r198	32
C8H	1	1	0	0	1	0	0	0	V_{200}"	V14+(V13-V14) X	1716	/	1966	r199	32
C9H	1	1	0	0	1	0	0	1	V_{201}"	V14+(V13-V14) X	1684	/	1966	r200	32
CAH	1	1	0	0	1	0	1	0	V_{202}"	V14+(V13-V14) X	1652	/	1966	r201	34
CBH	1	1	0	0	1	0	1	1	V_{203}"	V14+(V13-V14) X	1618	/	1966	r202	34
CCH	1	1	0	0	1	1	0	0	V_{204}"	V14+(V13-V14) X	1584	/	1966	r203	34
CDH	1	1	0	0	1	1	0	1	V_{205}"	V14+(V13-V14) X	1550	/	1966	r204	34
CEH	1	1	0	0	1	1	1	0	V_{206}"	V14+(V13-V14) X	1516	/	1966	r205	34
CFH	1	1	0	0	1	1	1	1	V_{207}"	V14+(V13-V14) X	1482	/	1966	r206	34
D0H	1	1	0	1	0	0	0	0	V_{208}"	V14+(V13-V14) X	1448	/	1966	r207	36
D1H	1	1	0	1	0	0	0	1	V_{209}"	V14+(V13-V14) X	1412	/	1966	r208	36
D2H	1	1	0	1	0	0	1	0	V_{210}"	V14+(V13-V14) X	1376	/	1966	r209	36
D3H	1	1	0	1	0	0	1	1	V_{211}"	V14+(V13-V14) X	1340	/	1966	r210	36
D4H	1	1	0	1	0	1	0	0	V_{212}"	V14+(V13-V14) X	1304	/	1966	r211	36
D5H	1	1	0	1	0	1	0	1	V_{213}"	V14+(V13-V14) X	1268	/	1966	r212	38
D6H	1	1	0	1	0	1	1	0	V_{214}"	V14+(V13-V14) X	1230	/	1966	r213	38
D7H	1	1	0	1	0	1	1	1	V_{215}"	V14+(V13-V14) X	1192	/	1966	r214	38
D8H	1	1	0	1	1	0	0	0	V_{216}"	V14+(V13-V14) X	1154	/	1966	r215	38
D9H	1	1	0	1	1	0	0	1	V_{217}"	V14+(V13-V14) X	1116	/	1966	r216	40
DAH	1	1	0	1	1	0	1	0	V_{218}"	V14+(V13-V14) X	1076	/	1966	r217	40
DBH	1	1	0	1	1	0	1	1	V_{219}"	V14+(V13-V14) X	1036	/	1966	r218	40
DCH	1	1	0	1	1	1	0	0	V_{220}"	V14+(V13-V14) X	996	/	1966	r219	42
DDH	1	1	0	1	1	1	0	1	V_{221}"	V14+(V13-V14) X	954	/	1966	r220	42
DEH	1	1	0	1	1	1	1	0	V_{222}"	V14+(V13-V14) X	912	/	1966	r221	42
DFH	1	1	0	1	1	1	1	1	V_{223}"	V14+(V13-V14) X	870	/	1966	r222	44
E0H	1	1	1	0	0	0	0	0	V_{224}"	V14+(V13-V14) X	826	/	1966	r223	44
E1H	1	1	1	0	0	0	0	1	V_{225}"	V14+(V13-V14) X	782	/	1966	r224	44
E2H	1	1	1	0	0	0	1	0	V_{226}"	V14+(V13-V14) X	738	/	1966	r225	46
E3H	1	1	1	0	0	0	1	1	V_{227}"	V14+(V13-V14) X	692	/	1966	r226	46
E4H	1	1	1	0	0	1	0	0	V_{228}"	V14+(V13-V14) X	646	/	1966	r227	48
E5H	1	1	1	0	0	1	0	1	V_{229}"	V14+(V13-V14) X	598	/	1966	r228	48
E6H	1	1	1	0	0	1	1	0	V_{230}"	V14+(V13-V14) X	550	/	1966	r229	50
E7H	1	1	1	0	0	1	1	1	V_{231}"	V14+(V13-V14) X	500	/	1966	r230	50
E8H	1	1	1	0	1	0	0	0	V_{232}"	V14+(V13-V14) X	450	/	1966	r231	52
E9H	1	1	1	0	1	0	0	1	V_{233}"	V14+(V13-V14) X	398	/	1966	r232	52
EAH	1	1	1	0	1	0	1	0	V_{234}"	V14+(V13-V14) X	346	/	1966	r233	54
EBH	1	1	1	0	1	0	1	1	V_{235}"	V14+(V13-V14) X	292	/	1966	r234	56
ECH	1	1	1	0	1	1	0	0	V_{236}"	V14+(V13-V14) X	236	/	1966	r235	56
EDH	1	1	1	0	1	1	0	1	V_{237}"	V14+(V13-V14) X	180	/	1966	r236	58
EEH	1	1	1	0	1	1	1	0	V_{238}"	V14+(V13-V14) X	122	/	1966	r237	60
EFH	1	1	1	0	1	1	1	1	V_{239}"	V14+(V13-V14) X	62	/	1966	r238	62
F0H	1	1	1	1	0	0	0	0	V_{240}"	V14				r239	64
F1H	1	1	1	1	0	0	0	1	V_{241}"	V15+(V14-V15) X	1258	/	1322	r240	66
F2H	1	1	1	1	0	0	1	0	V_{242}"	V15+(V14-V15) X	1192	/	1322	r241	68
F3H	1	1	1	1	0	0	1	1	V_{243}"	V15+(V14-V15) X	1124	/	1322	r242	70
F4H	1	1	1	1	0	1	0	0	V_{244}"	V15+(V14-V15) X	1054	/	1322	r243	72
F5H	1	1	1	1	0	1	0	1	V_{245}"	V15+(V14-V15) X	982	/	1322	r244	76
F6H	1	1	1	1	0	1	1	0	V_{246}"	V15+(V14-V15) X	906	/	1322	r245	80
F7H	1	1	1	1	0	1	1	1	V_{247}"	V15+(V14-V15) X	826	/	1322	r246	82
F8H	1	1	1	1	1	0	0	0	V_{248}"	V15+(V14-V15) X	744	/	1322	r247	86
F9H	1	1	1	1	1	0	0	1	V_{249}"	V15+(V14-V15) X	658	/	1322	r248	92
FAH	1	1	1	1	1	0	1	0	V_{250}"	V15+(V14-V15) X	566	/	1322	r249	98
FBH	1	1	1	1	1	0	1	1	V_{251}"	V15+(V14-V15) X	468	/	1322	r250	104
FCH	1	1	1	1	1	1	0	0	V_{252}"	V15+(V14-V15) X	364	/	1322	r251	112
FDH	1	1	1	1	1	1	0	1	V_{253}"	V15+(V14-V15) X	252	/	1322	r252	120
FEH	1	1	1	1	1	1	1	0	V_{254}"	V15+(V14-V15) X	132	/	1322	r253	132
FFH	1	1	1	1	1	1	1	1	V_{255}"	V15				TOTAL	10280

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 8 bits x 2 RGBs (6 dots)

Input width: 48 bits (2-pixel data)

(1) R,/L = H (Right shift)

Output	S_1	S_2	S_3	S_4	…	S_{383}	S_{384}
Data	D_{00} to D_{07}	D_{10} to D_{17}	D_{20} to D_{27}	D_{30} to D_{37}	…	D_{40} to D_{47}	D_{50} to D_{57}

(2) R,/L = L (Left shift)

Output	S_1	S_2	S_3	S_4	…	S_{383}	S_{384}
Data	D_{00} to D_{07}	D_{10} to D_{17}	D_{20} to D_{27}	D_{30} to D_{37}	…	D_{40} to D_{47}	D_{50} to D_{57}

POL	S_{2n-1} Note	S_{2n} Note
L	V_0 to V_7	V_8 to V_{15}
H	V_8 to V_{15}	V_0 to V_7

Note S_{2n-1} (Odd output), S_{2n} (Even output), n = 1, 2, ..., 192.

7. RELATIONSHIP BETWEEN MODE, STB, SRC, ORC, POL, AND OUTPUT WAVEFORM

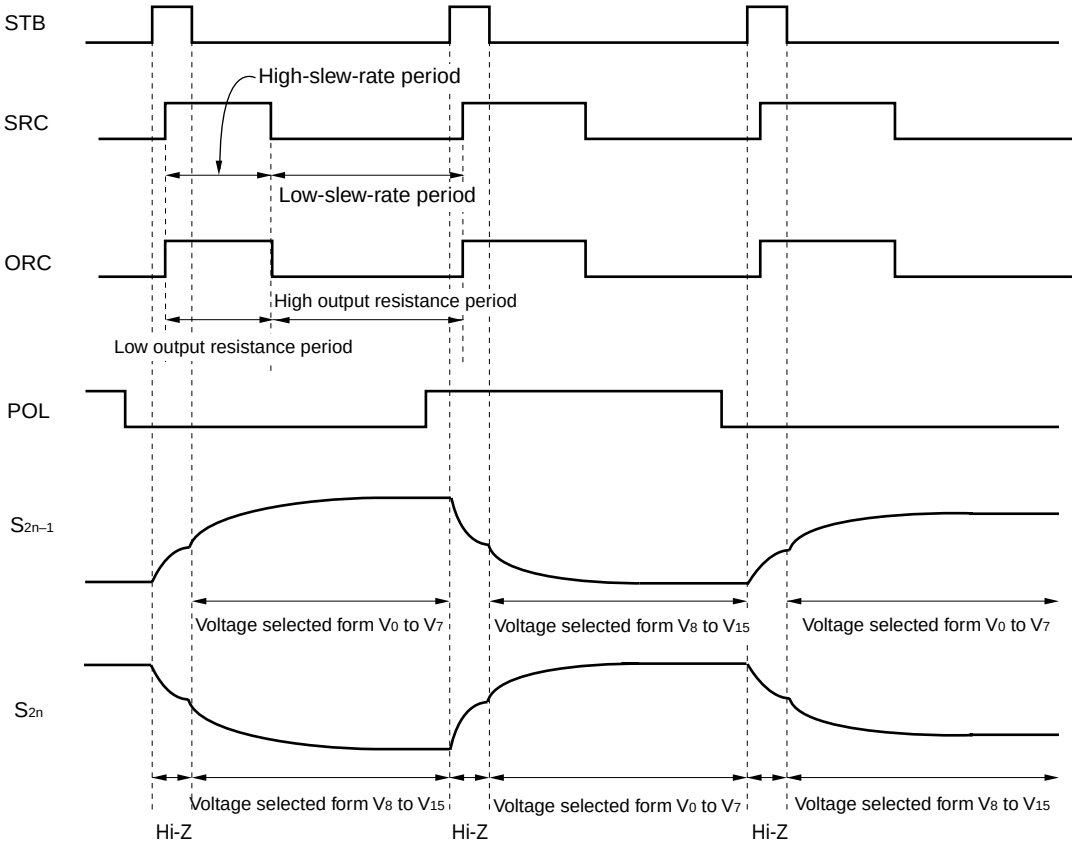
When the MODE pin is high level or left open and STB is high level, all outputs are reset (shorted) and the gray-scale voltage is output to LCD in synchronization with the falling edge of STB.

When the MODE pin is low level and STB is high level, all outputs became Hi-Z and the gray-scale voltage is output to the LCD in synchronization with the falling edge of STB.

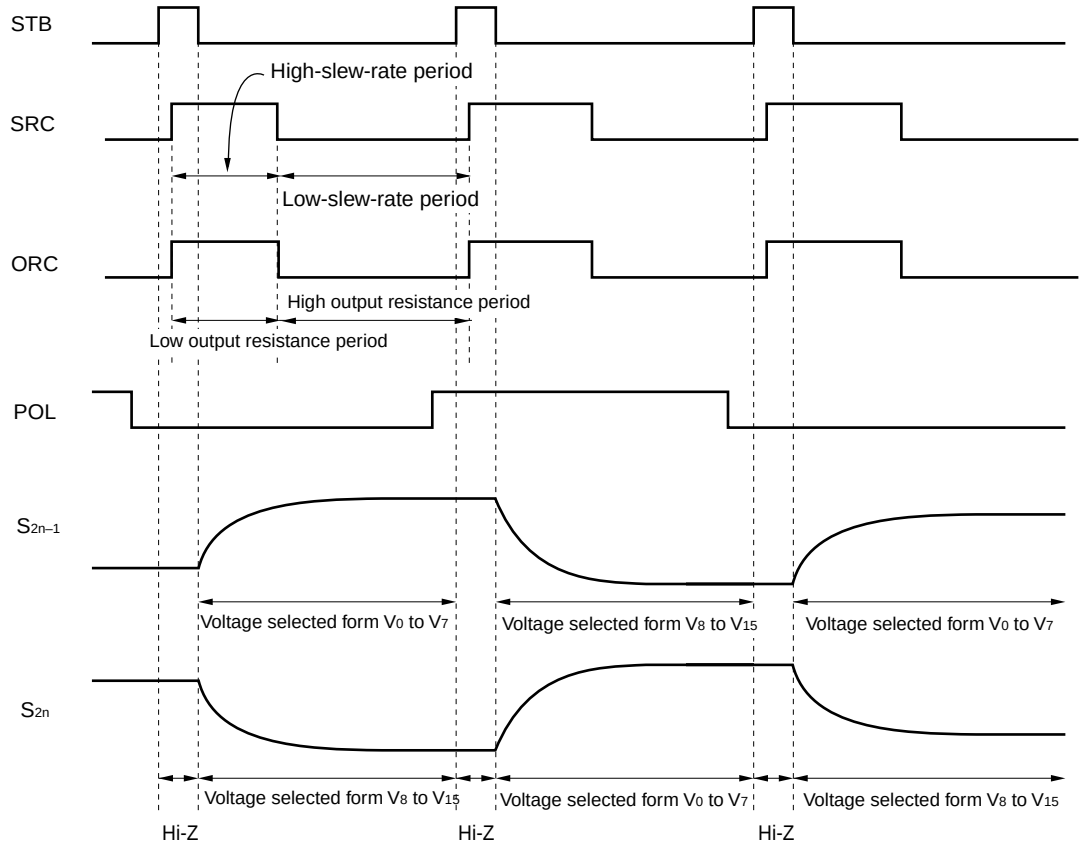
Also, setting the SRC pin to high level allows the bias current value of the output amplifier to rise temporarily, and setting the ORC pin to high level allows the output resistance value of the amplifier to lower temporarily.

For the timing and the processing of STB, SRC, or ORC during a high-level period, We recommend a thorough evaluation of the LCD panel specifications in advance.

(1) When MODE is high level or left open



(2) When MODE is low level



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8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic part supply voltage	V_{DD1}	–0.5 to +4.0	V
Driver part supply voltage	V_{DD2}	–0.5 to +17.0	V
Logic part input voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Driver part input voltage	V_{I2}	–0.5 to V_{DD2} + 0.5	V
Logic part output voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver part output voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Operating ambient temperature	T_A	–10 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
★	Logic part supply voltage	V_{DD1}		2.5		3.4	V
★	Driver part supply voltage	V_{DD2}	V_{SEL} = H	12.5	13.0	13.5	V
			V_{SEL} = L or open	14.5	15.0	15.5	
	High-level input voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
	Low-level input voltage	V_{IL}		0		0.3 V_{DD1}	V
★	γ-corrected voltage	V_0 to V_7		0.5 V_{DD2}+0.5		V_{DD2}–0.2	V
		V_8 to V_{15}		0.2		0.5 V_{DD2}–0.5	V
	Driver part output voltage	V_O		0.2		V_{DD2}–0.2	V
★	Clock frequency	f_{CLK}	2.5 V ≤ V_{DD1} ≤ 3.0 V			55	MHz
			3.0 V ≤ V_{DD1} ≤ 3.4 V			70	MHz

★ **Electrical Characteristics (T_A = –10 to +75°C, V_{DD1} = 2.5 to 3.4 V, V_{DD2} = 12.5 to 15.5 V, V_{SS1} = V_{SS2} = 0 V)**

	Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
	Input leakage current	I_{IL}					±1.0	μA
	High-level output voltage	V_{OH}	STHR (STHL), I_{OH} = 0 mA		V_{DD1}–0.1			V
	Low-level output voltage	V_{OL}	STHR (STHL), I_{OL} = 0 mA				0.1	V
★	γ-corrected power supply static current consumption	I_γ	V_{DD2} = 15.0 V	V_0, V_8	340	681	1020	mA
			V_0 to V_7 = V_8 to V_{15} = 7.0 V	V_7, V_{15}	–1020	–681	–340	mA
★	Driver output current	I_{VOH}	V_X = 12 V, V_{OUT} = 11 V **Note**				–0.40	mA
		I_{VOL}	V_X = 1 V, V_{OUT} = 2 V **Note**		0.65			mA
★	Output voltage deviation	ΔV_O	T_A = 25°C V_{SS2} + 1.0 V to V_{DD2} – 1.0 V			±10	±20	mV
★	Output swing voltage difference deviation	ΔV_{P-P1}	V_{DD1} = 3.3 V V_{DD2} = 15.0 V T_A = 25°C	V_{OUT} = 7.0 to 8.0 V **Note**		±5	±10	mV
		ΔV_{P-P2}		V_{OUT} = 4.0 to 11.0 V **Note**		±7	±15	mV
		ΔV_{P-P3}		V_{OUT} = 1.0 to 14.0 V **Note**		±10	±20	mV
★	Logic part dynamic current consumption	I_{DD1}	V_{DD1}			1.3	10	mA
★	Driver part dynamic current consumption	I_{DD2}	V_{DD2}, with no load			12	30	mA

Note V_X refers to the output voltage of analog output pins S_1 to S_{384}.
V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{384}.

Cautions 1. f_{STB} = 64 kHz, f_{CLK} = 54 MHz

2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

3. Refers to the current consumption per driver when cascades are connected under the assumption of SXGA single-sided mounting (10 units).

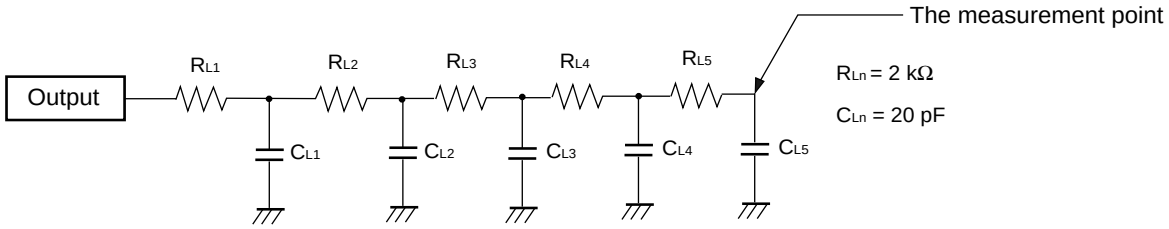
★ **Switching Characteristics (T_A = –10 to +75°C, V_{DD1} = 2.5 to 3.4 V, V_{DD2} = 12.5 to 15.5 V, V_{SS1} = V_{SS2} = 0 V)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start pulse delay time	t_{PLH1}	C_L = 15 pF			12	ns
★ Driver output delay time	t_{PLH2} Note	C_L = 100 pF, R_L = 10 kΩ			5	μs
	t_{PLH3} Note				10	μs
	t_{PHL2} Note				5	μs
	t_{PHL3} Note				10	μs
Input capacitance	C_{I1}	logic input, except STHR (STHL), T_A = 25°C		5	10	pF
	C_{I2}	STHR (STHL), T_A = 25°C		10	15	pF

Note t_{PLH2}, t_{PHL2} refer to the arrival time from falling edge of STB to target voltage ±10%

t_{PLH3}, t_{PHL3} refer to the arrival time from falling edge of STB to target voltage ±0.02 V (condition: V_O = 3.0 V ↔12.0 V)

★ **Test Condition**



★ **Timing Requirements (T_A = –10 to +75°C, V_{DD1} = 2.5 to 3.4 V, V_{SS1} = 0 V, $t_r = t_f$ = 5.0 ns)**

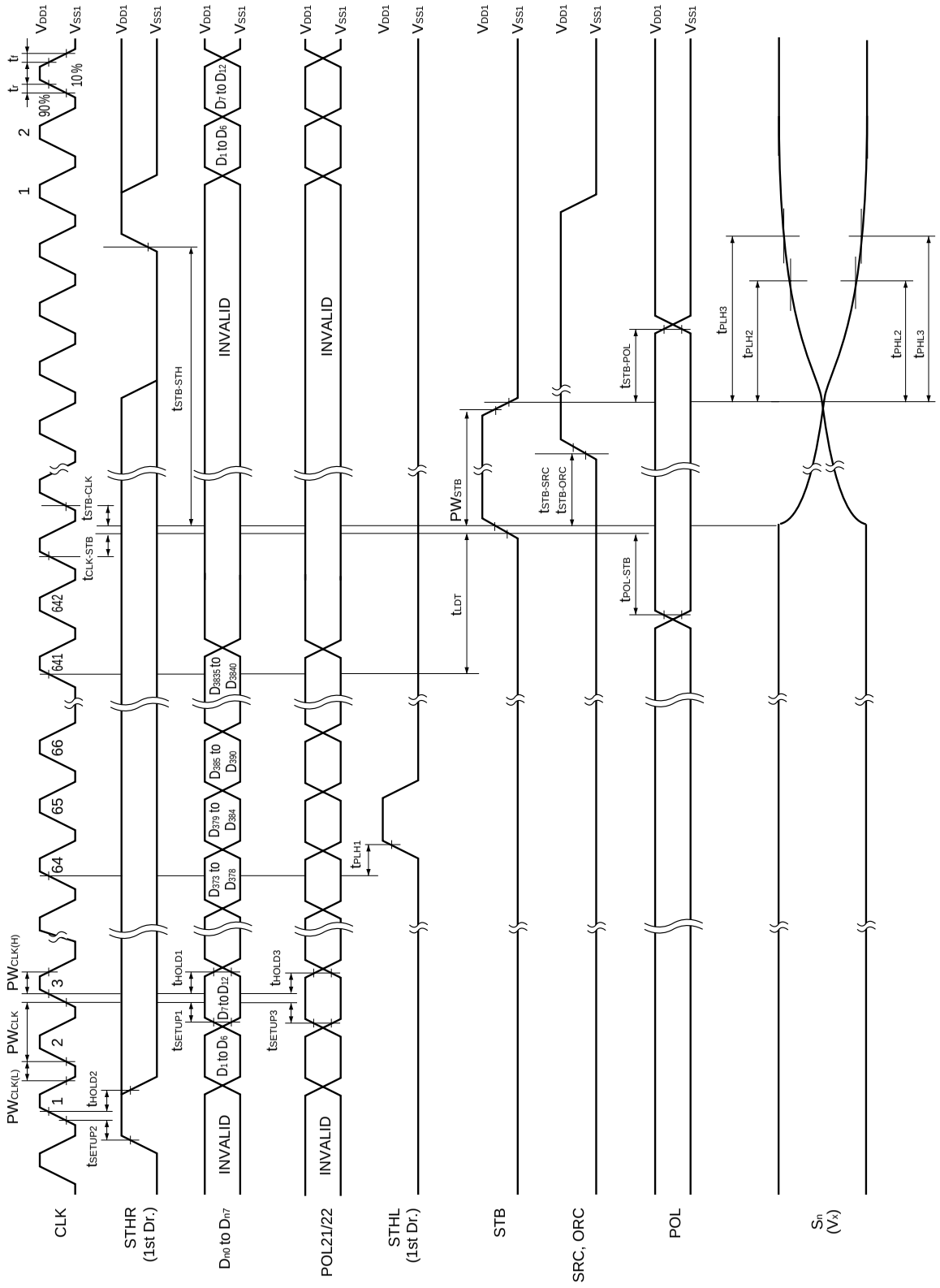
	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
★	Clock pulse width	PW_{CLK}	2.5 V ≤ V_{DD1} ≤ 3.0 V	18			ns
			3.0 V ≤ V_{DD1} ≤ 3.4 V	14			
★	Clock pulse high period	$PW_{CLK (H)}$	2.5 V ≤ V_{DD1} ≤ 3.0 V	6			ns
			3.0 V ≤ V_{DD1} ≤ 3.4 V	4			
	Clock pulse low period	$PW_{CLK (L)}$		4			ns
	Data setup time	t_{SETUP1}		0			ns
	Data hold time	t_{HOLD1}		4			ns
	Start pulse setup time	t_{SETUP2}		0			ns
	Start pulse hold time	t_{HOLD2}		4			ns
	POL21/22 setup time	t_{SETUP3}		0			ns
	POL21/22 hold time	t_{HOLD3}		4			ns
★	STB pulse width	PW_{STB}		1.0			μs
	Last data timing	t_{LDT}		2			CLK
	CLK-STB time	$t_{CLK-STB}$	CLK ↑→ STB↑	4			ns
	STB-CLK time	$t_{STB-CLK}$	STB ↑→ CLK↑	4			ns
	Time between STB and start pulse	$t_{STB-STH}$	STB ↑→ STHR (STHL) ↑	2			CLK
	POL-STB time	$t_{POL-STB}$	POL ↑ or ↓→ STB ↑	4			ns
	STB-POL time	$t_{STB-POL}$	STB ↓→ POL ↓ or ↑	4			ns
	STB-SRC time	$t_{STB-SRC}$	STB ↑ → SRC ↑	0			ns
	STB-ORC time	$t_{STB-ORC}$	STB ↓→ ORC ↑	0			ns

★ **Remark** Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

Switching Characteristic Waveform

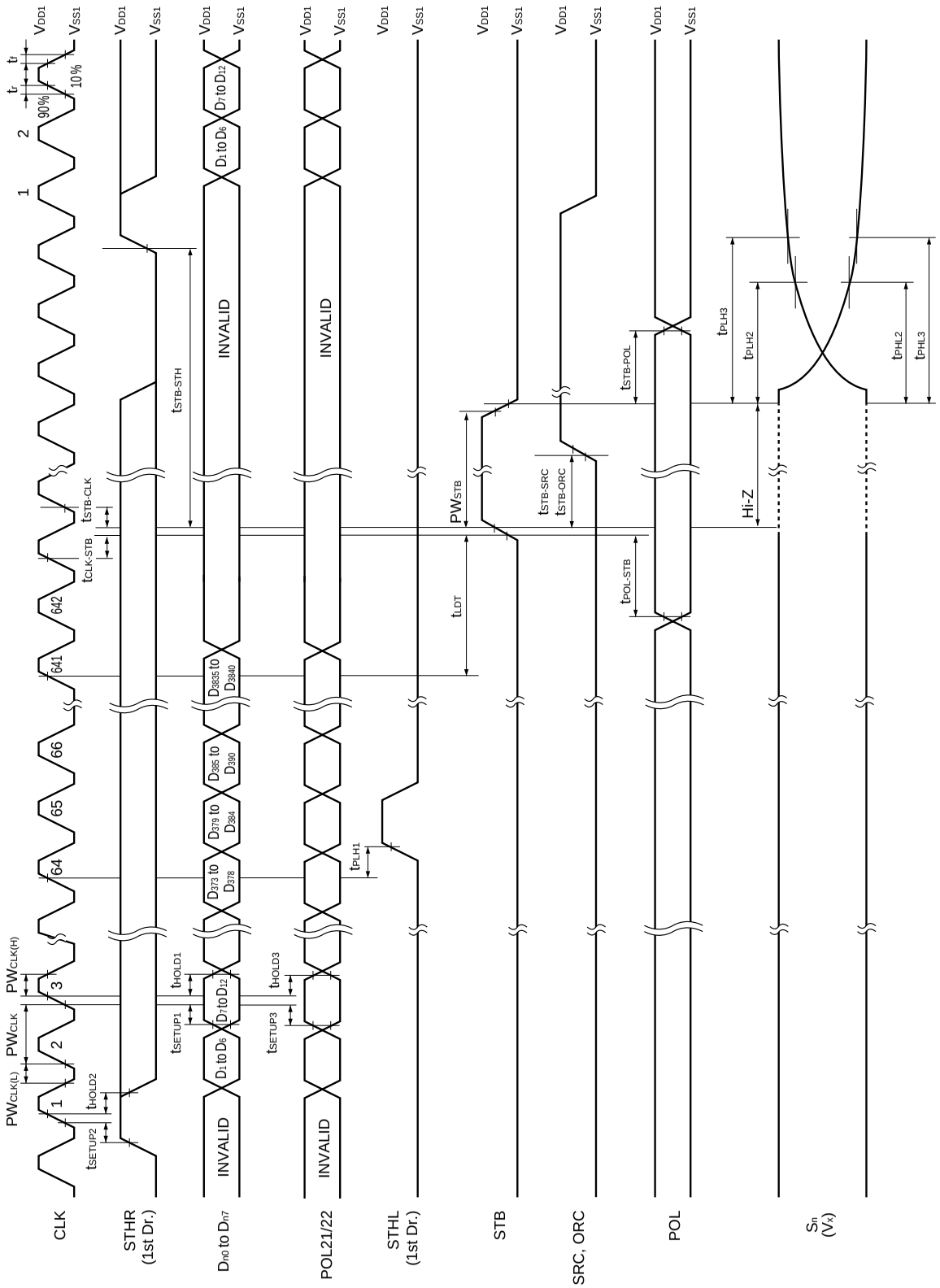
★ **(1) R,/L= H, MODE = H or open**

Unless otherwise specified, V_{IH}, V_{IL} are defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1} (Numbers clock and display data are example when in SXGA).



★ **(2) R,/L= H, MODE = L**

Unless otherwise specified, V_{IH}, V_{IL} are defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1} (Numbers clock and display data are example when in SXGA).



9. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD16721.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16721N-xxx: TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 sec, pressure 100g (per solder).
	ACF (Adhesive Conductive Film)	Temporaly bonding 70 to 100°C, pressure 3 to 8 kg/cm^2, time 3 to 5 sec. Real bonding 165 to 180°C, pressure 25 to 45 kg/cm^2, time 30 to 40 sec (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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