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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUITS

Phase-out/Discontinued

μPD16663

240-OUTPUT LCD COLUMN (SEGMENT) DRIVER WITH BUILT-IN RAM

DESCRIPTION

The μPD16663 is a column (segment) driver device with built-in RAM. It is capable of driving a full-dot LCD.

There are 240 outputs that, with the 240 × 160 × 4-bit built-in display RAM, enable a 16-gray scale display. The sixteen gray scales can be selected arbitrarily from a 49-stage palette. When combined with the μPD16667, this device can drive displays of 240 × 160 to 480 × 320 dots.

FEATURES

- Built-in display RAM: 240 × 160 × 4 bits
- Logic voltage: 3.0 to 3.6 V
- Duty cycle: 1/160
- Number of outputs: 240
- Gray scales: 16 (selectable from a palette of 49)
- Memory management: Packed pixel
- Compatible with 8-bit/16-bit data buses

ORDERING INFORMATION

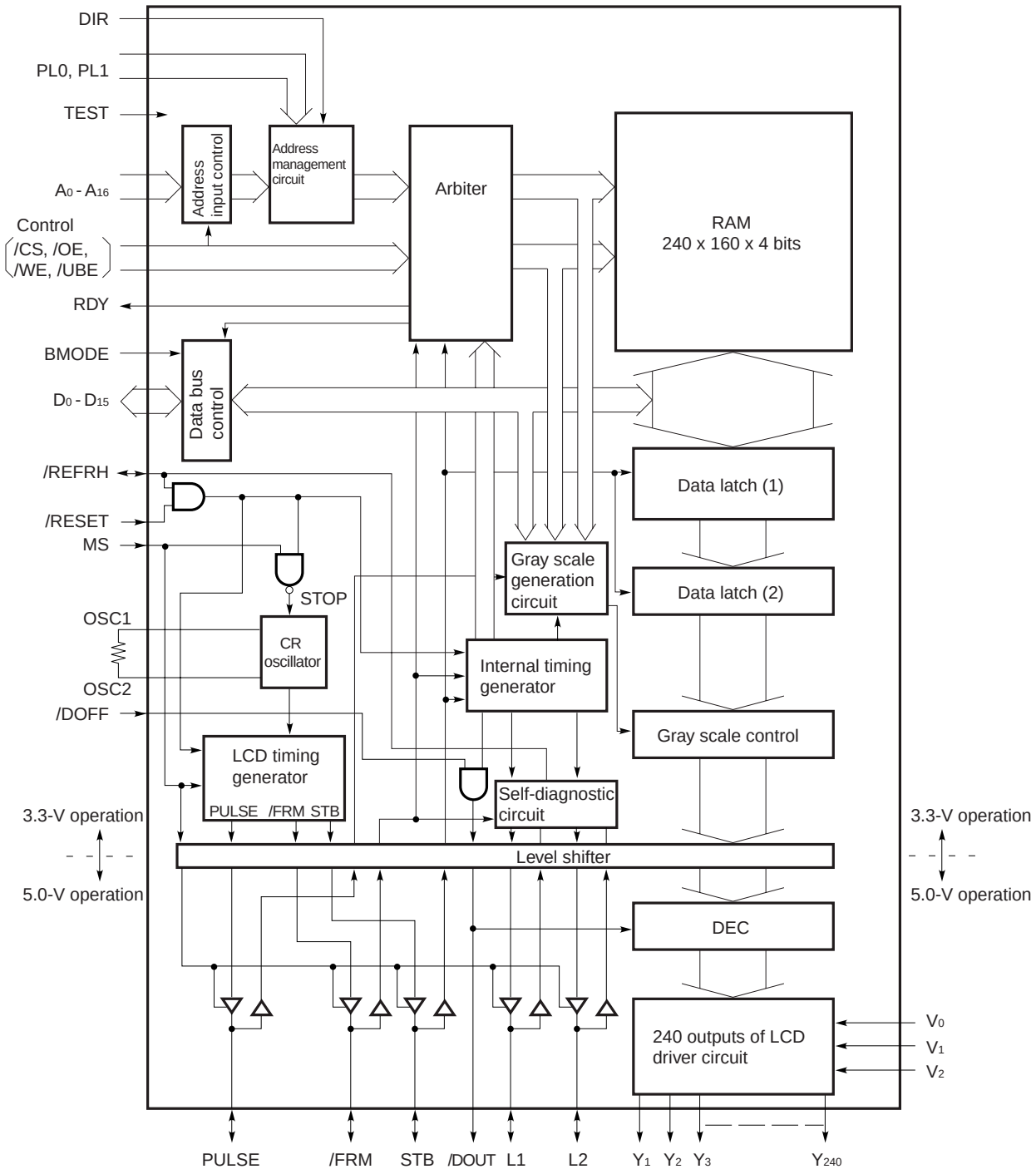
	Part number	Package
	μPD16663N-×××	TCP (TAB)
★	μPD16663N-051	2-side standard TCP

Remark The TCP's external shape is customized. To order the required shape, please contact an NEC salesperson.

Document No. S13392EJ1V0DS00 (1st edition)
Date Published December 1999 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

BLOCK DIAGRAM



Remark /xxx indicates active low signal.

1. PIN FUNCTIONS

Classification	Pin name[Note]	I/O	Function
CPU Interface (3.3 V)	D_0 to D_{15}	I/O	Data bus : 16 bits
	A_0 to A_{16}	I	Address bus : 17 bits
	/CS	I	Chip select
	/OE	I	Read signal
	/WE	I	Write signal
	/UBE	I	Upper byte enable
	RDY	O	Ready signal issued to CPU ("H" sets ready status)
Control signals (3.3 V)	PL0	I	Specifies the LSI placement position (No. 0 to 3)
	PL1	I	Specifies the LSI placement position (No. 0 to 3)
	DIR	I	Specifies the direction of the LCD panel placement
	MS	I	Selects between master/slave ("H" sets master mode)
	BMODE	I	Selects the data bus bit ("H" sets 8 bits, "L" sets 16 bits)
	/REFRH	I/O	Self-diagnostics reset pin (Wired-OR connection)
	TEST	I	Test pin ("H" sets test mode, pull-down resistor is built-in)
	/RESET	I	Reset signal
	/DOFF	I	Display OFF input signal
	OSC1	-	For external resistor for oscillator
	OSC2	-	For external resistor for oscillator
	STB	I/O	Column driving signal (MS pin "H" sets output, MS pin "L" sets input)
	/FRM	I/O	Frame signal (MS pin "H" sets output, MS pin "L" sets input)
	PULSE (5.0 V)	I/O	25-gray-scale pulse modulation clock
	L1	I/O	Row driver driving level select signal (line 1)
	L2	I/O	Row driver driving level select signal (line 2)
	/DOUT	O	Display OFF output signal
LCD drive	Y_1 to Y_{240}	O	LCD drive output
Power supply	GND	-	Ground (× 2 for 5 V, × 3 for 3.3 V)
	V_{CC1}	-	5-V power supply
	V_{CC2}	-	3.3-V power supply
	V_0	-	LCD drive analog power supply
	V_1	-	LCD drive analog power supply
	V_2	-	LCD drive analog power supply

Note 3.3-V pins : D_0 to D_{15}, A_0 to A_{16}, /CS, /OE, /WE, /UBE, RDY, BMODE, PL0, PL1, DIR, OSC1, OSC2, /RESET, /DOFF, TEST, MS

5-V pins :STB, /FRM, L1, L2, /DOUT, PULSE

Remark N.C. = Non-connection

2. BLOCK FUNCTION

(1) Address management circuit

Converts an address transferred from the system via A_0 to A_{16} to an address that corresponds to the on-chip RAM memory map.

This function enables address management for a display size of up to 480 x 320 dots using four μPD16663 LSIs, thus facilitating the configuration of LCD systems.

The allocation of addresses 1FFF80H to 1FFFEH (even addresses only) to the gray scale palette register also allows the user to select any 16 gray scales from a palette of 49.

(2) Arbiter

Resolves a conflict between a RAM access from the system and a RAM read on the LCD drive side.

(3) RAM

240 x 160 x 4 bits of static RAM (single port).

(4) Data bus control

Controls the direction in which data is transferred according to whether the system is reading or writing.

The bus width can also be switched between 8 and 16 bits with the BMODE pin.

(5) Gray scale generation circuit

Culls frames and modulates the pulse width to realize 49 gray scales.

(6) Internal timing generator

Generates the internal timing for each block from the /FRM and STB signals.

(7) CR oscillator

In master mode, this oscillator generates the clock referenced for the frame frequency. The frame frequency is determined by dividing this clock by 2592. To obtain a frame frequency of 70 Hz, therefore, an oscillation frequency of 181.44 kHz is required. Because the CR oscillator is on chip, adjust the oscillation frequency using an external resistor.

Oscillation is stopped in slave mode.

(8) LCD timing generator

In master mode, this generator generates /FRM (the frame signal), STB (the column driver signal strobe), and PULSE (the 49-gray-scale pulse modulation clock).

(9) Gray scale control

This is a circuit for realizing a 16-gray-scale display.

(10) Data latch (1)

Latches 240-pixel data read from RAM.

(11) Data latch (2)

Latches 240-pixel data in synchronization with the STB signal.

(12) Level shifter

Converts the internal circuit operating voltage (3.3 V) to the voltage required by the LCD driver and row driver interface (5 V).

(13) DEC

Decodes the gray scale display data into the corresponding LCD drive voltages V_0, V_1, and V_2.

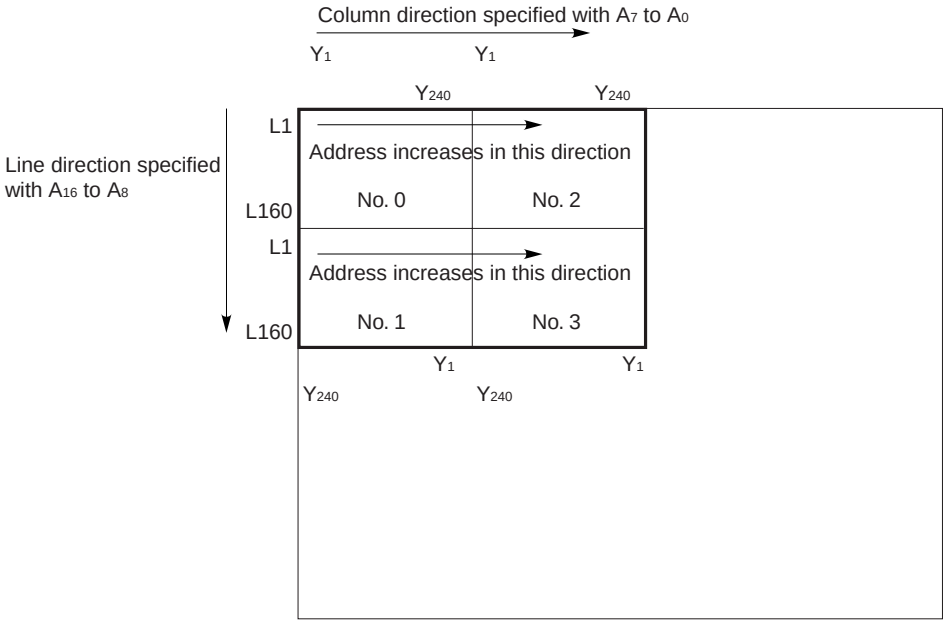
(14) LCD driver circuit

Creates the voltage to be applied to the LCD by selecting one of LCD drive power supplies V_0, V_1, or V_2, according to the gray scale data and display off signal (/DOFF).

(15) Self-diagnostic circuit

Automatically detects any mismatch between the operation timings of the master and slave chips cause by noise, etc., and issues a refresh signal to all the column drivers.

- **Address Map Image (Half VGA Size)**



3. DATA BUS

The byte data ordering on the data bus is little endian, which is the format commonly used in most NEC and Intel products.

(1) 16-bit data bus (BMODE = L)

Byte access

Address increases as shown →

D_0 to D_7	D_8 to D_{15}
00000H	00001H
00002H	00003H
00004H	00005H
:	:
:	:

Word access

Address increases as shown →

D_0 to D_7	D_8 to D_{15}
00000H	
00002H	
00004H	
:	
:	

In the same way as access from the system can be performed in word (16-bit) and byte (8-bit) units, valid data is indicated by D_0 to D_7 and/or D_8 to D_{15}, by means of the /UBE signal (higher byte enable) and A_0.

/CS	/OE	/WE	/UBE	A_0	MODE	I/O	
						D_0 to D_7	D_8 to D_{15}
H	×	×	×	×	Not Selected	Hi-z	Hi-z
L	L	H	L	L	Read	Dout	Dout
			L	H		Hi-z	Dout
			H	L		Dout	Hi-z
L	H	L	L	L	Write	Din	Din
			L	H		×	Din
			H	L		Din	×
L	H	H	×	×	Output Disable	Hi-z	Hi-z
L	×	×	H	H		Hi-z	Hi-z

Remark ×= Don't Care, Hi-z= High impedance

(2) 8-bit data bus (BMODE = H)

	D_0 to D_7
Address increases as shown →	00000H
	00001H
	00002H
	:
	:

/CS	/OE	/WE	MODE	I/O	
				D_0 to D_7	D_8 to D_{15}
H	×	×	Not Selected	Hi-z	**Note**
L	L	H	Read	Dout	**Note**
L	H	L	Write	Din	**Note**
L	H	H	Output Disable	Hi-z	**Note**

Note When BMODE = H, D_8 to D_{15} can be either left open or connected to GND because they and /UBE are pulled down internally.

Remark ×= Don't Care, Hi-z= High impedance

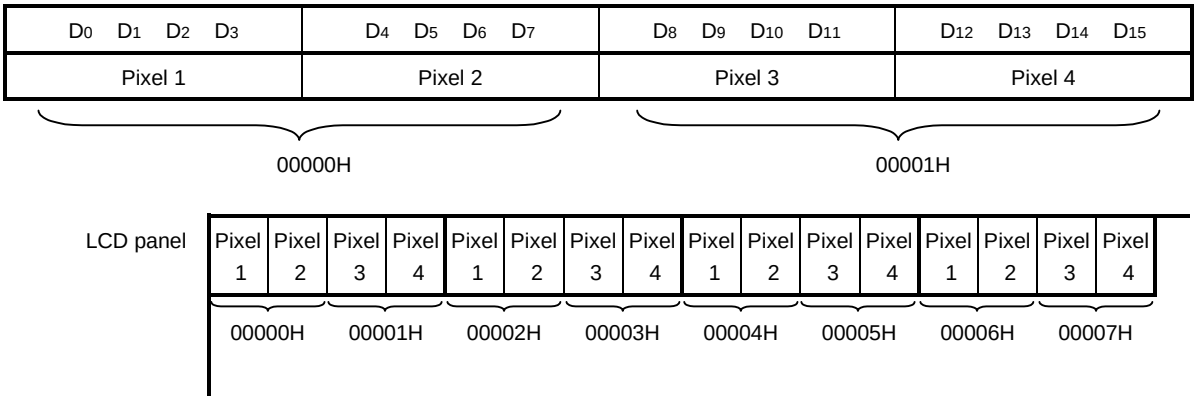
4. RELATIONSHIP BETWEEN DATA BITS AND PIXELS

16-gray scale display consists of 4 bits per pixel.

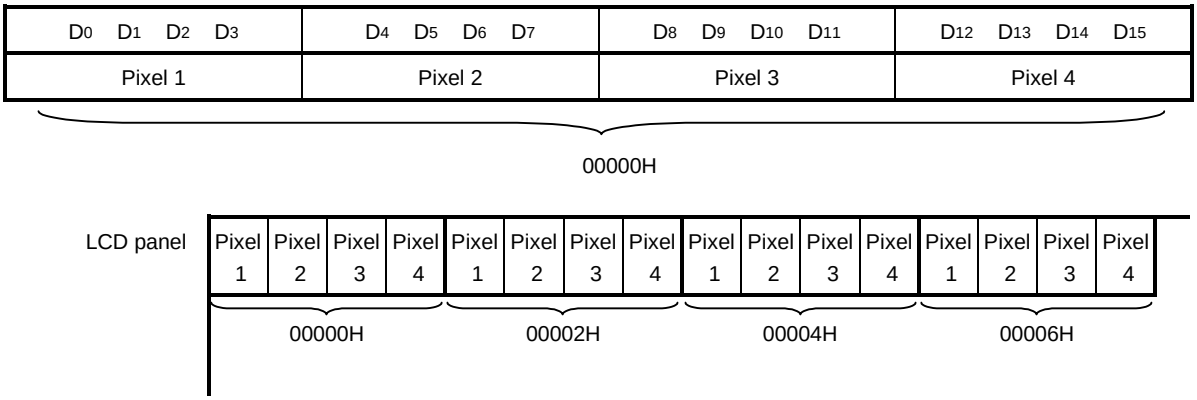
In the packed pixel format, RAM is configured with 2 pixels (4 pixels per word).

(1) BMODE = L

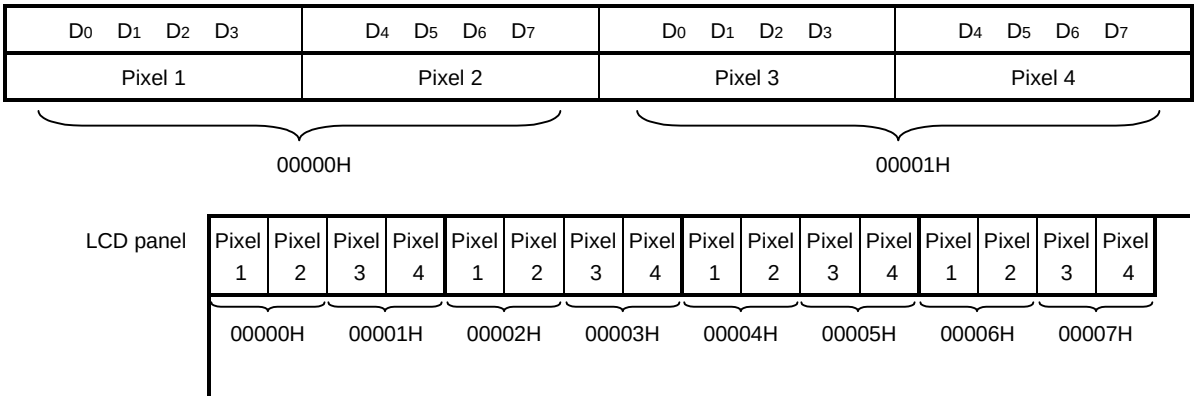
Byte (8-bit) access



Word (16-bit) access



(2) BMODE = H



5. GRAY SCALE CONTROL

Gray scale control in the μPD16663 realizes a palette of 49 gray scales, generated by culling frames and modulating the pulse width. From these 49 gray scales, 16 can be selected and recorded in the gray scale palette register.

5.1 Gray Scale Palette Register

The gray scale palette register is used to preselect 16 gray scales from a palette of 49. This register is allocated to addresses 1FF80H to 1FFFEH (even addresses only) and has the following relationship with gray scale data.

The gray scale palette register can be set according to the mapping positions of column drivers 0 to 3, as determined by PL0 and PL1.

★ **Gray Scale Palette Register (1/2)**

Address	LSI placement position No.	Gray scale data (Display data)				Initial value
		D_3/D_7	D_2/D_6	D_1/D_5	D_0/D_4	
1FF80 H	No. 0	0	0	0	0	Gray scale 0
1FF82 H		0	0	0	1	Gray scale 4
1FF84 H		0	0	1	0	Gray scale 8
1FF86 H		0	0	1	1	Gray scale 12
1FF88 H		0	1	0	0	Gray scale 16
1FF8A H		0	1	0	1	Gray scale 19
1FF8C H		0	1	1	0	Gray scale 21
1FF8E H		0	1	1	1	Gray scale 23
1FF90 H		1	0	0	0	Gray scale 25
1FF92 H		1	0	0	1	Gray scale 27
1FF94 H		1	0	1	0	Gray scale 29
1FF96 H		1	0	1	1	Gray scale 32
1FF98 H		1	1	0	0	Gray scale 36
1FF9A H		1	1	0	1	Gray scale 40
1FF9C H		1	1	1	0	Gray scale 44
1FF9E H		1	1	1	1	Gray scale 48
1FFA0 H	No. 1	0	0	0	0	Gray scale 0
1FFA2 H		0	0	0	1	Gray scale 4
1FFA4 H		0	0	1	0	Gray scale 8
1FFA6 H		0	0	1	1	Gray scale 12
1FFA8 H		0	1	0	0	Gray scale 16
1FFAA H		0	1	0	1	Gray scale 19
1FFAC H		0	1	1	0	Gray scale 21
1FFAE H		0	1	1	1	Gray scale 23
1FFB0 H		1	0	0	0	Gray scale 25
1FFB2 H		1	0	0	1	Gray scale 27
1FFB4 H		1	0	1	0	Gray scale 29
1FFB6 H		1	0	1	1	Gray scale 32
1FFB8 H		1	1	0	0	Gray scale 36
1FFBA H		1	1	0	1	Gray scale 40
1FFBC H		1	1	1	0	Gray scale 44
1FFBE H		1	1	1	1	Gray scale 48

Remark The gray scale palette register is initialized by the /RESET signal.

★ **Gray Scale Palette Register (2/2)**

Address	LSI placement position No.	Gray scale data (Display data)				Initial value
		D_3/D_7	D_2/D_6	D_1/D_5	D_0/D_4	
1FFC0 H	No. 2	0	0	0	0	Gray scale 0
1FFC2 H		0	0	0	1	Gray scale 4
1FFC4 H		0	0	1	0	Gray scale 8
1FFC6 H		0	0	1	1	Gray scale 12
1FFC8 H		0	1	0	0	Gray scale 16
1FFCA H		0	1	0	1	Gray scale 19
1FFCC H		0	1	1	0	Gray scale 21
1FFCE H		0	1	1	1	Gray scale 23
1FFD0 H		1	0	0	0	Gray scale 25
1FFD2 H		1	0	0	1	Gray scale 27
1FFD4 H		1	0	1	0	Gray scale 29
1FFD6 H		1	0	1	1	Gray scale 32
1FFD8 H		1	1	0	0	Gray scale 36
1FFDA H		1	1	0	1	Gray scale 40
1FFDC H		1	1	1	0	Gray scale 44
1FFDE H		1	1	1	1	Gray scale 48
1FFE0 H	No. 3	0	0	0	0	Gray scale 0
1FFE2 H		0	0	0	1	Gray scale 4
1FFE4 H		0	0	1	0	Gray scale 8
1FFE6 H		0	0	1	1	Gray scale 12
1FFE8 H		0	1	0	0	Gray scale 16
1FFEA H		0	1	0	1	Gray scale 19
1FFEC H		0	1	1	0	Gray scale 21
1FFEE H		0	1	1	1	Gray scale 23
1FFF0 H		1	0	0	0	Gray scale 25
1FFF2 H		1	0	0	1	Gray scale 27
1FFF4 H		1	0	1	0	Gray scale 29
1FFF6 H		1	0	1	1	Gray scale 32
1FFF8 H		1	1	0	0	Gray scale 36
1FFFA H		1	1	0	1	Gray scale 40
1FFFC H		1	1	1	0	Gray scale 44
1FFFE H		1	1	1	1	Gray scale 48

Remark The gray scale palette register is initialized by the /RESET signal.

5.2 Relationship Between Gray Scales and Gray Scale Palette Data

The relationship between the gray scales and gray scale palette data set with the gray scale palette register is shown in the table below.

Gray Scale Palette Data (1/2)

PMODE	Gray scale palette data						Remark
	D_5	D_4	D_3	D_2	D_1	D_0	
Gray scale 0	0	0	0	0	0	0	OFF
Gray scale 1	0	0	0	0	0	1	
Gray scale 2	0	0	0	0	1	0	
Gray scale 3	0	0	0	0	1	1	
Gray scale 4	0	0	0	1	0	0	
Gray scale 5	0	0	0	1	0	1	
Gray scale 6	0	0	0	1	1	0	
Gray scale 7	0	0	0	1	1	1	
Gray scale 8	0	0	1	0	0	0	
Gray scale 9	0	0	1	0	0	1	
Gray scale 10	0	0	1	0	1	0	
Gray scale 11	0	0	1	0	1	1	
Gray scale 12	0	0	1	1	0	0	
Gray scale 13	0	0	1	1	0	1	
Gray scale 14	0	0	1	1	1	0	
Gray scale 15	0	0	1	1	1	1	
Gray scale 16	0	1	0	0	0	0	
Gray scale 17	0	1	0	0	0	1	
Gray scale 18	0	1	0	0	1	0	
Gray scale 19	0	1	0	0	1	1	
Gray scale 20	0	1	0	1	0	0	
Gray scale 21	0	1	0	1	0	1	
Gray scale 22	0	1	0	1	1	0	
Gray scale 23	0	1	0	1	1	1	
Gray scale 24	0	1	1	0	0	0	
Gray scale 25	0	1	1	0	0	1	
Gray scale 26	0	1	1	0	1	0	
Gray scale 27	0	1	1	0	1	1	
Gray scale 28	0	1	1	1	0	0	
Gray scale 29	0	1	1	1	0	1	
Gray scale 30	0	1	1	1	1	0	

Gray Scale Palette Data (2/2)

PMODE	Gray scale palette data						Remark
	D_5	D_4	D_3	D_2	D_1	D_0	
Gray scale 31	0	1	1	1	1	1	
Gray scale 32	1	0	0	0	0	0	
Gray scale 33	1	0	0	0	0	1	
Gray scale 34	1	0	0	0	1	0	
Gray scale 35	1	0	0	0	1	1	
Gray scale 36	1	0	0	1	0	0	
Gray scale 37	1	0	0	1	0	1	
Gray scale 38	1	0	0	1	1	0	
Gray scale 39	1	0	0	1	1	1	
Gray scale 40	1	0	1	0	0	0	
Gray scale 41	1	0	1	0	0	1	
Gray scale 42	1	0	1	0	1	0	
Gray scale 43	1	0	1	0	1	1	
Gray scale 44	1	0	1	1	0	0	
Gray scale 45	1	0	1	1	0	1	
Gray scale 46	1	0	1	1	1	0	
Gray scale 47	1	0	1	1	1	1	
Gray scale 48	1	1	0	0	0	0	ON

6. LSI MAPPING AND ADDRESS MANAGEMENT

Addresses can be managed when using up to four μPD16663 LSIs, which enables the configuration of a half VGA size LCD (320 x 480 dots). In this case, the data bus and /CS, /WE, and /OE pins can be used commonly.

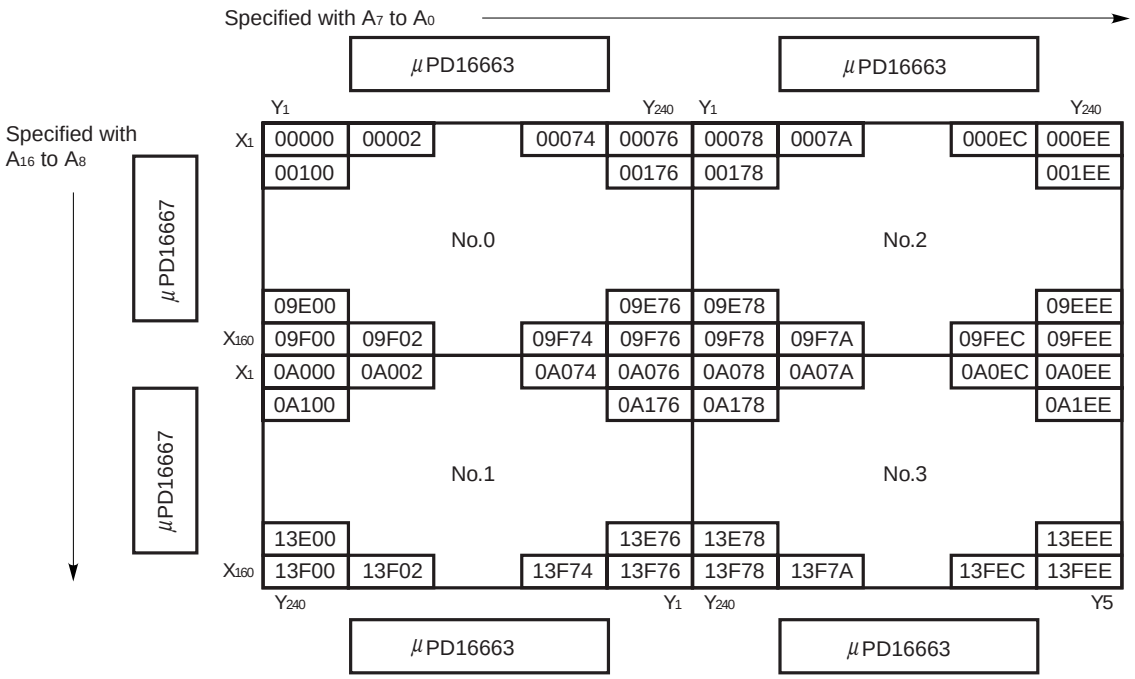
The system can handle each LCD screen as a single area in memory, eliminating the need to decode multiple μPD16663 LSIs.

The LSI No. and layout are specified by the PL0 and PL1 pins, and the DIR pin is used to determine the direction of the LCD contents (height, width).

PL1	PL0	LSI placement position No.
0	0	No. 0
0	1	No. 1
1	0	No. 2
1	1	No. 3

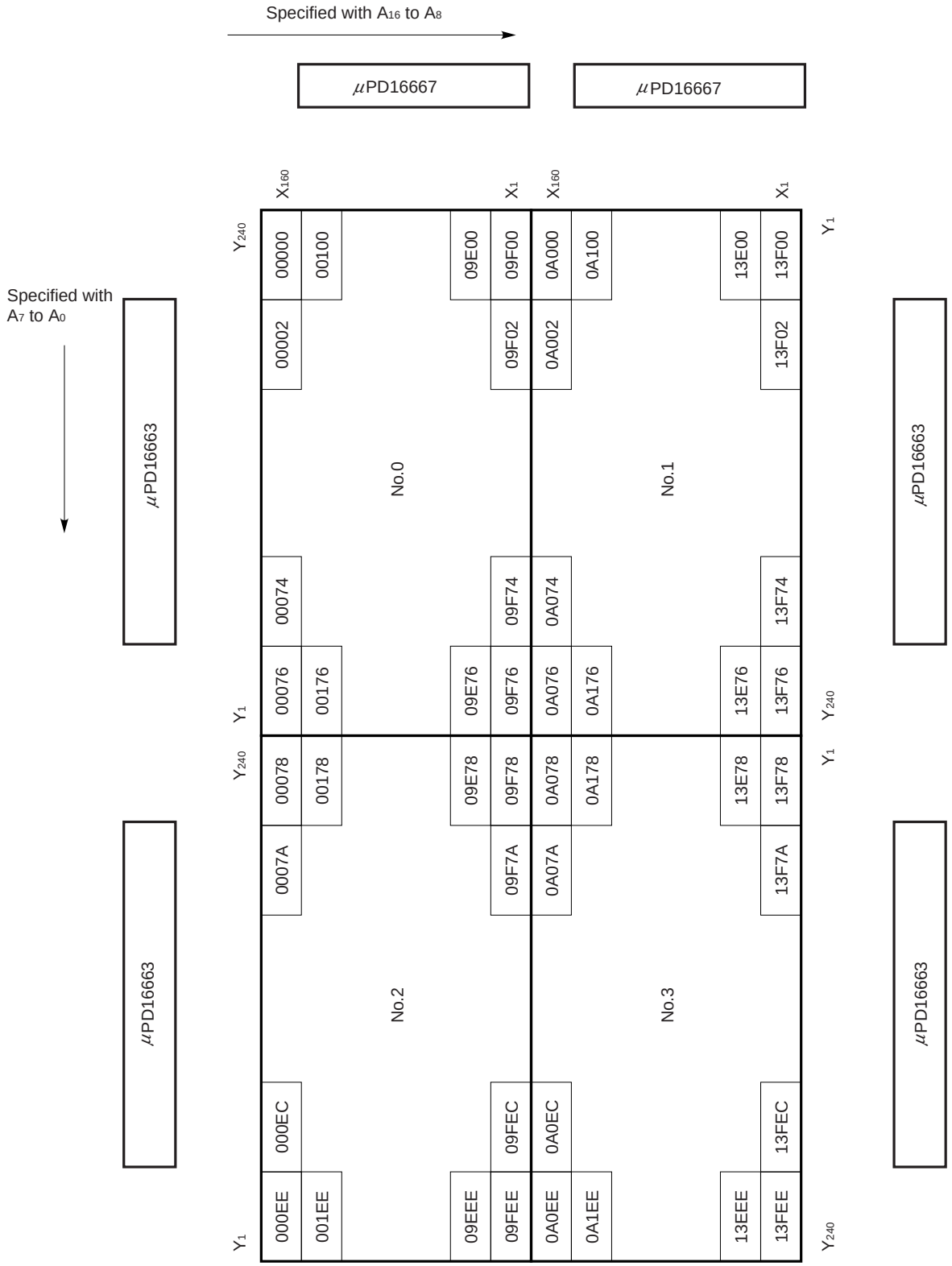
6.1 Addresses for Half-VGA Size Horizontal Rectangle

DIR = "0"



6.2 Addresses for Half-VGA Size Vertical Rectangle

DIR = "1"

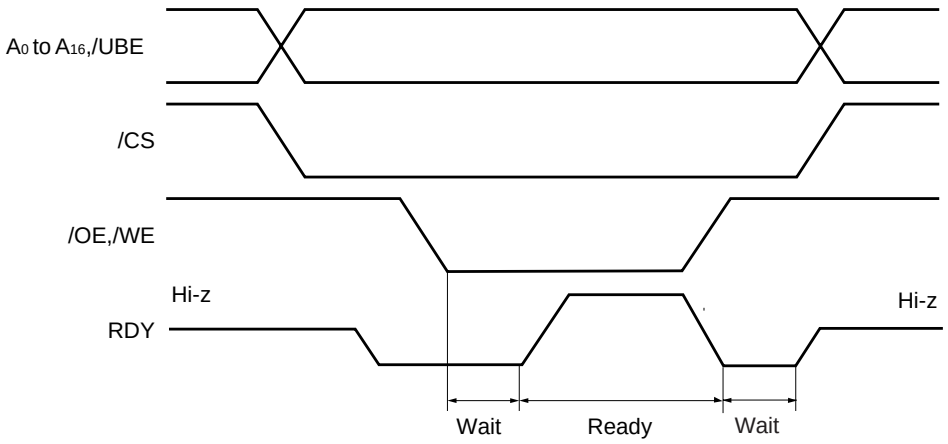


7. CPU INTERFACE

7.1 RDY (Ready) Pin Functions

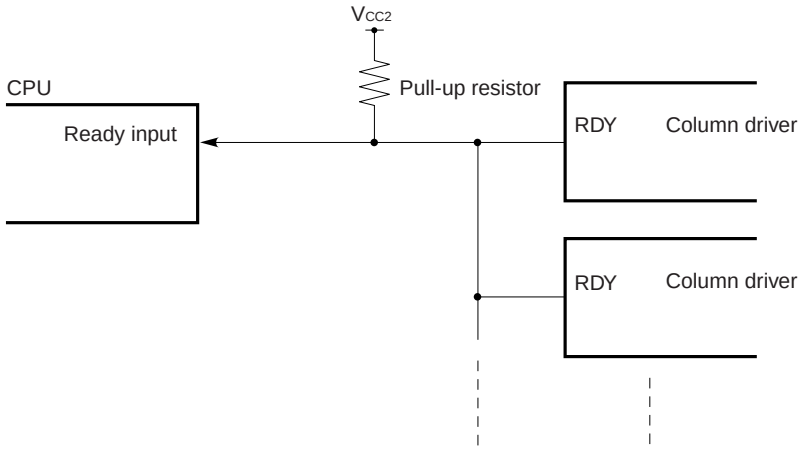
Single port RAM is used as the on-chip RAM in the μPD16663. The RDY pin is used to make the CPU wait, in order to prevent contention between a CPU access and a read on the LCD side.

7.1.1 Timing



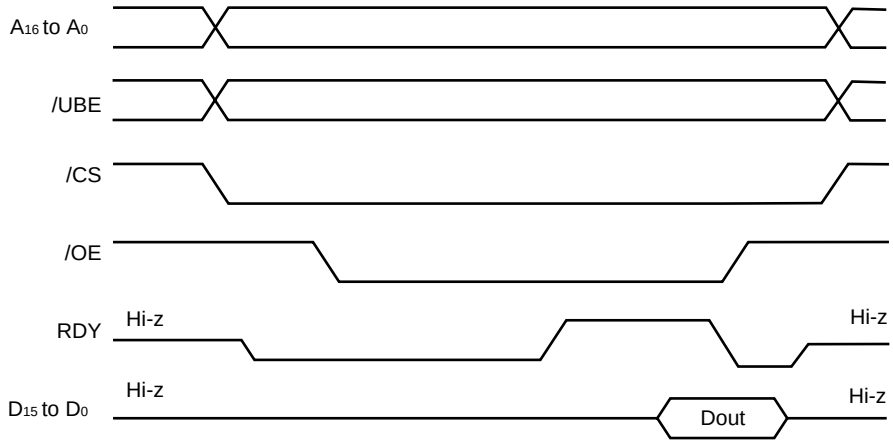
7.1.2 RDY pin connection

The RDY pin uses a 3-state buffer. Connect an external pull-up resistor to the RDY pin. When more than one μPD16663 LSI is being used, use a wired-OR connection for the RDY pin of each LSI.

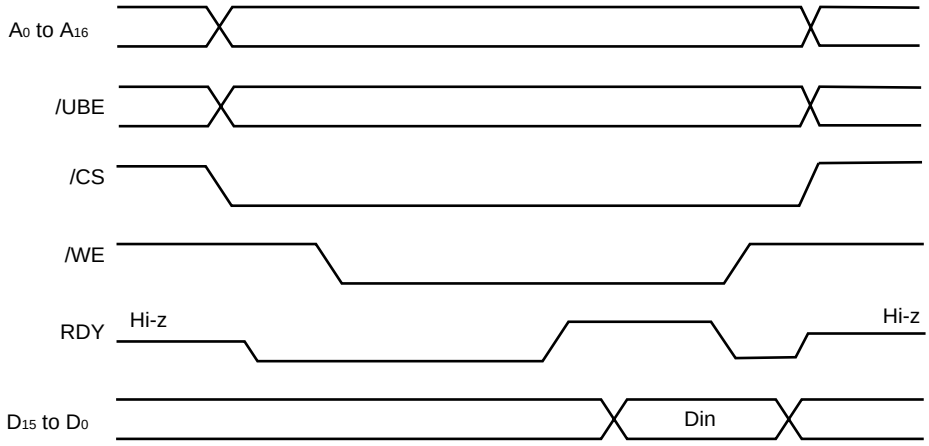


7.2 Access Timing

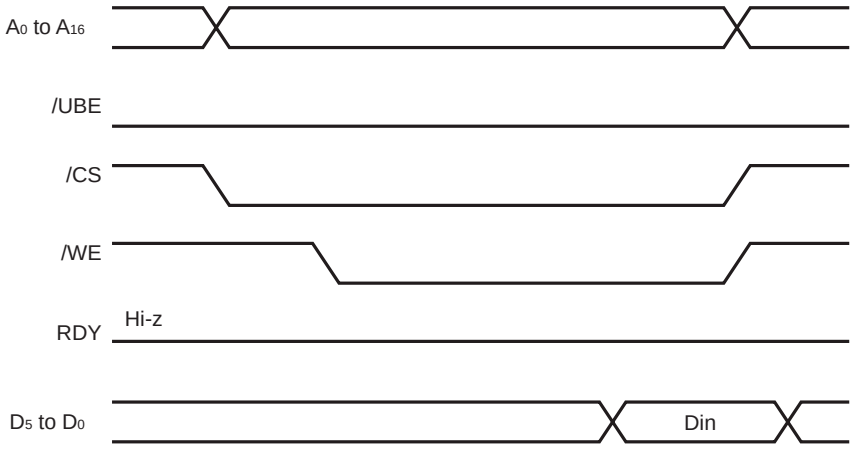
(1) Display data read timing



(2) Display data write timing



(3) Gray scale palette data write timing



★ 8. INITIALIZATION FUNCTION

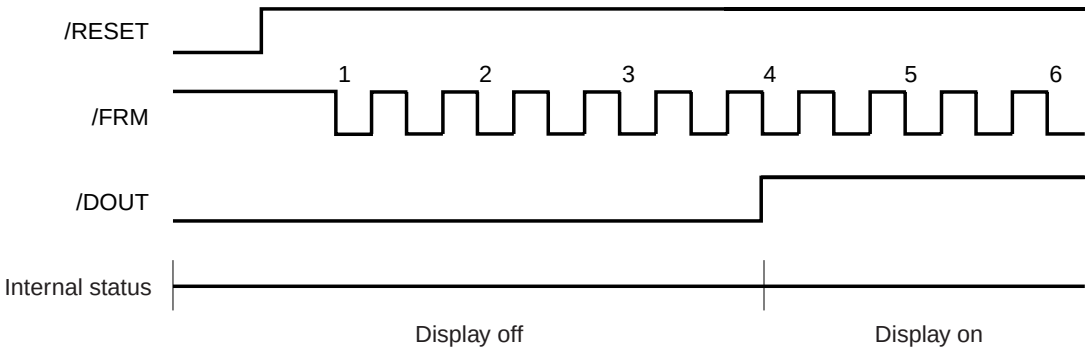
Two initialization functions are available in the μPD16663.

8.1 Initialization by /RESET

/RESET is used for forcible external initialization of the LSI. When /RESET = L, the internal statuses of the μPD16663 are as follows.

- Oscillation stopped
- LCD timing generator initialized
- Internal timing generator initialized
- Self-diagnostic circuit initialized
- Gray scale palette register initialized
- Display off

The display remains off for 4 frame cycles after /RESET release, even if the /DOFF pin is H.



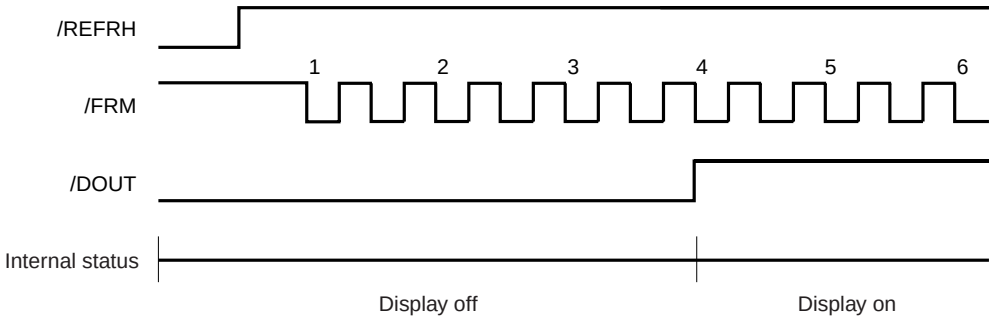
Be sure to initialize the LSI by /RESET when turning on the power.

8.2 Initialization by /REFRH

/REFRH is a pin used by the internal self-diagnostic circuit to initialize the LSI when there are mismatches in the timing of the column drivers due to external noise, etc. When /REFRH = L, the internal statuses of the μPD16663 are as follows.

- Oscillation stopped
- LCD timing generator initialized
- Internal timing generator initialized
- Display off

The display remains off for 4 frame cycles after /REFRH release, even if the /DOFF pin is H.



★ 9. DISPLAY OFF FUNCTION

When /DOFF = L, the column driver outputs (Y_n) are all at the V_1 level. Moreover, because the /DOUT output is also L, the /DOFF' signal of the row driver becomes L, causing all the row driver outputs (X_n) to also be at the V_1 level. The display is therefore forcibly put in the off status, regardless of the display data.

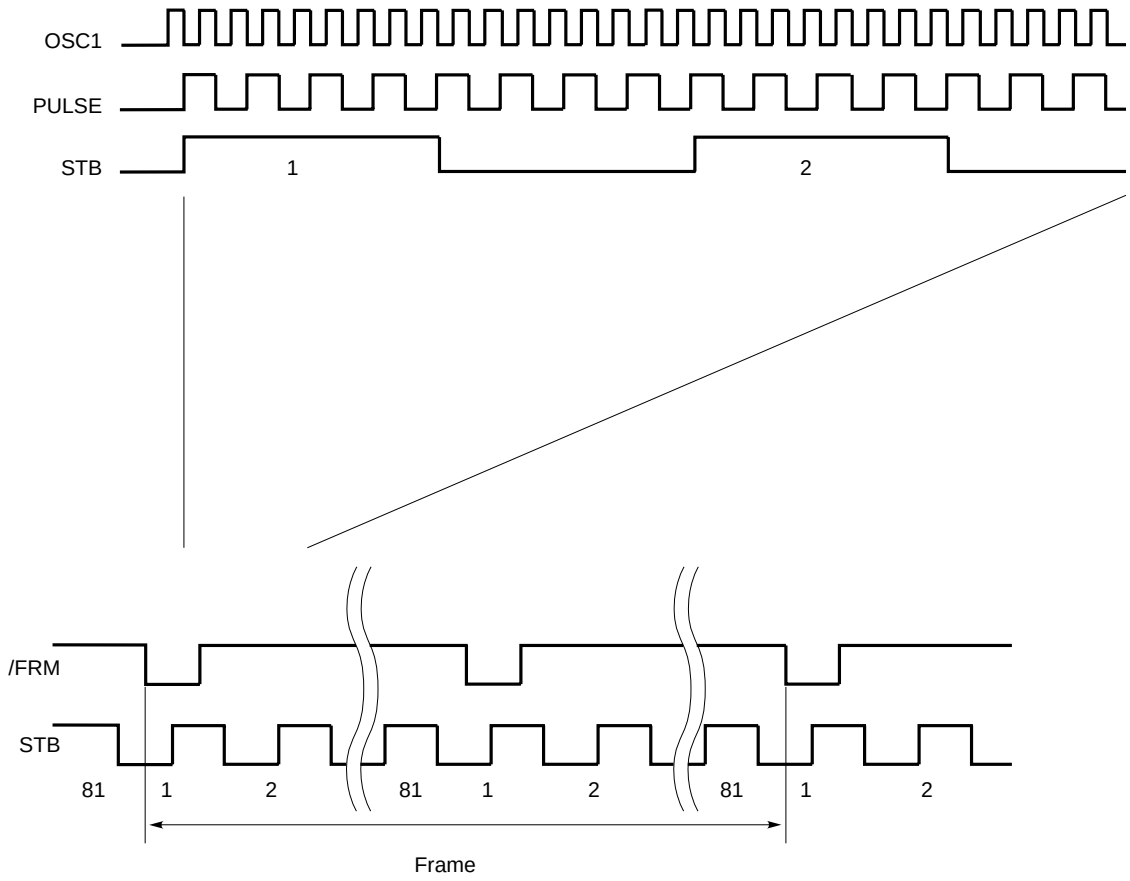
Remark /DOFF' is the row driver input pin.

10. LCD TIMING GENERATOR CIRCUIT

If master mode is entered by setting MS to H, /FRM and STB are generated at a timing that is 1/160 of the duty ratio, and driver voltage selection signals L1 and L2 are generated for the row driver.

/FRM is generated twice per frame, STB 81 times per 1/2 frame or 162 times per frame.

(1) /FRM, STB signal generation



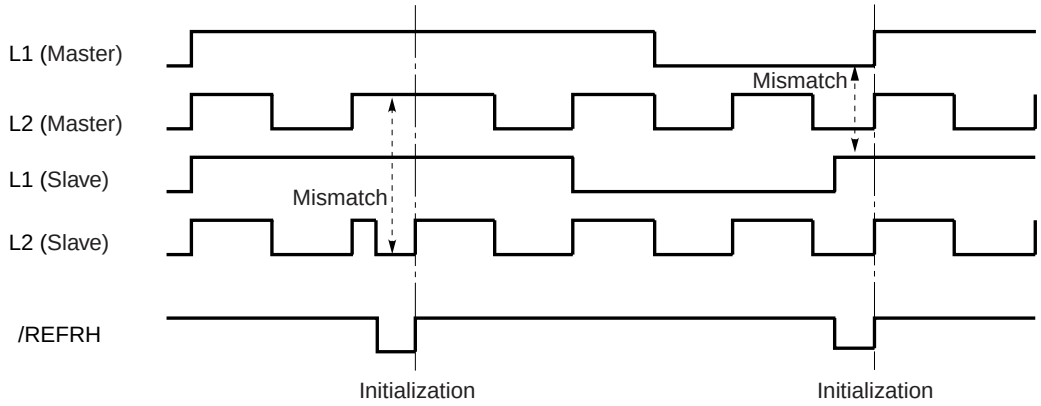
(2) L1, L2 signal generation

STB	1	2	3	4	…	1	2	3	4	…	1	2	3	4	…	1	2	3	4	…
L1	1	1	1	1	…	1	1	1	1	…	0	0	0	0	…	0	0	0	0	…
L2	1	0	1	0	…	0	1	0	1	…	0	1	0	1	…	1	0	1	0	…

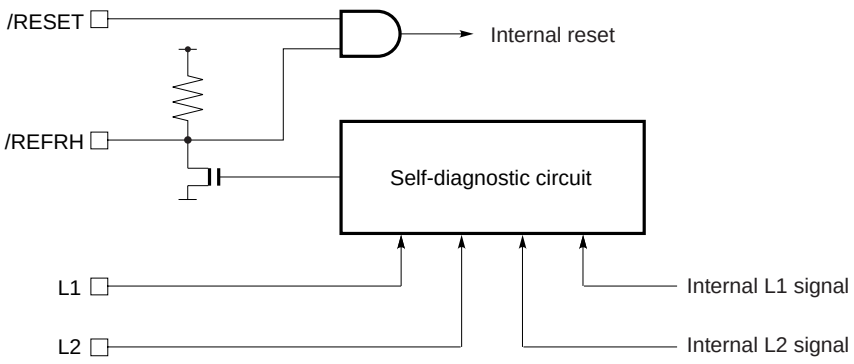
11. SELF-DIAGNOSTIC FUNCTION

This function is provided to monitor whether there are any mismatches in the timing of the column drivers due to factors such as external noise. The slave chip compares L1 and L2 of the master chip with its own internally generated L1 and L2, and if a mismatch is detected, it issues a refresh signal to all the column drivers. Upon the receipt of a refresh signal, an internal reset is instigated, and the timing is initialized. At this time, the display remains off for a period equal to 4 frame cycles plus the time /REFRH is L.

Monitoring for an L1, L2 mismatch takes place every 1/2 frame at the rising edge of /FRM.



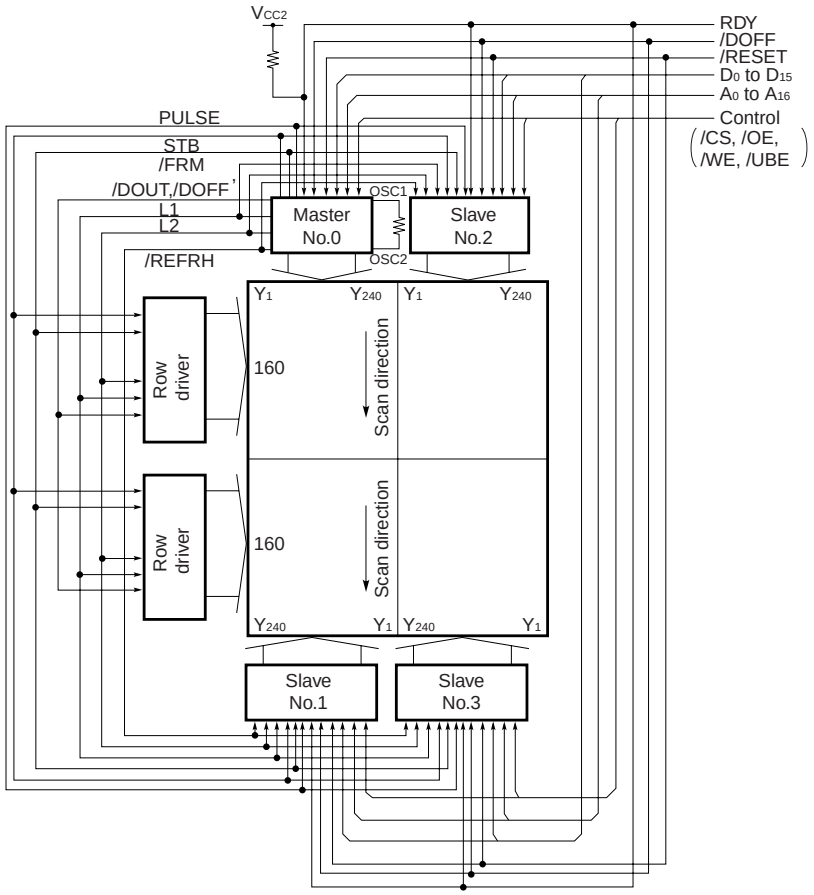
Block Configuration (Slave)



12. EXAMPLE SYSTEM CONFIGURATION

The following example shows the configuration of a system using four μPD16663 LSIs and two row drivers to drive a half VGA size (480 x 320 dots, landscape) LCD panel.

- The LSI No. is set for each column driver using the PL0 and PL1 pins.
- The DIR pin on each column driver is set to low.
- One of the column drivers is specified as the master; the remaining are all slaves. The master column driver supplies signals to the slave column drivers and the row drivers.
- An oscillator resistor is attached across the OSC1 and OSC2 pins of the master, while those of the slaves are left open.
- The signals issued by the system (D_0 to D_{15}, A_0 to A_{16}, /CS, /OE, /WE, /UBE, RDY, /RESET, /DOFF) are connected in parallel to all the column drivers. A pull-up resistor is connected to the RDY signal.
- The TEST pin is used for testing the LSI, so either leave it open or connect it to GND when configuring the system.



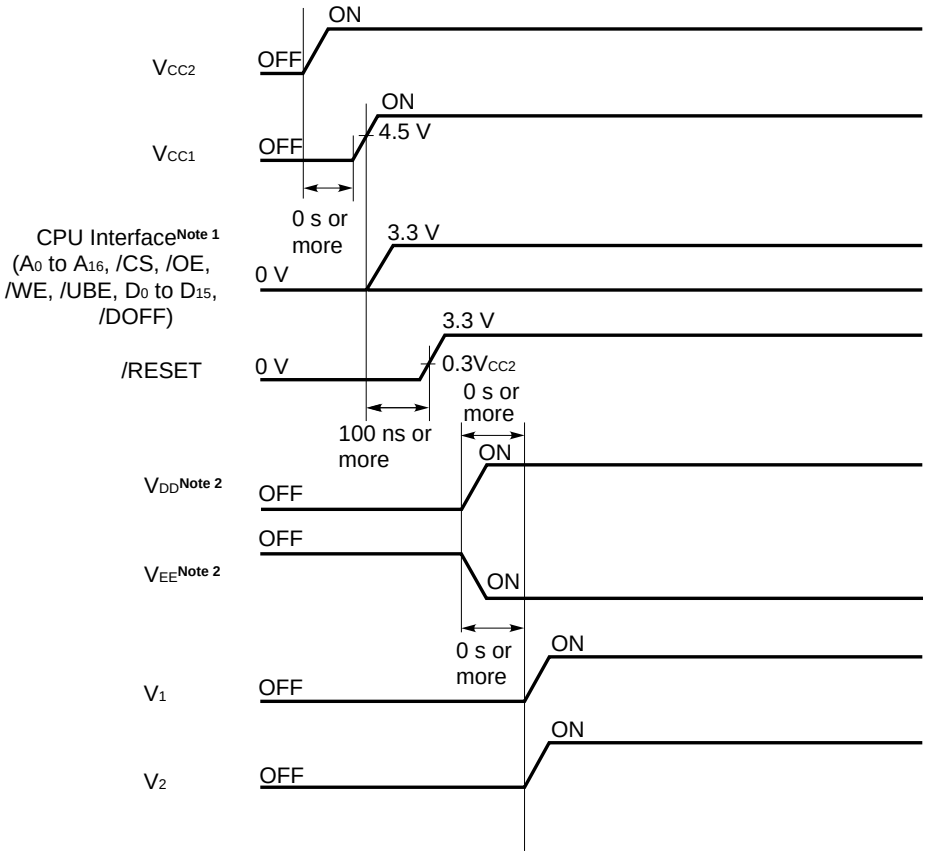
Remark The /DOFF' pin is an input pin of row driver.

13. CHIPSET POWER APPLICATION

It is recommended that the power be applied to the chipset in the following order.

$V_{CC2} \rightarrow V_{CC1} \rightarrow$ CPU interface $\rightarrow V_{DD}, V_{EE} \rightarrow V_1, V_2$

The LCD drive power supplies V_1 and V_2 must be applied last.



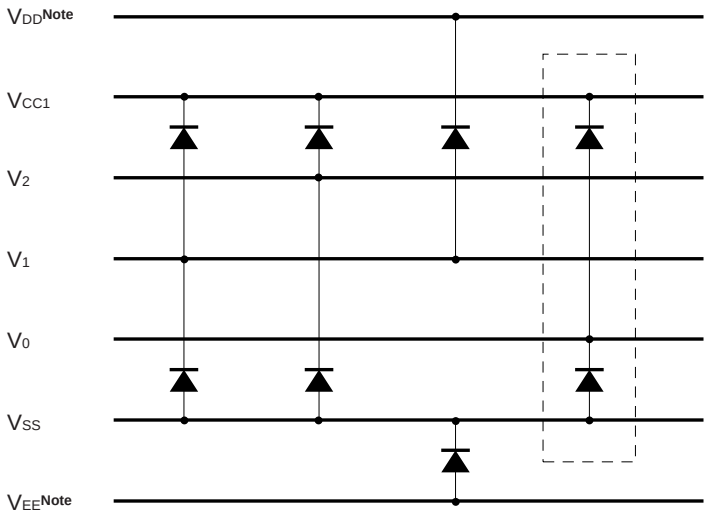
Notes1. The select signals (PL0, PL1, DIR, MS, and BMODE) can be input at the same time as V_{CC2}.

2. V_{DD} and V_{EE} do not have to be ON at the same time. V_{DD} and V_{EE} are the row driver LCD power supplies.

Caution Turn off the power of the chipset in the reverse order to the one above.

14. EXAMPLE OF SCHOTTKY BARRIER DIODE LAYOUT FOR POWER SUPPLY PROTECTION WITHIN THE MODULE

(Use Schottky barrier diodes that are V_f = 0.5 V or less.)



Those diodes within the dotted line must be placed when V_0 is 0 V (GND) or less.

Note V_{DD} and V_{EE} are the row driver LCD power supplies.

15. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = +25°C)

Item	Symbol	Rating	Units
Power supply voltage (1)[Note 1]	V_{CC1}	–0.5 to +6.5	V
Power supply voltage (2)[Note 2]	V_{CC2}	–0.5 to +4.5	V
Input/output voltage (1)[Note 1]	$V_{I/O1}$	–0.5 to V_{CC1} + 0.5	V
Input/output voltage (2)[Note 2]	$V_{I/O2}$	–0.5 to V_{CC2} + 0.5	V
Input/output voltage (3)[Note 3,4]	$V_{I/O3}$	–0.5 to V_{CC1} + 0.5	V
Operating ambient temperature	T_A	–20 to +70	°C
Storage temperature	T_{stg}	–40 to +125	°C

Notes 1. 5-V signals (/FRM, STB, /DOUT, L1, L2, PULSE)

2. 3.3-V signals (MS, DIR, PL0 to PL1, A_0 to A_{16}, /CS, /OE, /WE, /UBE, RDY, D_0 to D_{15}, /RESET, OSC1, OSC2, /DOFF, TEST, BMODE, /REFRH)

3. LCD driver power supply (V_0, V_1, V_2, Y_1 to Y_{240})

4. Ensure that $V_0 < V_1 < V_2$.

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Ranges (T_A = –20°C to +70°C, V_0 = 0 V)

Item	Symbol	MIN.	TYP.	MAX.	Units
Power supply voltage (1)	V_{CC1}	4.5	5.0	5.5	V
Power supply voltage (2)	V_{CC2}	3.0	3.3	3.6	V
Input voltage (1)[Note 1]	V_{I1}	0		V_{CC1}	V
Input voltage (2)[Note 2]	V_{I2}	0		V_{CC2}	V
V_1 input voltage	V_1	V_0		V_2	V
V_2 input voltage	V_2	V_1		V_{CC1}	V
OSC external resistor	R_{OSC}	30	62	90	kΩ

Notes 1. 5-V signals (/FRM, STB, L1, L2, PULSE)

2. 3.3-V signals (MS, DIR, PL0 to PL1, A_0 to A_{16}, /CS, /OE, /WE, /UBE, RDY, D_0 to D_{15}, /RESET, OSC1, OSC2, /DOFF, TEST, BMODE, /REFRH)

DC Characteristics (Unless Specified Otherwise, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = –20°C to +70°C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
High-level input voltage (1) for V_{CC1} Note 1	V_{IH1}		0.7V_{CC1}			V
Low-level input voltage (1) for V_{CC1} Note 1	V_{IL1}				0.3V_{CC1}	V
High-level input voltage (2) for V_{CC2} Note 2	V_{IH2}		0.7V_{CC2}			V
Low-level input voltage (2) for V_{CC2} Note 2	V_{IL2}				0.3V_{CC2}	V
High-level input voltage (2) for V_{CC2} Note 4	V_{IH3}		0.8V_{CC2}			V
Low-level input voltage (2) for V_{CC2} Note 4	V_{IL3}				0.2V_{CC2}	V
High-level output voltage (1) for V_{CC1} Note 3	V_{OH1}	I_{OH} = -1 mA	V_{CC1} – 0.4			V
Low-level output voltage (1) for V_{CC1} Note 3	V_{OL1}	I_{OL} = 2 mA			0.4	V
High-level output voltage (2) for V_{CC1} Note 1	V_{OH2}	I_{OH} = -2 mA	V_{CC1} – 0.4			V
Low-level output voltage (2) for V_{CC1} Note 1, 4	V_{OL2}	I_{OL} = 4 mA			0.4	V
High-level input voltage (3) for V_{CC2} Note 5	V_{OH3}	I_{OH} = -1 mA	V_{CC2} – 0.4			V
Low-level output voltage (3) for V_{CC2} Note 5	V_{OL3}	I_{OL} = 2 mA			0.4	V
Input leakage current (1)	I_{I1}	For other than TEST pin, V_I = V_{CC2} or GND			±10	μA
Input leakage current (2)	I_{I2}	Pull-down (TEST pin) V_I = V_{CC2}	10	40	100	μA
Display current drain (1)	I_{MAS1}	Master, for V_{CC1} Note 6			150	μA
Display current drain (2)	I_{MAS2}	Master, for V_{CC2} Note 6			350	μA
Display current drain (3)	I_{SLV1}	Slave, for V_{CC1} Note 6			100	μA
Display current drain (4)	I_{SLV2}	Slave, for V_{CC2} Note 6			250	μA
LCD driver output ON resistance Note 7	R_{ON}			1	2	kΩ

Notes 1. 5-V signals (/FRM, STB, L1, L2, PULSE)

2. 3.3-V signals (MS, DIR, PL0, PL1, A_0 to A_{16}, /CS, /OE, /WE, /UBE, RDY, D_0 to D_{15}, /RESET, /DOFF, TEST, BMODE)

3. /DOUT pin

4. /REFRH pin

5. D_0 to D_{15}, RDY, OSC2 pins

6. Frame frequency 70 Hz, no-load output, CPU not being accessed (D_0 to D_{15}, A_0 to A_{16}, /UBE = GND, /CS, /OE, /WE = V_{CC2})

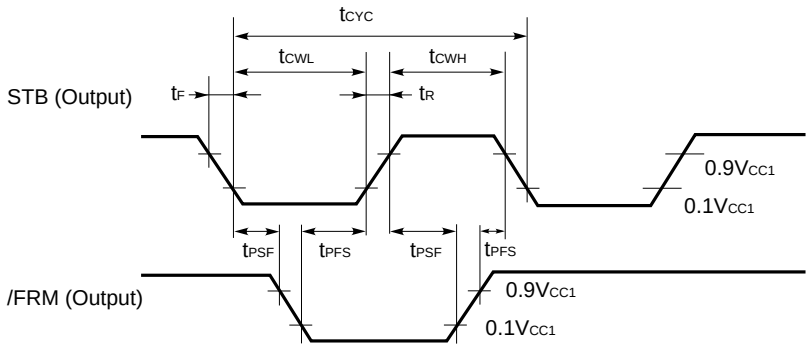
7. Resistance across Y pin and V pin (V_0, V_1, or V_2) when a load current (ION = 100 μA) is flowing through any one of pins Y_1 to Y_{240}.

AC Characteristics 1 Display Data Send Timing

(1) Master mode

(Unless specified otherwise, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = –20°C to +70°C, frame frequency 70 Hz (f_{OSC} = 181.44 kHz), output load: 100 pF)

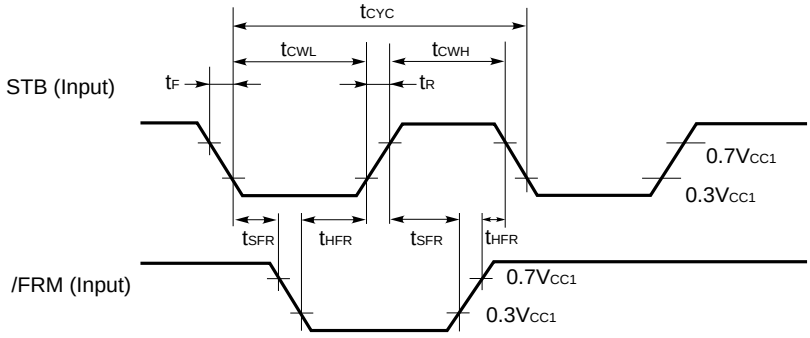
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
STB clock cycle time	t_{CYC}		87	16/f_{OSC}		μs
STB high level width	t_{CWH}		43	8/f_{OSC}		μs
STB low level width	t_{CWL}		43	8/f_{OSC}		μs
STB rise time	t_R				100	ns
STB fall time	t_F				100	ns
STB-/FRM delay	t_{PSF}		20			μs
/FRM-STB delay	t_{PFS}		20			μs



(2) Slave mode

(Unless specified otherwise, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = –20°C to +70°C)

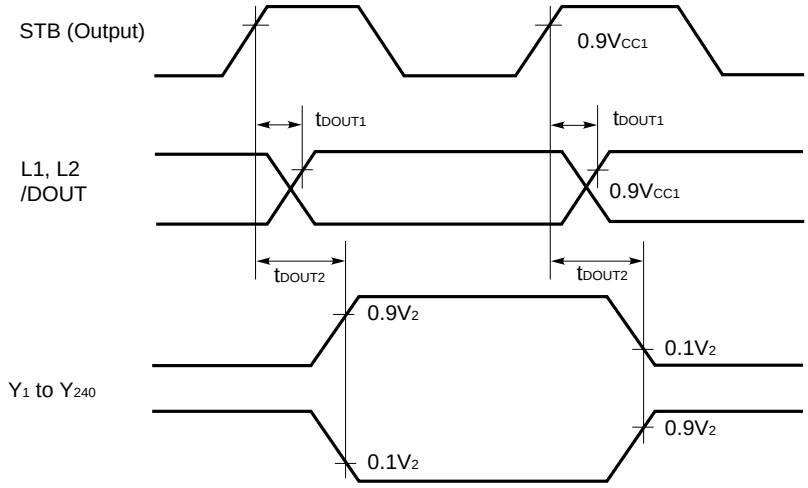
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
STB clock cycle time	t_{CYC}		10			μs
STB high level width	t_{CWH}		4			μs
STB low level width	t_{CWL}		4			μs
STB rise time	t_R				150	ns
STB fall time	t_F				150	ns
/FRM setup time	t_{SFR}		1			μs
/FRM hold time	t_{HFR}		1			μs



(3) Items common to both master and slaves

(Unless specified otherwise, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = –20°C to +70°C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Output delay (L1, L2, /DOUT)	t_{DOUT1}	No-load output		50	100	ns
Output delay (Y_1 to Y_{240})	t_{DOUT2}	No-load output		90	150	ns

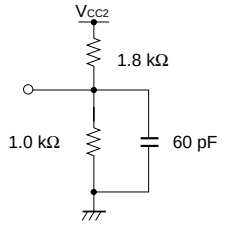


AC Characteristics 2 Drawing Access Timing

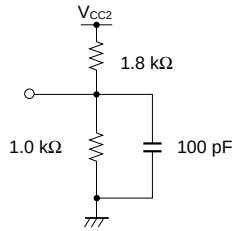
(Unless specified otherwise, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 3.0 to 3.6 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = −20°C to +70°C, $t_r = t_f$ = 5 ns)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
/OE//WE recovery time	t_{RY}		30			ns
Address setup time	t_{AS}		10			ns
Address hold time	t_{AH}		20			ns
RDY output delay time	t_{RYR}	CL = 15 pF			30	ns
RDY float time Note 3	t_{RYZ}				30	ns
Wait status time Note 1	t_{RYW}				35	ns
Ready status time (no contention) Note 1	t_{RYF1}			60	100	ns
Ready status time (contention) Note 1	t_{RYF2}			650	1,200	ns
Data access time (read cycle) Note 2	t_{ACS}				100	ns
Data float time (read cycle) Note 3	t_{HZ}				40	ns
/CS-/OE time (read cycle)	t_{CSOE}		10			ns
/OE-/CS time (read cycle)	t_{OECS}		20			ns
Write pulse width 1 (write cycle 1) Note 1	t_{WP1}		50			ns
Write pulse width 2 (write cycle 2) Note 1	t_{WP2}		50			ns
Data setup time (write cycle 1, 2)	t_{DW}		20			ns
Data hold time (write cycle 1, 2)	t_{DH}		20			ns
/CS-/WE time (write cycle 1, 2)	t_{CSWE}		10			ns
/WE-/CS time (write cycle 1, 2)	t_{WECS}		20			ns
Reset pulse width	t_{WRES}		100			ns
RDY-/OE time	t_{RDOE}				**Note 4**	-
RDY-/WE time	t_{RDWE}				**Note 4**	-

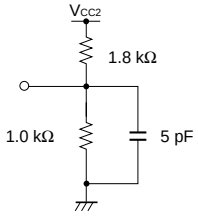
Notes 1. Load circuit



2. Load circuit

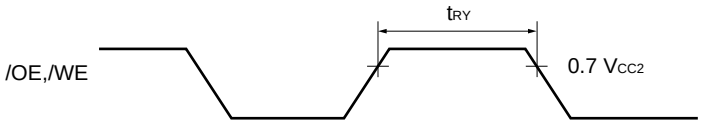


3. Load circuit

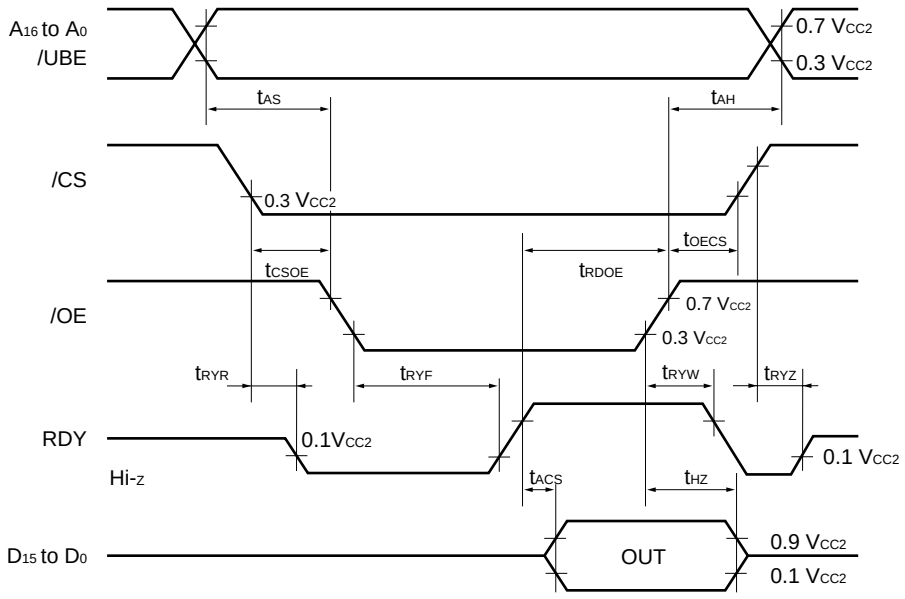


4. If the time from the rising edge of RDY to /OE or /WE is long, the display may be adversely affected. It is therefore recommended that t_{RDOE} and t_{RDWE} be set to a value not exceeding 1000 ns.

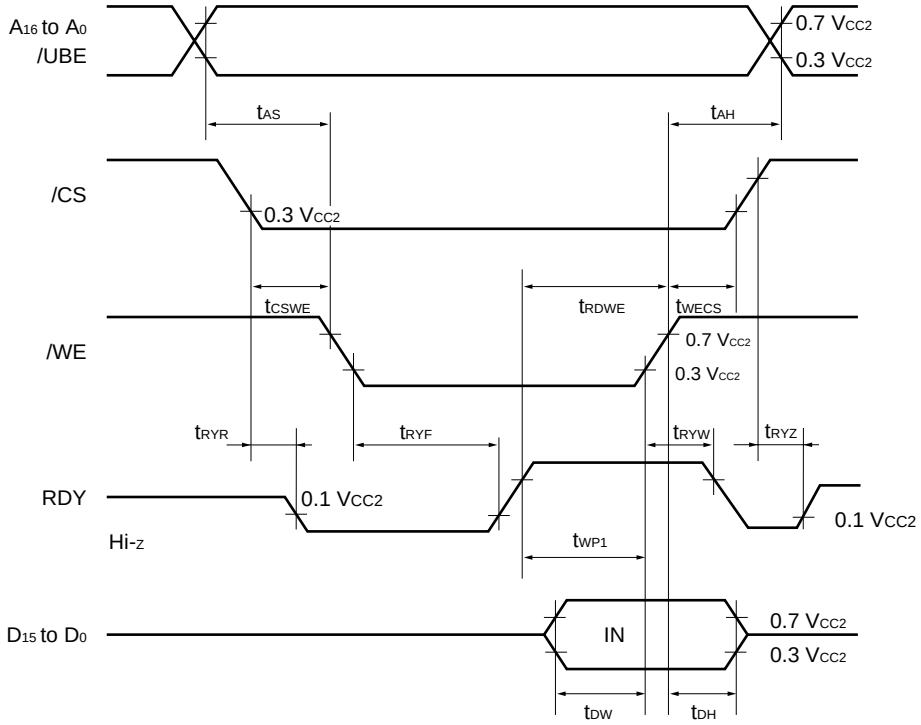
/OE, /WE Recovery Time



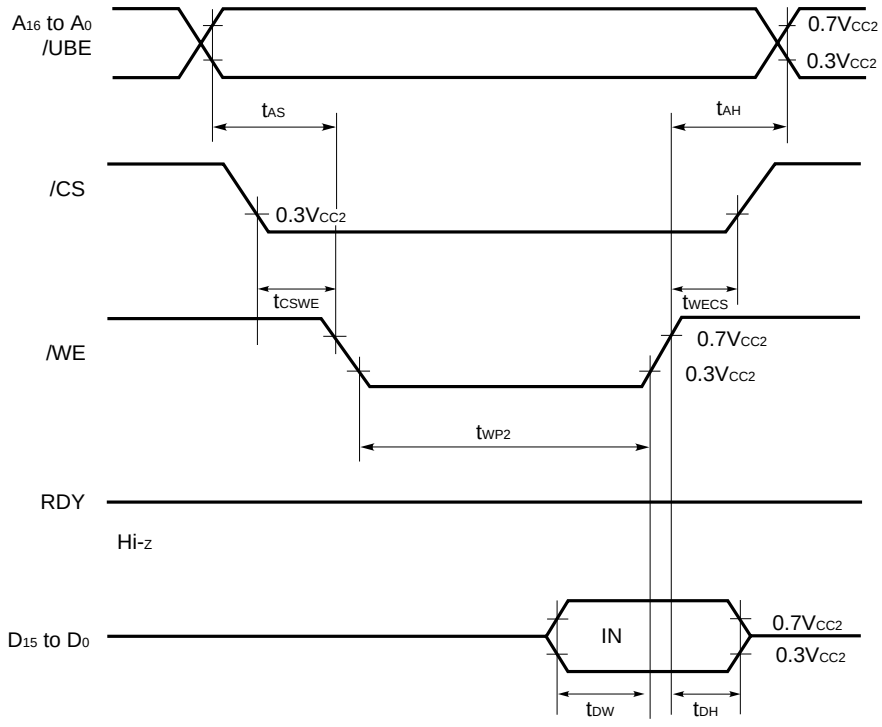
Read Cycle



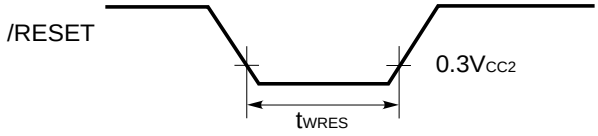
Write Cycle 1 (Display Data Write)



Write Cycle 2 (Gray Scale Palette Data Write)



Reset Pulse Width



AC Characteristics 3 CR Oscillator

(V_{CC2} = 3.0 to 3.6 V, T_A = –20°C to +70°C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Units
Oscillation frequency	f_{OSC}	External resistor (62 kΩ)	160	190	220	kHz
Frame frequency	-	External resistor (62 kΩ)	61.7	73.3	84.9	Hz

Relationship between oscillation frequency and frame frequency / STB frequency

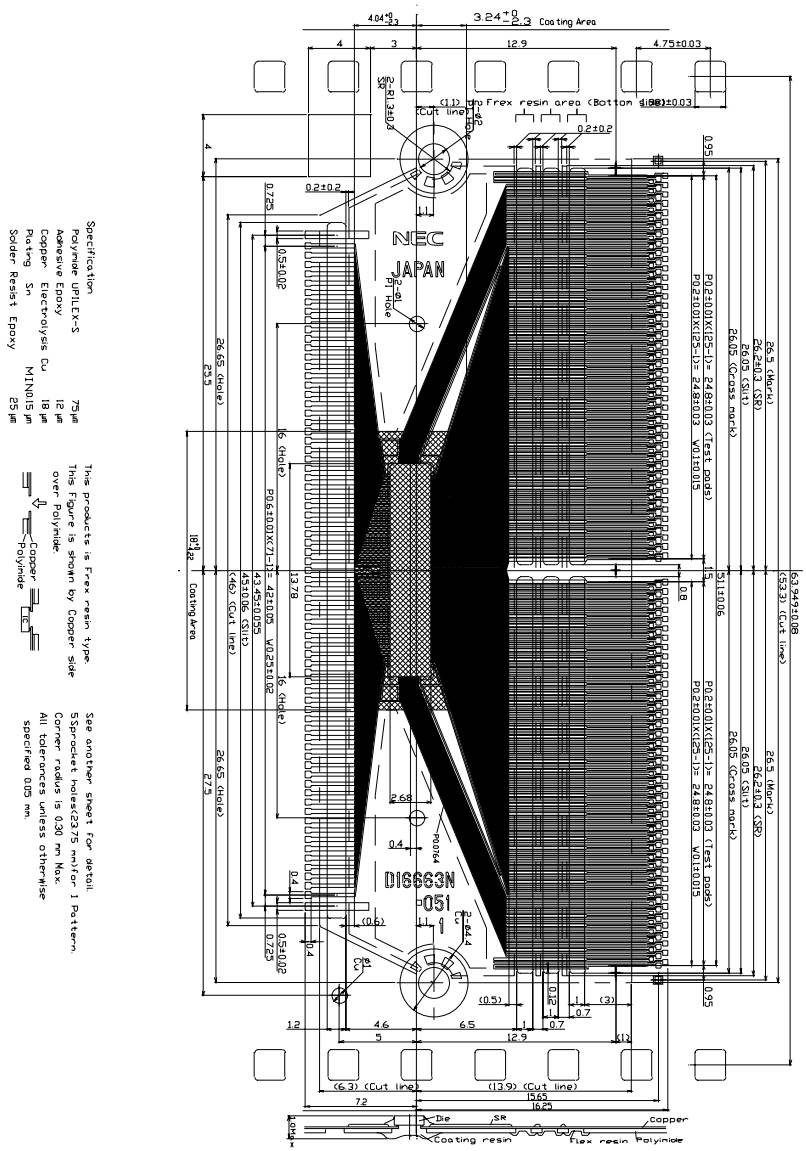
The relationship between the oscillation frequency and the frame frequency / STB frequency is as follows.

$$\text{Frame frequency} = \frac{1}{162 \times 2 \times 8} \times \text{oscillation frequency}$$

$$\text{STB frequency} = \frac{1}{2 \times 8} \times \text{oscillation frequency}$$

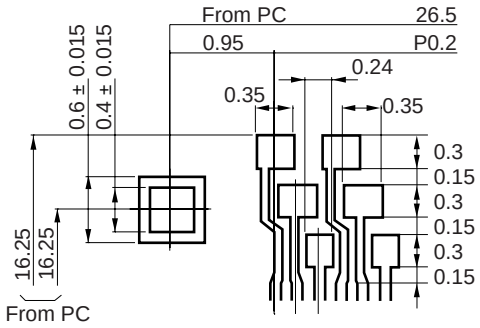
16. PACKAGE DRAWINGS

Standard TCP Package Drawings (μPD16663N-051) (1/3)

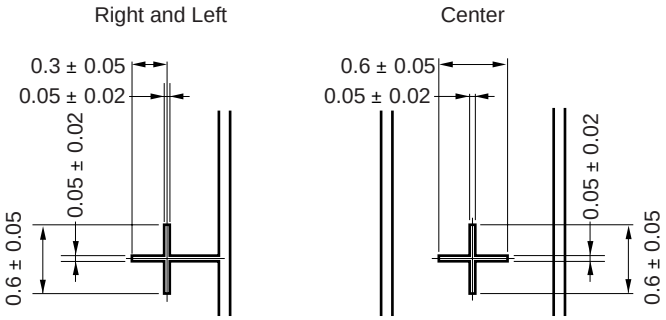


Standard TCP Package Drawings (μPD16663N-051) (2/3)

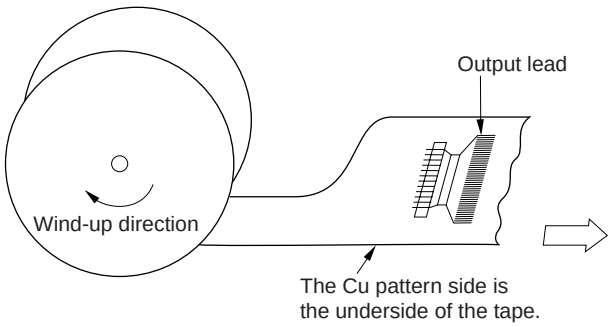
Test pad details



Alignment details

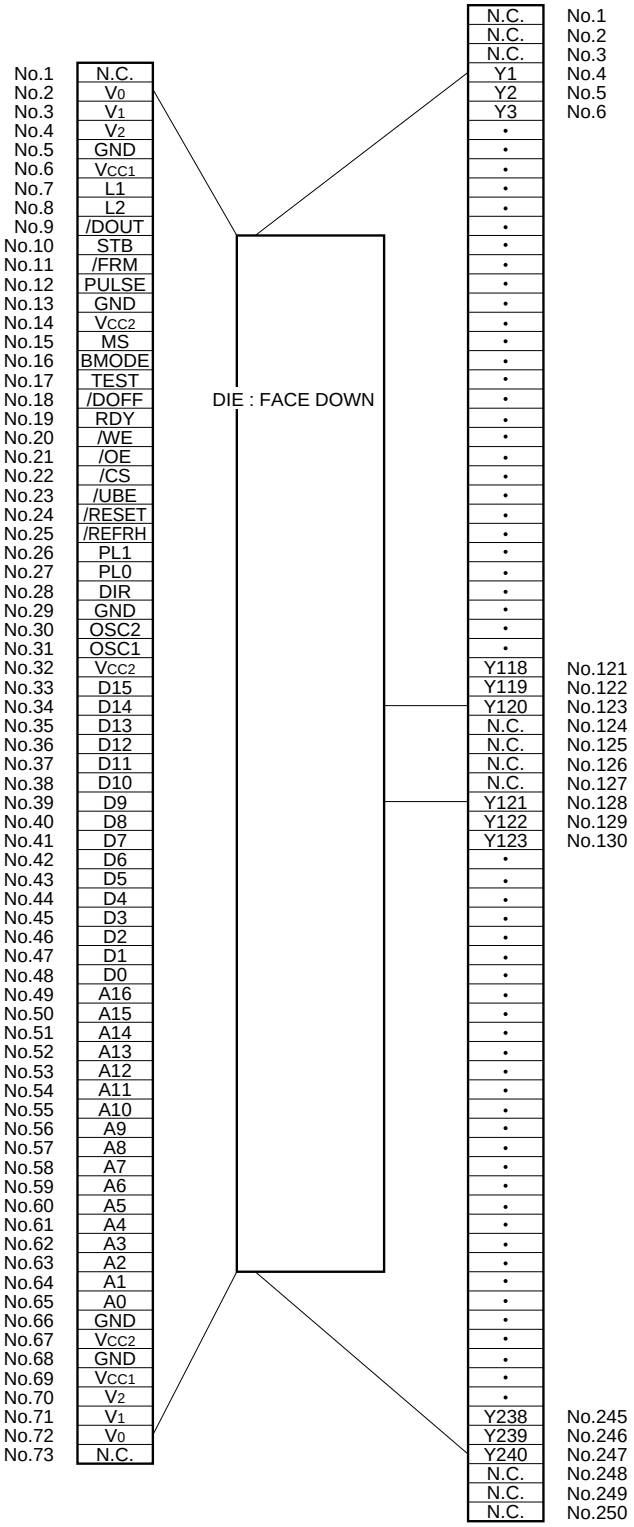


TCP tape winding direction



Standard TCP Package Drawings (μPD16663N-051) (3/3)

Pin connection diagram



[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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