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Old Company Name in Catalogs and Other Documents

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April 1st, 2010
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DATA SHEET

RENESAS

MOS INTEGRATED CIRCUIT

μPD16641

240-OUTPUT TFT-LCD SOURCE DRIVER (64-GRAY SCALES)

DESCRIPTION

The μPD16641 is a source driver for TFT-LCD 64-gray scale displays. Its logic circuit operates at 3.3 V and the driver circuit operates at 3.3 or 5.0 V (selectable). The input data is digital data at 6 bits x 3 dots, and 260,000 colors can be displayed in 64-value outputs γ-corrected by the internal D/A converter and 11 external power supplies.

The clock frequency is 33 MHz, and the μPD16641 can be used in TFT-LCD panels conforming to the VGA standards.

FEATURES

- CMOS level input
- 240 outputs
- 6 bits (gray scale data) x 3 dots input
- 64-value output by 11 external power supplies and internal D/A converter
- High-speed data transfer: f_{CLK} = 33 MHz MAX. (internal data transfer speed when V_{DD1} = 3.0 V)
- Pre-charge-less output buffer
- Level of γ-corrected power supply can be inverted.
- Driver power supply voltage selectable is possible (V_{sel} = H: 3.3 V, V_{sel} = L: 5.0 V)
- Output voltage range: 2.8 V_{P-P} MAX. (driver power supply voltage V_{DD2} = 3.0)
  4.3 V_{P-P} MAX. (driver power supply voltage V_{DD2} = 4.5)
- Loaded with slim TCP

ORDERING INFORMATION

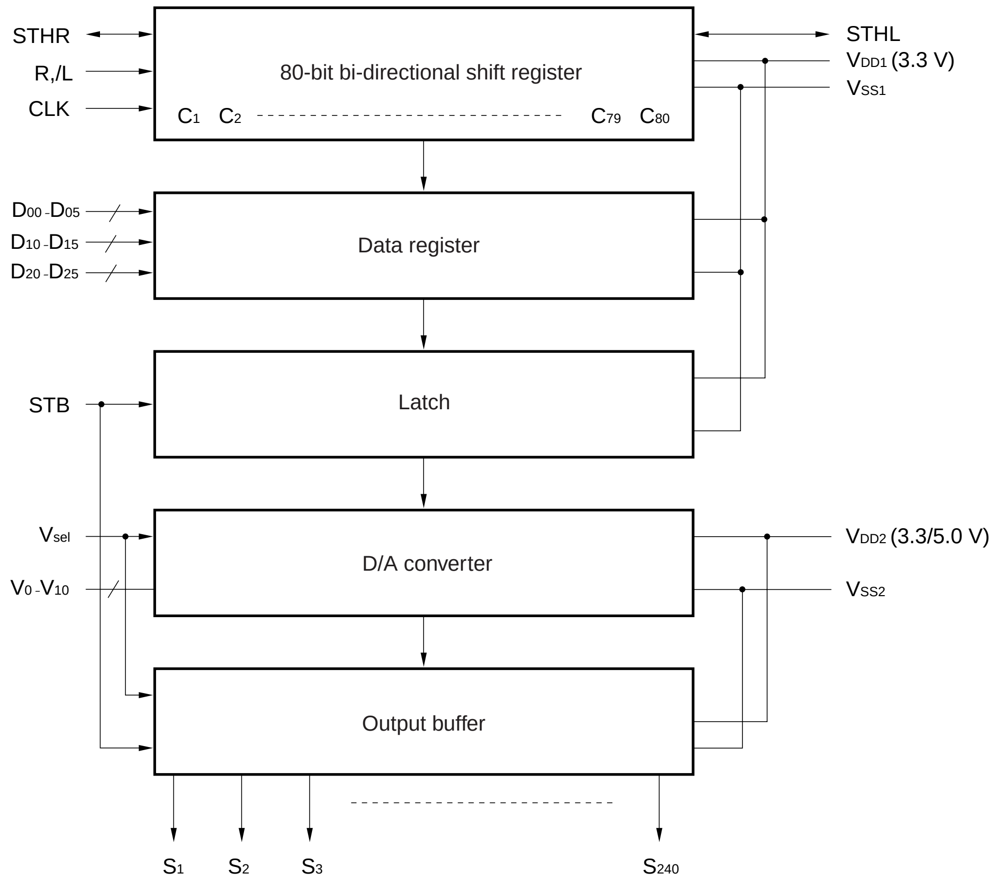
Part Number	Package
μPD16641N-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order your TCP's external shape, please contact one of our sales representatives.

Document No. S10565EJ2V0DS00 (2nd edition)
Date Published July 2005 NS CP (K)
Printed in Japan

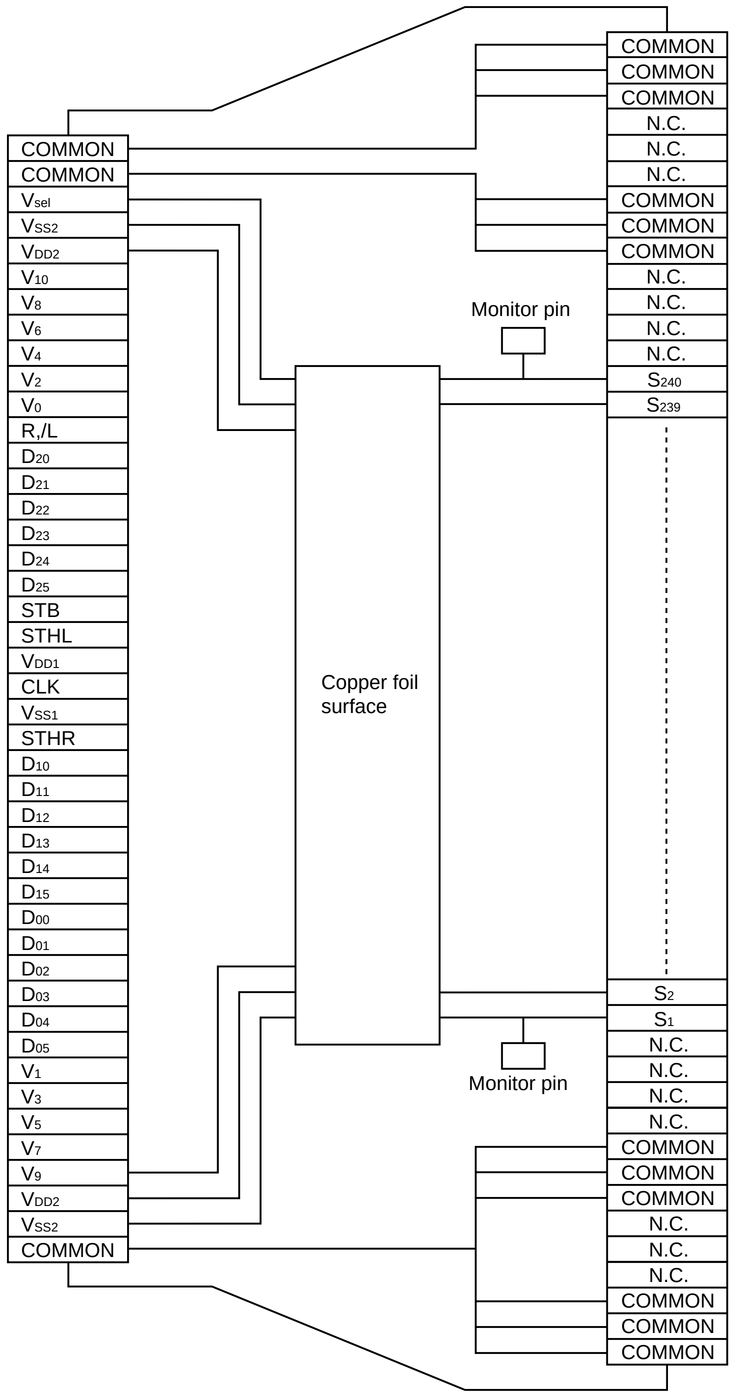
The mark ★ shows major revised points.

★ 1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (μPD16641N-xxx) (Copper Foil Surface)



Remarks 1. N.C.: No connection

2. O_{sel} and V_{sel} pins are internally pulled up.

Therefore, the number of input pins can be reduced by opening or short-circuiting these pins to V_{SS2} by means of TCP writing.

★ 3. PIN FUNCTIONS

Pin Symbol	Pin Name	I/O	Description
S_1 to S_{240}	Driver output	Output	Output 64-gray scale analog voltages converted from digital signals.
D_{00} to D_{05} D_{10} to D_{15} D_{20} to D_{25}	Display data input	Input	Inputs 18-bit-wide display gray scale data (6 bits) x 3 dots (RGB). D_{X0} : LSB, D_{X5} : MSB
R,/L	Shift direction select input	Input	This pin inputs/outputs start pulses in cascade mode. Shift direction of shift register is as follows: R,/L = H : STHR input, $S_1 \rightarrow S_{240}$, STHL output R,/L = L : STHL input, $S_{240} \rightarrow S_1$, STHR output
STHR	Right shift start pulse I/O	I/O	R,/L = H : Inputs start pulse R,/L = L : Outputs start pulse
STHL	Left shift start pulse I/O	I/O	R,/L = H : Outputs start pulse R,/L = L : Inputs start pulse
V_{sel}	Driver voltage selection	Input	Selects driver voltage. This pin is internally pulled up by V_{DD2} power supply. V_{sel} = V_{DD2} or open: V_{DD2} = 3.3 V ± 0.3 V V_{sel} = L: V_{DD2} = 5.0 V ± 0.5 V
CLK	Shift clock input	Input	Inputs shift clock to shift register. Display data is loaded to data register at rising edge of this pin. Start pulse output goes H level at rising edge of 80th clock after start pulse has been input, and serves as start pulse to driver in next stage. 80th clock of driver in first stage serves as start pulse of driver in next stage.
STB	Latch input	Input	Contents of data register are latched at rising edge, transferred to D/A converter, and output as analog voltage corresponding to display data. Contents of internal shift register are cleared after STB has been input. One pulse of this signal is input when μPD16641 is started, and then device operates normally. For STB input timing, refer to **Switching Characteristic Waveform.**
V_0-V_{10}	γ-corrected power supply	–	Inputs γ-corrected power from external source. $V_{SS2} \le V_{10} \le V_9 \le V_8 \le V_7 \le V_6 \le V_5 \le V_4 \le V_3 \le V_2 \le V_1 \le V_0 \le V_{DD2}$ or $V_{SS2} \le V_0 \le V_1 \le V_2 \le V_3 \le V_4 \le V_5 \le V_6 \le V_7 \le V_8 \le V_9 \le V_{10} \le V_{DD2}$ Maintain gray scale power supply during gray scale voltage output.
V_{DD1}	Logic circuit power supply	–	3.3 V ± 0.3 V
V_{DD2}	Driver circuit power supply	–	V_{sel} = V_{DD2} or open: V_{DD2} = 3.3 V ± 0.3 V V_{sel} = L: V_{DD2} = 5.0 V ± 0.5 V
V_{SS1}	Logic ground	–	Ground
V_{SS2}	Driver ground	–	Ground

Caution Be sure to turn on power in the order V_{DD1}, logic input, V_{DD2}, and gray scale power (V_0-V_{10}), and turn off power in the reverse order, to prevent the μPD16641 from being damaged by latchup.

Be sure to observe this power sequence even during a transition period.

4. RELATION BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The 11 major points on the γ-characteristic curve of the LCD panel are arbitrarily set by external power supplies V_0 through V_{10}. If the display data is 00H or 3FH, gray scale voltage V_0 or V_{10} is output. If the display data is in the range 01H to 3EH, the high-order 3 bits select an external powers pair V_{n+1}, V_n. The low-order 3 bits evenly divide the range of V_{n+1}, V_n into eight segments by means of D/A conversion (however, the ranges from V_9-V_8 and from V_2-V_1 are divided into seven segments) to output a 64-grayscale voltage.

D_{X5} (MSB)	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0} (LSB)

High-order 3 bits : γ-corrected power selected (V_{n+1}-V_n)

Low-order 3 bits : 3-bit D/A (range V_n-V_{n+1} is divided into 7 or 8 segments)

D_{X5}	D_{X4}	D_{X3}	V_{n+1}-V_n
0	0	0	V_1-V_2
0	0	1	V_2-V_3
0	1	0	V_3-V_4
0	1	1	V_4-V_5
1	0	0	V_5-V_6
1	0	1	V_6-V_7
1	1	0	V_7-V_8
1	1	1	V_8-V_9

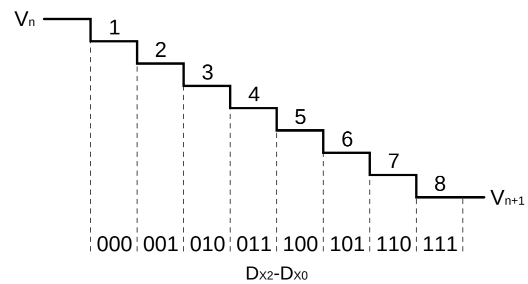


Figure 4–1. Relation between Input Data and γ-corrected Voltage

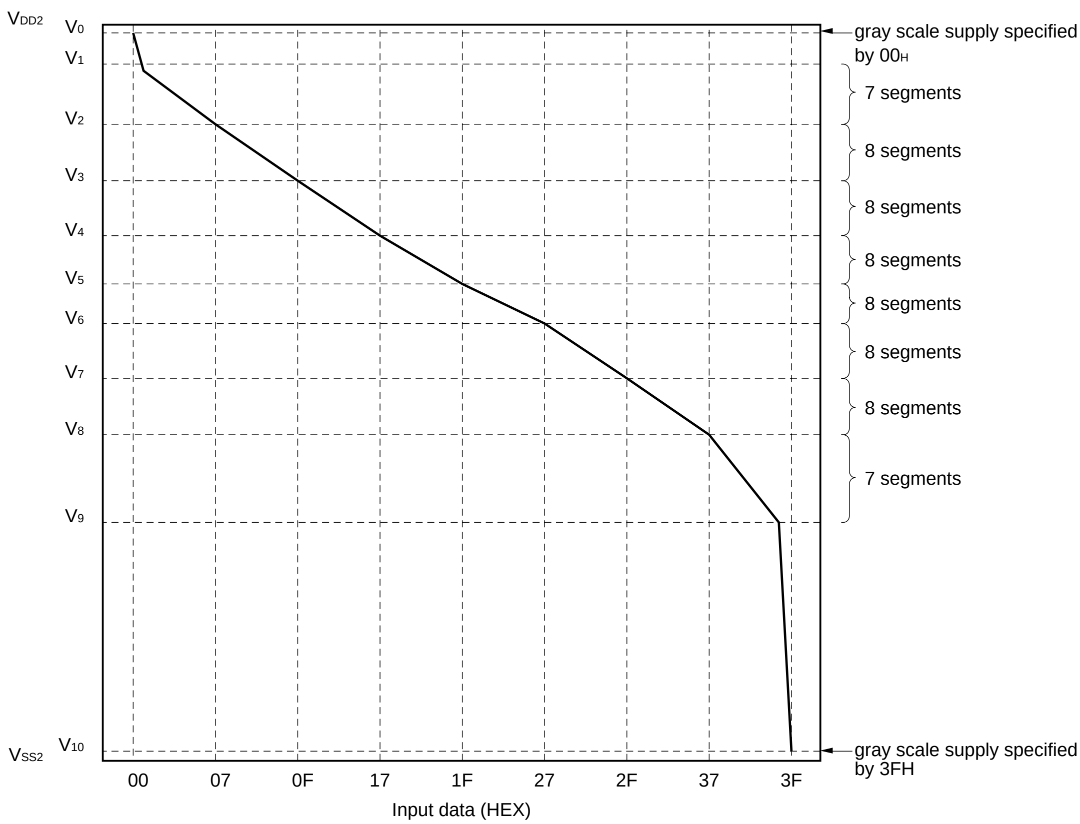


Table 4–1. Relation between Input Data and Output Voltage (1/2)

Input Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage
00H	0	0	0	0	0	0	V_0
01H	0	0	0	0	0	1	$V_2 + (V_1 - V_2) \times 6/7$
02H	0	0	0	0	1	0	$V_2 + (V_1 - V_2) \times 5/7$
03H	0	0	0	0	1	1	$V_2 + (V_1 - V_2) \times 4/7$
04H	0	0	0	1	0	0	$V_2 + (V_1 - V_2) \times 3/7$
05H	0	0	0	1	0	1	$V_2 + (V_1 - V_2) \times 2/7$
06H	0	0	0	1	1	0	$V_2 + (V_1 - V_2) \times 1/7$
07H	0	0	0	1	1	1	V_2
08H	0	0	1	0	0	0	$V_3 + (V_2 - V_3) \times 7/8$
09H	0	0	1	0	0	1	$V_3 + (V_2 - V_3) \times 6/8$
0AH	0	0	1	0	1	0	$V_3 + (V_2 - V_3) \times 5/8$
0BH	0	0	1	0	1	1	$V_3 + (V_2 - V_3) \times 4/8$
0CH	0	0	1	1	0	0	$V_3 + (V_2 - V_3) \times 3/8$
0DH	0	0	1	1	0	1	$V_3 + (V_2 - V_3) \times 2/8$
0EH	0	0	1	1	1	0	$V_3 + (V_2 - V_3) \times 1/8$
0FH	0	0	1	1	1	1	V_3
10H	0	1	0	0	0	0	$V_4 + (V_3 - V_4) \times 7/8$
11H	0	1	0	0	0	1	$V_4 + (V_3 - V_4) \times 6/8$
12H	0	1	0	0	1	0	$V_4 + (V_3 - V_4) \times 5/8$
13H	0	1	0	0	1	1	$V_4 + (V_3 - V_4) \times 4/8$
14H	0	1	0	1	0	0	$V_4 + (V_3 - V_4) \times 3/8$
15H	0	1	0	1	0	1	$V_4 + (V_3 - V_4) \times 2/8$
16H	0	1	0	1	1	0	$V_4 + (V_3 - V_4) \times 1/8$
17H	0	1	0	1	1	1	V_4
18H	0	1	1	0	0	0	$V_5 + (V_4 - V_5) \times 7/8$
19H	0	1	1	0	0	1	$V_5 + (V_4 - V_5) \times 6/8$
1AH	0	1	1	0	1	0	$V_5 + (V_4 - V_5) \times 5/8$
1BH	0	1	1	0	1	1	$V_5 + (V_4 - V_5) \times 4/8$
1CH	0	1	1	1	0	0	$V_5 + (V_4 - V_5) \times 3/8$
1DH	0	1	1	1	0	1	$V_5 + (V_4 - V_5) \times 2/8$
1EH	0	1	1	1	1	0	$V_5 + (V_4 - V_5) \times 1/8$
1FH	0	1	1	1	1	1	V_5
20H	1	0	0	0	0	0	$V_6 + (V_5 - V_6) \times 7/8$
21H	1	0	0	0	0	1	$V_6 + (V_5 - V_6) \times 6/8$
22H	1	0	0	0	1	0	$V_6 + (V_5 - V_6) \times 5/8$
23H	1	0	0	0	1	1	$V_6 + (V_5 - V_6) \times 4/8$
24H	1	0	0	1	0	0	$V_6 + (V_5 - V_6) \times 3/8$
25H	1	0	0	1	0	1	$V_6 + (V_5 - V_6) \times 2/8$
26H	1	0	0	1	1	0	$V_6 + (V_5 - V_6) \times 1/8$
27H	1	0	0	1	1	1	V_6
28H	1	0	1	0	0	0	$V_7 + (V_6 - V_7) \times 7/8$
29H	1	0	1	0	0	1	$V_7 + (V_6 - V_7) \times 6/8$
2AH	1	0	1	0	1	0	$V_7 + (V_6 - V_7) \times 5/8$
2BH	1	0	1	0	1	1	$V_7 + (V_6 - V_7) \times 4/8$
2CH	1	0	1	1	0	0	$V_7 + (V_6 - V_7) \times 3/8$
2DH	1	0	1	1	0	1	$V_7 + (V_6 - V_7) \times 2/8$
2EH	1	0	1	1	1	0	$V_7 + (V_6 - V_7) \times 1/8$
2FH	1	0	1	1	1	1	V_7

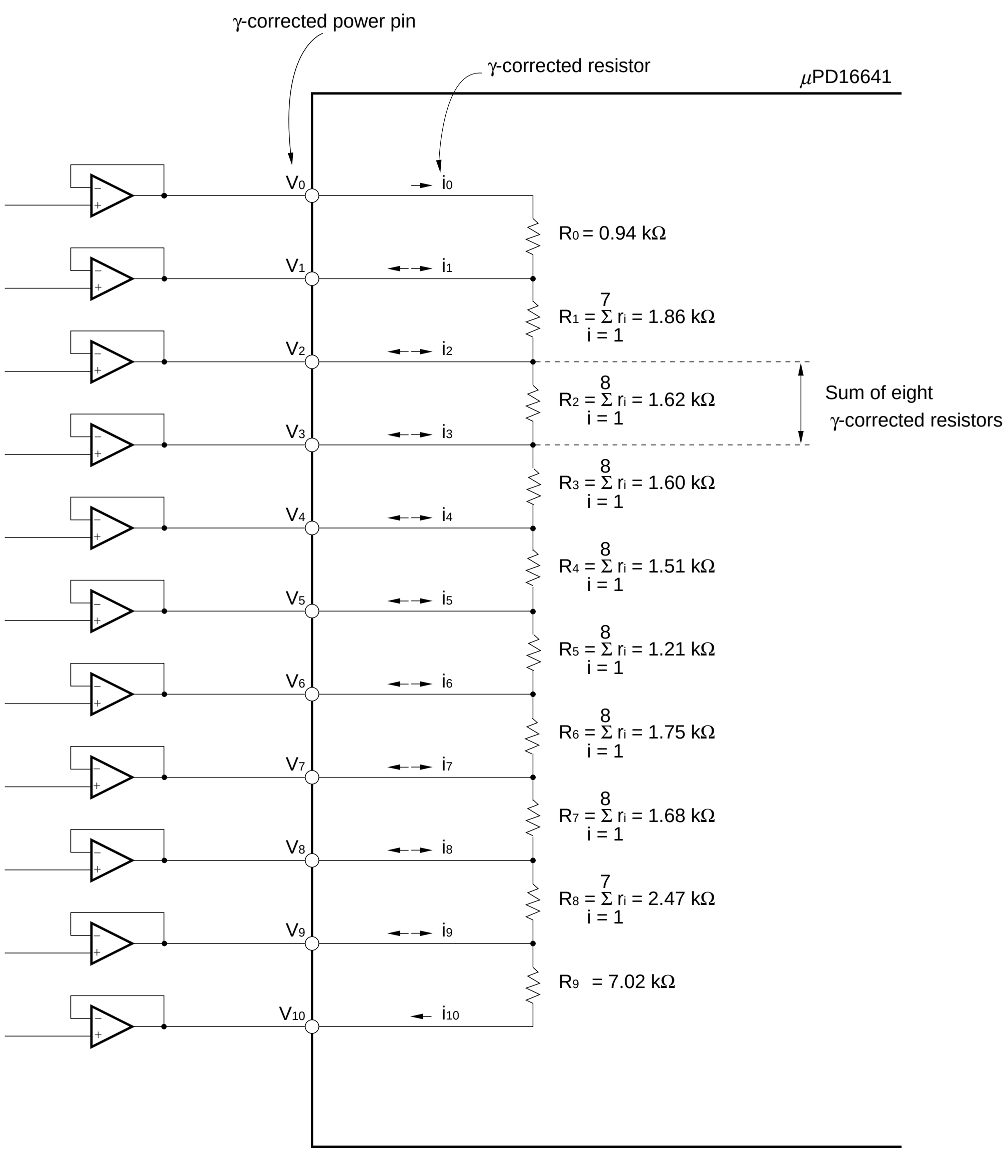
Table 4–1. Relation between Input Data and Output Voltage (2/2)

Input Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage
30H	1	1	0	0	0	0	$V_8 + (V_7 - V_8) \times 7/8$
31H	1	1	0	0	0	1	$V_8 + (V_7 - V_8) \times 6/8$
32H	1	1	0	0	1	0	$V_8 + (V_7 - V_8) \times 5/8$
33H	1	1	0	0	1	1	$V_8 + (V_7 - V_8) \times 4/8$
34H	1	1	0	1	0	0	$V_8 + (V_7 - V_8) \times 3/8$
35H	1	1	0	1	0	1	$V_8 + (V_7 - V_8) \times 2/8$
36H	1	1	0	1	1	0	$V_8 + (V_7 - V_8) \times 1/8$
37H	1	1	0	1	1	1	V_8
38H	1	1	1	0	0	0	$V_9 + (V_8 - V_9) \times 6/7$
39H	1	1	1	0	0	1	$V_9 + (V_8 - V_9) \times 5/7$
3AH	1	1	1	0	1	0	$V_9 + (V_8 - V_9) \times 4/7$
3BH	1	1	1	0	1	1	$V_9 + (V_8 - V_9) \times 3/7$
3CH	1	1	1	1	0	0	$V_9 + (V_8 - V_9) \times 2/7$
3DH	1	1	1	1	0	1	$V_9 + (V_8 - V_9) \times 1/7$
3EH	1	1	1	1	1	0	V_9
3FH	1	1	1	1	1	1	V_{10}

4.1 γ-corrected Power Circuit

The reference power supply of the D/A converter consists of a ladder circuit with a total of 64 resistors, and resistance Σr_i between γ-corrected power pins differs depending on each pair of γ-corrected power pins. One pair of γ-corrected power pins consists of seven or eight series resistors, and resistance Σr_i in the figure below is indicated as the sum of the seven or eight resistors. The resistance ratio between the γ-corrected power pins (Σr_i ratio) is designed to be a value relatively close to the ratio of the γ-corrected voltages V_1-V_9 (gray-scale voltages in 8 steps) used in an actual LCD panel. Under ideal conditions where there is no difference between the two, therefore, there is no voltage difference between the voltage of the γ-corrected power supplies and the gray-scale voltages in 8 steps of the resistor ladder circuits of the μPD16641, and no current flows into the γ-corrected power pins V_1-V_9. As a result, a voltage-follower circuit is not necessary.

★ **Figure 4–2. γ-corrected Power Circuit**



5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 6 bits x RGB (3 dots)
Input width : 18 bits (1-pixel data)

(1) R,/L = H (right shift)

Output	S_1	S_2	S_3	…	S_{239}	S_{240}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	…	D_{10} to D_{15}	D_{20} to D_{25}

(2) R,/L = L (left shift)

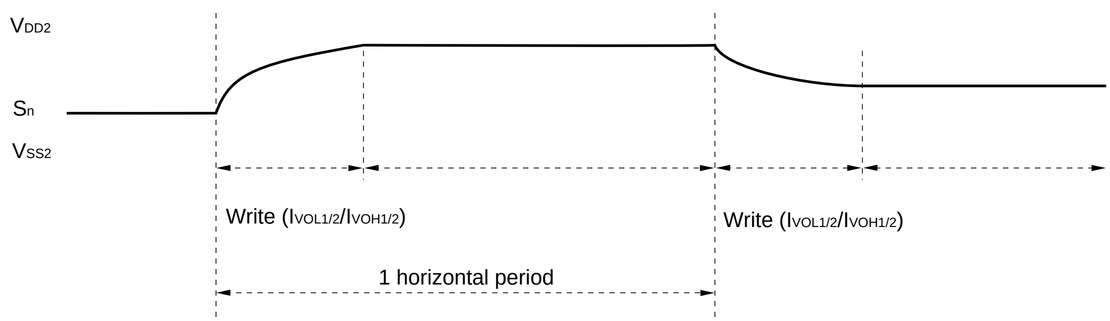
Output	S_1	S_2	S_3	…	S_{239}	S_{240}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	…	D_{10} to D_{15}	D_{20} to D_{25}

6. OPERATION OF OUTPUT BUFFER

The output buffer consists of an operational amplifier circuit that does not perform pre-charge operation. Therefore, driver output current $I_{VOH1/2}$ is the charging current to the LCD, and $I_{VOL1/2}$ is the discharging current.

The chip has the driving capability to charge or discharge a liquid load with C_L = 80 pF to 3 τ in less than 10 μs.

Figure 6–1. LCD Panel Driving Waveform



7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ($V_{SS1} = V_{SS2} = 0$ V)

Parameter	Symbol	Ratings	Unit
Logic power supply	V_{DD1}	–0.3 to +4.5	V
Driver power supply	V_{DD2}	–0.3 to +7.0	V
Input voltage	V_I	–0.3 to $V_{DD1,2}$ + 0.3	V
Output voltage	V_O	–0.3 to $V_{DD1,2}$ + 0.3	V
Operating ambient temperature	T_A	–10 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

★ **Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.**

Recommended Operating Range (T_A = –10 to +75°C, $V_{SS1} = V_{SS2} = 0$ V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD1}		3.0	3.3	3.6	V
Driver supply voltage	V_{DD2}	V_{sel} = H	3.0	3.3	3.6	V
		V_{sel} = L	4.5	5.0	5.5	V
High-level input voltage	V_{IH}	R,/L, CLK, STB, STHR (STHL), D_{00}-D_{05},D_{10}-D_{15}, D_{20}-D_{25}	0.7 V_{DD1}		V_{DD1}	V
Low-level input voltage	V_{IL}		0		0.3 V_{DD1}	V
γ-corrected supply voltage	V_0-V_{10}		V_{SS2}+0.1		V_{DD2}–0.1	V
Maximum clock frequency	f_{CLK}				33	MHz
Output load capacitance	C_L				150	pF

Electrical Characteristics (T_A = –10 to +75°C, V_{DD1} = 3.0 to 3.6 V, V_{DD2} = 3.0 to 3.6 V or 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{IL}	D_{00}-D_{05}, D_{10}-D_{15}, D_{20}-D_{25}, R,/L, STB, STHR (STRL)				±1.0	μA
Pull-up resistor	R_{PU}	V_{DD2} = 5.0 V, V_{sel}, V_{sel} = 0 V		40	100	250	kΩ
High level output voltage	V_{OH}	STHR(STHL), I_O = –1.0 mA		V_{DD1} – 0.5			V
Low level output voltage	V_{OL}	STHR(STHL), I_O = +1.0 mA				0.5	V
Static current consumption of γ-corrected power (V_{DD2} = 3.3 V)	I_{vn1}	V_{DD1} = 3.3 V, V_{DD2} = 3.3 V, V_0 = 3.20 V, V_1 = 3.07 V, V_2 = 2.80 V, V_3 = 2.57 V, V_4 = 2.34 V, V_5 = 2.12 V, V_6 = 1.95 V, V_7 = 1.70 V, V_8 = 1.46 V, V_9 = 1.11 V, V_{10} = 0.10 V Note1	V_{10}	–200	–150		μA
			V_9-V_1		±10		μA
			V_0		150	200	μA
Static current consumption of γ-corrected power (V_{DD2} = 5.0 V)	I_{vn2}	V_{DD1} = 3.3 V, V_{DD2} = 5.0 V, V_0 = 4.90 V, V_1 = 4.69 V, V_2 = 4.28 V, V_3 = 3.92 V, V_4 = 3.56 V, V_5 = 3.23 V, V_6 = 2.96 V, V_7 = 2.58 V, V_8 = 2.20 V, V_9 = 1.66 V, V_{10} = 0.1 V Note1	V_{10}	–300	–250		μA
			V_9-V_1		±10		μA
			V_0		250	300	μA
Driver output current (V_{DD2} = 3.3 V)	I_{VOH1}	STB = 3.3 V, V_{OUT} = 2.2 V, V_X = 3.2 V Note2, V_{DD1} = V_{DD2} = 3.3 V			–3	–0.075	mA
	I_{VOL1}	STB = 3.3 V, V_{OUT} = 1.1 V, V_X = 0.1 V Note2, V_{DD1} = V_{DD2} = 3.3 V		0.075	0.25		mA
Driver output current (V_{DD2} = 5.0 V)	I_{VOH2}	STB = 5.0 V, V_{OUT} = 3.9 V, V_X = 4.9 V Note2, V_{DD1} = 3.3 V, V_{DD2} = 5.0 V			–0.3	–0.1	mA
	I_{VOL2}	STB = 5.0 V, V_{OUT} = 1.1 V, V_X = 0.1 V Note2, V_{DD1} = 3.3 V, V_{DD2} = 5.0 V		0.1	0.25		mA
Output voltage deviation	ΔV_O	V_{DD1} = 3.3 V, V_{DD2} = 3.3 V, V_{OUT} = 1.65 V			±20	±25	mV
		V_{DD1} = 3.3 V, V_{DD2} = 5.0 V, V_{OUT} = 2.50 V			±20	±25	mV
Output voltage range	V_O	Input data: 00H to 3FH		V_{SS2} + 0.1		V_{DD2} – 0.1	V
Dynamic logic current consumption	I_{DD1}	No load Note3				2.0	mA
Dynamic driver current consumption	I_{DD21}	No load, V_{DD2} = 3.3 V ± 0.3 V Note3				5.0	mA
	I_{DD22}	No load, V_{DD2} = 5.0 V ± 0.5 V Note3				6.5	mA

Notes 1. Apply ideal voltage to V_1-V_9 that is calculated from internal resistor.

2. V_X is output voltage of analog output pins S_1 to S_{240}.
V_{OUT} is the voltage applied to analog output pins S_1 to S_{240}.

3. The STB cycle is specified at 31 μs and f_{CLK} = 16 MHz. Input data:1010 ... (checkerboard pattern)
Refers to current consumption per driver when cascades are connected under the assumption of VGA single-sided mounting (8 units).

Switching Characteristics (T_A = –10 to +75°C, V_{DD1} = 3.0 to 3.6 V, V_{DD2} = 3.0 to 3.6 V or 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 3.0 ns)

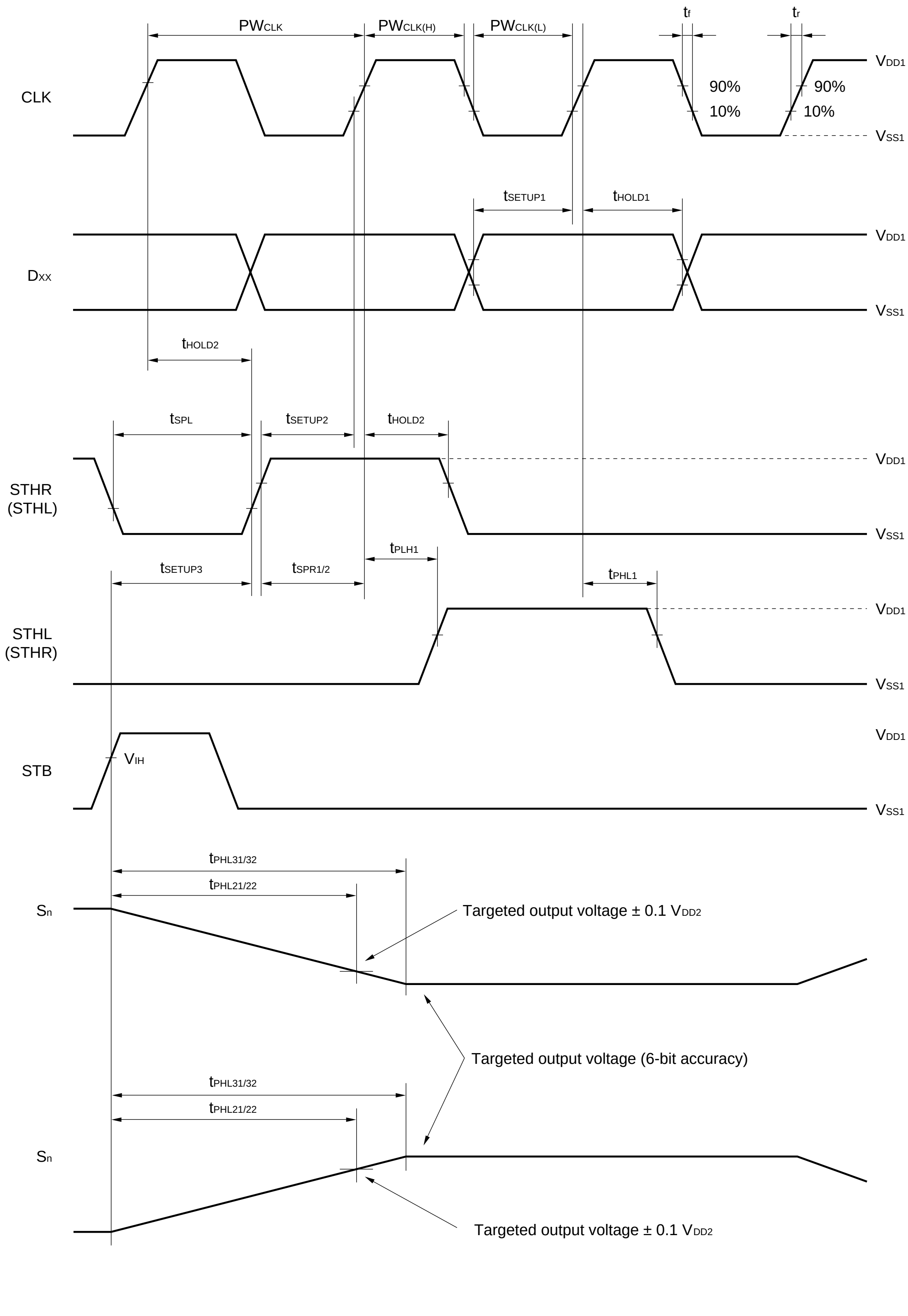
Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Start pulse delay time	t_{PLH1}	C_L = 15 pF		2.0		17	ns
	t_{PHL1}			2.0		17	ns
Driver output delay time	t_{PLH21}	V_{DD2} = 3.3 V, 2 kΩ +75 pF x 2	V_O: 0.1 V → 3.2 V		6.0	12	μs
	t_{PLH31}				8.0	14	μs
	t_{PHL21}		V_O: 3.2 V → 0.1 V		6.0	10	μs
	t_{PHL31}				8.0	12	μs
Driver output delay time	t_{PLH22}	V_{DD2} = 5.0 V, 2 kΩ +75 pF x 2	V_O: 0.1 V → 4.9 V		6.0	10	μs
	t_{PLH32}				8.0	12	μs
	t_{PHL22}		V_O: 4.9 V → 0.1 V		6.0	8.0	μs
	t_{PHL32}				8.0	10	μs
Input capacitance	C_{I1}	V_0-V_{10}, T_A = 25°C			100		pF
	C_{I2}	STHR(STHL), T_A = 25°C			10	15	pF
	C_{I3}	STHR(STHL), except V_0-V_{10}, T_A = 25 °C			7.0	10	pF

Timing Requirements (T_A = –10 to +75°C, V_{DD1} = 3.0 to 3.6 V, V_{DD2} = 3.0 to 3.6 V or 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 3.0 ns)

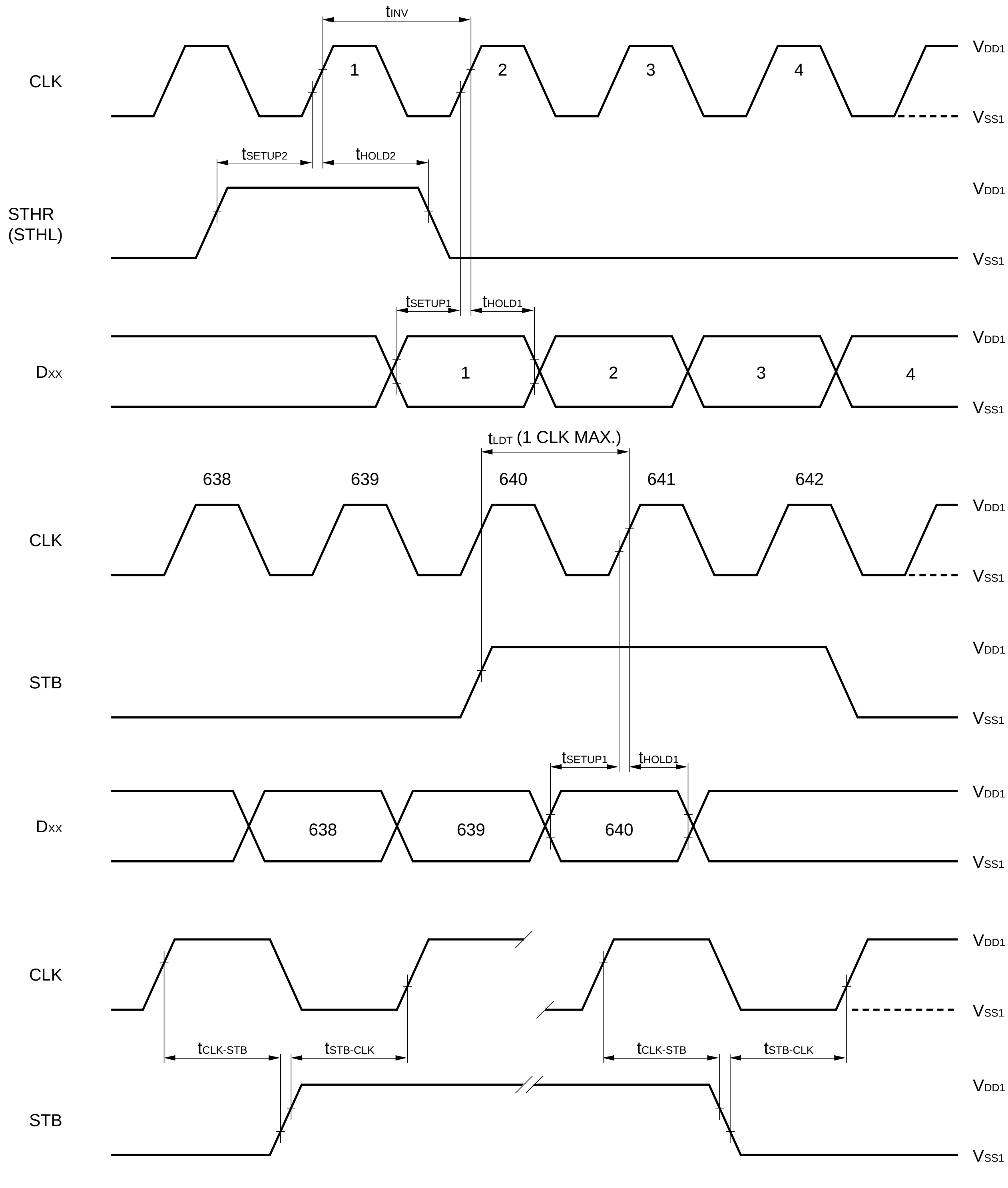
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW_{CLK}		22			ns
Clock pulse low period	$PW_{CLK\ (L)}$		4.0			ns
Clock pulse high period	$PW_{CLK\ (H)}$		4.0			ns
Data setup time	t_{SETUP1}		2.0			ns
Data hold time	t_{HOLD1}		2.0			ns
Start pulse setup time	t_{SETUP2}		2.0			ns
Start pulse hold time	t_{HOLD2}		2.0			ns
Start pulse low period	t_{SPL}		2			CLK
Start pulse rise time	t_{SPR}			80		CLK
Final data timing	t_{SETUP3}		2			CLK
CLK-STB time	t_{INV}			1		CLK
STB-CLK time	t_{LDT}		1			CLK
Time between STB and start pulse	$t_{CLK\text{-}STB}$	CLK↑→STB↑ or ↓	7.0			ns
STB-POL time	$t_{STB\text{-}CLK}$	STB↑ or ↓ →CLK↑	7.0			ns

Switching Characteristic Waveform (R,/L= H) (1/2)

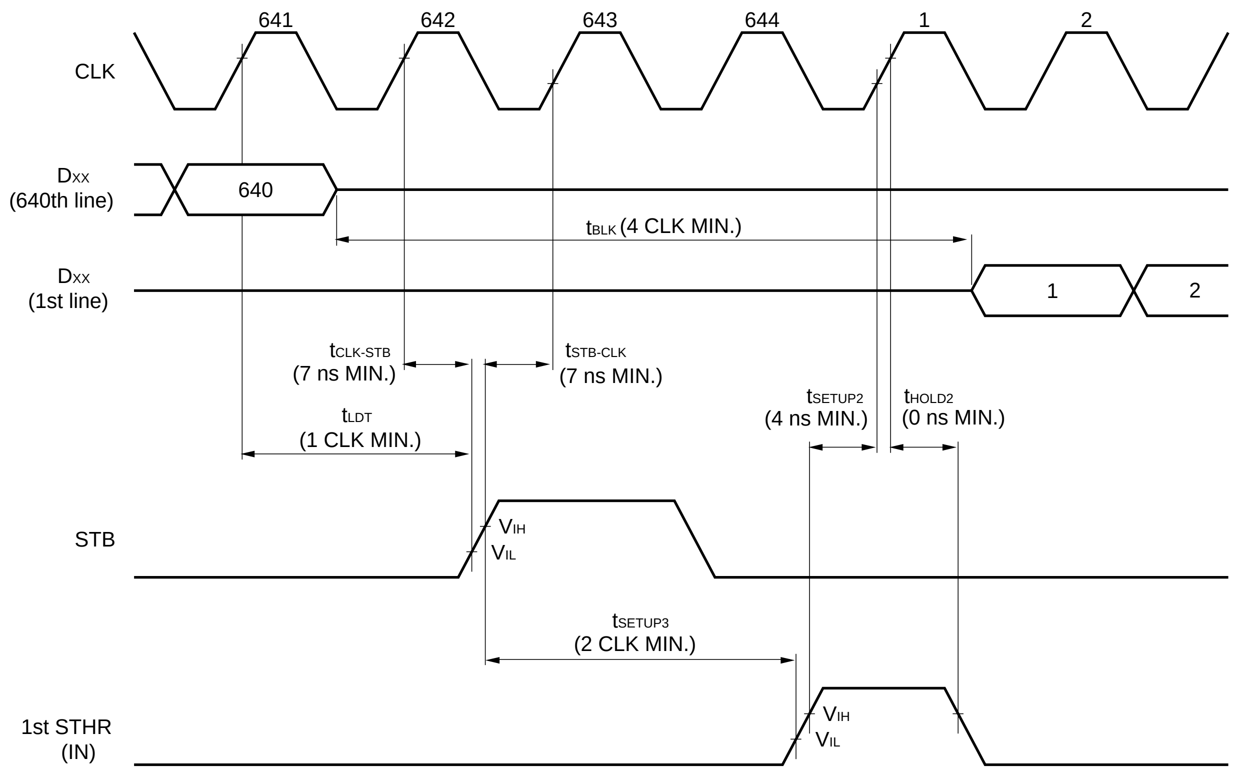
Unless otherwise specified, the input level is defined to V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.



Switching Characteristic Waveform (2/2)

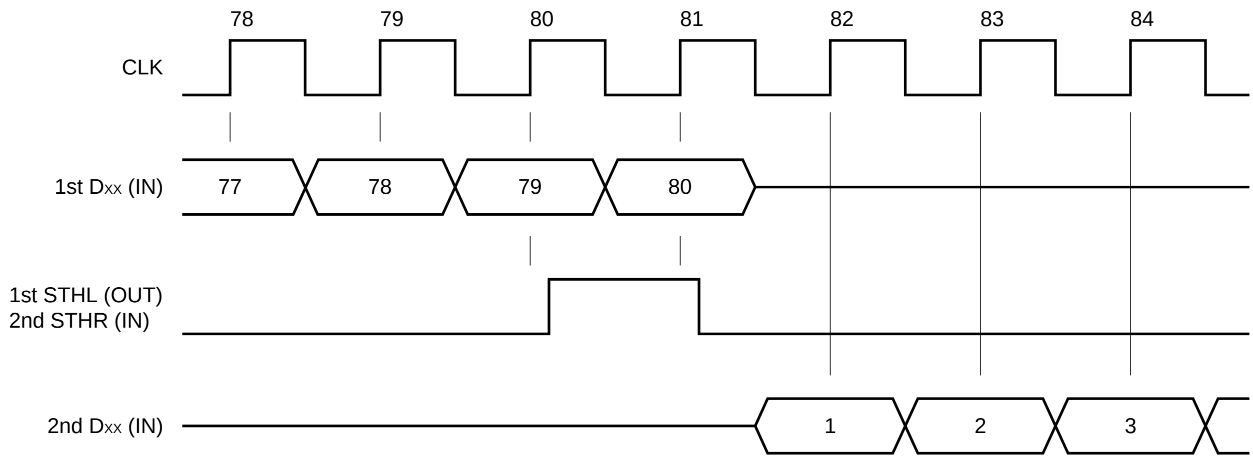


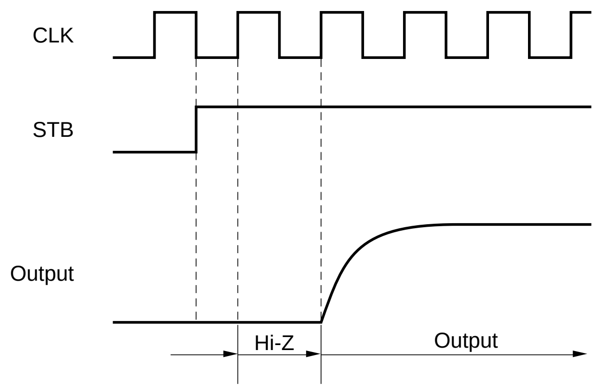
Relation between STB/STHR, STHL and blanking period



Remark t_{LDT}: For strobe data, it must delay over 1 clock and input from the clock edge of the last data.
t_{SETUP}: Delay two or more clocks of start pulse inputs of the following line from the rising edge of a strobe signal.
t_{BLK}: It is necessary for blanking period of display data over four or more clocks.

Data input timing in cascade connection





★ 8. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD16641.

For more details, refer to the

[Semiconductor Device Mount Manual] (http://www.necel.com/pkg/en/mount/index.html)

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16641N-xxx: TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 sec, pressure 100g (per solder).
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C, pressure 3 to 8 kg/cm^2, time 3 to 5 sec. Real bonding 165 to 180°C pressure 25 to 45 kg/cm^2, time 30 to 40 sec. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

NOTES FOR CMOS DEVICES

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ **POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ **INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)