To our customers,

Old Company Name in Catalogs and Other Documents

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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD16638A

300/309-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

The μPD16638A is a source driver for TFT-LCDs capable of supporting displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 3 dots (1 pixel), which can realize a full-color display of 260,000 colors by the output of 64 values that have been γ-corrected by an internal D/A converter and 2 sets of 9 external power supplies. Because the output dynamic range is as large as 8.3 V_{p-p}, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, in order to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a non-chip 6-bit D/A converter circuit whose odd output pins and even output pins output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 40 MHz when driving at 3.0 V, this driver is applicable to SVGA and XGA-standard TFT-LCD panels.

FEATURES

- CMOS level input
- Output number selectable (300/309)
- Input of 6 bits (gradation data) by 3 dots
- Capable of outputting 64 values by means of 2 sets of 9 external power supplies (18 units) and a D/A converter
- Output dynamic range 8.3 V_{p-p} MIN. (@ V_{DD2} = 8.5 V)
- High-speed data transfer: $f_{MAX.}$ = 40 MHz (internal data transfer speed when operating at 3.0 V)
- Applicable for dot-line inversion, n-line inversion and column line inversion
- Single bank arrangement is possible (loaded with slim or bending TCP)

ORDERING INFORMATION

Part Number	Package
μPD16638AN-×××	TCP (TAB package)

Remark The TCP's external shape is customized. To order your TCP's external shape, please contact a NEC salesperson.

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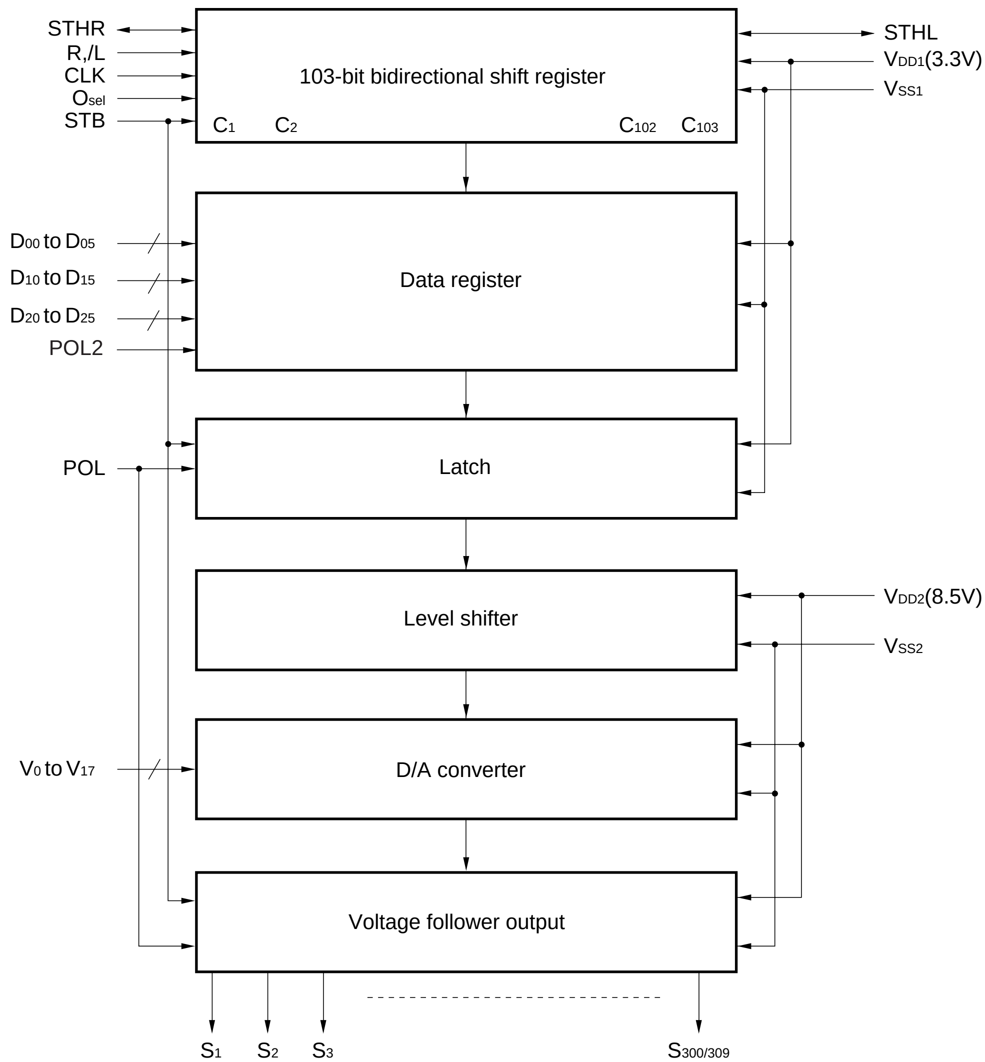
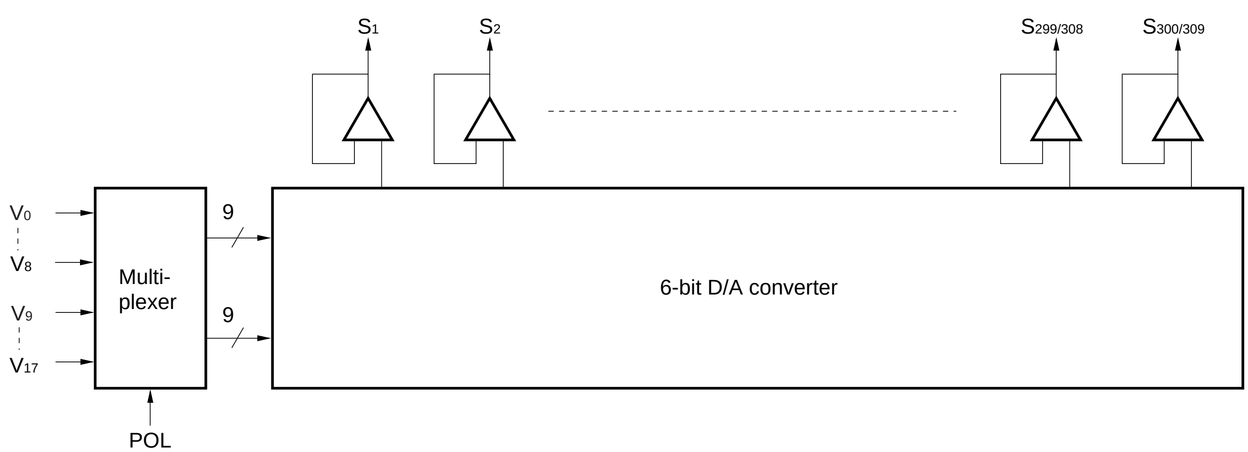
Printed in Japan

The mark ★ shows major revised points.

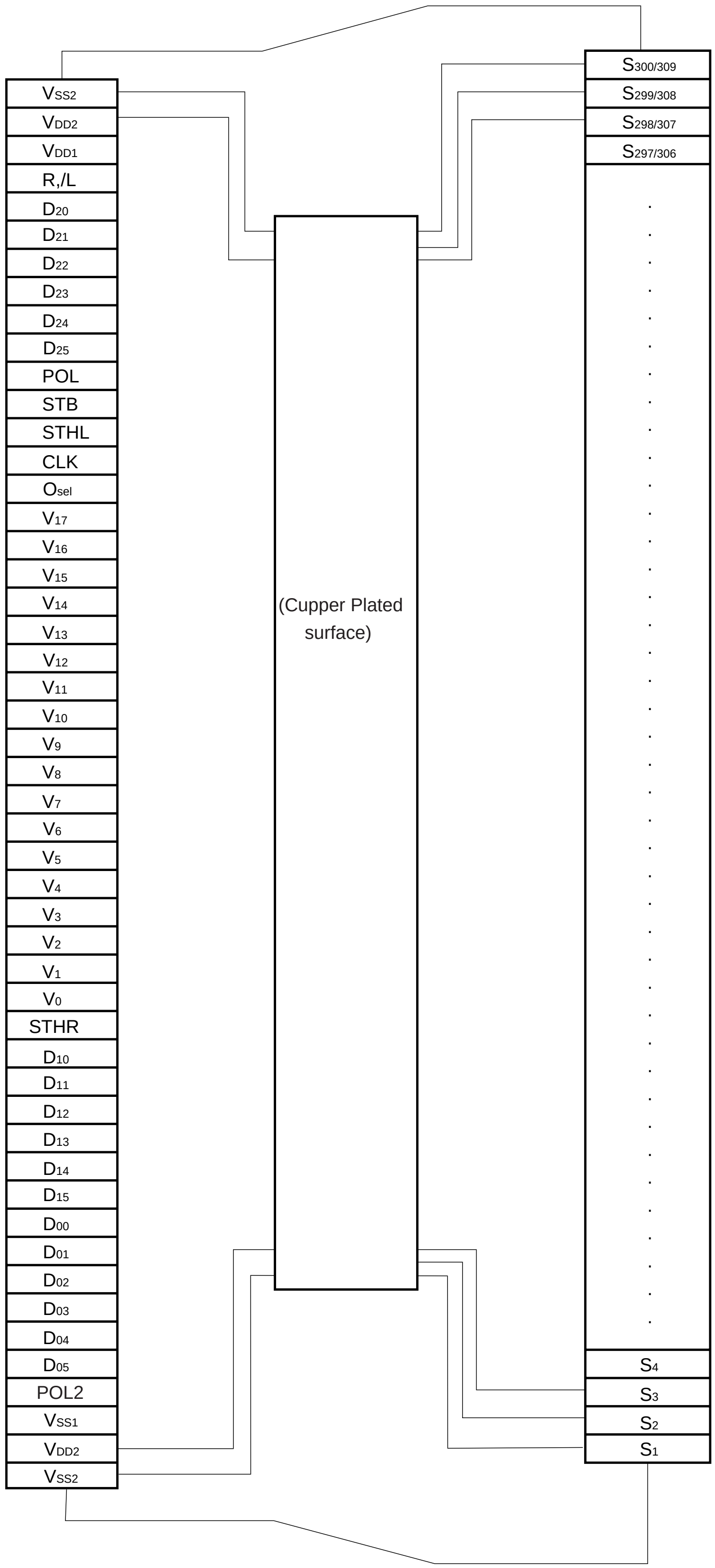
★ BLOCK DIAGRAM



★ RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



PIN CONFIGURATION (μPD16638AN-×××)



Remark This figure does not specify the TCP package. LPC terminal is pulled up to the V_{DD1} in the chip.

1. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S_1 to $S_{300/309}$	Driver output	The D/A converted 64-gray-scale analog voltage is output.
D_{00} to D_{05} D_{10} to D_{15} D_{20} to D_{25}	Display data input	The display data is input with a width of 18 bits, viz., the gray scale data (6 bits) by 3 dots (1 pixels). D_{X0}: LSB, D_{X5}: MSB
R,/L	Shift direction control input	These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows. R,/L = H : STHR input, $S_1 \rightarrow S_{300/309}$, STHL output R,/L = L : STHL input, $S_{300/309} \rightarrow S_1$, STHR output
STHR	Right shift start pulse input/output	R,/L = H : Becomes the start pulse input pin. R,/L = L : Becomes the start pulse output pin.
STHL	Left shift start pulse input/output	R,/L = H : Becomes the start pulse output pin. R,/L = L : Becomes the start pulse input pin.
O_{sel}	Number of output pins select pin	This pin selects the number of output pins. O_{sel} = H: 300-output mode O_{sel} = L: 309-output mode
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. O_{sel} = H: At the rising edge of the 100th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. O_{sel} = L: At the rising edge of the 103rd clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver.
STB	Latch input	The contents of the data register are transferred to the latch circuit at the rising edge, and at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	POL = H: The S_{2n-1} output uses V_0 to V_8 as the reference supply. The S_{2n} output uses V_9 to V_{17} as the reference supply. POL = L : The S_{2n-1} output uses V_0 to V_8 as the reference supply. The S_{2n} output uses V_0 to V_8 as the reference supply. S_{2n-1} indicates the odd output: and S_{2n} indicates the even output. Input of the POL signal is allowed the setup time($t_{POL\text{-}STB}$) with respect to STB's rising edge.
POL2	Data inversion	POL2 = H : Display data is inverted. POL2 = L : Display data is not inverted.
V_0 to V_{17}	γ-corrected power supplies	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 >$ $V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{16} > V_{17} > V_{SS2}$
V_{DD1}	Test pin Logic power supply	3.3 V ±0.3 V
V_{DD2}	Driver power supply	8.0 V to 9.0 V
V_{SS1}	Logic ground	Grounding
V_{SS2}	Driver ground	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_{17} in that order. Reverse this sequence to shut down. (Simultaneous power application to V_{DD2} and V_0 to V_{17} is possible.)

2. To stabilize the supply voltage, be sure to insert a 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals (V_0, V_1, V_2, ⋯, V_{17}) and V_{SS2}.

★ 2. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches.

Figure 2–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γ-corrected voltages V_0 to V_{17}, and the input data. Be sure to maintain the voltage relationships of

$V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_{COM} > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{16} > V_{17} > V_{SS2}$.

Figures 2–2 and 2–3 show the relationship between the input data and the output data. This driver IC is designed for only single-sided mounting. Therefore, do not use it for γ-corrected power supply level inversion in double-sided mounting. Because the current flowing through ladder resistors r_0 to r_{62} is small, its use for double-sided mounting impairs the IC's stable operation when the level of the γ-corrected power supply terminal is inverted thus causing display failures. Input γ-corrected power supply voltage by using an operational amplifier to maintain driver output accuracy.

Figure 2–1. Relationship between Input Data and Output Voltage

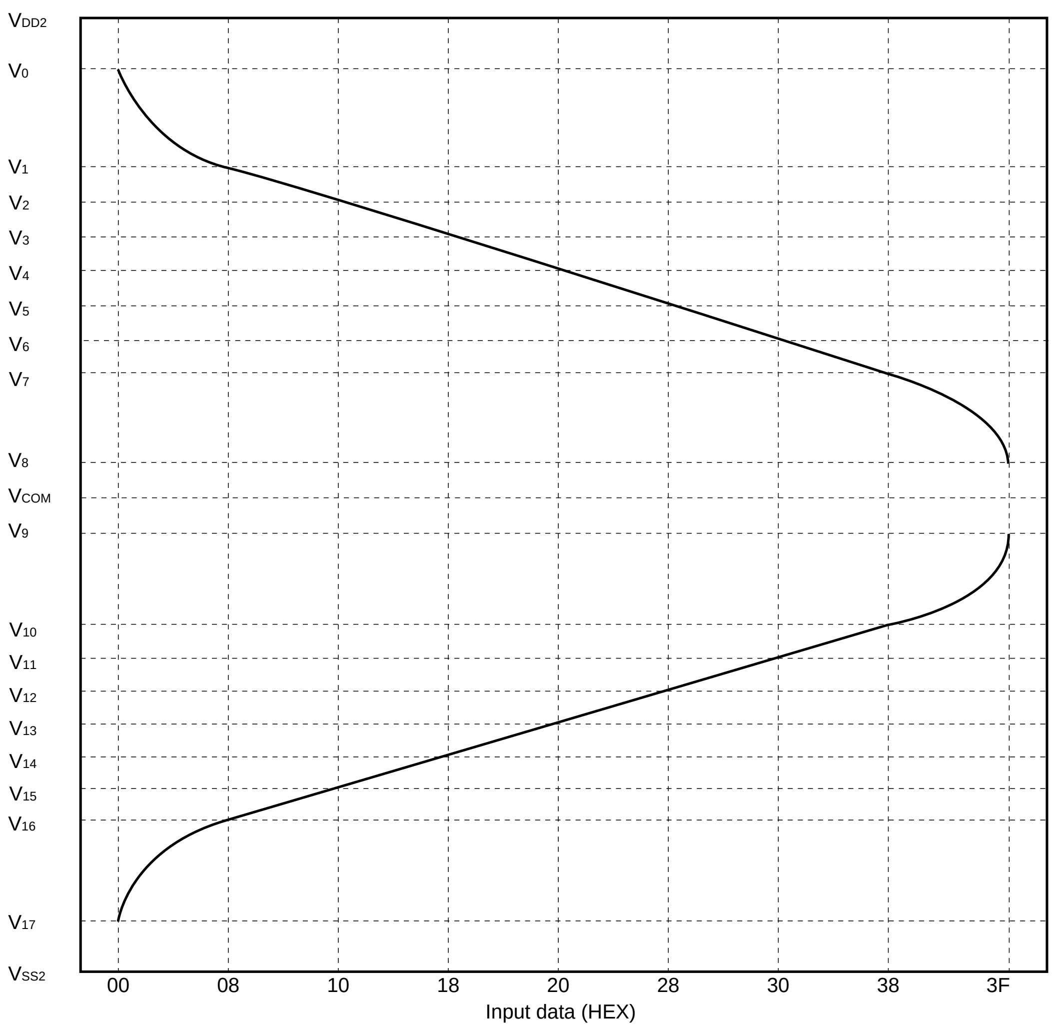
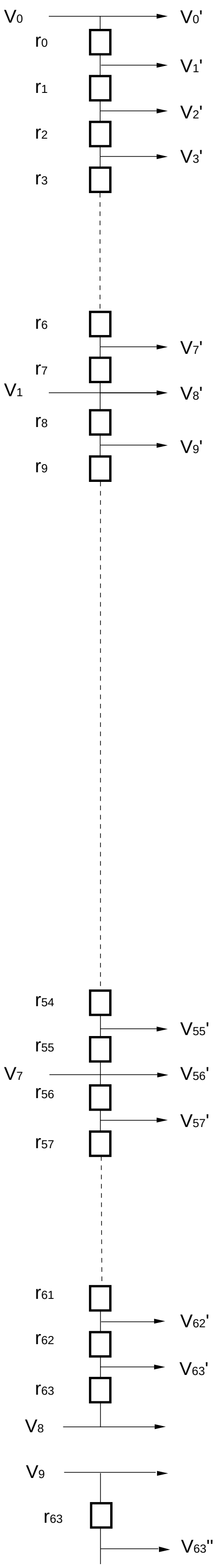


Figure 2–2. Relationship between Input Data and Output Voltage(1/2)

$V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8$



Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage	
00_H	0	0	0	0	0	0	V_0'	V_0
01_H	0	0	0	0	0	1	V_1'	$V_1+(V_0-V_1)\times3500/4000$
02_H	0	0	0	0	1	0	V_2'	$V_1+(V_0-V_1)\times3000/4000$
03_H	0	0	0	0	1	1	V_3'	$V_1+(V_0-V_1)\times2500/4000$
04_H	0	0	0	1	0	0	V_4'	$V_1+(V_0-V_1)\times2000/4000$
05_H	0	0	0	1	0	1	V_5'	$V_1+(V_0-V_1)\times1500/4000$
06_H	0	0	0	1	1	0	V_6'	$V_1+(V_0-V_1)\times1000/4000$
07_H	0	0	0	1	1	1	V_7'	$V_1+(V_0-V_1)\times500/4000$
08_H	0	0	1	0	0	0	V_8'	V_1
09_H	0	0	1	0	0	1	V_9'	$V_2+(V_1-V_2)\times1750/2000$
$0A_H$	0	0	1	0	1	0	V_{10}'	$V_2+(V_1-V_2)\times1500/2000$
$0B_H$	0	0	1	0	1	1	V_{11}'	$V_2+(V_1-V_2)\times1250/2000$
$0C_H$	0	0	1	1	0	0	V_{12}'	$V_2+(V_1-V_2)\times1000/2000$
$0D_H$	0	0	1	1	0	1	V_{13}'	$V_2+(V_1-V_2)\times750/2000$
$0E_H$	0	0	1	1	1	0	V_{14}'	$V_2+(V_1-V_2)\times500/2000$
$0F_H$	0	0	1	1	1	1	V_{15}'	$V_2+(V_1-V_2)\times250/2000$
10_H	0	1	0	0	0	0	V_{16}'	V_2
11_H	0	1	0	0	0	1	V_{17}'	$V_3+(V_2-V_3)\times1750/2000$
12_H	0	1	0	0	1	0	V_{18}'	$V_3+(V_2-V_3)\times1500/2000$
13_H	0	1	0	0	1	1	V_{19}'	$V_3+(V_2-V_3)\times1250/2000$
14_H	0	1	0	1	0	0	V_{20}'	$V_3+(V_2-V_3)\times1000/2000$
15_H	0	1	0	1	0	1	V_{21}'	$V_3+(V_2-V_3)\times750/2000$
16_H	0	1	0	1	1	0	V_{22}'	$V_3+(V_2-V_3)\times500/2000$
17_H	0	1	0	1	1	1	V_{23}'	$V_3+(V_2-V_3)\times250/2000$
18_H	0	1	1	0	0	0	V_{24}'	V_3
19_H	0	1	1	0	0	1	V_{25}'	$V_4+(V_3-V_4)\times1750/2000$
$1A_H$	0	1	1	0	1	0	V_{26}'	$V_4+(V_3-V_4)\times1500/2000$
$1B_H$	0	1	1	0	1	1	V_{27}'	$V_4+(V_3-V_4)\times1250/2000$
$1C_H$	0	1	1	1	0	0	V_{28}'	$V_4+(V_3-V_4)\times1000/2000$
$1D_H$	0	1	1	1	0	1	V_{29}'	$V_4+(V_3-V_4)\times750/2000$
$1E_H$	0	1	1	1	1	0	V_{30}'	$V_4+(V_3-V_4)\times500/2000$
$1F_H$	0	1	1	1	1	1	V_{31}'	$V_4+(V_3-V_4)\times250/2000$
20_H	1	0	0	0	0	0	V_{32}'	V_4
21_H	1	0	0	0	0	1	V_{33}'	$V_5+(V_4-V_5)\times1750/2000$
22_H	1	0	0	0	1	0	V_{34}'	$V_5+(V_4-V_5)\times1500/2000$
23_H	1	0	0	0	1	1	V_{35}'	$V_5+(V_4-V_5)\times1250/2000$
24_H	1	0	0	1	0	0	V_{36}'	$V_5+(V_4-V_5)\times1000/2000$
25_H	1	0	0	1	0	1	V_{37}'	$V_5+(V_4-V_5)\times750/2000$
26_H	1	0	0	1	1	0	V_{38}'	$V_5+(V_4-V_5)\times500/2000$
27_H	1	0	0	1	1	1	V_{39}'	$V_5+(V_4-V_5)\times250/2000$
28_H	1	0	1	0	0	0	V_{40}'	V_5
29_H	1	0	1	0	0	1	V_{41}'	$V_6+(V_5-V_6)\times1750/2000$
$2A_H$	1	0	1	0	1	0	V_{42}'	$V_6+(V_5-V_6)\times1500/2000$
$2B_H$	1	0	1	0	1	1	V_{43}'	$V_6+(V_5-V_6)\times1250/2000$
$2C_H$	1	0	1	1	0	0	V_{44}'	$V_6+(V_5-V_6)\times1000/2000$
$2D_H$	1	0	1	1	0	1	V_{45}'	$V_6+(V_5-V_6)\times750/2000$
$2E_H$	1	0	1	1	1	0	V_{46}'	$V_6+(V_5-V_6)\times500/2000$
$2F_H$	1	0	1	1	1	1	V_{47}'	$V_6+(V_5-V_6)\times250/2000$
30_H	1	1	0	0	0	0	V_{48}'	V_6
31_H	1	1	0	0	0	1	V_{49}'	$V_7+(V_6-V_7)\times1750/2000$
32_H	1	1	0	0	1	0	V_{50}'	$V_7+(V_6-V_7)\times1500/2000$
33_H	1	1	0	0	1	1	V_{51}'	$V_7+(V_6-V_7)\times1250/2000$
34_H	1	1	0	1	0	0	V_{52}'	$V_7+(V_6-V_7)\times1000/2000$
35_H	1	1	0	1	0	1	V_{53}'	$V_7+(V_6-V_7)\times750/2000$
36_H	1	1	0	1	1	0	V_{54}'	$V_7+(V_6-V_7)\times500/2000$
37_H	1	1	0	1	1	1	V_{55}'	$V_7+(V_6-V_7)\times250/2000$
38_H	1	1	1	0	0	0	V_{56}'	V_7
39_H	1	1	1	0	0	1	V_{57}'	$V_8+(V_7-V_8)\times3500/4000$
$3A_H$	1	1	1	0	1	0	V_{58}'	$V_8+(V_7-V_8)\times3000/4000$
$3B_H$	1	1	1	0	1	1	V_{59}'	$V_8+(V_7-V_8)\times2500/4000$
$3C_H$	1	1	1	1	0	0	V_{60}'	$V_8+(V_7-V_8)\times2000/4000$
$3D_H$	1	1	1	1	0	1	V_{61}'	$V_8+(V_7-V_8)\times1500/4000$
$3E_H$	1	1	1	1	1	0	V_{62}'	$V_8+(V_7-V_8)\times1000/4000$
$3F_H$	1	1	1	1	1	1	V_{63}'	$V_8+(V_7-V_8)\times500/4000$

	(Ω)
r_0	500
r_1	500
r_2	500
r_3	500
r_4	500
r_5	500
r_6	500
r_7	500
r_8	250
r_9	250
r_{10}	250
r_{11}	250
r_{12}	250
r_{13}	250
r_{14}	250
r_{15}	250
r_{16}	250
r_{17}	250
r_{18}	250
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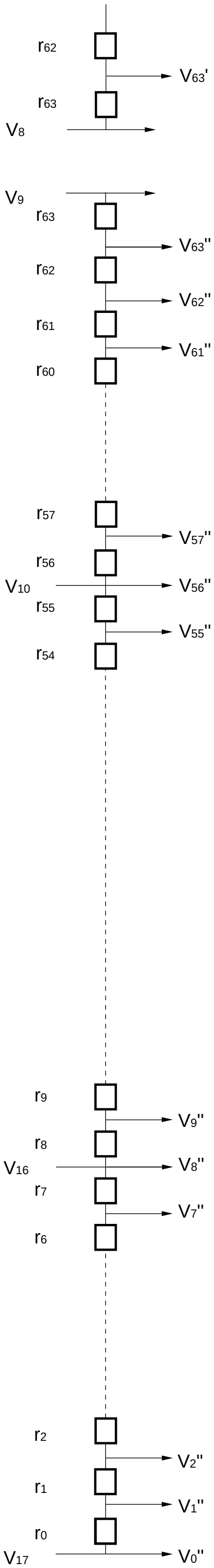
r_{51}	250
r_{52}	250
r_{53}	250
r_{54}	250
r_{55}	250
r_{56}	500
r_{57}	500
r_{58}	500
r_{59}	500
r_{60}	500
r_{61}	500
r_{62}	500
r_{63}	500
r_{total}	20000

Caution There is no connection V_8 and V_9 in the chip.

Figure 2–3. Relationship between Input Data and Output Voltage(2/2)

$V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{16} > V_{17} > V_{SS2}$



Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage	
3F$_H$	1	1	1	1	1	1	V_{63}''	$V_{10}+(V_9-V_{10})\times 3500/4000$
3E$_H$	1	1	1	1	1	0	V_{62}''	$V_{10}+(V_9-V_{10})\times 3000/4000$
3D$_H$	1	1	1	1	0	1	V_{61}''	$V_{10}+(V_9-V_{10})\times 2500/4000$
3C$_H$	1	1	1	1	0	0	V_{60}''	$V_{10}+(V_9-V_{10})\times 2000/4000$
3B$_H$	1	1	1	0	1	1	V_{59}''	$V_{10}+(V_9-V_{10})\times 1500/4000$
3A$_H$	1	1	1	0	1	0	V_{58}''	$V_{10}+(V_9-V_{10})\times 1000/4000$
39$_H$	1	1	1	0	0	1	V_{57}''	$V_{10}+(V_9-V_{10})\times 500/4000$
38$_H$	1	1	1	0	0	0	V_{56}''	V_{10}
37$_H$	1	1	0	1	1	1	V_{55}''	$V_{11}+(V_{10}-V_{11})\times 1750/2000$
36$_H$	1	1	0	1	1	0	V_{54}''	$V_{11}+(V_{10}-V_{11})\times 1500/2000$
35$_H$	1	1	0	1	0	1	V_{53}''	$V_{11}+(V_{10}-V_{11})\times 1250/2000$
34$_H$	1	1	0	1	0	0	V_{52}''	$V_{11}+(V_{10}-V_{11})\times 1000/2000$
33$_H$	1	1	0	0	1	1	V_{51}''	$V_{11}+(V_{10}-V_{11})\times 750/2000$
32$_H$	1	1	0	0	1	0	V_{50}''	$V_{11}+(V_{10}-V_{11})\times 500/2000$
31$_H$	1	1	0	0	0	1	V_{49}''	$V_{11}+(V_{10}-V_{11})\times 250/2000$
30$_H$	1	1	0	0	0	0	V_{48}''	V_{11}
2F$_H$	1	0	1	1	1	1	V_{47}''	$V_{12}+(V_{11}-V_{12})\times 1750/2000$
2E$_H$	1	0	1	1	1	0	V_{46}''	$V_{12}+(V_{11}-V_{12})\times 1500/2000$
2D$_H$	1	0	1	1	0	1	V_{45}''	$V_{12}+(V_{11}-V_{12})\times 1250/2000$
2C$_H$	1	0	1	1	0	0	V_{44}''	$V_{12}+(V_{11}-V_{12})\times 1000/2000$
2B$_H$	1	0	1	0	1	1	V_{43}''	$V_{12}+(V_{11}-V_{12})\times 750/2000$
2A$_H$	1	0	1	0	1	0	V_{42}''	$V_{12}+(V_{11}-V_{12})\times 500/2000$
29$_H$	1	0	1	0	0	1	V_{41}''	$V_{12}+(V_{11}-V_{12})\times 250/2000$
28$_H$	1	0	1	0	0	0	V_{40}''	V_{12}
27$_H$	1	0	0	1	1	1	V_{39}''	$V_{13}+(V_{12}-V_{13})\times 1750/2000$
26$_H$	1	0	0	1	1	0	V_{38}''	$V_{13}+(V_{12}-V_{13})\times 1500/2000$
25$_H$	1	0	0	1	0	1	V_{37}''	$V_{13}+(V_{12}-V_{13})\times 1250/2000$
24$_H$	1	0	0	1	0	0	V_{36}''	$V_{13}+(V_{12}-V_{13})\times 1000/2000$
23$_H$	1	0	0	0	1	1	V_{35}''	$V_{13}+(V_{12}-V_{13})\times 750/2000$
22$_H$	1	0	0	0	1	0	V_{34}''	$V_{13}+(V_{12}-V_{13})\times 500/2000$
21$_H$	1	0	0	0	0	1	V_{33}''	$V_{13}+(V_{12}-V_{13})\times 250/2000$
20$_H$	1	0	0	0	0	0	V_{32}''	V_{13}
1F$_H$	0	1	1	1	1	1	V_{31}''	$V_{14}+(V_{13}-V_{14})\times 1750/2000$
1E$_H$	0	1	1	1	1	0	V_{30}''	$V_{14}+(V_{13}-V_{14})\times 1500/2000$
1D$_H$	0	1	1	1	0	1	V_{29}''	$V_{14}+(V_{13}-V_{14})\times 1250/2000$
1C$_H$	0	1	1	1	0	0	V_{28}''	$V_{14}+(V_{13}-V_{14})\times 1000/2000$
1B$_H$	0	1	1	0	1	1	V_{27}''	$V_{14}+(V_{13}-V_{14})\times 750/2000$
1A$_H$	0	1	1	0	1	0	V_{26}''	$V_{14}+(V_{13}-V_{14})\times 500/2000$
19$_H$	0	1	1	0	0	1	V_{25}''	$V_{14}+(V_{13}-V_{14})\times 250/2000$
18$_H$	0	1	1	0	0	0	V_{24}''	V_{14}
17$_H$	0	1	0	1	1	1	V_{23}''	$V_{15}+(V_{14}-V_{15})\times 1750/2000$
16$_H$	0	1	0	1	1	0	V_{22}''	$V_{15}+(V_{14}-V_{15})\times 1500/2000$
15$_H$	0	1	0	1	0	1	V_{21}''	$V_{15}+(V_{14}-V_{15})\times 1250/2000$
14$_H$	0	1	0	1	0	0	V_{20}''	$V_{15}+(V_{14}-V_{15})\times 1000/2000$
13$_H$	0	1	0	0	1	1	V_{19}''	$V_{15}+(V_{14}-V_{15})\times 750/2000$
12$_H$	0	1	0	0	1	0	V_{18}''	$V_{15}+(V_{14}-V_{15})\times 500/2000$
11$_H$	0	1	0	0	0	1	V_{17}''	$V_{15}+(V_{14}-V_{15})\times 250/2000$
10$_H$	0	1	0	0	0	0	V_{16}''	V_{15}
0F$_H$	0	0	1	1	1	1	V_{15}''	$V_{16}+(V_{15}-V_{16})\times 1750/2000$
0E$_H$	0	0	1	1	1	0	V_{14}''	$V_{16}+(V_{15}-V_{16})\times 1500/2000$
0D$_H$	0	0	1	1	0	1	V_{13}''	$V_{16}+(V_{15}-V_{16})\times 1250/2000$
0C$_H$	0	0	1	1	0	0	V_{12}''	$V_{16}+(V_{15}-V_{16})\times 1000/2000$
0B$_H$	0	0	1	0	1	1	V_{11}''	$V_{16}+(V_{15}-V_{16})\times 750/2000$
0A$_H$	0	0	1	0	1	0	V_{10}''	$V_{16}+(V_{15}-V_{16})\times 500/2000$
09$_H$	0	0	1	0	0	1	V_9''	$V_{16}+(V_{15}-V_{16})\times 250/2000$
08$_H$	0	0	1	0	0	0	V_8''	V_{16}
07$_H$	0	0	0	1	1	1	V_7''	$V_{17}+(V_{16}-V_{17})\times 3500/4000$
06$_H$	0	0	0	1	1	0	V_6''	$V_{17}+(V_{16}-V_{17})\times 3000/4000$
05$_H$	0	0	0	1	0	1	V_5''	$V_{17}+(V_{16}-V_{17})\times 2500/4000$
04$_H$	0	0	0	1	0	0	V_4''	$V_{17}+(V_{16}-V_{17})\times 2000/4000$
03$_H$	0	0	0	0	1	1	V_3''	$V_{17}+(V_{16}-V_{17})\times 1500/4000$
02$_H$	0	0	0	0	1	0	V_2''	$V_{17}+(V_{16}-V_{17})\times 1000/4000$
01$_H$	0	0	0	0	0	1	V_1''	$V_{17}+(V_{16}-V_{17})\times 500/4000$
00$_H$	0	0	0	0	0	0	V_0''	V_{17}

	(Ω)
r_{63}	500
r_{62}	500
r_{61}	500
r_{60}	500
r_{59}	500
r_{58}	500
r_{57}	500
r_{56}	500
r_{55}	250
r_{54}	250
r_{53}	250
r_{52}	250
r_{51}	250
r_{50}	250
r_{49}	250
r_{48}	250
r_{47}	250
r_{46}	250
r_{45}	250
r_{44}	250
r_{43}	250
r_{42}	250
r_{41}	250
r_{40}	250
r_{39}	250
r_{38}	250
r_{37}	250
r_{36}	250
r_{35}	250
r_{34}	250
r_{33}	250
r_{32}	250
r_{31}	250
r_{30}	250
r_{29}	250
r_{28}	250
r_{27}	250
r_{26}	250
r_{25}	250
r_{24}	250
r_{23}	250
r_{22}	250
r_{21}	250
r_{20}	250
r_{19}	250
r_{18}	250
r_{17}	250
r_{16}	250
r_{15}	250
r_{14}	250
r_{13}	250
r_{12}	250
r_{11}	250
r_{10}	250
r_9	250
r_8	250
r_7	500
r_6	500
r_5	500
r_4	500
r_3	500
r_2	500
r_1	500
r_0	500
r_{total}	20000

Caution There is no connection V_8 and V_9 in the chip.

3. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 6 bits × 1 RGBs (3 dots)
Input width : 18 bits (1-pixel data)

R,/L = H (Right shift)

Output	S_1	S_2	S_3	S_4	···	$S_{299/308}$	$S_{300/309}$
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{00} to D_{05}	···	D_{10} to D_{15}	D_{20} to D_{25}

R,/L = L (Left shift)

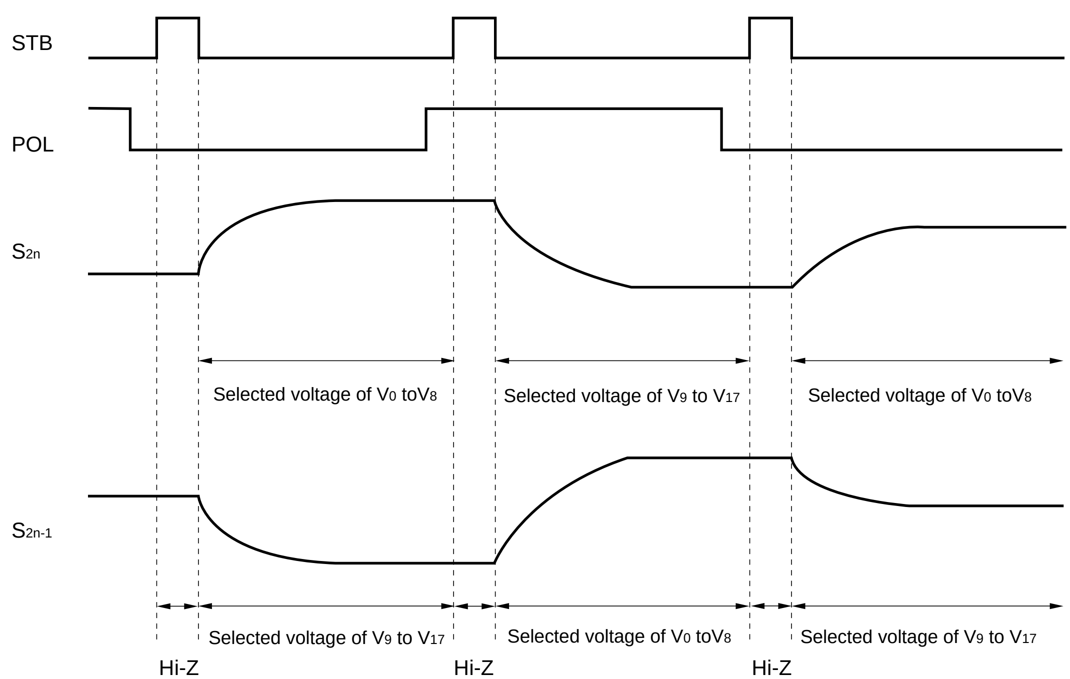
Output	S_1	S_2	S_3	S_4	···	$S_{299/308}$	$S_{300/309}$
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{00} to D_{05}	···	D_{10} to D_{15}	D_{20} to D_{25}

POL	S_{2n-1} Note	S_{2n} Note
H	V_0 to V_8	V_9 to V_{17}
L	V_9 to V_{17}	V_0 to V_8

Note S_{2n-1} (Odd output), S_{2n} (Even output) n = 1, 2, ·····, 155(Except S310)

4. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



5. ELECTRICAL SPECIFICATIONS

★ **Absolute Maximum Ratings (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)**

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +5.0	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +10.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} +0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} +0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} +0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} +0.5	V
Operating Ambient Temperature Range	T_A	–10 to +75	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range (T_A = –10 to +75 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}	3.0	3.3	3.6	V
Driver Part Supply Voltage	V_{DD2}	8.0	8.5	9.0	V
High-Level Input Voltage	V_{IH}	0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}	0		0.3 V_{DD1}	V
γ-Corrected Voltage	V_0 to V_{17}	V_{SS2}		V_{DD2}	V
Driver System Output Voltage	V_O	V_{SS2} + 0.1		V_{DD2} – 0.1	V
Maximum Clock Frequency	$f_{MAX.}$	40			MHz

★ Electrical Specifications (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 8.5 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input Leak Current	I_L					±1.0	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = 0 mA		V_{DD1} – 0.1			V
Low-Level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = 0 mA				0.1	V
γ-Corrected Supply Current	I_γ	V_0 to V_8 = V_9 to V_{17} = 4.0V	V_0 pin, V_9 pin	100	200	400	μA
			V_8 pin, V_{17} pin	–400	–200	–100	μA
Driver Output Current	V_{VOH}	V_X = 7.0 V, V_{OUT} = 6.5 V Note				–30	μA
	V_{VOL}	V_X = 1.0 V, V_{OUT} = 1.5 V Note		30			μA
Output Voltage Deviation	ΔV_O	V_{OUT} = 2.0 V, 4.25 V, 6.5 V			±10	±20	mV
Output swing difference deviation	ΔV_{P-P}				±5		mV
Output Voltage Range	V_O			0.1		V_{DD2} – 0.1	V
Logic System Dynamic Current Consumption	I_{DD1}	V_{DD1}, with no load			2.0	3.5	mA
Driver System Dynamic Current Consumption	I_{DD2}	V_{DD2}, with no load			2.5	6.0	mA

Note V_X refers to the output voltage of analog output pins S_1 to $S_{300/309}$.
V_{OUT} refers to the voltage applied to analog output pins S_1 to $S_{300/309}$.

Cautions 1. The STB cycle is defined to be 20 μs at f_{CLK} = 40 MHz.

2. The TYP. values refer to an all-black or all-white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

3. Refers to the current consumption per driver when cascades are connected assuming XGA single-sided mounting (10 units).

★ Switching Characteristics (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 8.5 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V)

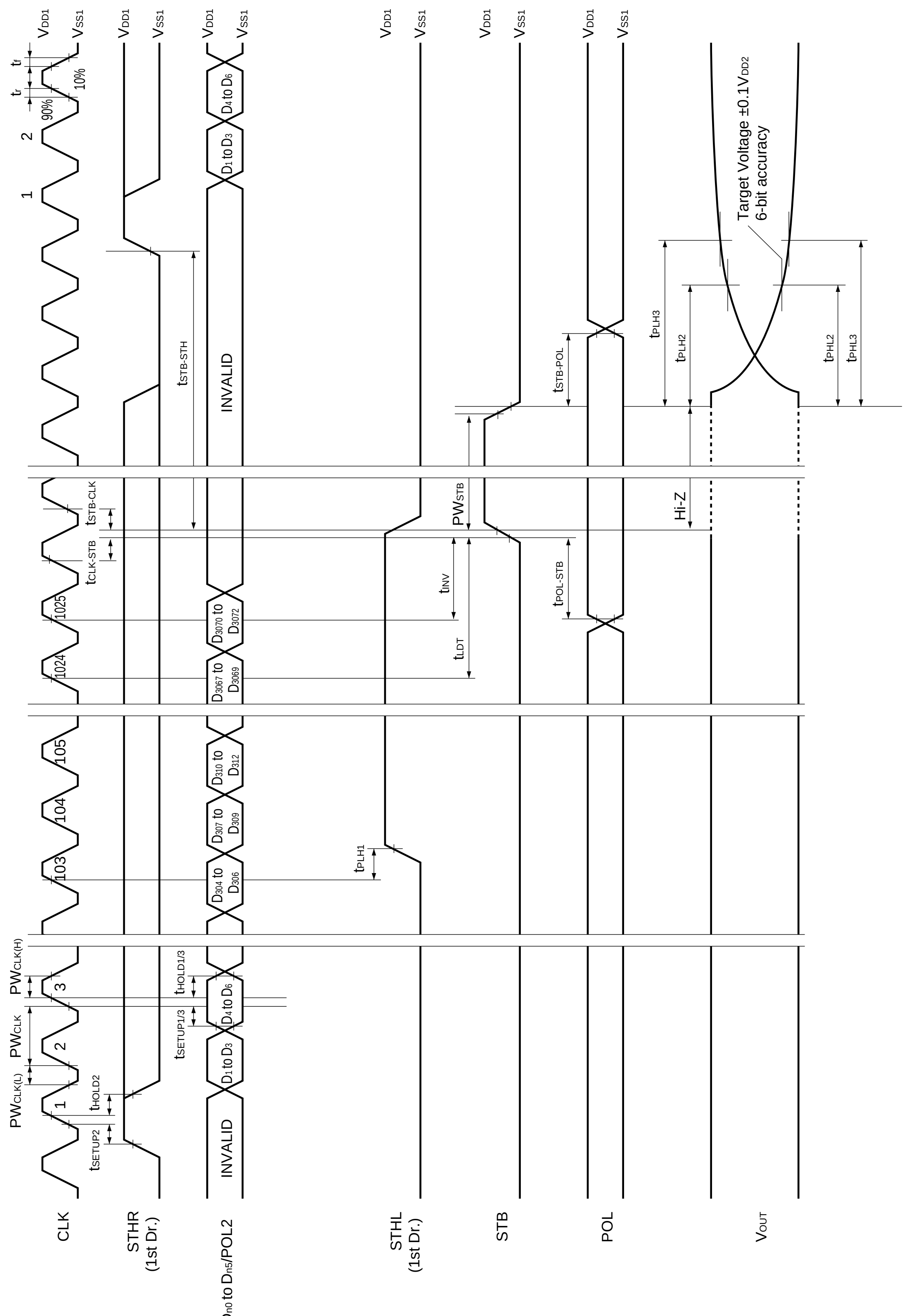
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 10 pF		10	20	ns
Driver Output Delay Time 1	t_{PLH2}	C_L = 31.5 pF × 2, R_L = 4.5 kΩ		4	7	μs
	t_{PLH3}			7	10	μs
	t_{PHL2}			4	7	μs
	t_{PHL3}			7	10	μs
Input Capacitance	C_{I1}	STHR (STHL) excluded, T_A = 25°C		5	10	pF
	C_{I2}	STHR (STHL), T_A = 25°C		5	10	pF

★ **Timing Requirements (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ±0.3 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 8.0 ns)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		25			ns
Clock Pulse High Period	$PW_{CLK(H)}$		6			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		6			ns
Data Setup Time	t_{SETUP1}		3			ns
Data Hold Time	t_{HOLD1}		3			ns
Start Pulse Setup Time	t_{SETUP2}		5			ns
Start Pulse Hold Time	t_{HOLD2}		1			ns
POL2 Setup Time	t_{SETUP3}		3			ns
POL2 Hold Time	t_{HOLD3}		3			ns
Start Pulse Low Period	t_{SPL}		6			ns
STB Pulse Width	PW_{STB}		2			CLK
					4	μs
Data Invalid Period	t_{INV}		1			CLK
Last Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	CLK ↑ → STB ↑	6			ns
STB-CLK Time	$t_{STB-CLK}$	STB ↑ → CLK ↑	6			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	STB ↓ → STHR(STHL) ↑	1			CLK
POL-STB Time	$t_{POL-STB}$	POL ↑ or ↓ → STB ↑	–5			ns
STB-POL Time	$t_{STB-POL}$	STB ↓ → POL ↓ or ↑	6			ns

★ 6. SWITCHING CHARACTERISTICS WAVEFORM (R,/L = H)

(Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.)



7. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met when soldering the μPD16638A.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices when other soldering processes are used, or when the soldering is done under different conditions.

μPD16638AN-××× : TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350 °C: heating for 2 to 3 seconds: pressure 100 g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100 °C: pressure 3 to 8 kg/cm^2 : time 3 to 5 secs. Real bonding 165 to 180 °C: pressure 25 to 45 kg/cm^2 : time 30 to 40 secs. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution For detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability / Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)