To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD16637

384 OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64 GRAY SCALES)

The μPD16637 is a source driver for TFT-LCDs capable of dealing with displays with 64 gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as 12.3 V_{P-P}, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 55 MHz when driving at 3.0 V, this driver is applicable to XGA-standard TFT-LCD panels.

FEATURES

- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter
- Output dynamic range 12.3 V_{P-P} min. (@ V_{DD2} = 12.5 V)
- Power supply voltage of driver part = V_{DD2} = 13.0 ±0.5 V
- CMOS level input
- Input of 6 bits (gradation data) by 6 dots
- High-speed data transfer: $f_{max.}$ = 55 MHz (internal data transfer speed when operating at 3.0 V)
- Display data inversion function (POL2 terminal.)
- 384 outputs
- Single bank arrangement is possible (loaded with slim TCP)

ORDERING INFORMATION

Part Number	Package
μPD16637N-×××	TCP (TAB package)

The TCP's external shape is customized. To order your TCP's external shape, please contact an NEC salesperson.

Document No. S12578EJ1V0DS00 (1st edition)
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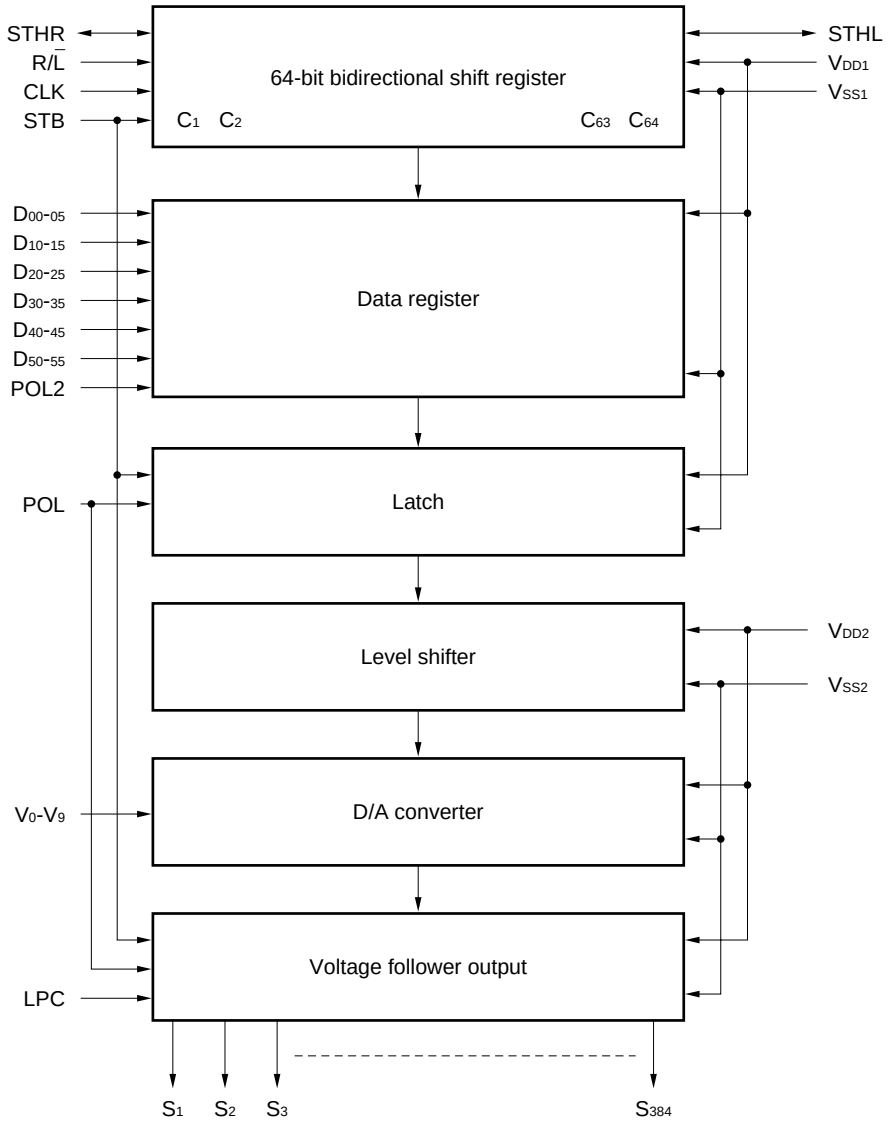
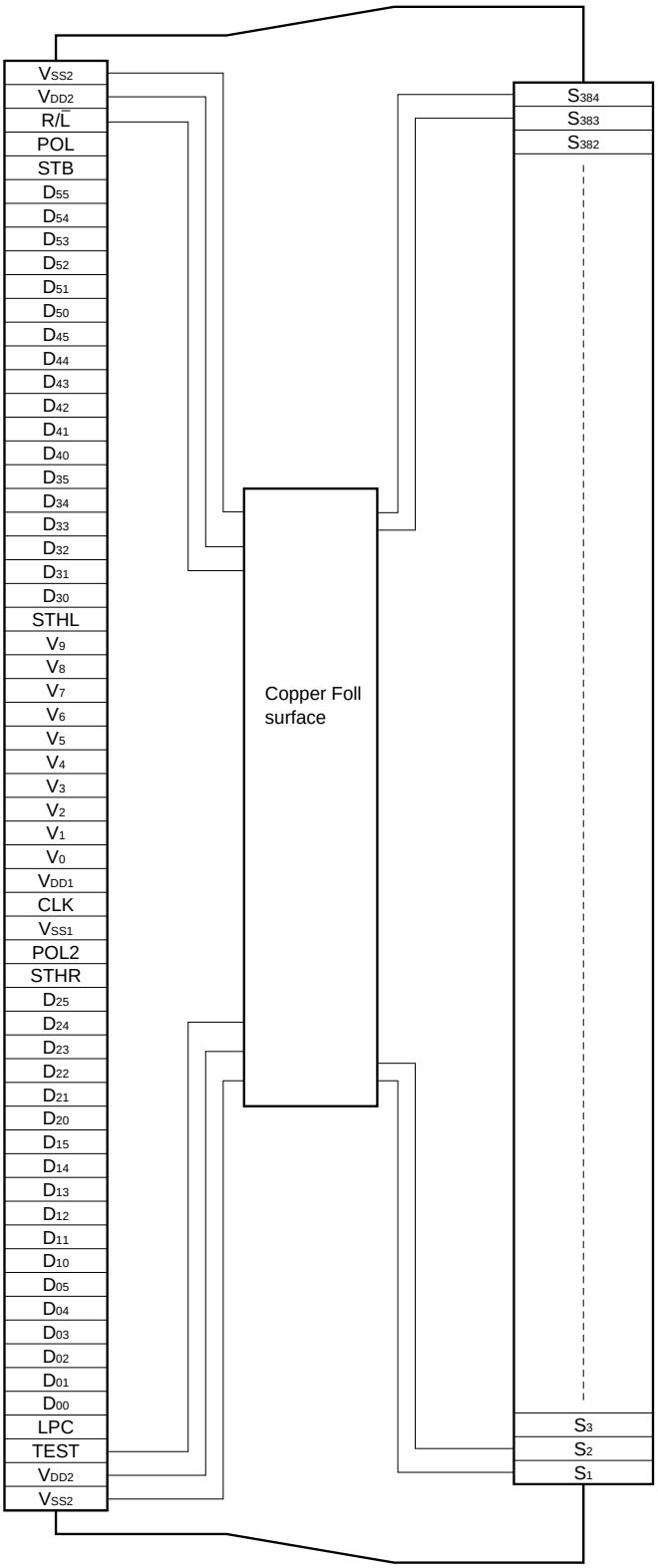
1. BLOCK DIAGRAM

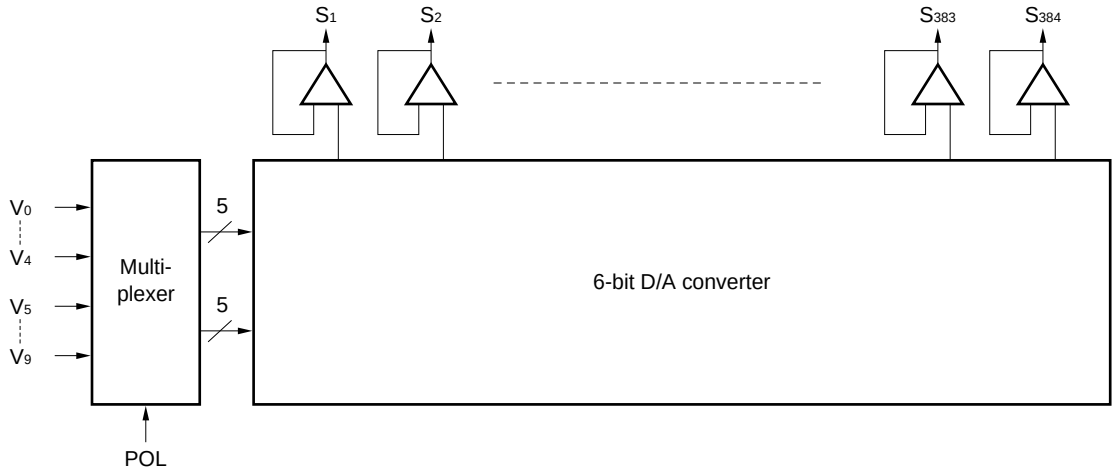


2. PIN CONFIGURATION (μPD16637N-×××)



Remark This figure does not specify the TCP package.
It is possible to reduce a number of input lead by wiring POL2 terminal to V_{SS2} on TCP if data inversion function is not necessary.

3. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



POL	S_{2n-1}	S_{2n}
L	V_0 to V_4	V_5 to V_9
H	V_5 to V_9	V_0 to V_4

S_{2n-1} (odd output), S_{2n} (even output) n =1, 2, ·····, 192

4. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S_1 to S_{384}	Driver output	The D/A converted 64-gray-scale analog voltage is output.
D_{01} to D_{05}	Display data input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D_{X0}: LSB, D_{X5}: MSB
D_{10} to D_{15}		
D_{20} to D_{25}		
D_{31} to D_{35}		
D_{40} to D_{45}		
D_{50} to D_{55}		
$R/\overline{L}$	Shift direction switching input	These refer to the start pulse input/output pins when cascades are connected. The shift direction of the shift registers are as follows. $R/\overline{L}$ = H: STHR input, $S_1 \rightarrow S_{384}$, STHL output $R/\overline{L}$ = L : STHL input, $S_{384} \rightarrow S_1$, STHR output
STHR	Right shift start pulse input/output	$R/\overline{L}$ = H: Becomes the start pulse input pin. $R/\overline{L}$ = L : Becomes the start pulse output pin.
STHL	Left shift start pulse input/output	$R/\overline{L}$ = H: Becomes the start pulse input pin. $R/\overline{L}$ = L : Becomes the start pulse output pin.
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. The initial-level driver's 64th clock becomes valid as the next-level driver's start pulse is input. If 66 clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch input	The contents of the data register are transferred to the latch at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
LPC	Low power control input	The output buffer constant current source is blocked, reducing current consumption. In lower power mode (LPC = 'H': DC-level input possible), the ordinary static current consumption can be reduced by approx. 50 %. The condition that low power mode can be used is that the load constant is at least 5 kΩ + 100 pF.
POL	Polarity input	POL = L ; The S_{2n-1} output uses V_5 to V_9 as the reference supply; and the S_{2n} output uses V_0 to V_4 as the reference supply. POL = H; The S_{2n-1} output uses V_0 to V_4 as the reference supply; and the S_{2n} output uses V_5 to V_9 as the reference supply.
POL2	Data inversion	POL2 = H : Display data is inverted. POL2 = L : Display data is not inverted.
V_0 to V_9	γ-corrected power supplies	Input the γ-corrected power supplies from outside. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS}$
TEST	Test pin	Set it to 'OPEN'.
V_{DD1}	Logic power supply	3.3 V ±0.3 V
V_{DD2}	Driver power supply	13.0 V ±13.5 V
V_{SS1}	Logic ground	Grounding
V_{SS2}	Driver ground	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_9 in that order. Reverse this sequence to shut down. (Simultaneous power application to V_{DD2} and V_0 to V_9 is possible.)

2. To stabilize the supply voltage, please be sure to insert a 0.47 μF bypass capacitor between $-V_{DD1}$-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals (V_0, V_1, V_2, ⋯, V_9) and V_{SS2}.

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches. The ladder resistors r_0 to r_{62} are so designed that the ratios between the LCD panel's γ-corrected voltages and V_0' to V_{63}' and V_0" to V_{63}" are roughly equal; and their respective resistance values are as shown on page 9. Among the 5-by-2 γ-corrected voltages, input gray scale voltages of the same polarity with respect to the common voltage, for the respective five γ-corrected voltages of V_0 to V_4 and V_5 to V_9. If fine gray scale voltage precision is not necessary, the voltage follower circuit supplied to the γ-corrected power supplies V_1 to V_3 and V_6 to V_8 can be deleted.

Figure 1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γ-corrected voltages V_0 to V_9 and the input data. Be sure to maintain the voltage relationships of $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$. Figures 2-1 and 2-2 show the relationship between the input data and the output data. Table 1 shows the resistance values of the resistor strings.

This driver IC is designed for single-sided mounting. Therefore, please do not use it for γ-corrected power supply level inversion in double-sided mounting.

Because the current flowing through ladder resistors r_0 to r_{62} is small, its use for double-sided mounting impairs the IC's stable operation when the level of the γ-corrected power supply terminal is inverted thus causing display failures.

Figure 1. Relationship Between Input Data and Output Voltage

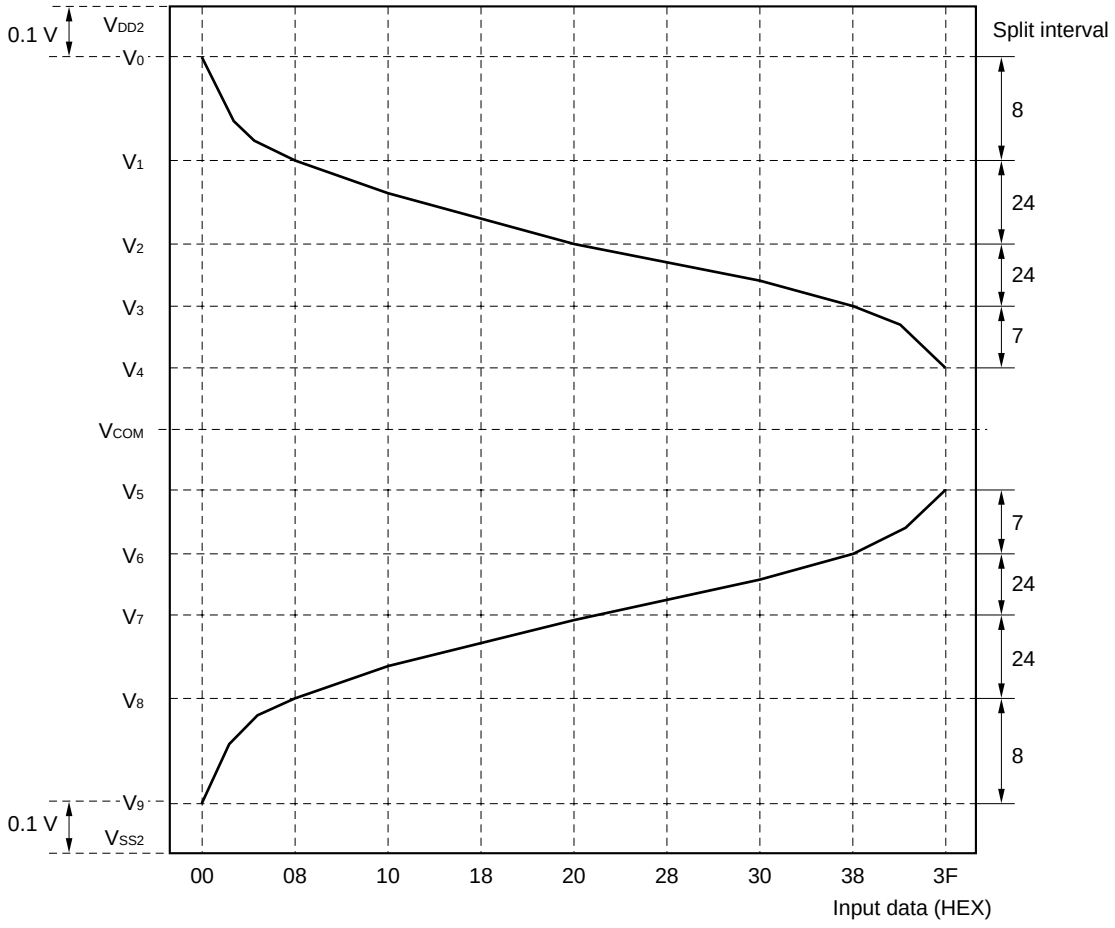
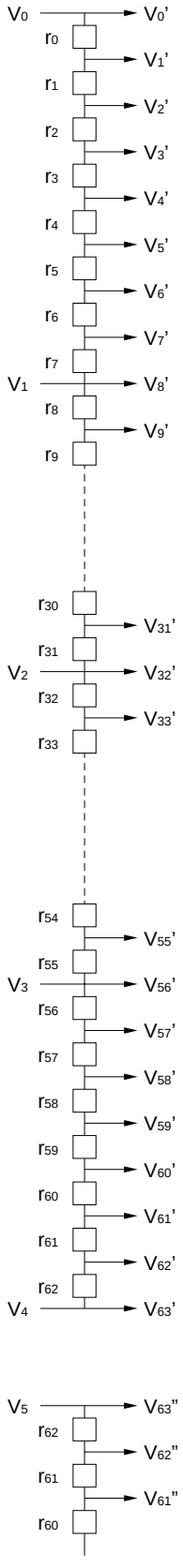
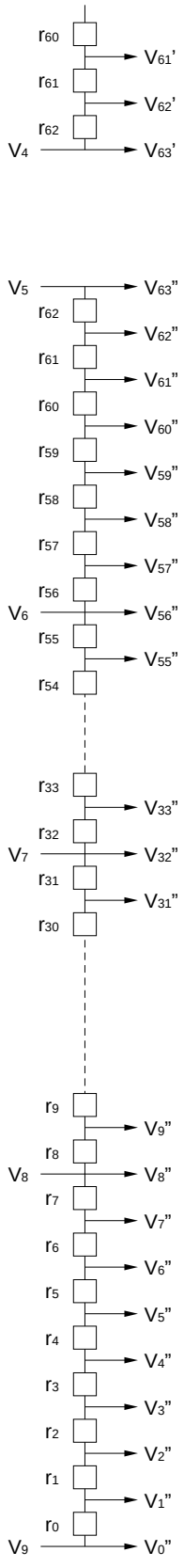


Figure 2-1. Relationship Between Input Data and Output Voltage: $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5$



Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage	
00_H	0	0	0	0	0	0	V_0'	V_0
01_H	0	0	0	0	0	1	V_1'	$V_1 + (V_0 - V_1) \times 4300/5100$
02_H	0	0	0	0	1	0	V_2'	$V_1 + (V_0 - V_1) \times 3550/5100$
03_H	0	0	0	0	1	1	V_3'	$V_1 + (V_0 - V_1) \times 2850/5100$
04_H	0	0	0	1	0	0	V_4'	$V_1 + (V_0 - V_1) \times 2200/5100$
05_H	0	0	0	1	0	1	V_5'	$V_1 + (V_0 - V_1) \times 1600/5100$
06_H	0	0	0	1	1	0	V_6'	$V_1 + (V_0 - V_1) \times 1050/5100$
07_H	0	0	0	1	1	1	V_7'	$V_1 + (V_0 - V_1) \times 500/5100$
08_H	0	0	1	0	0	0	V_8'	V_0
09_H	0	0	1	0	0	1	V_9'	$V_1 + (V_0 - V_1) \times 5200/5700$
$0A_H$	0	0	1	0	1	0	V_{10}'	$V_1 + (V_0 - V_1) \times 4800/5700$
$0B_H$	0	0	1	0	1	1	V_{11}'	$V_1 + (V_0 - V_1) \times 4400/5700$
$0C_H$	0	0	1	1	0	0	V_{12}'	$V_1 + (V_0 - V_1) \times 4050/5700$
$0D_H$	0	0	1	1	0	1	V_{13}'	$V_1 + (V_0 - V_1) \times 3700/5700$
$0E_H$	0	0	1	1	1	0	V_{14}'	$V_1 + (V_0 - V_1) \times 3350/5700$
$0F_H$	0	0	1	1	1	1	V_{15}'	$V_1 + (V_0 - V_1) \times 3050/5700$
10_H	0	1	0	0	0	0	V_{16}'	$V_1 + (V_0 - V_1) \times 2750/5700$
11_H	0	1	0	0	0	1	V_{17}'	$V_1 + (V_0 - V_1) \times 2450/5700$
12_H	0	1	0	0	1	0	V_{18}'	$V_1 + (V_0 - V_1) \times 2200/5700$
13_H	0	1	0	0	1	1	V_{19}'	$V_1 + (V_0 - V_1) \times 1950/5700$
14_H	0	1	0	1	0	0	V_{20}'	$V_1 + (V_0 - V_1) \times 1700/5700$
15_H	0	1	0	1	0	1	V_{21}'	$V_1 + (V_0 - V_1) \times 1500/5700$
16_H	0	1	0	1	1	0	V_{22}'	$V_1 + (V_0 - V_1) \times 1300/5700$
17_H	0	1	0	1	1	1	V_{23}'	$V_1 + (V_0 - V_1) \times 1100/5700$
18_H	0	1	1	0	0	0	V_{24}'	$V_1 + (V_0 - V_1) \times 950/5700$
19_H	0	1	1	0	0	1	V_{25}'	$V_1 + (V_0 - V_1) \times 800/5700$
$1A_H$	0	1	1	0	1	0	V_{26}'	$V_1 + (V_0 - V_1) \times 650/5700$
$1B_H$	0	1	1	0	1	1	V_{27}'	$V_1 + (V_0 - V_1) \times 500/5700$
$1C_H$	0	1	1	1	0	0	V_{28}'	$V_1 + (V_0 - V_1) \times 400/5700$
$1D_H$	0	1	1	1	0	1	V_{29}'	$V_1 + (V_0 - V_1) \times 300/5700$
$1E_H$	0	1	1	1	1	0	V_{30}'	$V_1 + (V_0 - V_1) \times 200/5700$
$1F_H$	0	1	1	1	1	1	V_{31}'	$V_1 + (V_0 - V_1) \times 100/5700$
20_H	1	0	0	0	0	0	V_{32}'	V_2
21_H	1	0	0	0	0	1	V_{33}'	$V_3 + (V_2 - V_3) \times 2450/2550$
22_H	1	0	0	0	1	0	V_{34}'	$V_3 + (V_2 - V_3) \times 2350/2550$
23_H	1	0	0	0	1	1	V_{35}'	$V_3 + (V_2 - V_3) \times 2250/2550$
24_H	1	0	0	1	0	0	V_{36}'	$V_3 + (V_2 - V_3) \times 2150/2550$
25_H	1	0	0	1	0	1	V_{37}'	$V_3 + (V_2 - V_3) \times 2050/2550$
26_H	1	0	0	1	1	0	V_{38}'	$V_3 + (V_2 - V_3) \times 1950/2550$
27_H	1	0	0	1	1	1	V_{39}'	$V_3 + (V_2 - V_3) \times 1850/2550$
28_H	1	0	1	0	0	0	V_{40}'	$V_3 + (V_2 - V_3) \times 1750/2250$
29_H	1	0	1	0	0	1	V_{41}'	$V_3 + (V_2 - V_3) \times 1650/2250$
$2A_H$	1	0	1	0	1	0	V_{42}'	$V_3 + (V_2 - V_3) \times 1550/2250$
$2B_H$	1	0	1	0	1	1	V_{43}'	$V_3 + (V_2 - V_3) \times 1450/2250$
$2C_H$	1	0	1	1	0	0	V_{44}'	$V_3 + (V_2 - V_3) \times 1350/2250$
$2D_H$	1	0	1	1	0	1	V_{45}'	$V_3 + (V_2 - V_3) \times 1250/2250$
$2E_H$	1	0	1	1	1	0	V_{46}'	$V_3 + (V_2 - V_3) \times 1150/2250$
$2F_H$	1	0	1	1	1	1	V_{47}'	$V_3 + (V_2 - V_3) \times 1050/2250$
30_H	1	1	0	0	0	0	V_{48}'	$V_3 + (V_2 - V_3) \times 950/2250$
31_H	1	1	0	0	0	1	V_{49}'	$V_3 + (V_2 - V_3) \times 850/2250$
32_H	1	1	0	0	1	0	V_{50}'	$V_3 + (V_2 - V_3) \times 750/2250$
33_H	1	1	0	0	1	1	V_{51}'	$V_3 + (V_2 - V_3) \times 650/2250$
34_H	1	1	0	1	0	0	V_{52}'	$V_3 + (V_2 - V_3) \times 550/2250$
35_H	1	1	0	1	0	1	V_{53}'	$V_3 + (V_2 - V_3) \times 450/2250$
36_H	1	1	0	1	1	0	V_{54}'	$V_3 + (V_2 - V_3) \times 300/2250$
37_H	1	1	0	1	1	1	V_{55}'	$V_3 + (V_2 - V_3) \times 150/2250$
38_H	1	1	1	0	0	0	V_{56}'	V_3
39_H	1	1	1	0	0	1	V_{57}'	$V_4 + (V_3 - V_4) \times 2300/2500$
$3A_H$	1	1	1	0	1	0	V_{58}'	$V_4 + (V_3 - V_4) \times 2100/2500$
$3B_H$	1	1	1	0	1	1	V_{59}'	$V_4 + (V_3 - V_4) \times 1850/2500$
$3C_H$	1	1	1	1	0	0	V_{60}'	$V_4 + (V_3 - V_4) \times 1600/2500$
$3D_H$	1	1	1	1	0	1	V_{61}'	$V_4 + (V_3 - V_4) \times 1300/2500$
$3E_H$	1	1	1	1	1	0	V_{62}'	$V_4 + (V_3 - V_4) \times 800/2500$
$3F_H$	1	1	1	1	1	1	V_{63}'	V_4

Figure 2-2. Relationship Between Input Data and Output Voltage: $V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$



Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage	
$3F_H$	1	1	1	1	1	1	V_{63}"	V_5
$3E_H$	1	1	1	1	1	0	V_{62}"	$V_6 + (V_5 - V_6) \times 1700/2500$
$3D_H$	1	1	1	1	0	1	V_{61}"	$V_6 + (V_5 - V_6) \times 1200/2500$
$3C_H$	1	1	1	1	0	0	V_{60}"	$V_6 + (V_5 - V_6) \times 900/2500$
$3B_H$	1	1	1	0	1	1	V_{59}"	$V_6 + (V_5 - V_6) \times 650/2500$
$3A_H$	1	1	1	0	1	0	V_{58}"	$V_6 + (V_5 - V_6) \times 400/2500$
39_H	1	1	1	0	0	1	V_{57}"	$V_6 + (V_5 - V_6) \times 200/2500$
38_H	1	1	1	0	0	0	V_{56}"	V_6
37_H	1	1	0	1	1	1	V_{55}"	$V_7 + (V_6 - V_7) \times 2400/2550$
36_H	1	1	0	1	1	0	V_{54}"	$V_7 + (V_6 - V_7) \times 2250/2550$
35_H	1	1	0	1	0	1	V_{53}"	$V_7 + (V_6 - V_7) \times 2100/2550$
34_H	1	1	0	1	0	0	V_{52}"	$V_7 + (V_6 - V_7) \times 2000/2550$
33_H	1	1	0	0	1	1	V_{51}"	$V_7 + (V_6 - V_7) \times 1900/2550$
32_H	1	1	0	0	1	0	V_{50}"	$V_7 + (V_6 - V_7) \times 1800/2550$
31_H	1	1	0	0	0	1	V_{49}"	$V_7 + (V_6 - V_7) \times 1700/2550$
30_H	1	1	0	0	0	0	V_{48}"	$V_7 + (V_6 - V_7) \times 1600/2550$
$2F_H$	1	0	1	1	1	1	V_{47}"	$V_7 + (V_6 - V_7) \times 1500/2550$
$2E_H$	1	0	1	1	1	0	V_{46}"	$V_7 + (V_6 - V_7) \times 1400/2550$
$2D_H$	1	0	1	1	0	1	V_{45}"	$V_7 + (V_6 - V_7) \times 1300/2550$
$2C_H$	1	0	1	1	0	0	V_{44}"	$V_7 + (V_6 - V_7) \times 1200/2550$
$2B_H$	1	0	1	0	1	1	V_{43}"	$V_7 + (V_6 - V_7) \times 1100/2550$
$2A_H$	1	0	1	0	1	0	V_{42}"	$V_7 + (V_6 - V_7) \times 1000/2550$
29_H	1	0	1	0	0	1	V_{41}"	$V_7 + (V_6 - V_7) \times 900/2550$
28_H	1	0	1	0	0	0	V_{40}"	$V_7 + (V_6 - V_7) \times 800/2550$
27_H	1	0	0	1	1	1	V_{39}"	$V_7 + (V_6 - V_7) \times 700/2550$
26_H	1	0	0	1	1	0	V_{38}"	$V_7 + (V_6 - V_7) \times 600/2550$
25_H	1	0	0	1	0	1	V_{37}"	$V_7 + (V_6 - V_7) \times 500/2550$
24_H	1	0	0	1	0	0	V_{36}"	$V_7 + (V_6 - V_7) \times 400/2550$
23_H	1	0	0	0	1	1	V_{35}"	$V_7 + (V_6 - V_7) \times 300/2550$
22_H	1	0	0	0	1	0	V_{34}"	$V_7 + (V_6 - V_7) \times 200/2550$
21_H	1	0	0	0	0	1	V_{33}"	$V_7 + (V_6 - V_7) \times 100/2550$
20_H	1	0	0	0	0	0	V_{32}"	V_7
$1F_H$	0	1	1	1	1	1	V_{31}"	$V_8 + (V_7 - V_8) \times 5600/5700$
$1E_H$	0	1	1	1	1	0	V_{30}"	$V_8 + (V_7 - V_8) \times 5500/5700$
$1D_H$	0	1	1	1	0	1	V_{29}"	$V_8 + (V_7 - V_8) \times 5400/5700$
$1C_H$	0	1	1	1	0	0	V_{28}"	$V_8 + (V_7 - V_8) \times 5300/5700$
$1B_H$	0	1	1	0	1	1	V_{27}"	$V_8 + (V_7 - V_8) \times 5200/5700$
$1A_H$	0	1	1	0	1	0	V_{26}"	$V_8 + (V_7 - V_8) \times 5050/5700$
19_H	0	1	1	0	0	1	V_{25}"	$V_8 + (V_7 - V_8) \times 4900/5700$
18_H	0	1	1	0	0	0	V_{24}"	$V_8 + (V_7 - V_8) \times 4750/5700$
17_H	0	1	0	1	1	1	V_{23}"	$V_8 + (V_7 - V_8) \times 4600/5700$
16_H	0	1	0	1	1	0	V_{22}"	$V_8 + (V_7 - V_8) \times 4400/5700$
15_H	0	1	0	1	0	1	V_{21}"	$V_8 + (V_7 - V_8) \times 4200/5700$
14_H	0	1	0	1	0	0	V_{20}"	$V_8 + (V_7 - V_8) \times 4000/5700$
13_H	0	1	0	0	1	1	V_{19}"	$V_8 + (V_7 - V_8) \times 3750/5700$
12_H	0	1	0	0	1	0	V_{18}"	$V_8 + (V_7 - V_8) \times 3500/5700$
11_H	0	1	0	0	0	1	V_{17}"	$V_8 + (V_7 - V_8) \times 3250/5700$
10_H	0	1	0	0	0	0	V_{16}"	$V_8 + (V_7 - V_8) \times 2950/5700$
$0F_H$	0	0	1	1	1	1	V_{15}"	$V_8 + (V_7 - V_8) \times 2650/5700$
$0E_H$	0	0	1	1	1	0	V_{14}"	$V_8 + (V_7 - V_8) \times 2350/5700$
$0D_H$	0	0	1	1	0	1	V_{13}"	$V_8 + (V_7 - V_8) \times 2000/5700$
$0C_H$	0	0	1	1	0	0	V_{12}"	$V_8 + (V_7 - V_8) \times 2650/5700$
$0B_H$	0	0	1	0	1	1	V_{11}"	$V_8 + (V_7 - V_8) \times 1300/5700$
$0A_H$	0	0	1	0	1	0	V_{10}"	$V_8 + (V_7 - V_8) \times 900/5700$
09_H	0	0	1	0	0	1	V_9"	$V_8 + (V_7 - V_8) \times 500/5700$
08_H	0	0	1	0	0	0	V_8"	V_8
07_H	0	0	0	1	1	1	V_7"	$V_9 + (V_8 - V_9) \times 4600/5100$
06_H	0	0	0	1	1	0	V_6"	$V_9 + (V_8 - V_9) \times 4050/5100$
05_H	0	0	0	1	0	1	V_5"	$V_9 + (V_8 - V_9) \times 3500/5100$
04_H	0	0	0	1	0	0	V_4"	$V_9 + (V_8 - V_9) \times 2900/5100$
03_H	0	0	0	0	1	1	V_3"	$V_9 + (V_8 - V_9) \times 2250/5100$
02_H	0	0	0	0	1	0	V_2"	$V_9 + (V_8 - V_9) \times 1550/5100$
01_H	0	0	0	0	0	1	V_1"	$V_9 + (V_8 - V_9) \times 800/5100$
00_H	0	0	0	0	0	0	V_0"	V_9

Table 1. Resistance values of the resistor strings

	Resistor Name	Resistance Value (Ω)	Resistor Name	Resistance Value (Ω)	
V_0, V_9 →	r_0	800	r_{32}	100	← V_2, V_7
	r_1	750	r_{33}	100	
	r_2	700	r_{34}	100	
	r_3	650	r_{35}	100	
	r_4	600	r_{36}	100	
	r_5	550	r_{37}	100	
	r_6	550	r_{38}	100	
	r_7	500	r_{39}	100	
V_1, V_8 →	r_8	500	r_{40}	100	
	r_9	400	r_{41}	100	
	r_{10}	400	r_{42}	100	
	r_{11}	350	r_{43}	100	
	r_{12}	350	r_{44}	100	
	r_{13}	350	r_{45}	100	
	r_{14}	300	r_{46}	100	
	r_{15}	300	r_{47}	100	
	r_{16}	300	r_{48}	100	
	r_{17}	250	r_{49}	100	
	r_{18}	250	r_{50}	100	
	r_{19}	250	r_{51}	190	
	r_{20}	200	r_{52}	100	
	r_{21}	200	r_{53}	150	
	r_{22}	200	r_{54}	150	
	r_{23}	150	r_{55}	150	
	r_{24}	150	r_{56}	200	← V_3, V_6
	r_{25}	150	r_{57}	200	
	r_{26}	150	r_{58}	250	
	r_{27}	100	r_{59}	250	
	r_{28}	100	r_{60}	300	
	r_{29}	100	r_{61}	500	
	r_{30}	100	r_{62}	800	← V_4, V_5
V_2, V_7 →	r_{31}	100	Total	15850	

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 6 bits × 2 RGBs (6 dots)
Input width : 36 bits (2-pixel data)

$R/\overline{L}$ = H (Right shift)

Output	S_1	S_2	S_3	S_4	S_5	⋯	S_{383}	S_{384}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	D_{40} to D_{45}	⋯	D_{40} to D_{45}	D_{50} to D_{55}

$R/\overline{L}$ = L (Left shift)

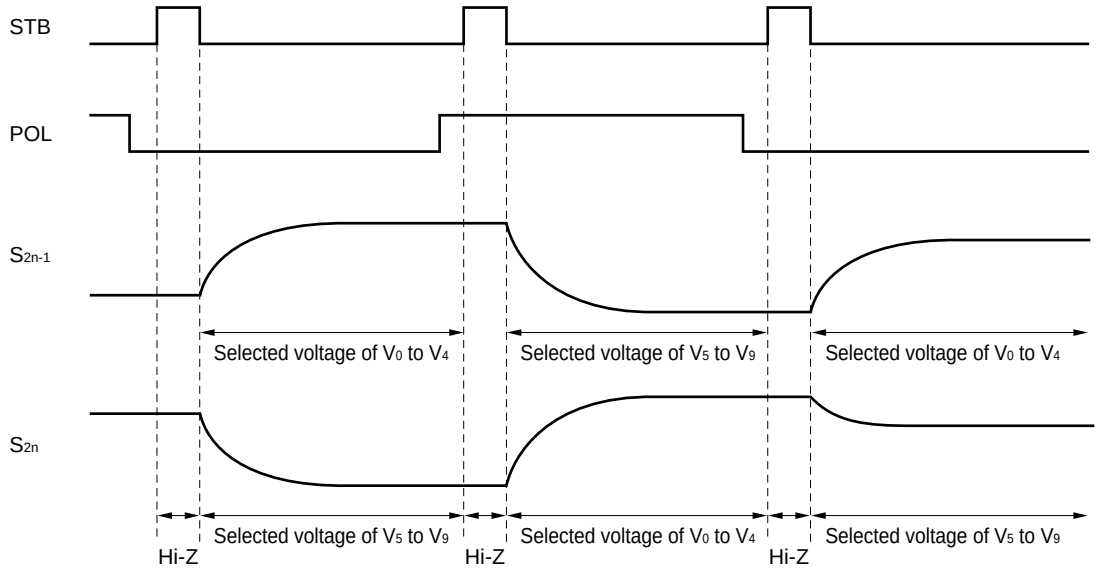
Output	S_1	S_2	S_3	S_4	S_5	⋯	S_{383}	S_{384}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	D_{40} to D_{45}	⋯	D_{40} to D_{45}	D_{50} to D_{55}

POL	S_{2n-1}	S_{2n}
L	V_0 to V_4	V_5 to V_9
H	V_5 to V_9	V_0 to V_4

S_{2n-1} (Odd output), S_{2n} (Even output) n = 1, 2, ·····, 192

7. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB rising edge.



8. CAUTION OF OPERATION

μPD16637 is full dot inversion driver with change charge buffer for discharge buffer on every other horizontal line. Since the output polarity of last line on a frame can not be same with the output polarity of first line on a next frame (Figure 3), necessary to polarity change and output operation in the interval of two frames (Figure 4).

Figure 3.

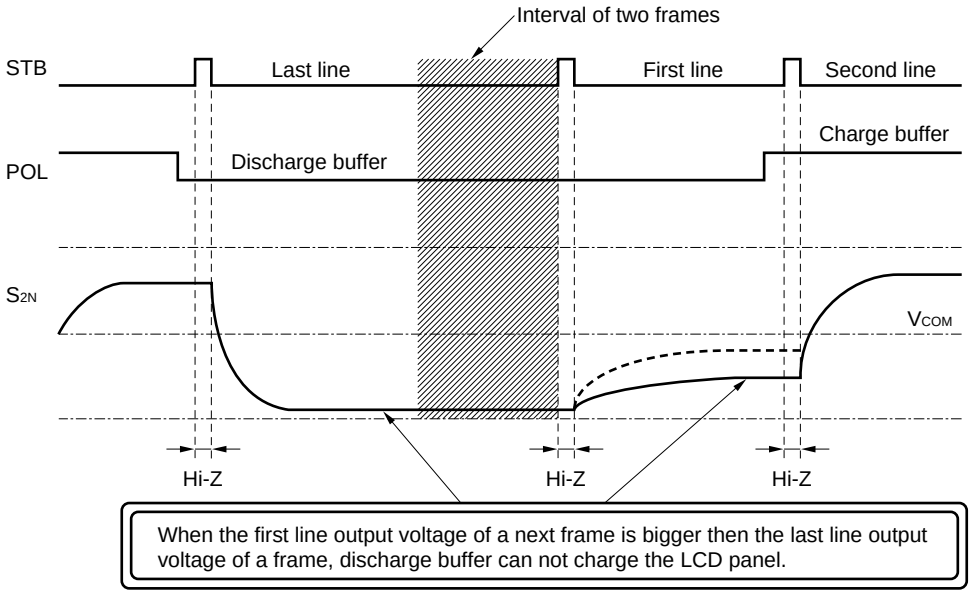
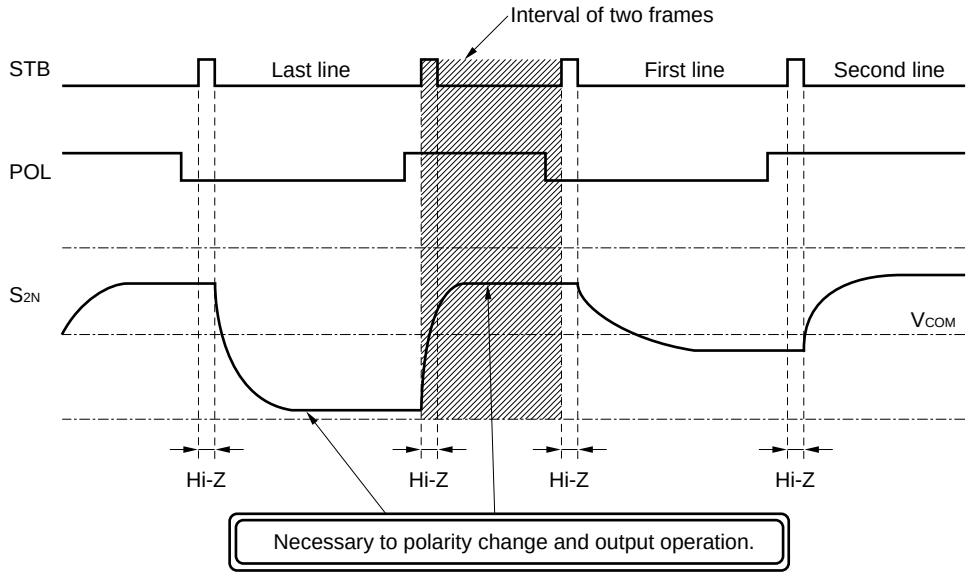


Figure 4.



9. ELECTRIC SPECIFICATION

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +6.5	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +15.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} +0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} +0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} +0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} +0.5	V
Operating Temperature Range	T_A	–10 to +75	°C
Storage Temperature Range	$T_{stg.}$	–55 to +125	°C

Recommended Operating Range (T_A = –10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}	3.0	3.3	3.6	V
Driver Part Supply Voltage	V_{DD2}	12.5	13.0	13.5	V
High-Level Input Voltage	V_{IH}	0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}	0		0.3 V_{DD1}	V
γ-Corrected Voltage	V_0 to V_9	V_{SS2} + 0.1		V_{DD2} – 0.1	V
Driver Part Output Voltage	V_O	V_{SS2} + 0.1		V_{DD2} – 0.1	V
Maximum Clock Frequency	$f_{max.}$	55			MHz

Electrical Specifications (T_A = –10 to +75°C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 13.0 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input Leak Current	I_L					±1.0	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), I_O = 0 mA		V_{DD1} – 0.1			V
Low-Level Output Voltage	V_{OL}	STHR (STHL), I_O = 0 mA				0.1	V
γ-Corrected Supply Current	I_{Vn}	V_{DD2} = 13.0 V	V_0, V_5		0.4	0.8	mA
		V_0 – V_4 = V_5 – V_9 = 6 V	V_4, V_9		–0.4	–0.8	mA
Driver Output Current	V_{VOH}	V_X = 10 V, V_{OUT} = 1 V[Note]				–3.0	mA
	V_{VOL}	V_X = 1 V, V_{OUT} = 10 V[Note]		3.0			mA

Note V_X refers to the output voltage of analog output pins S_1 to S_{384}.
V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{384}.

Electrical Specifications (T_A = –10 to +75°C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 13.0 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output Voltage Deviation[Note 1]	ΔV_O	Input data: 00_H to $3F_H$		±8	±20	mV
Average Output Voltage Variation[Note 2]	ΔV_{AV}	Input data: 00_H to $3F_H$		±11		mV
Output Voltage Range	V_O	Input data: 00_H to $3F_H$	0.1		V_{DD2} – 0.1	V
Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1}; when with no load[Notes 3, 4]		3.3	9.0	mA
Driver Part Dynamic Current Consumption	I_{DD22}	V_{DD2}; when with no load[Notes 3, 4]		14.9	30.0	mA

Notes 1. The output voltage deviation refers to the voltage difference between adjoining output pins when the display data is the same (within the chip).

2. The average output voltage variation refers to the average output voltage difference between chips. The average output voltage refers to the average voltage between chips when the display data is the same.

3. The STB cycle is defined to be 16.6 μs at f_{CLK} = 40 MHz.
The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

4. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).

Switching Characteristics (T_A = –10 to +75°C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 13.0 V ±0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 25 pF		9.7	12	ns
Driver Output Delay Time 1	t_{PHL2}	C_L = 200 pF, R_L = 5 kΩ		2.0	8	μs
Driver Output Delay Time 2	t_{PHL3}	C_L = 200 pF, R_L = 5 kΩ		2.8	12	μs
Driver Output Delay Time 3	t_{PLH2}	C_L = 200 pF, R_L = 5 kΩ		2.1	8	μs
Driver Output Delay Time 4	t_{PLH3}	C_L = 200 pF, R_L = 5 kΩ		2.7	12	μs
Input Capacitance 1	C_1	STHR, STHL excluded T_A = 25°C		9.8	15	pF
Input Capacitance 2	C_2	STHR, STHL T_A = 25°C		8.5	15	pF

Timing Requirement

(T_A = –10 to +75°C, V_{DD1} = 3.3 V ±0.3 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 8.0 ns)

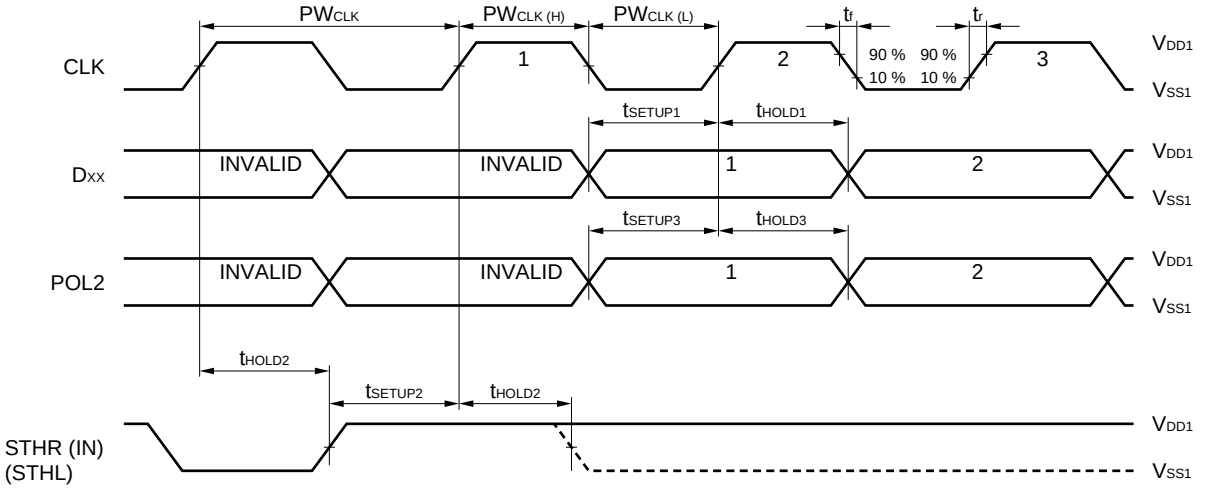
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		18			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		4			ns
Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
Data Setup Time	t_{SETUP1}		3			ns
Data Hold Time	t_{HOLD1}		3			ns
Start Pulse Setup Time	t_{SETUP2}		5			ns
Start Pulse Hold Time	t_{HOLD2}		5			ns
POL2 Setup Time	t_{SETUP3}		4			ns
POL2 Hold Time	t_{HOLD3}		4			ns
Start Pulse Low Period	t_{SPL}		5			ns
STB Pulse Width	PW_{STB}		0.5			μs
Data Invalid Period	t_{INV}		1			CLK
Final Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	CLK ↑ → STB ↓	5			ns
STB-CLK Time	$t_{STB-CLK}$	STB ↓ → CLK ↑	5			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	STB ↓ → STHR ↑	50			ns
POL-STB Time	$t_{POL-STB}$	POL ↑ or ↓ → STB ↑	–5			ns
STB-POL Time	$t_{STB-POL}$	STB ↓ → POL ↓ or ↑	5			ns

10. SWITCHING CHARACTERISTICS WAVEFORM (R/$\overline{L}$ = H)

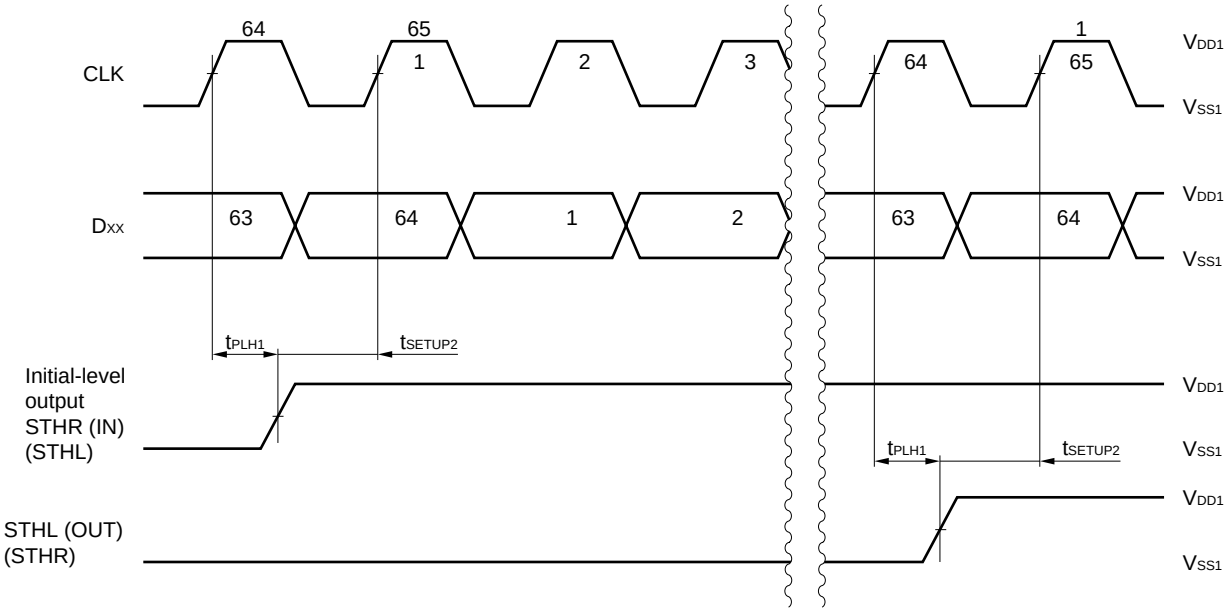
In ( ): R/$\overline{L}$ = L

Unless otherwise specified, the input level is defined to be 0.5 V_{DD1}.

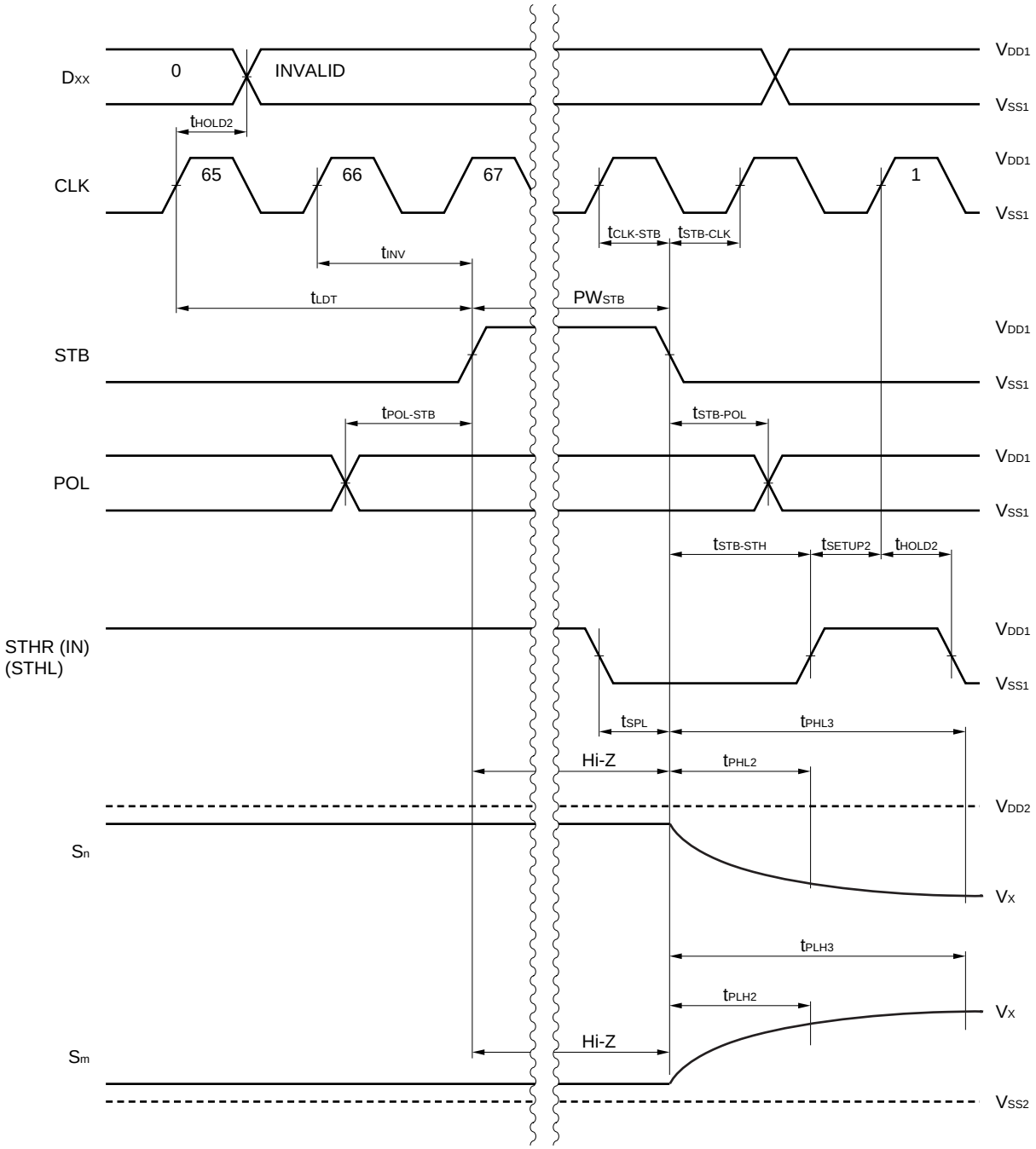
(1) Initial-Stage Driver's Input/Output Waveform



(2) Second- to Final-Stage Driver's Input/Output Timing



(3) Driver Output Timing



V_X refers to the final output voltage. t_{PLH2} and t_{PHL2} refer to the time required to reach an output precision level of 10% (0.1 V_X); and t_{PLH3} and t_{PHL3} refer to the time required to reach an output precision level of 6 bits.

11. RECOMMENDED MOUNTING CONDITIONS

When mounting this product, please make sure that the following recommended conditions are satisfied.

For packaging methods and conditions other than those recommended below, please contact NEC sales personnel.

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C; heating for 2 to 3 seconds; pressure 100 g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C; pressure 3 to 8 kg/cm^2; time 3 to 5 secs. Real bonding 165 to 180°C; pressure 25 to 45 kg/cm^2; time 30 to 40 secs. (When using the anisotropic conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

REFERENCE

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)

[MEMO]

M4 96.5