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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD16634A

300-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64 GRAY SCALE)

DESCRIPTION

The μPD16634A is a source driver for TFT-LCDs capable of dealing with displays 64 gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected by an internal D/A converter and 5-by-2 external power modules. Because the ★ output dynamic range is as large as V_{SS2}+0.1 V to V_{DD2}–0.1 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also to be able to deal with dot-line inversion when mounted on a single side, this source driver equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequent of 40 MHz when drivng at 3.0 V, this driver is applicable to XGA-standard TFT-LCD panels.

FEATURES

- 300 outputs
- CMOS level input
- Input of 6 bits (gradation data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter
- ★ • Output dynamic range : V_{SS2}+0.1 V to V_{DD2}–0.1 V
- ★ • Logic part supply voltage (V_{DD1}) : 3.3 V ± 0.3 V
- ★ • Driver part supply voltage (V_{DD2}) : 8.0 V ± 0.5 V
- High-speed data transfer: f_{MAX}=40 MHz MIN.(internal data transfer rate when operating at 3.0 V)
- Output voltage polarity inversion is possible (POL)
- Display data inversion function (POL2)
- Single bank arrangement is possible(loaded with slim TCP).

ORDERING INFORMATION

Part Number	Package
μPD16634AN-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order your TCP's external shape, please contact a NEC salesperson.

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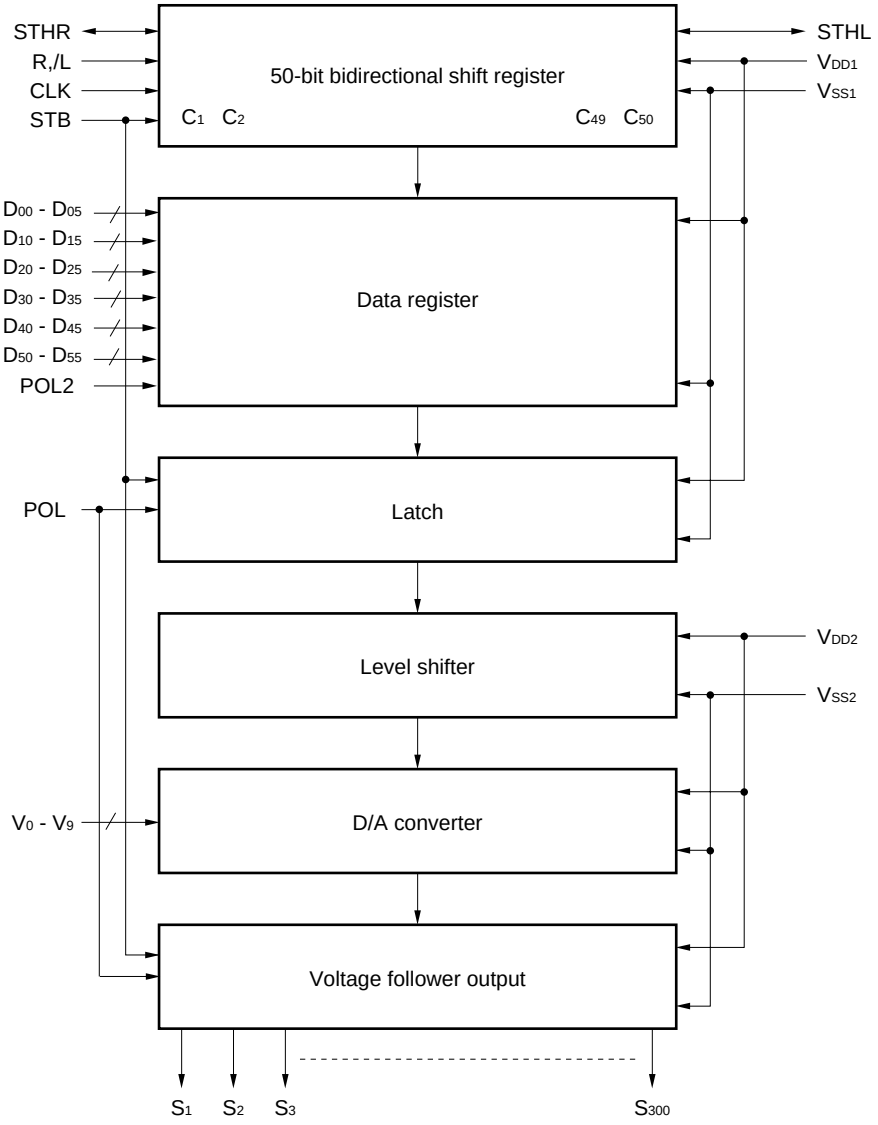
Printed in Japan

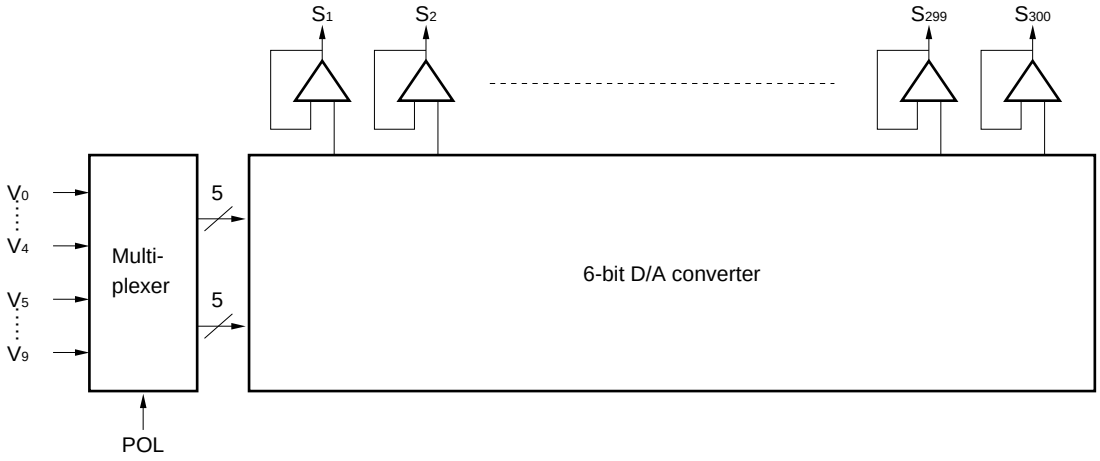
The mark ★ shows major revised points.

1. BLOCK DIAGRAM

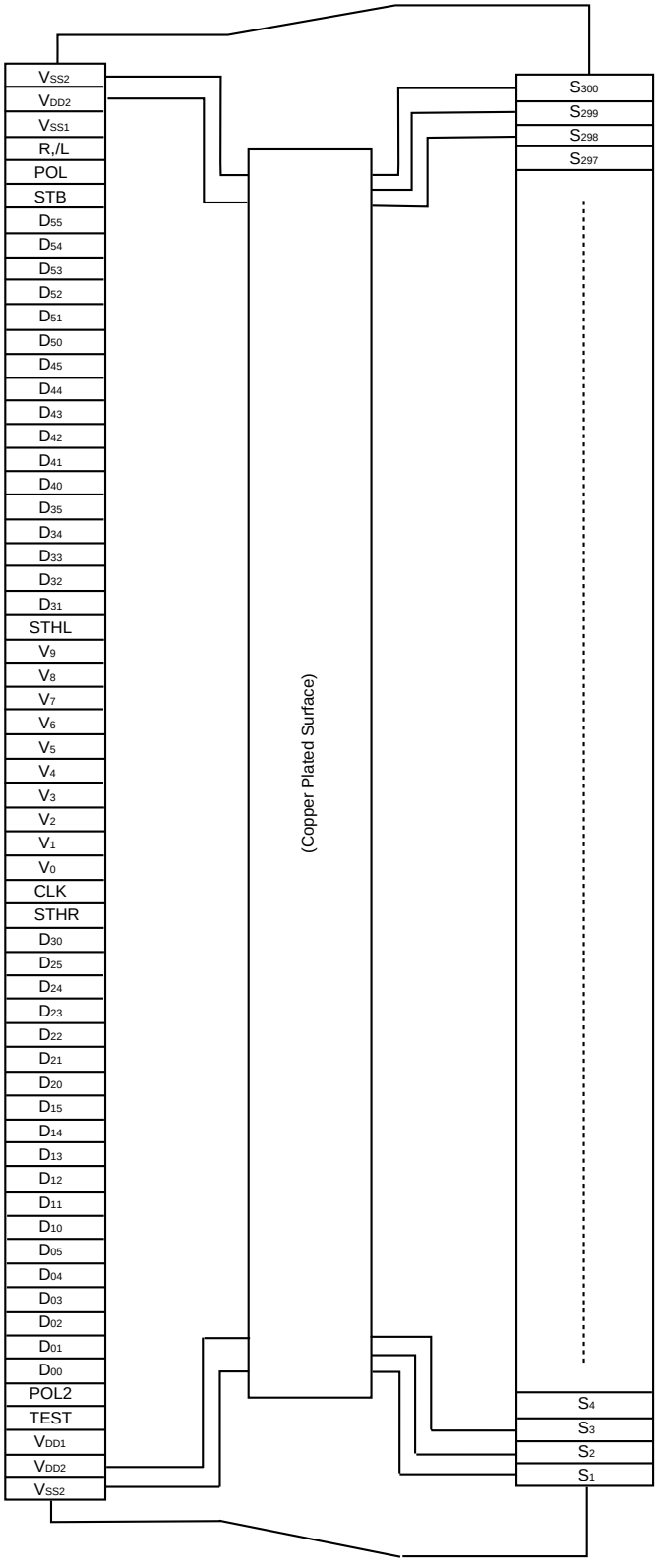


Remark /xxx indicates active low signal.

★ 2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD16634AN-xxx)



Caution This figure does not specify the TCP package. Therefore POL2 pins can be reduced by opening or short-circuiting to V_{SS2} by TCP wiring. POL2 pin can short to V_{SS1} on TCP. So when you not use "data inversion function", can reduce input pins.

4. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S_1 to S_{300}	Driver output	The D/A converted 64-gray-scale analog voltage is output
D_{00} to D_{05}	Display data input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D_{X0} : LSB, D_{X5} : MSB
D_{10} to D_{15}		
D_{20} to D_{25}		
D_{30} to D_{35}		
D_{40} to D_{45}		
D_{50} to D_{55}		
R,/L	Shift direction switching input	These refer to the start pulse input/output pins when cascades are connected. The shift directions of the shift registers are as follows. R,/L = H : STHR input, $S_1 \rightarrow S_{300}$, STHL output R,/L = L : STHL input, $S_{300} \rightarrow S_1$, STHR output
STHR	Right shift start pulse input/output	R,/L = H : Becomes the start pulse input pin. R,/L = L : Becomes the start pulse output pin.
STHL	Left shift start pulse input/output	R,/L = H : Becomes the start pulse input pin. R,/L = L : Becomes the start pulse output pin.
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 50th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. The initial-level driver's 50th clock becomes valid as the next-level driver's start pulse is input. If 52 clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch input	The contents of the data register are transferred to the latch at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	POL = L ; The S_{2n-1} output uses V_0 to V_4 as the reference supply; and the S_{2n} output uses V_5 to V_9 as the reference supply. POL = H ; The S_{2n-1} output uses V_5 to V_9 as the reference supply; and the S_{2n} output uses V_0 to V_4 as the reference supply. S_{2n-1} indicates the odd output; and S_{2n} indicates the even output. Input of the POL signal is allowed the setup time ($t_{POL-STB}$) with respect to STB's rising edge.
POL2	Data inversion input	POL2 = H : Display data is inverted. POL2 = L : Display data is not inverted.
V_0 to V_9	γ-corrected power supplies	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$
TEST	Test pin	Set it to open.
V_{DD1}	Logic circuit power supply	3.3 V ± 0.3 V
V_{DD2}	Driver circuit power supply	8.0 V ± 0.5 V
V_{SS1}	Logic ground	Grounding
V_{SS2}	Driver ground	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_9 in that order. Reverse this sequence to shut down.(Simultaneous power application to V_{DD2} and V_0 to V_9 is possible.)

2. To stabilize the supply voltage, please be sure to insert 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increase precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals(V_0,V_1,V_2...,V_9) and V_{SS2}.

3. We recommend to use Operational Amplifier to lower input impedance of γ-corrected voltage.

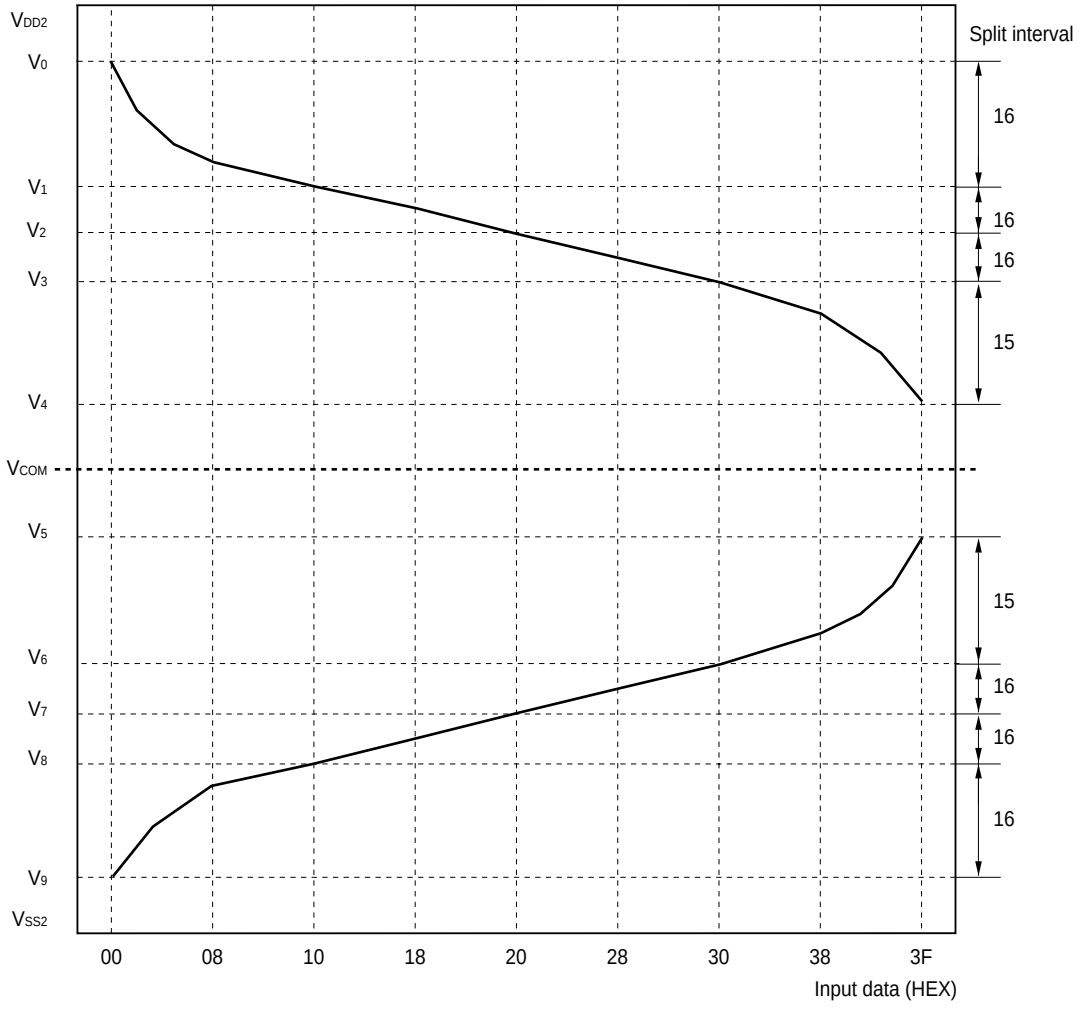
5. RELATIONHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches. The ladder resistors r_0 to r_{62} are so designed that the ratios between the LCD panel's γ-corrected voltages and V_0' to V_{63}', V_0" to V_{63}" are roughly equal; and their respective resistance values are as shown in Table 6-1. Among the 5-by 2 γ-corrected voltages, input gray scale voltages of the same polarity with respect to the common voltage, for the respective five γ-corrected voltages of V_0 to V_4 and V_5 to V_9. If fine gray scale voltage precision is not necessary, the voltage follower circuit supplied to the γ-corrected power supplies V_1 to V_3 and V_6 to V_8 can be deleted.

Figure 5-1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γ-corrected voltages V_0 to V_9 and the input data. Be sure to maintain the voltage relationships of $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$. Figure 6-1 and 6-2 show the relationship between the input data and the output data.

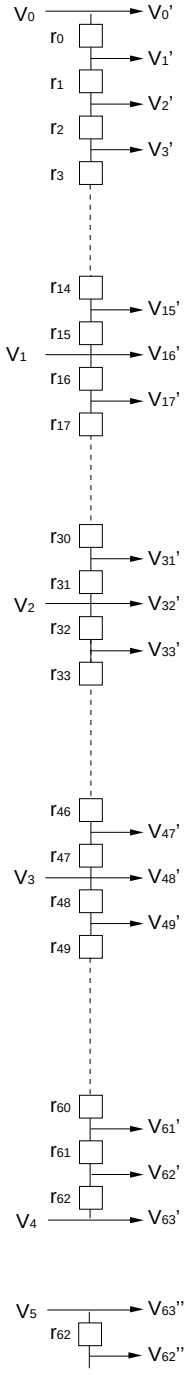
This driver IC is designed for single-sided mounting. Therefore, please do not use it for γ-corrected power supply level inversion in double-sided mounting.

★ **Figure 5-1. Relationship between Input Data and Output Voltage**



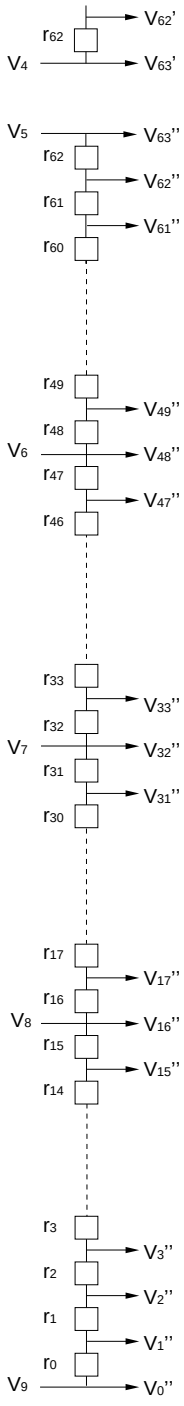
6. RESISTOR STRINGS

Figure 6-1. Relationship Between Input Data and Output Voltage : $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5$, POL2 = L



Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage	
00H	0	0	0	0	0	0	V_0'	V_0
01H	0	0	0	0	0	1	V_1'	$V_1 + (V_0 - V_1) \times$ 7250/8050
02H	0	0	0	0	1	0	V_2'	$V_1 + (V_0 - V_1) \times$ 6500/8050
03H	0	0	0	0	1	1	V_3'	$V_1 + (V_0 - V_1) \times$ 5800/8050
04H	0	0	0	1	0	0	V_4'	$V_1 + (V_0 - V_1) \times$ 5150/8050
05H	0	0	0	1	0	1	V_5'	$V_1 + (V_0 - V_1) \times$ 4550/8050
06H	0	0	0	1	1	0	V_6'	$V_1 + (V_0 - V_1) \times$ 4000/8050
07H	0	0	0	1	1	1	V_7'	$V_1 + (V_0 - V_1) \times$ 3450/8050
08H	0	0	1	0	0	0	V_8'	$V_1 + (V_0 - V_1) \times$ 2950/8050
09H	0	0	1	0	0	1	V_9'	$V_1 + (V_0 - V_1) \times$ 2450/8050
0AH	0	0	1	0	1	0	V_{10}'	$V_1 + (V_0 - V_1) \times$ 2050/8050
0BH	0	0	1	0	1	1	V_{11}'	$V_1 + (V_0 - V_1) \times$ 1650/8050
0CH	0	0	1	1	0	0	V_{12}'	$V_1 + (V_0 - V_1) \times$ 1300/8050
0DH	0	0	1	1	0	1	V_{13}'	$V_1 + (V_0 - V_1) \times$ 950/8050
0EH	0	0	1	1	1	0	V_{14}'	$V_1 + (V_0 - V_1) \times$ 600/8050
0FH	0	0	1	1	1	1	V_{15}'	$V_1 + (V_0 - V_1) \times$ 300/8050
10H	0	1	0	0	0	0	V_{16}'	V_1
11H	0	1	0	0	0	1	V_{17}'	$V_2 + (V_1 - V_2) \times$ 2450/2750
12H	0	1	0	0	1	0	V_{18}'	$V_2 + (V_1 - V_2) \times$ 2200/2750
13H	0	1	0	0	1	1	V_{19}'	$V_2 + (V_1 - V_2) \times$ 1950/2750
14H	0	1	0	1	0	0	V_{20}'	$V_2 + (V_1 - V_2) \times$ 1700/2750
15H	0	1	0	1	0	1	V_{21}'	$V_2 + (V_1 - V_2) \times$ 1500/2750
16H	0	1	0	1	1	0	V_{22}'	$V_2 + (V_1 - V_2) \times$ 1300/2750
17H	0	1	0	1	1	1	V_{23}'	$V_2 + (V_1 - V_2) \times$ 1100/2750
18H	0	1	1	0	0	0	V_{24}'	$V_2 + (V_1 - V_2) \times$ 950/2750
19H	0	1	1	0	0	1	V_{25}'	$V_2 + (V_1 - V_2) \times$ 800/2750
1AH	0	1	1	0	1	0	V_{26}'	$V_2 + (V_1 - V_2) \times$ 650/2750
1BH	0	1	1	0	1	1	V_{27}'	$V_2 + (V_1 - V_2) \times$ 500/2750
1CH	0	1	1	1	0	0	V_{28}'	$V_2 + (V_1 - V_2) \times$ 400/2750
1DH	0	1	1	1	0	1	V_{29}'	$V_2 + (V_1 - V_2) \times$ 300/2750
1EH	0	1	1	1	1	0	V_{30}'	$V_2 + (V_1 - V_2) \times$ 200/2750
1FH	0	1	1	1	1	1	V_{31}'	$V_2 + (V_1 - V_2) \times$ 100/2750
20H	1	0	0	0	0	0	V_{32}'	V_2
21H	1	0	0	0	0	1	V_{33}'	$V_3 + (V_2 - V_3) \times$ 1500/1600
22H	1	0	0	0	1	0	V_{34}'	$V_3 + (V_2 - V_3) \times$ 1400/1600
23H	1	0	0	0	1	1	V_{35}'	$V_3 + (V_2 - V_3) \times$ 1300/1600
24H	1	0	0	1	0	0	V_{36}'	$V_3 + (V_2 - V_3) \times$ 1200/1600
25H	1	0	0	1	0	1	V_{37}'	$V_3 + (V_2 - V_3) \times$ 1100/1600
26H	1	0	0	1	1	0	V_{38}'	$V_3 + (V_2 - V_3) \times$ 1000/1600
27H	1	0	0	1	1	1	V_{39}'	$V_3 + (V_2 - V_3) \times$ 900/1600
28H	1	0	1	0	0	0	V_{40}'	$V_3 + (V_2 - V_3) \times$ 800/1600
29H	1	0	1	0	0	1	V_{41}'	$V_3 + (V_2 - V_3) \times$ 700/1600
2AH	1	0	1	0	1	0	V_{42}'	$V_3 + (V_2 - V_3) \times$ 600/1600
2BH	1	0	1	0	1	1	V_{43}'	$V_3 + (V_2 - V_3) \times$ 500/1600
2CH	1	0	1	1	0	0	V_{44}'	$V_3 + (V_2 - V_3) \times$ 400/1600
2DH	1	0	1	1	0	1	V_{45}'	$V_3 + (V_2 - V_3) \times$ 300/1600
2EH	1	0	1	1	1	0	V_{46}'	$V_3 + (V_2 - V_3) \times$ 200/1600
2FH	1	0	1	1	1	1	V_{47}'	$V_3 + (V_2 - V_3) \times$ 100/1600
30H	1	1	0	0	0	0	V_{48}'	V_3
31H	1	1	0	0	0	1	V_{49}'	$V_4 + (V_3 - V_4) \times$ 3350/3450
32H	1	1	0	0	1	0	V_{50}'	$V_4 + (V_3 - V_4) \times$ 3250/3450
33H	1	1	0	0	1	1	V_{51}'	$V_4 + (V_3 - V_4) \times$ 3150/3450
34H	1	1	0	1	0	0	V_{52}'	$V_4 + (V_3 - V_4) \times$ 3050/3450
35H	1	1	0	1	0	1	V_{53}'	$V_4 + (V_3 - V_4) \times$ 2950/3450
36H	1	1	0	1	1	0	V_{54}'	$V_4 + (V_3 - V_4) \times$ 2800/3450
37H	1	1	0	1	1	1	V_{55}'	$V_4 + (V_3 - V_4) \times$ 2650/3450
38H	1	1	1	0	0	0	V_{56}'	$V_4 + (V_3 - V_4) \times$ 2500/3450
39H	1	1	1	0	0	1	V_{57}'	$V_4 + (V_3 - V_4) \times$ 2300/3450
3AH	1	1	1	0	1	0	V_{58}'	$V_4 + (V_3 - V_4) \times$ 2100/3450
3BH	1	1	1	0	1	1	V_{59}'	$V_4 + (V_3 - V_4) \times$ 1850/3450
3CH	1	1	1	1	0	0	V_{60}'	$V_4 + (V_3 - V_4) \times$ 1600/3450
3DH	1	1	1	1	0	1	V_{61}'	$V_4 + (V_3 - V_4) \times$ 1300/3450
3EH	1	1	1	1	1	0	V_{62}'	$V_4 + (V_3 - V_4) \times$ 800/3450
3FH	1	1	1	1	1	1	V_{63}'	V_4

Figure 6-2. Relationship Between Input Data and Output Voltage : $V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$, POL2 = L



Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage	
00H	0	0	0	0	0	0	V_0''	V_9
01H	0	0	0	0	0	1	V_1''	$V_9 + (V_8 - V_9) \times 800/8050$
02H	0	0	0	0	1	0	V_2''	$V_9 + (V_8 - V_9) \times 1550/8050$
03H	0	0	0	0	1	1	V_3''	$V_9 + (V_8 - V_9) \times 2250/8050$
04H	0	0	0	1	0	0	V_4''	$V_9 + (V_8 - V_9) \times 2900/8050$
05H	0	0	0	1	0	1	V_5''	$V_9 + (V_8 - V_9) \times 3500/8050$
06H	0	0	0	1	1	0	V_6''	$V_9 + (V_8 - V_9) \times 4050/8050$
07H	0	0	0	1	1	1	V_7''	$V_9 + (V_8 - V_9) \times 4600/8050$
08H	0	0	1	0	0	0	V_8''	$V_9 + (V_8 - V_9) \times 5100/8050$
09H	0	0	1	0	0	1	V_9''	$V_9 + (V_8 - V_9) \times 5600/8050$
0AH	0	0	1	0	1	0	V_{10}''	$V_9 + (V_8 - V_9) \times 6000/8050$
0BH	0	0	1	0	1	1	V_{11}''	$V_9 + (V_8 - V_9) \times 6400/8050$
0CH	0	0	1	1	0	0	V_{12}''	$V_9 + (V_8 - V_9) \times 6750/8050$
0DH	0	0	1	1	0	1	V_{13}''	$V_9 + (V_8 - V_9) \times 7100/8050$
0EH	0	0	1	1	1	0	V_{14}''	$V_9 + (V_8 - V_9) \times 7450/8050$
0FH	0	0	1	1	1	1	V_{15}''	$V_9 + (V_8 - V_9) \times 7750/8050$
10H	0	1	0	0	0	0	V_{16}''	V_8
11H	0	1	0	0	0	1	V_{17}''	$V_8 + (V_7 - V_8) \times 300/2750$
12H	0	1	0	0	1	0	V_{18}''	$V_8 + (V_7 - V_8) \times 550/2750$
13H	0	1	0	0	1	1	V_{19}''	$V_8 + (V_7 - V_8) \times 800/2750$
14H	0	1	0	1	0	0	V_{20}''	$V_8 + (V_7 - V_8) \times 1050/2750$
15H	0	1	0	1	0	1	V_{21}''	$V_8 + (V_7 - V_8) \times 1250/2750$
16H	0	1	0	1	1	0	V_{22}''	$V_8 + (V_7 - V_8) \times 1450/2750$
17H	0	1	0	1	1	1	V_{23}''	$V_8 + (V_7 - V_8) \times 1650/2750$
18H	0	1	1	0	0	0	V_{24}''	$V_8 + (V_7 - V_8) \times 1800/2750$
19H	0	1	1	0	0	1	V_{25}''	$V_8 + (V_7 - V_8) \times 1950/2750$
1AH	0	1	1	0	1	0	V_{26}''	$V_8 + (V_7 - V_8) \times 2100/2750$
1BH	0	1	1	0	1	1	V_{27}''	$V_8 + (V_7 - V_8) \times 2250/2750$
1CH	0	1	1	1	0	0	V_{28}''	$V_8 + (V_7 - V_8) \times 2350/2750$
1DH	0	1	1	1	0	1	V_{29}''	$V_8 + (V_7 - V_8) \times 2450/2750$
1EH	0	1	1	1	1	0	V_{30}''	$V_8 + (V_7 - V_8) \times 2550/2750$
1FH	0	1	1	1	1	1	V_{31}''	$V_8 + (V_7 - V_8) \times 2650/2750$
20H	1	0	0	0	0	0	V_{32}''	V_7
21H	1	0	0	0	0	1	V_{33}''	$V_7 + (V_6 - V_7) \times 100/1600$
22H	1	0	0	0	1	0	V_{34}''	$V_7 + (V_6 - V_7) \times 200/1600$
23H	1	0	0	0	1	1	V_{35}''	$V_7 + (V_6 - V_7) \times 300/1600$
24H	1	0	0	1	0	0	V_{36}''	$V_7 + (V_6 - V_7) \times 400/1600$
25H	1	0	0	1	0	1	V_{37}''	$V_7 + (V_6 - V_7) \times 500/1600$
26H	1	0	0	1	1	0	V_{38}''	$V_7 + (V_6 - V_7) \times 600/1600$
27H	1	0	0	1	1	1	V_{39}''	$V_7 + (V_6 - V_7) \times 700/1600$
28H	1	0	1	0	0	0	V_{40}''	$V_7 + (V_6 - V_7) \times 800/1600$
29H	1	0	1	0	0	1	V_{41}''	$V_7 + (V_6 - V_7) \times 900/1600$
2AH	1	0	1	0	1	0	V_{42}''	$V_7 + (V_6 - V_7) \times 1000/1600$
2BH	1	0	1	0	1	1	V_{43}''	$V_7 + (V_6 - V_7) \times 1100/1600$
2CH	1	0	1	1	0	0	V_{44}''	$V_7 + (V_6 - V_7) \times 1200/1600$
2DH	1	0	1	1	0	1	V_{45}''	$V_7 + (V_6 - V_7) \times 1300/1600$
2EH	1	0	1	1	1	0	V_{46}''	$V_7 + (V_6 - V_7) \times 1400/1600$
2FH	1	0	1	1	1	1	V_{47}''	$V_7 + (V_6 - V_7) \times 1500/1600$
30H	1	1	0	0	0	0	V_{48}''	V_6
31H	1	1	0	0	0	1	V_{49}''	$V_6 + (V_5 - V_6) \times 100/3450$
32H	1	1	0	0	1	0	V_{50}''	$V_6 + (V_5 - V_6) \times 200/3450$
33H	1	1	0	0	1	1	V_{51}''	$V_6 + (V_5 - V_6) \times 300/3450$
34H	1	1	0	1	0	0	V_{52}''	$V_6 + (V_5 - V_6) \times 400/3450$
35H	1	1	0	1	0	1	V_{53}''	$V_6 + (V_5 - V_6) \times 500/3450$
36H	1	1	0	1	1	0	V_{54}''	$V_6 + (V_5 - V_6) \times 650/3450$
37H	1	1	0	1	1	1	V_{55}''	$V_6 + (V_5 - V_6) \times 800/3450$
38H	1	1	1	0	0	0	V_{56}''	$V_6 + (V_5 - V_6) \times 950/3450$
39H	1	1	1	0	0	1	V_{57}''	$V_6 + (V_5 - V_6) \times 1150/3450$
3AH	1	1	1	0	1	0	V_{58}''	$V_6 + (V_5 - V_6) \times 1350/3450$
3BH	1	1	1	0	1	1	V_{59}''	$V_6 + (V_5 - V_6) \times 1600/3450$
3CH	1	1	1	1	0	0	V_{60}''	$V_6 + (V_5 - V_6) \times 1850/3450$
3DH	1	1	1	1	0	1	V_{61}''	$V_6 + (V_5 - V_6) \times 2150/3450$
3EH	1	1	1	1	1	0	V_{62}''	$V_6 + (V_5 - V_6) \times 2650/3450$
3FH	1	1	1	1	1	1	V_{63}''	V_5

Table 6-1. Ladder Resistance Values (r_0 to r_{62}) : Reference Value

	Resistor Name	Resistance Value (Ω)	Resistor Name	Resistance Value (Ω)	
V_0, V_9 →	r_0	800	r_{32}	100	← V_2, V_7
	r_1	750	r_{33}	100	
	r_2	700	r_{34}	100	
	r_3	650	r_{35}	100	
	r_4	600	r_{36}	100	
	r_5	550	r_{37}	100	
	r_6	550	r_{38}	100	
	r_7	500	r_{39}	100	
	r_8	500	r_{40}	100	
	r_9	400	r_{41}	100	
	r_{10}	400	r_{42}	100	
	r_{11}	350	r_{43}	100	
	r_{12}	350	r_{44}	100	
	r_{13}	350	r_{45}	100	
	r_{14}	300	r_{46}	100	
	r_{15}	300	r_{47}	100	
V_1, V_8 →	r_{16}	300	r_{48}	100	← V_3, V_6
	r_{17}	250	r_{49}	100	
	r_{18}	250	r_{50}	100	
	r_{19}	250	r_{51}	100	
	r_{20}	200	r_{52}	100	
	r_{21}	200	r_{53}	150	
	r_{22}	200	r_{54}	150	
	r_{23}	150	r_{55}	150	
	r_{24}	150	r_{56}	200	
	r_{25}	150	r_{57}	200	
	r_{26}	150	r_{58}	250	
	r_{27}	100	r_{59}	250	
	r_{28}	100	r_{60}	300	
	r_{29}	100	r_{61}	500	
	r_{30}	100	r_{62}	800	← V_4, V_5
V_2, V_7 →	r_{31}	100	Total	15850	

7. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 6 bits x 2 RGBs (6 dots)

Input width : 36 bits (2-pixel data)

(1) R,/L = H (right shift)

Output	S_1	S_2	S_3	S_4	S_5	…	S_{299}	S_{300}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	D_{40} to D_{45}	…	D_{40} to D_{45}	D_{50} to D_{55}

(2) R,/L = L (left shift)

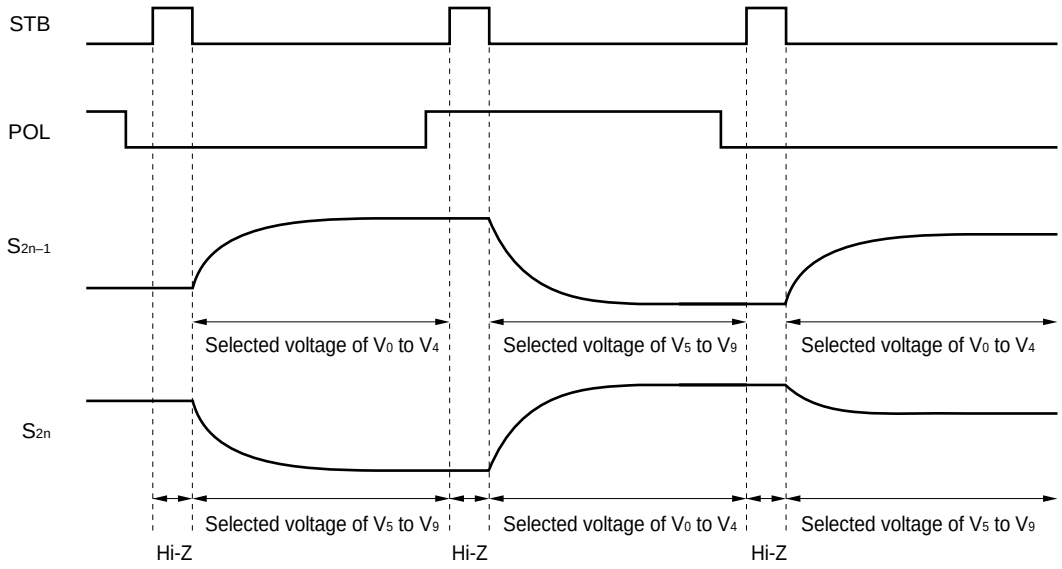
Output	S_1	S_2	S_3	S_4	S_5	…	S_{299}	S_{300}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	D_{40} to D_{45}	…	D_{40} to D_{45}	D_{50} to D_{55}

POL	S_{2n-1}	S_{2n}
L	V_0 to V_4	V_5 to V_9
H	V_5 to V_9	V_0 to V_4

Remark S_{2n-1} (Odd output), S_{2n} (Even output)n = 1,2,.....,150

8. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.

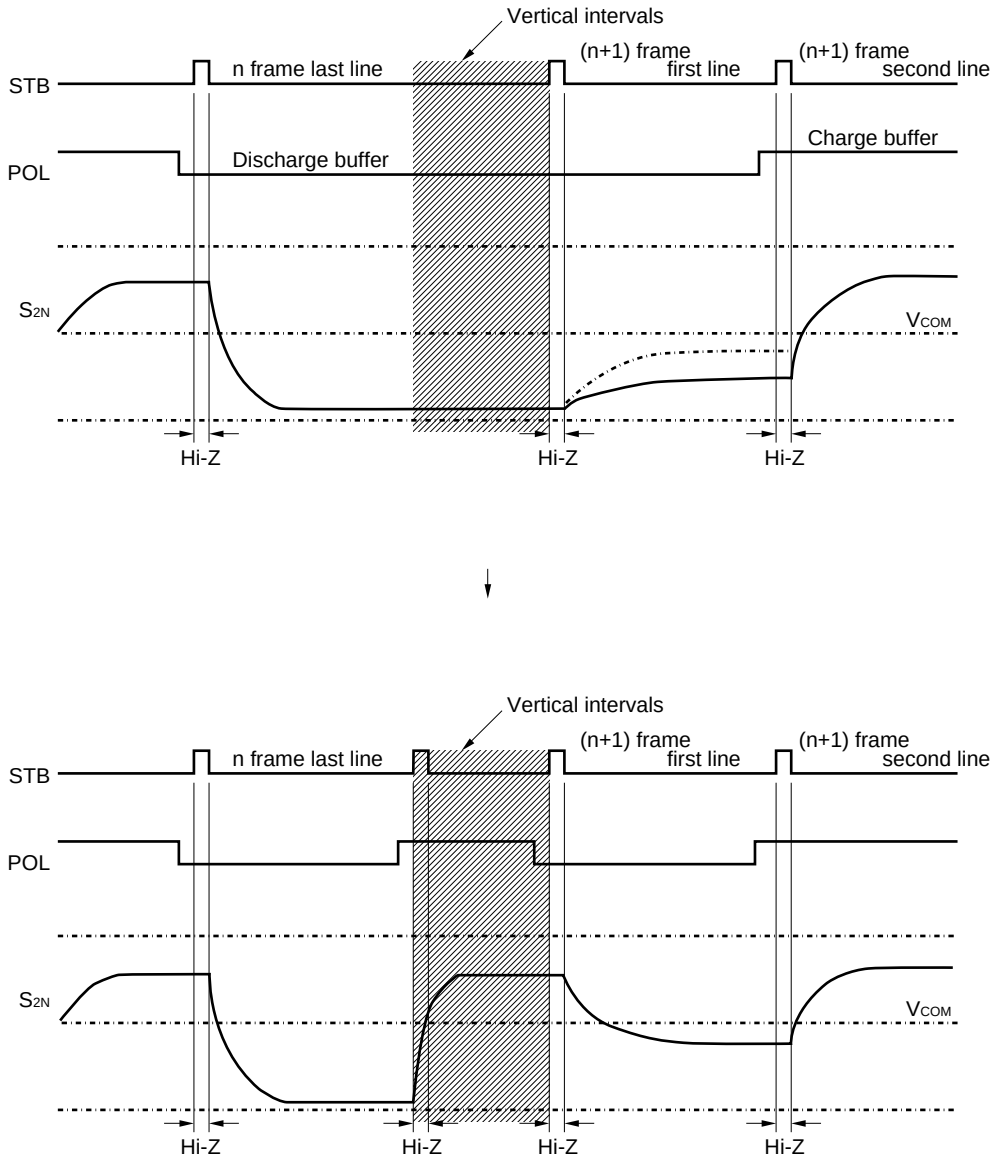


9. CAUTIONS ABOUT FRAME INVERSION

In the case of dot inversion, n frame last line and (n+1) frame first line is the same polarity. When write the same polarity twice; there are two cases as follows.

(1) Last line output in n frame > First line output in (n+1) frame → Positive to write
(2) Last line output in n frame < First line output in (n+1) frame → Not possible to write

μPD16634A has charge buffer and discharge buffer, so need to inversion polarity and write in the case of both ways.



10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic part supply voltage	V_{DD1}	–0.5 to +5.0	V
Driver part supply voltage	V_{DD2}	–0.5 to +10.0	V
Logic part input voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Driver part input voltage	V_{I2}	–0.5 to V_{DD2} + 0.5	V
Logic part output voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver part output voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Operating ambient temperature	T_A	–10 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

★ **Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.**

Recommended Operating Range (T_A = –10 to +75 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic part supply voltage	V_{DD1}	3.0	3.3	3.6	V
Driver part supply voltage	V_{DD2}	7.5	8.0	8.5	V
High-level input voltage	V_{IH}	0.7V_{DD1}		V_{DD1}	V
Low-level input voltage	V_{IL}	0		0.3V_{DD1}	V
γ-corrected supply voltage	V_0 to V_9	V_{SS2}		V_{DD2}	V
Driver part output voltage	V_O	V_{SS2} + 0.1		V_{DD2} – 0.1	V
Maximum clock frequency	$f_{MAX.}$	40			MHz

Electrical Characteristics (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 8.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{IL}				±1.0	μA
High-level output voltage	V_{OH}	STHR(STHL),I_O=0 mA	V_{DD1}–0.1			V
Low-level output voltage	V_{OL}	STHR(STHL),I_O=0 mA			0.1	V
γ-corrected supply current	I_γ	V_0–V_9 = 8 V V_0,V_9		0.3	0.6	mA
Driver output current	I_{VOH}	V_X=7 V, V_{OUT}=1 V Note1			–0.5	mA
	I_{VOL}	V_X=1 V, V_{OUT}=7 V Note1	0.5			mA
Output voltage deviation Note2	ΔV_O	Input data : 00H to 3FH		±5	±20	mV
Average output voltage variation Note3	ΔV_{AV}	Input data : 00H to 3FH		±10		mV
Output voltage range	V_O	Input data : 00H to 3FH	0.1		V_{DD2}–0.1	V
Logic part dynamic current consumption Notes4,5	I_{DD1}	V_{DD1}, when with no load		0.5	3.5	mA
★ Driver part dynamic current consumption Notes4,5	I_{DD2}	V_{DD2}, when with no load		2.2	8.0	mA

Notes 1. V_X refers to the output voltage of analog output pins S_1 to S_{300}.
V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{300}.

2. The output voltage deviation refers to the voltage difference between adjoining output pins when the display data is the same (within the chip).

3. The average output voltage variation refers to the average output voltage difference between chips. The average output voltage refers to the average voltage between chips when the display data is the same.

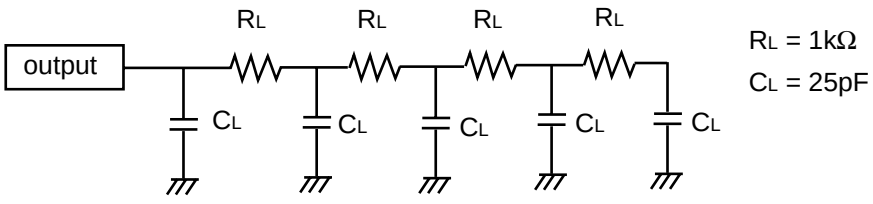
4. The STB cycle is defined to be 20 μs at f_{CLK} = 40 MHz. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

5. Refers to the current consumption per driver when cascades are connected under the assumption of SVGA single-sided mounting (10 units).

Switching Characteristics (T_A = –10 to +75 ºC, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 8.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start pulse delay time	t_{PLH1}	C_L = 25 pF		13	20	ns
Driver output delay time	t_{PHL2}	C_L = 125 pF, R_L = 4 kΩ Note		3.7	8	μs
	t_{PHL3}			5.3	14	μs
	t_{PLH2}			3.0	8	μs
	t_{PLH3}			5.3	14	μs
Input capacitance	C_1	STHR,STHL excluded, T_A = 25 °C		5.4	15	pF
	C_2			7.6	15	pF

Note Load condition

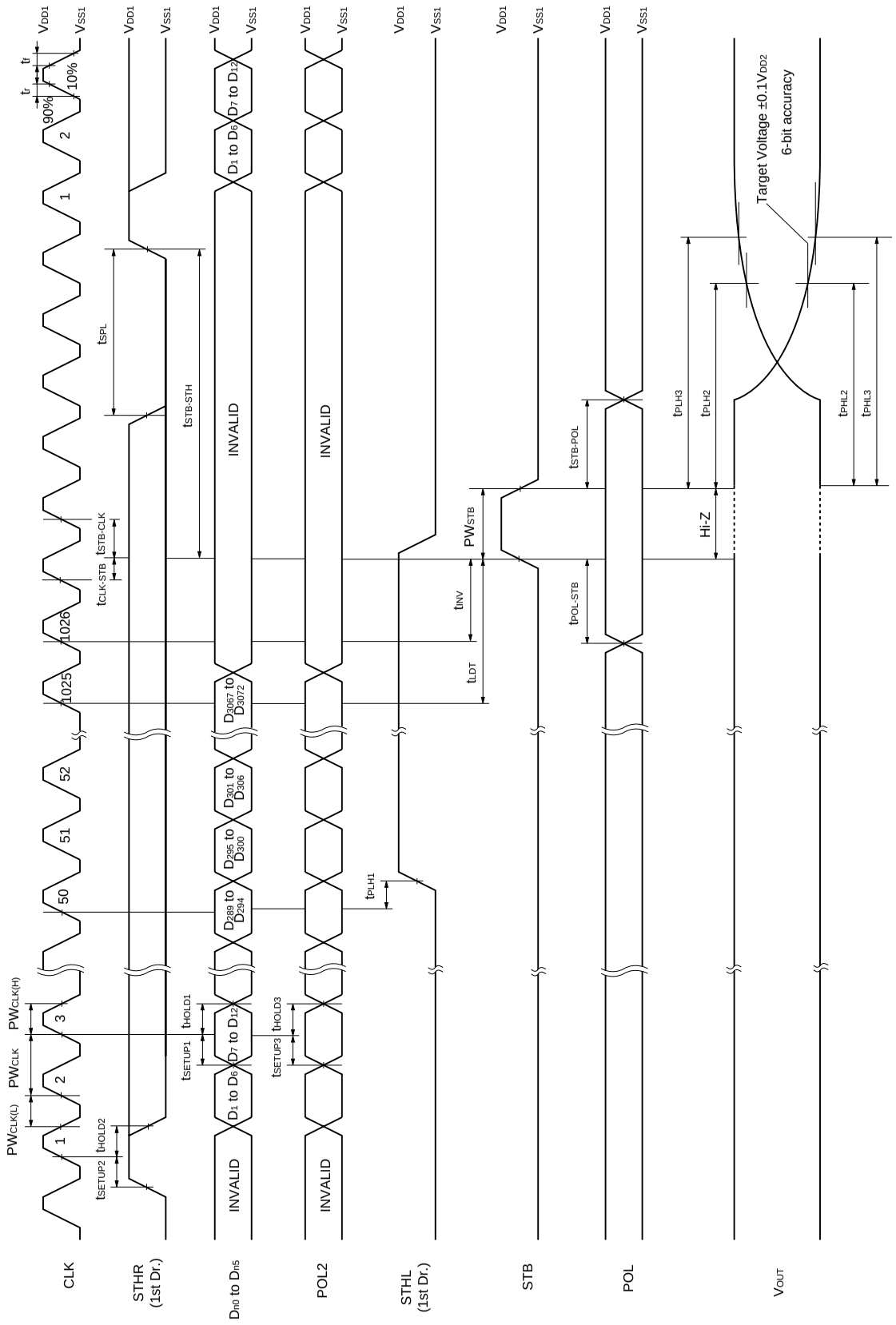


Timing Requirements (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 8.0 ns)

	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
	Clock pulse width	PW_{CLK}		25			ns
	Clock pulse low period	$PW_{CLK (L)}$		6			ns
	Clock pulse high period	$PW_{CLK (H)}$		6			ns
	Data setup time	t_{SETUP1}		6			ns
	Data hold time	t_{HOLD1}		6			ns
	Start pulse setup time	t_{SETUP2}		5			ns
	Start pulse hold time	t_{HOLD2}		5			ns
	Start pulse low period	t_{SPL}		6			ns
	POL2 setup time	t_{SETUP3}		6			ns
	POL2 hold time	t_{HOLD3}		6			ns
	STB pulse width	PW_{STB}		1			μs
	Data invalid period	t_{INV}		1			CLK
	Final data timing	t_{LDT}		2			CLK
★	CLK-STB time	$t_{CLK-STB}$	CLK↑→STB↑	6			ns
★	STB-CLK time	$t_{STB-CLK}$	STB↑ →CLK↑	6			ns
	Time between STB and start pulse	$t_{STB-STH}$	STB↓ →CLK↑	60			ns
	POL-STB time	$t_{POL-STB}$	POL↑or↓ →STB↑	–5			ns
	STB-POL time	$t_{STB-POL}$	STB↓ →POL↑ or↓	6			ns

★ 11. SWITCHING CHARACTERISTIC WAVEFORM(R,/L= H)

Unless otherwise specified, the input level is defined to be 0.5 V_{DD1}.



12. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD16634A.

For more details, refer to the **Semiconductor Device Mounting Technology Manual(C10535E).**

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16634AN-xxx : TCP(TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350 °C, heating for 2 to 3 sec ; pressure 100g(per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100 °C ; pressure 3 to 8 kg/cm^2; time 3 to 5 sec. Real bonding 165 to 180 °C pressure 25 to 45 kg/cm^2 time 30 to 40secs(When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite,Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System(C10983E)

Quality Grades to NEC's Semiconductor Devices(C11531E)

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