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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

μPD16631A

240 OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64 GRAY SCALE)

The μPD16631A is source driver for TFT-LCDs capable of dealing with display with 64 gray ascale. Data input is based on digital input configured as 6-bits by 6 dots, which can realize a full-color display of 260,000 colors by output of 64 values γcorrected by an internal D/A converter and 5-by-2 external power modules.

Because the output dynamic range is as large as 10 V_{P-P}, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gradation voltages of differing polarity. Assuring a maximum clock frequency of 33 MHz when driving 3 V, this driver is applicable to VGA-standard TFT-LCD panels.

FEATURES

- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter
- Output dynamic range 11.5 V_{P-P} max. (when V_{DD2} = 13.5 V)
- CMOS level input
- Input of 6 bits (gradation data) by 6 dots
- High-speed data transfer: $f_{max.}$ = 33 MHz (internal data transfer speed when operating at 3.0 V)
- 240 outputs
- Single bank arrangement possible (loaded with slim TCP)

ORDERING INFORMATION

Part Number	Package
μPD16631AN-xxx	TCP (TAB package)

The TCP's external shape is customized. To order your TCP's external shape, please contact a NEC salesperson.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

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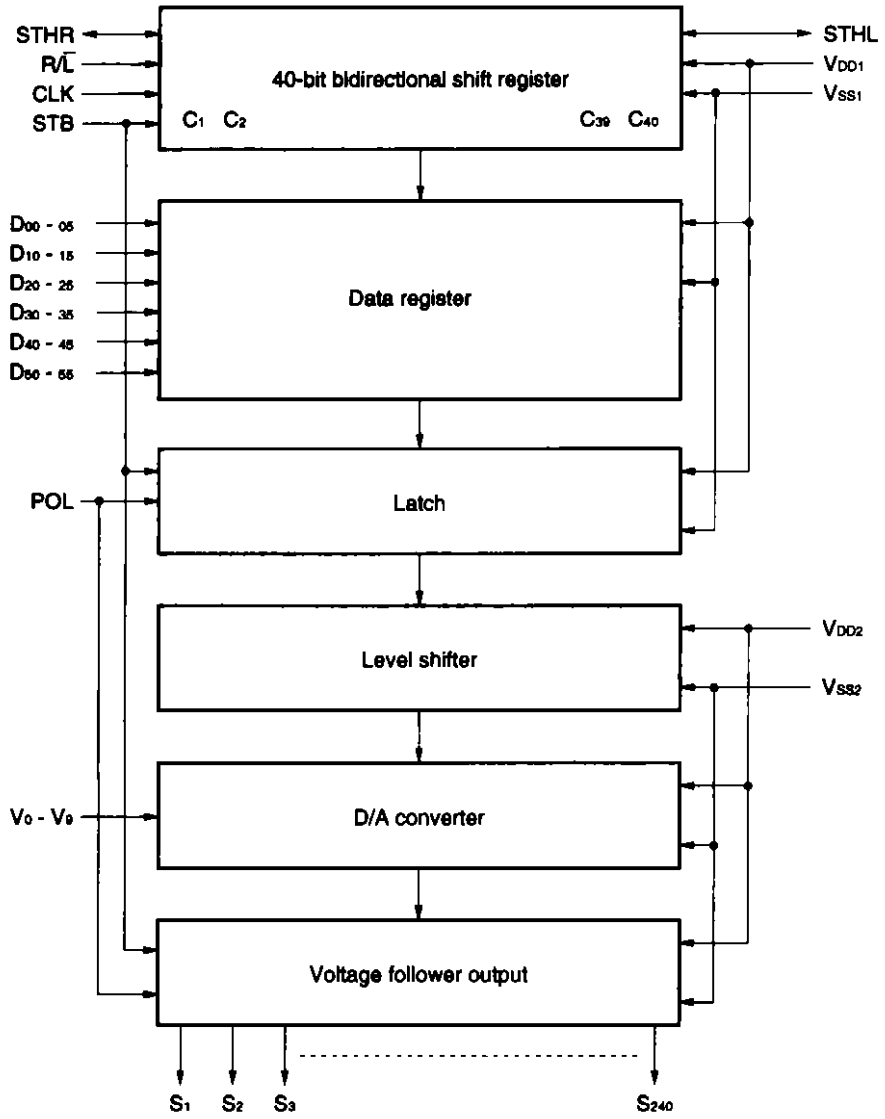
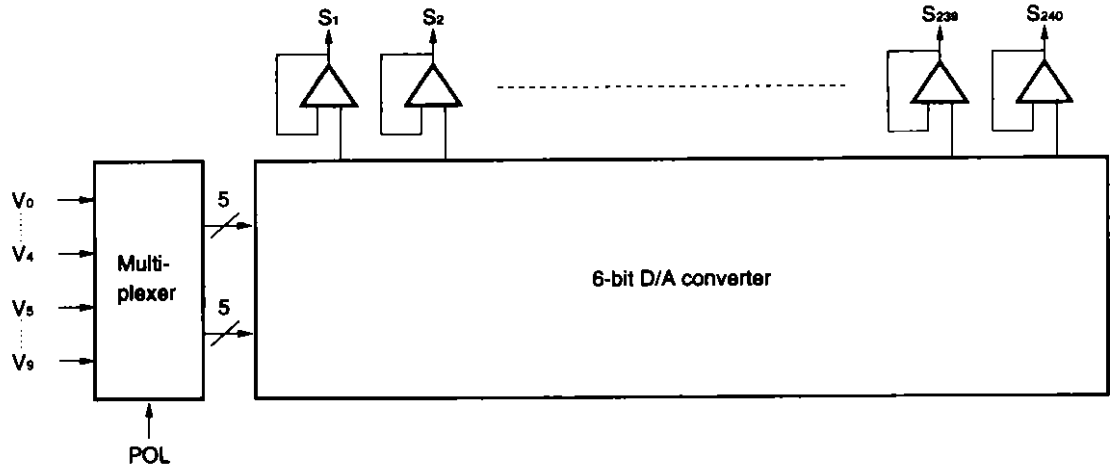
Date Published April 1996 P
Printed in Japan

1. BLOCK DIAGRAM



2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



POL	S_{2n-1}	S_{2n}
L	V_0 to V_4	V_5 to V_9
H	V_6 to V_9	V_0 to V_4

S_{2n-1} (odd output), S_{2n} (even output) n = 1, 2, ···, 120

3. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S_1 to S_{240}	Driver output	The analog voltage of the D/A-converted 64 gray-scale is output.
D_{00} to D_{05}	Display data input	The display data is input with a width of 36 bits, viz., the gradation data (6 bits) by 6 dots (RGB). D_{X0}: LSB, D_{X5}: MSB
D_{10} to D_{15}		
D_{20} to D_{25}		
D_{20} to D_{25}		
D_{20} to D_{25}		
D_{20} to D_{25}		
R/$\overline{L}$	Shift direction switching input	These refer to the start pulse input/output pins when cascades are connected. The shift directions of the shift registers are as follows. R/$\overline{L}$ = H: STHR input, $S_1 \rightarrow S_{240}$, STHL output R/$\overline{L}$ = L: STHL input, $S_{240} \rightarrow S_1$, STHR output
STHR	Right shift start pulse input/output	R/$\overline{L}$ = H: Becomes the start pulse input pin. R/$\overline{L}$ = L: Becomes the start pulse output pin.
STHL	Left shift start pulse input/output	R/$\overline{L}$ = H: Becomes the start pulse output pin. R/$\overline{L}$ = L: Becomes the start pulse input pin.
CLK	Shift clock input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 40th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. The initial-level driver's 40th clock becomes valid as the next-level driver's start pulse is input. If 42 clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch input	The contents of the data register are transferred to the latch at the rising edge. And, at the trailing edge, the gradation voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	POL = L; The S_{2n-1} output uses V_0 to V_4 as the reference supply; and the S_{2n} output uses V_5 to V_9 as the reference supply. POL = H; The S_{2n-1} output uses V_5 to V_9 as the reference supply; and the S_{2n} output uses V_0 to V_4 as the reference supply. S_{2n-1} indicates the odd output; and S_{2n} indicates the even output. Input of the POL signal is allowed the setup time ($t_{POL-STB}$) with respect to STB's rising edge.
V_0 to V_9	γcorrected power supplies	Input the γcorrected power supplies from outside. The γcorrected power supplies can not be applied by inverting their levels. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale power supply at a constant level. $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$
TEST	Test pin	Set it to open condition.
V_{DD1}	Logic power supply	3.3 V $^{+2.2}_{-0.3}$ V
V_{DD2}	Driver power supply	13.0 V $^{+0.5}_{-2.0}$ V
V_{SS1}	Logic ground	Conect to the system ground.
V_{SS2}	Driver ground	Conect to the system ground.

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_9 in that order. Reverse this sequence to shut down.

2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.1. μF is also advised between the γcorrected power supply terminals (V_0, V_1, V_2, ……, V_9) and V_{SS}.

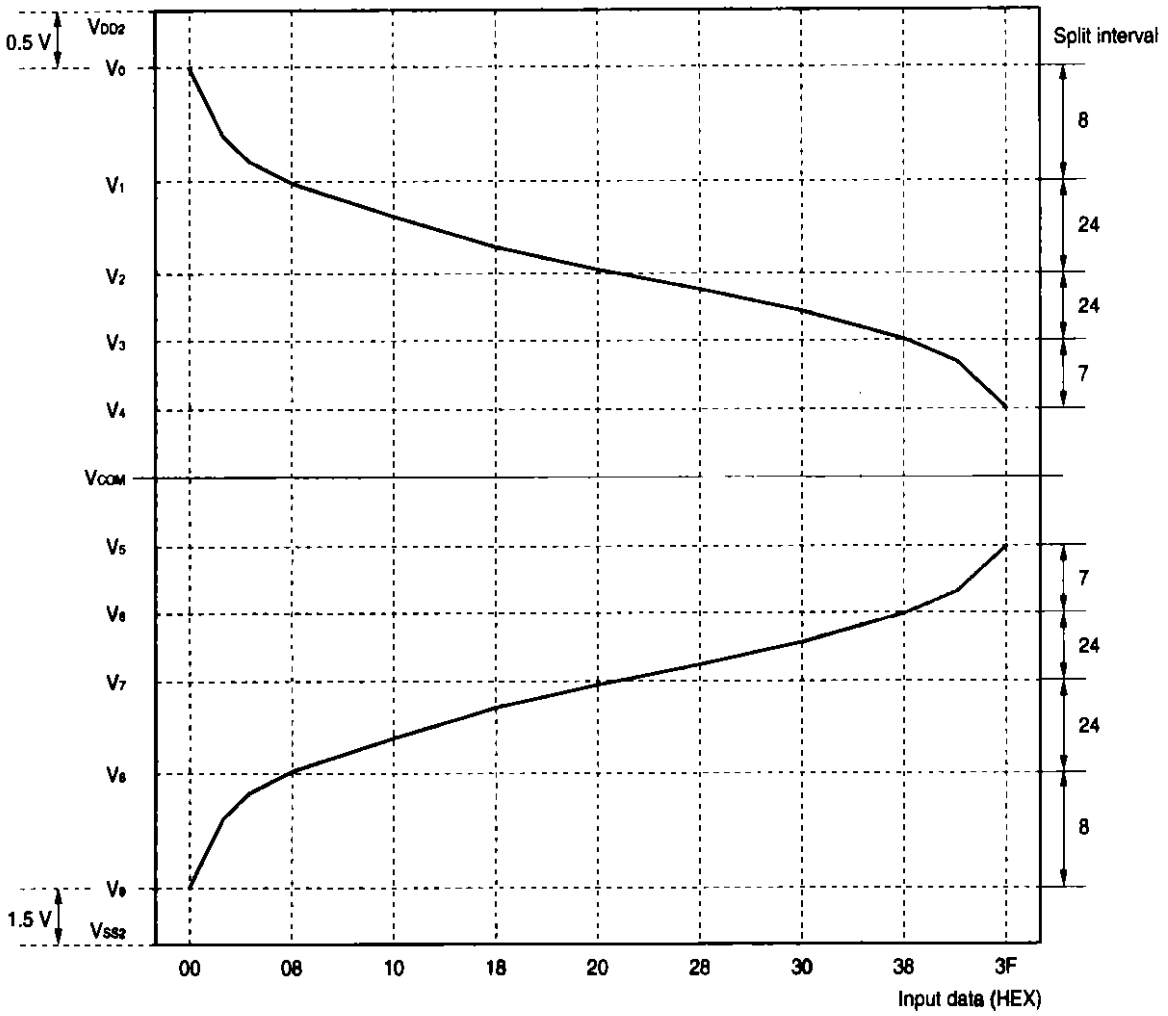
4. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches. The ladder resistors r_0 to r_{62} are so designed that the ratios between the LCD panel's γcorrected voltages and V_0' to V_{63}' and V_0'' to V_{63}'' are roughly equal; and their respective resistance values are as shown on page 8. Among the 5-by-2 γcorrected voltages, please input gray scale voltages of the same polarity with respect to the common voltage, for the respective five γcorrected voltages of V_0 to V_4 and V_5 to V_9. If fine gray scale voltage precision is not necessary, the voltage follower circuit supplied to the γcorrected power supplies V_1 to V_3 and V_6 to V_8 can be deleted.

Figure 1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γcorrected voltages V_0 to V_9 and the input data. Here, the voltage relationships have necessity to be set as $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$. Figures 2-1 and 2-2 show the relationship between the input data and the output data. Table 1 shows the resistance values of the resistor strings.

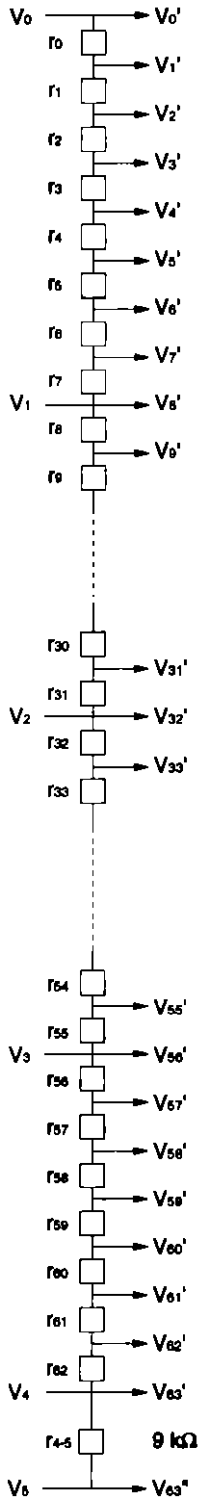
This driver IC is designed for single bank arrangement. Therefore, be sure not to use it for dual bank arrangement. The bias current flowing through ladder resistors r_0 to r_{62} is so small that its use for dual bank arangement impairs the IC's stable operation and causes display failures when the level of the γcorrected power supply terminal is inverted.

Figure 1. Relationship Between Input Data and Output Voltage



Resistor Strings

Figure 2-1. Relationship Between Input Data and Output Voltage: $V_{DD2} > V_0 > V_1 > V_2 > V_3 > V_4 > V_5$

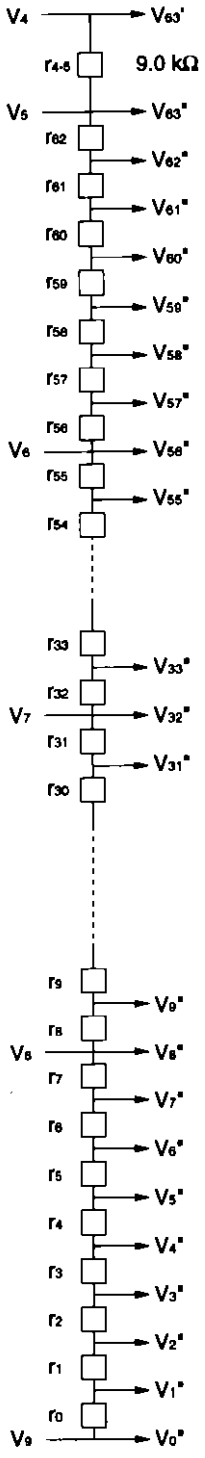


Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage	
00H	0	0	0	0	0	0	V_0'	V_0
01H	0	0	0	0	0	1	V_1'	$V_1 + (V_0 - V_1) \times$ 4500/5300
02H	0	0	0	0	1	0	V_2'	$V_1 + (V_0 - V_1) \times$ 3700/5300
03H	0	0	0	0	1	1	V_3'	$V_1 + (V_0 - V_1) \times$ 2900/5300
04H	0	0	0	1	0	0	V_4'	$V_1 + (V_0 - V_1) \times$ 2200/5300
05H	0	0	0	1	0	1	V_5'	$V_1 + (V_0 - V_1) \times$ 1500/5300
06H	0	0	0	1	1	0	V_6'	$V_1 + (V_0 - V_1) \times$ 900/5300
07H	0	0	0	1	1	1	V_7'	$V_1 + (V_0 - V_1) \times$ 400/5300
08H	0	0	1	0	0	0	V_8'	V_1
09H	0	0	1	0	0	1	V_9'	$V_2 + (V_1 - V_2) \times$ 3600/4000
0AH	0	0	1	0	1	0	V_{10}'	$V_2 + (V_1 - V_2) \times$ 3300/4000
0BH	0	0	1	0	1	1	V_{11}'	$V_2 + (V_1 - V_2) \times$ 3000/4000
0CH	0	0	1	1	0	0	V_{12}'	$V_2 + (V_1 - V_2) \times$ 2700/4000
0DH	0	0	1	1	0	1	V_{13}'	$V_2 + (V_1 - V_2) \times$ 2400/4000
0EH	0	0	1	1	1	0	V_{14}'	$V_2 + (V_1 - V_2) \times$ 2200/4000
0FH	0	0	1	1	1	1	V_{15}'	$V_2 + (V_1 - V_2) \times$ 2000/4000
10H	0	1	0	0	0	0	V_{16}'	$V_2 + (V_1 - V_2) \times$ 1800/4000
11H	0	1	0	0	0	1	V_{17}'	$V_2 + (V_1 - V_2) \times$ 1600/4000
12H	0	1	0	0	1	0	V_{18}'	$V_2 + (V_1 - V_2) \times$ 1400/4000
13H	0	1	0	0	1	1	V_{19}'	$V_2 + (V_1 - V_2) \times$ 1300/4000
14H	0	1	0	1	0	0	V_{20}'	$V_2 + (V_1 - V_2) \times$ 1200/4000
15H	0	1	0	1	0	1	V_{21}'	$V_2 + (V_1 - V_2) \times$ 1100/4000
16H	0	1	0	1	1	0	V_{22}'	$V_2 + (V_1 - V_2) \times$ 1000/4000
17H	0	1	0	1	1	1	V_{23}'	$V_2 + (V_1 - V_2) \times$ 900/4000
18H	0	1	1	0	0	0	V_{24}'	$V_2 + (V_1 - V_2) \times$ 800/4000
19H	0	1	1	0	0	1	V_{25}'	$V_2 + (V_1 - V_2) \times$ 700/4000
1AH	0	1	1	0	1	0	V_{26}'	$V_2 + (V_1 - V_2) \times$ 600/4000
1BH	0	1	1	0	1	1	V_{27}'	$V_2 + (V_1 - V_2) \times$ 500/4000
1CH	0	1	1	1	0	0	V_{28}'	$V_2 + (V_1 - V_2) \times$ 400/4000
1DH	0	1	1	1	0	1	V_{29}'	$V_2 + (V_1 - V_2) \times$ 300/4000
1EH	0	1	1	1	1	0	V_{30}'	$V_2 + (V_1 - V_2) \times$ 200/4000
1FH	0	1	1	1	1	1	V_{31}'	$V_2 + (V_1 - V_2) \times$ 100/4000
20H	1	0	0	0	0	0	V_{32}'	V_2
21H	1	0	0	0	0	1	V_{33}'	$V_3 + (V_2 - V_3) \times$ 2600/2700
22H	1	0	0	0	1	0	V_{34}'	$V_3 + (V_2 - V_3) \times$ 2500/2700
23H	1	0	0	0	1	1	V_{35}'	$V_3 + (V_2 - V_3) \times$ 2400/2700
24H	1	0	0	1	0	0	V_{36}'	$V_3 + (V_2 - V_3) \times$ 2300/2700
25H	1	0	0	1	0	1	V_{37}'	$V_3 + (V_2 - V_3) \times$ 2200/2700
26H	1	0	0	1	1	0	V_{38}'	$V_3 + (V_2 - V_3) \times$ 2100/2700
27H	1	0	0	1	1	1	V_{39}'	$V_3 + (V_2 - V_3) \times$ 2000/2700
28H	1	0	1	0	0	0	V_{40}'	$V_3 + (V_2 - V_3) \times$ 1900/2700
29H	1	0	1	0	0	1	V_{41}'	$V_3 + (V_2 - V_3) \times$ 1800/2700
2AH	1	0	1	0	1	0	V_{42}'	$V_3 + (V_2 - V_3) \times$ 1700/2700
2BH	1	0	1	0	1	1	V_{43}'	$V_3 + (V_2 - V_3) \times$ 1600/2700
2CH	1	0	1	1	0	0	V_{44}'	$V_3 + (V_2 - V_3) \times$ 1500/2700
2DH	1	0	1	1	0	1	V_{45}'	$V_3 + (V_2 - V_3) \times$ 1400/2700
2EH	1	0	1	1	1	0	V_{46}'	$V_3 + (V_2 - V_3) \times$ 1300/2700
2FH	1	0	1	1	1	1	V_{47}'	$V_3 + (V_2 - V_3) \times$ 1200/2700
30H	1	1	0	0	0	0	V_{48}'	$V_3 + (V_2 - V_3) \times$ 1100/2700
31H	1	1	0	0	0	1	V_{49}'	$V_3 + (V_2 - V_3) \times$ 1000/2700
32H	1	1	0	0	1	0	V_{50}'	$V_3 + (V_2 - V_3) \times$ 900/2700
33H	1	1	0	0	1	1	V_{51}'	$V_3 + (V_2 - V_3) \times$ 800/2700
34H	1	1	0	1	0	0	V_{52}'	$V_3 + (V_2 - V_3) \times$ 700/2700
35H	1	1	0	1	0	1	V_{53}'	$V_3 + (V_2 - V_3) \times$ 600/2700
36H	1	1	0	1	1	0	V_{54}'	$V_3 + (V_2 - V_3) \times$ 400/2700
37H	1	1	0	1	1	1	V_{55}'	$V_3 + (V_2 - V_3) \times$ 200/2700
38H	1	1	1	0	0	0	V_{56}'	V_3
39H	1	1	1	0	0	1	V_{57}'	$V_4 + (V_3 - V_4) \times$ 2300/2500
3AH	1	1	1	0	1	0	V_{58}'	$V_4 + (V_3 - V_4) \times$ 2100/2500
3BH	1	1	1	0	1	1	V_{59}'	$V_4 + (V_3 - V_4) \times$ 1800/2500
3CH	1	1	1	1	0	0	V_{60}'	$V_4 + (V_3 - V_4) \times$ 1500/2500
3DH	1	1	1	1	0	1	V_{61}'	$V_4 + (V_3 - V_4) \times$ 1200/2500
3EH	1	1	1	1	1	0	V_{62}'	$V_4 + (V_3 - V_4) \times$ 800/2500
3FH	1	1	1	1	1	1	V_{63}'	V_4

Caution V_4 and V_5 are interconnected inside the IC by resistors r_{4-5} (9.0 kΩ).

Resistor Strings

Figure 2-2. Relationship Between Input Data and Output Voltage: $V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$



Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage	
00H	0	0	0	0	0	0	V_0"	V_9
01H	0	0	0	0	0	1	V_1"	$V_9 + (V_8 - V_9) \times$ 800/5300
02H	0	0	0	0	1	0	V_2"	$V_9 + (V_8 - V_9) \times$ 1600/5300
03H	0	0	0	0	1	1	V_3"	$V_9 + (V_8 - V_9) \times$ 2400/5300
04H	0	0	0	1	0	0	V_4"	$V_9 + (V_8 - V_9) \times$ 3100/5300
05H	0	0	0	1	0	1	V_5"	$V_9 + (V_8 - V_9) \times$ 3800/5300
06H	0	0	0	1	1	0	V_6"	$V_9 + (V_8 - V_9) \times$ 4400/5300
07H	0	0	0	1	1	1	V_7"	$V_9 + (V_8 - V_9) \times$ 4900/5300
08H	0	0	1	0	0	0	V_8"	V_8
09H	0	0	1	0	0	1	V_9"	$V_8 + (V_7 - V_8) \times$ 400/4000
0AH	0	0	1	0	1	0	V_{10}"	$V_8 + (V_7 - V_8) \times$ 700/4000
0BH	0	0	1	0	1	1	V_{11}"	$V_8 + (V_7 - V_8) \times$ 1000/4000
0CH	0	0	1	1	0	0	V_{12}"	$V_8 + (V_7 - V_8) \times$ 1300/4000
0DH	0	0	1	1	0	1	V_{13}"	$V_8 + (V_7 - V_8) \times$ 1600/4000
0EH	0	0	1	1	1	0	V_{14}"	$V_8 + (V_7 - V_8) \times$ 1800/4000
0FH	0	0	1	1	1	1	V_{15}"	$V_8 + (V_7 - V_8) \times$ 2000/4000
10H	0	1	0	0	0	0	V_{16}"	$V_8 + (V_7 - V_8) \times$ 2200/4000
11H	0	1	0	0	0	1	V_{17}"	$V_8 + (V_7 - V_8) \times$ 2400/4000
12H	0	1	0	0	1	0	V_{18}"	$V_8 + (V_7 - V_8) \times$ 2600/4000
13H	0	1	0	0	1	1	V_{19}"	$V_8 + (V_7 - V_8) \times$ 2700/4000
14H	0	1	0	1	0	0	V_{20}"	$V_8 + (V_7 - V_8) \times$ 2800/4000
15H	0	1	0	1	0	1	V_{21}"	$V_8 + (V_7 - V_8) \times$ 2900/4000
16H	0	1	0	1	1	0	V_{22}"	$V_8 + (V_7 - V_8) \times$ 3000/4000
17H	0	1	0	1	1	1	V_{23}"	$V_8 + (V_7 - V_8) \times$ 3100/4000
18H	0	1	1	0	0	0	V_{24}"	$V_8 + (V_7 - V_8) \times$ 3200/4000
19H	0	1	1	0	0	1	V_{25}"	$V_8 + (V_7 - V_8) \times$ 3300/4000
1AH	0	1	1	0	1	0	V_{26}"	$V_8 + (V_7 - V_8) \times$ 3400/4000
1BH	0	1	1	0	1	1	V_{27}"	$V_8 + (V_7 - V_8) \times$ 3500/4000
1CH	0	1	1	1	0	0	V_{28}"	$V_8 + (V_7 - V_8) \times$ 3600/4000
1DH	0	1	1	1	0	1	V_{29}"	$V_8 + (V_7 - V_8) \times$ 3700/4000
1EH	0	1	1	1	1	0	V_{30}"	$V_8 + (V_7 - V_8) \times$ 3800/4000
1FH	0	1	1	1	1	1	V_{31}"	$V_8 + (V_7 - V_8) \times$ 3900/4000
20H	1	0	0	0	0	0	V_{32}"	V_7
21H	1	0	0	0	0	1	V_{33}"	$V_7 + (V_6 - V_7) \times$ 100/2700
22H	1	0	0	0	1	0	V_{34}"	$V_7 + (V_6 - V_7) \times$ 200/2700
23H	1	0	0	0	1	1	V_{35}"	$V_7 + (V_6 - V_7) \times$ 300/2700
24H	1	0	0	1	0	0	V_{36}"	$V_7 + (V_6 - V_7) \times$ 400/2700
25H	1	0	0	1	0	1	V_{37}"	$V_7 + (V_6 - V_7) \times$ 500/2700
26H	1	0	0	1	1	0	V_{38}"	$V_7 + (V_6 - V_7) \times$ 600/2700
27H	1	0	0	1	1	1	V_{39}"	$V_7 + (V_6 - V_7) \times$ 700/2700
28H	1	0	1	0	0	0	V_{40}"	$V_7 + (V_6 - V_7) \times$ 800/2700
29H	1	0	1	0	0	1	V_{41}"	$V_7 + (V_6 - V_7) \times$ 900/2700
2AH	1	0	1	0	1	0	V_{42}"	$V_7 + (V_6 - V_7) \times$ 1000/2700
2BH	1	0	1	0	1	1	V_{43}"	$V_7 + (V_6 - V_7) \times$ 1100/2700
2CH	1	0	1	1	0	0	V_{44}"	$V_7 + (V_6 - V_7) \times$ 1200/2700
2DH	1	0	1	1	0	1	V_{45}"	$V_7 + (V_6 - V_7) \times$ 1300/2700
2EH	1	0	1	1	1	0	V_{46}"	$V_7 + (V_6 - V_7) \times$ 1400/2700
2FH	1	0	1	1	1	1	V_{47}"	$V_7 + (V_6 - V_7) \times$ 1500/2700
30H	1	1	0	0	0	0	V_{48}"	$V_7 + (V_6 - V_7) \times$ 1600/2700
31H	1	1	0	0	0	1	V_{49}"	$V_7 + (V_6 - V_7) \times$ 1700/2700
32H	1	1	0	0	1	0	V_{50}"	$V_7 + (V_6 - V_7) \times$ 1800/2700
33H	1	1	0	0	1	1	V_{51}"	$V_7 + (V_6 - V_7) \times$ 1900/2700
34H	1	1	0	1	0	0	V_{52}"	$V_7 + (V_6 - V_7) \times$ 2000/2700
35H	1	1	0	1	0	1	V_{53}"	$V_7 + (V_6 - V_7) \times$ 2100/2700
36H	1	1	0	1	1	0	V_{54}"	$V_7 + (V_6 - V_7) \times$ 2300/2700
37H	1	1	0	1	1	1	V_{55}"	$V_7 + (V_6 - V_7) \times$ 2500/2700
38H	1	1	1	0	0	0	V_{56}"	V_6
39H	1	1	1	0	0	1	V_{57}"	$V_6 + (V_5 - V_6) \times$ 200/2500
3AH	1	1	1	0	1	0	V_{58}"	$V_6 + (V_5 - V_6) \times$ 400/2500
3BH	1	1	1	0	1	1	V_{59}"	$V_6 + (V_5 - V_6) \times$ 700/2500
3CH	1	1	1	1	0	0	V_{60}"	$V_6 + (V_5 - V_6) \times$ 1000/2500
3DH	1	1	1	1	0	1	V_{61}"	$V_6 + (V_5 - V_6) \times$ 1300/2500
3EH	1	1	1	1	1	0	V_{62}"	$V_6 + (V_5 - V_6) \times$ 1700/2500
3FH	1	1	1	1	1	1	V_{63}"	V_5

Caution V_4 and V_5 are interconnected inside the IC by resistors r_{4-5} (9.0 kΩ).

LADDER RESISTANCE VALUES (r_0 to r_{62})

Resistor Name	Resistance Value (Ω)	Resistor Name	Resistance Value (Ω)
r_0	800	r_{32}	100
r_1	800	r_{33}	100
r_2	800	r_{34}	100
r_3	700	r_{35}	100
r_4	700	r_{36}	100
r_5	600	r_{37}	100
r_6	500	r_{38}	100
r_7	400	r_{39}	100
r_8	400	r_{40}	100
r_9	300	r_{41}	100
r_{10}	300	r_{42}	100
r_{11}	300	r_{43}	100
r_{12}	300	r_{44}	100
r_{13}	200	r_{45}	100
r_{14}	200	r_{46}	100
r_{15}	200	r_{47}	100
r_{16}	200	r_{48}	100
r_{17}	200	r_{49}	100
r_{18}	100	r_{50}	100
r_{19}	100	r_{51}	100
r_{20}	100	r_{52}	100
r_{21}	100	r_{53}	200
r_{22}	100	r_{54}	200
r_{23}	100	r_{55}	200
r_{24}	100	r_{56}	200
r_{25}	100	r_{57}	200
r_{26}	100	r_{58}	300
r_{27}	100	r_{59}	300
r_{28}	100	r_{60}	300
r_{29}	100	r_{61}	400
r_{30}	100	r_{62}	800
r_{31}	100	Total	14500

V_0, V_9 → r_0 … r_{31} ← V_2, V_7

V_2, V_8 → r_7 … r_8

V_2, V_7 → r_{31}

V_3, V_6 → r_{55} … r_{56}

V_4, V_5 → r_{62}

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 1-pixel data (6 bits) by RGB (6 dots)
Input width : 36 bits

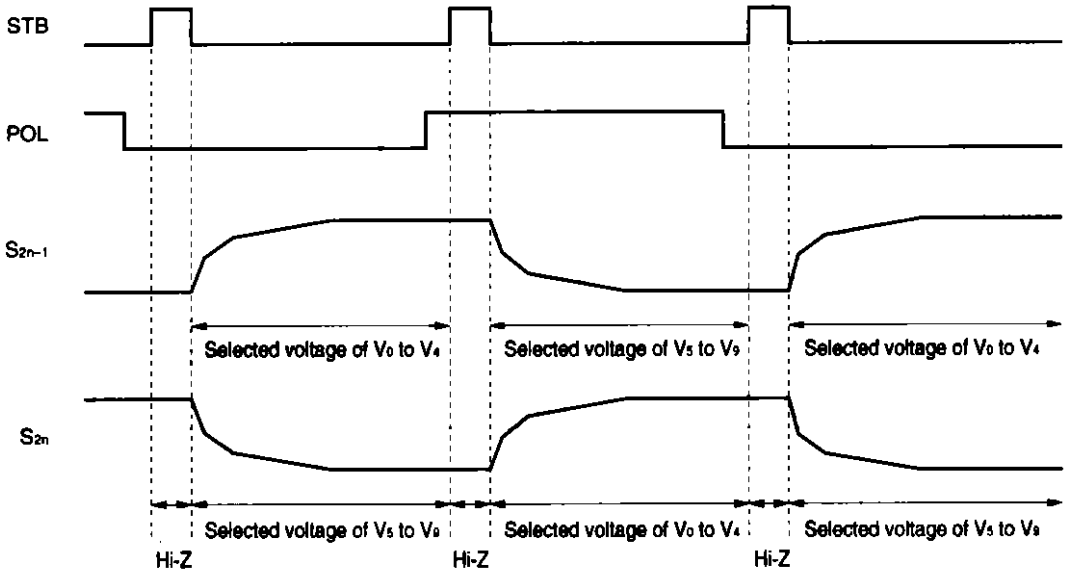
$R/\overline{L}$ = H (Right shift)

Output	S_1	S_2	S_3	···	S_{239}	S_{240}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	···	D_{40} to D_{45}	D_{05} to D_{55}

$R/\overline{L}$ = L (Left shift)

Output	S_1	S_2	S_3	···	S_{239}	S_{240}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	···	D_{40} to D_{45}	D_{05} to D_{55}

Relationship Between STB, POL, and Output Waveform



POL	S_{2nD1}	S_{2n}
L	V_0 to V_4	V_5 to V_9
H	V_5 to V_9	V_0 to V_4

S_{2nD1} (Odd output), S_{2n} (Even output) n = 1, 2, ···, 120

Absolute Maximum Ratings (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	−0.5 to +6.5	V
Driver Part Supply Voltage	V_{DD2}	−0.5 to +15.0	V
-Logic Part Input Voltage	V_{I1}	−0.5 to V_{DD1} + 0.5	V
Driver Part Input Voltage	V_{I2}	−0.5 to V_{DD2} + 0.5	V
Logic Part Output Voltage	V_{O1}	−0.5 to V_{DD1} + 0.5	V
Driver Part Output Voltage	V_{O2}	−0.5 to V_{DD2} + 0.5	V
Allowable Dissipation	P_D	150	mW
Operating Temperature	T_A	−10 to +75	°C
Storage Temperature	$T_{stg.}$	−55 to +125	°C

Recommended Operating Range (T_A = −10 to +75 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}	3.0	3.3	5.5	V
Driver Part Supply Voltage	V_{DD2}	11.0	13.0	13.5	V
High-Level Output Voltage	V_{IH}	0.8 V_{DD1}		V_{DD1}	V
Low-Level Output Voltage	V_{IL}	0		0.2 V_{DD1}	V
γCorrected Voltage	V_0 toV_9	V_{SS2} + 1.5		V_{DD2} - 0.5	V
Driver Part Output Voltage	V_O	V_{SS2} + 1.5		V_{DD2} - 0.5	V
Maximum Clock Frequency	$f_{max.}$	33			MHz

Electrical Specifications (T_A = −10 to +75 °C, V_{DD1} = 3.3 V $^{+2.2\ V}_{-0.3\ V}$, V_{DD2} = 13.0 V $^{+0.5\ V}_{-0.2\ V}$, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input Leak Current	I_L			−1.0		1.0	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), I_O = 0 mA		V_{DD1} − 0.1			V
Low-Level Output Voltage	V_{OL}	STHR (STHL), I_O = 0 mA				0.1	V
γCorrected Supply Current		V_0 − V_9 = 10 V	V_0, V_9			0.6	mA
Driver Output Current	I_{VOH}	V_X − V_{OUT} = 6 V				− 0.1	mA
	I_{VOL}	V_X − V_{OUT} = 6 V		0.1			mA

V_X refers to the output voltage of analog output pins S_1 to S_{240}.
V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{240}.

Electrical Specifications (T_A = −10 to +75 °C, V_{DD1} = 3.3 V $^{+2.2\ V}_{-0.3\ V}$, V_{DD2} = 13.0 V $^{+0.5\ V}_{-0.2\ V}$, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output Voltage Deviation[Note 1]	ΔVo	Input data: 00H to 3FH			±20	mV
Mean Output Voltage Variation[Note 2]	ΔVAV	Input data: 00H to 3FH		±10		mV
Output Voltage Range	Vo	Input data: 00H to 3FH	1.5		VDD2 − 0.5	V
Logic Part Dynamic Current Consumption	IDD1	VDD1; when with no load[Note 3, 4] 3.3 V		0.4	12.0	mA
Driver Part Dynamic Current Consumption	IDD2	VDD2; when with no load[Note 3, 4]		2.0	9.2	mA
Logic Part Static Current Consumption	IDD3	VDD1			10	μA
Driver Part Static Current Consumption	IDD4	VDD2		1.5	5.0	mA

Notes 1. The output voltage deviation refers to the voltage difference between adjoining output pins when the display data is the same (within the chip).

2. The mean output voltage variation refers to the mean output voltage difference between chips. The mean output voltage refers to the mean voltage between chips when the display data is the same.

3. The STB cycle is defined to be 30 μs at fCLK = 25 MHz.
The TYP. values refer to an all black or all white input pattern.
The MAX. value refers to the measured values in the dot checkerboard input pattern.

4. Refers to the current consumption per driver when cascades are connected under the assumption of VGA single-sided mounting (8 units).

Switching Characteristics (T_A = −10 to +75 °C, V_{DD1} = 3.3 V $^{+2.2\ V}_{-0.3\ V}$, V_{DD2} = 13.0 V $^{+0.5\ V}_{-0.2\ V}$, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	tPLH1	CL = 25 pF			15	ns
Driver Output Delay Time 1	tPHL2	CL = 50 pF, R = 50 kΩ			11	μs
Driver Output Delay Time 2	tPHL3	CL = 50 pF, R = 50 kΩ			17	μs
Driver Output Delay Time 3	tPLH2	CL = 50 pF, R = 50 kΩ			11	μs
Driver Output Delay Time 4	tPLH3	CL = 50 pF, R = 50 kΩ			17	μs
γCorrected Power Supply Capacitance	Cγ	TA = 25 °C		750		pF
Input Capacitance 1	C1	STHR, STHL excluded TA = 25 °C			18	pF
Input Capacitance 2	C2	STHR, STHL TA = 25 °C			20	pF

Timig Requirement (T_A = D10 to +75 °C, V_{DD1} = 3.3 V $^{+2.2\ V}_{-0.3\ V}$, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 12ns)

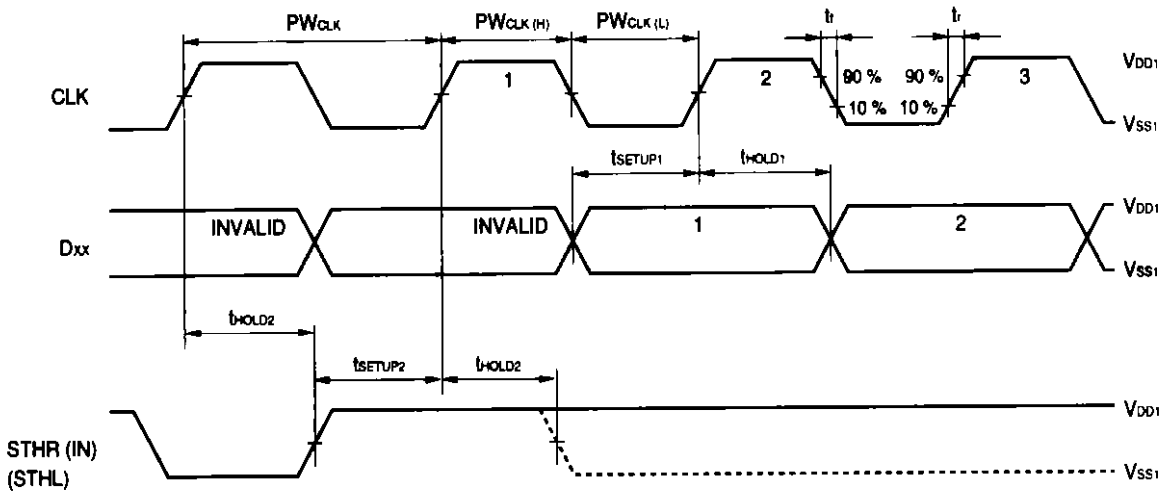
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		30			ns
Clock Pulse Low Period	$PW_{CLK\ (L)}$		6.0			ns
Clock Pulse High Period	$PW_{CLK\ (H)}$		6.0			ns
Data Setup Time	t_{SETUP1}		6.0			ns
Data Hold Time	t_{HOLD1}		6.0			ns
Start Pulse Setup Time	t_{SETUP2}		6.0			ns
Start Pulse Hold Time	t_{HOLD2}		6.0			ns
Start Pulse Low Period	t_{SPL}		6.0			ns
STB Pulse Width	PW_{STB}		200			ns
Data Invalid Period	t_{INV}		1			CLK
Final Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	CLK ↑→ STB ↓	6.0			ns
STB-CLK Time	$t_{STB-CLK}$	STB ↓→ CLK ↑	6.0			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	STB ↓→ STHR ↑	50			ns
POL-STB Time	$t_{POL-STB}$	POL ↑ or ↓ → STB ↑	−5.0			ns
STB-POL Time	$t_{STB-POL}$	STB ↓→ POL ↑ or ↓	6.0			ns

Switching Characteristics Waveform (R/$\overline{L}$ = H)

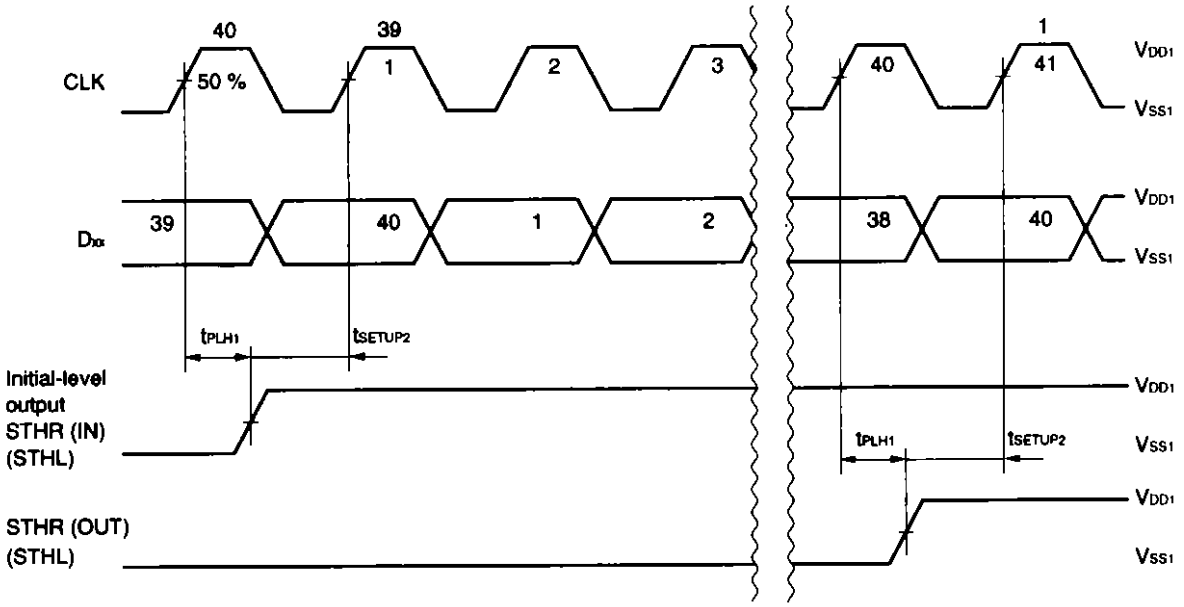
In ( ): R/$\overline{L}$ = L

Unless otherwise specified, the input level is defined to be 0.5 V_{DD1}.

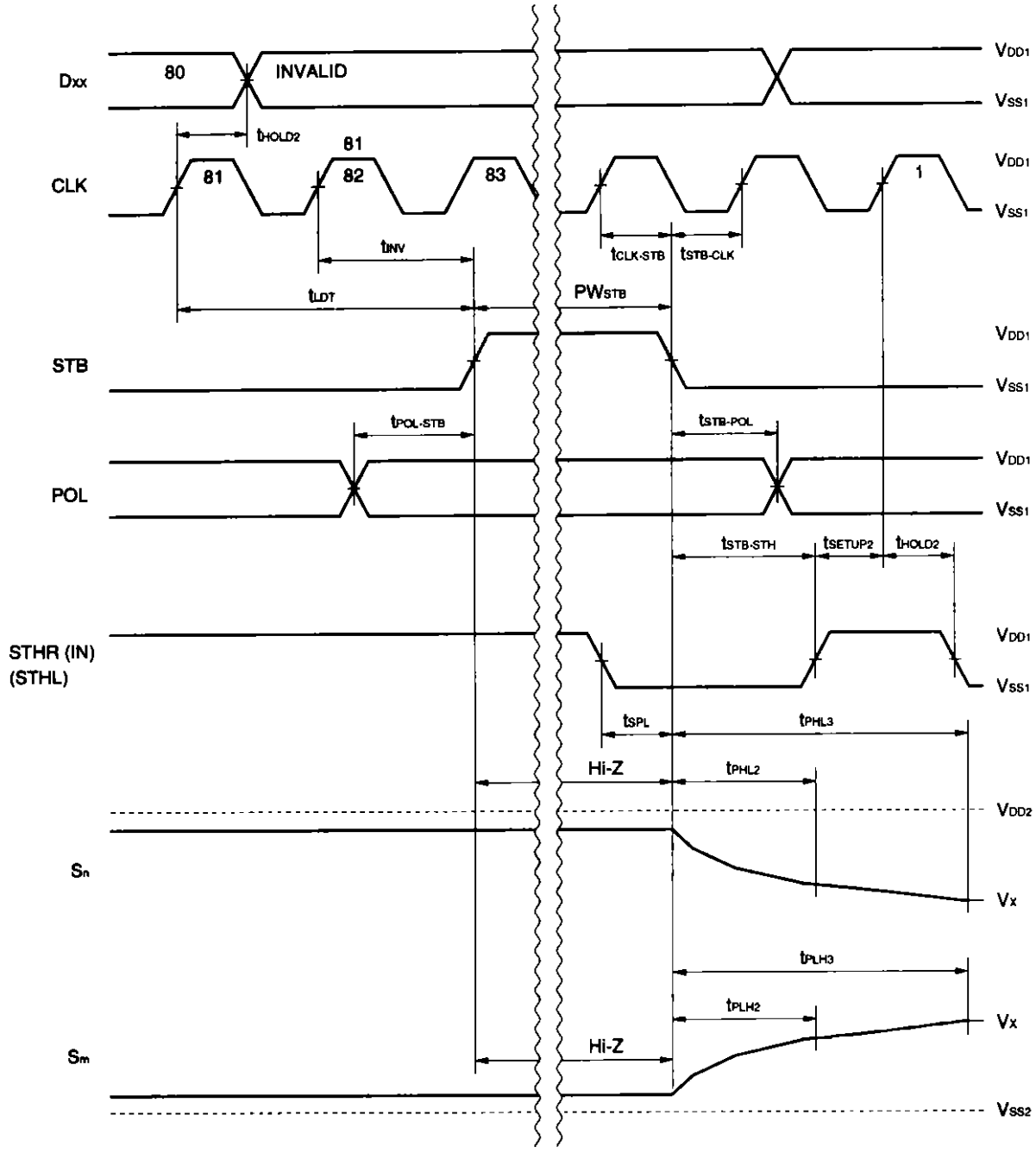
1. Initial-Stage Driver's Input/Output Waveform



2. Second- to Final-Stage Drivers's Input/Output Timing



3. DRIVER OUTPUT TIMING



Vx refers to the final output voltage, t_{PLH2}, t_{PHL2} refers to the time required to reach an output precision level of 10 % (0.1 Vx); and t_{PLH3}, t_{PHL3} refers to the time required to reach an output precision level of 6 bits.

RECOMMENDED MOUNTING CONDITIONS

The following mounting conditions for the μPD16631A are recommended.

For any other mounting conditions, consult NEC.

Mounting conditions	Mounting method	Conditions
Thermocompression	Soldering	Heating tool: 300 to 350 °C, time: 2 to 3 seconds, pressure: 100 g (per piece)
	ACF (sheet adhesive agent)	Preliminary adhesion: 70 to 100 °C, Pressure: 3 to 8 kg/cm², Time: 3 to 5 seconds Actual adhesion: 165 to 180 °C, Pressure: 25 to 45 kg/cm², Time: 30 to 40 seconds (with Sumitomo Bakelite's anisotropic film SUMIZAC1003)

Caution 1. For the mounting conditions for ACF, consult the ACF manufacturer before using the ACF.

2. Do not use two or more mounting methods in combination.

REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	IEI-1212
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	C10535E