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Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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MOS INTEGRATED CIRCUIT
μPD166100, 166101

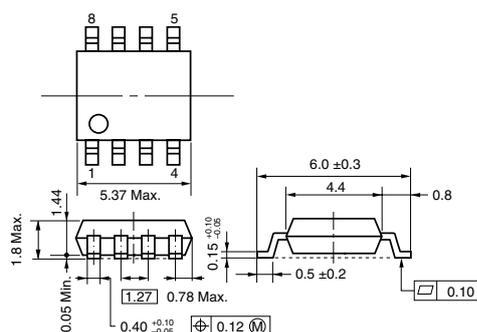
N-CHANNEL LOW SIDE INTELLIGENT POWER DEVICE

The μPD166100, 166101 are N-channel Low-side Driver for Solenoids and Lamp Drivers. It build in protection functions.

FEATURES

- Built in current limit and thermal shutdown circuit.
Thermal shutdown will automatically restart after the channel temperature has cool down.
- Low on-state resistance: $R_{DS(ON)} = 160\text{ m}\Omega$
($V_{IN} = 5\text{ V}$, $I_{OUT} = 0.8\text{ A}$, $T_{ch} = 25^\circ\text{C}$)
- Built in dynamic clamp circuit
- μPD166101: Dual channel Low-side switch
- Small and surface mount package
(Power SOP 8)

PACKAGE DRAWING (unit: mm)



<R> ORDERING INFORMATION

Part Number	Lead plating	Packing	Package
μPD166100GR-E1-AZ ^{Note}	Sn-Bi	Tape 2500 p/reel	Power SOP 8
μPD166100GR-E2-AZ ^{Note}	Sn-Bi	Tape 2500 p/reel	Power SOP 8
μPD166101GR-E1-AZ ^{Note}	Sn-Bi	Tape 2500 p/reel	Power SOP 8
μPD166101GR-E2-AZ ^{Note}	Sn-Bi	Tape 2500 p/reel	Power SOP 8

Note Pb-free (This product does not contain Pb in the external electrode.)

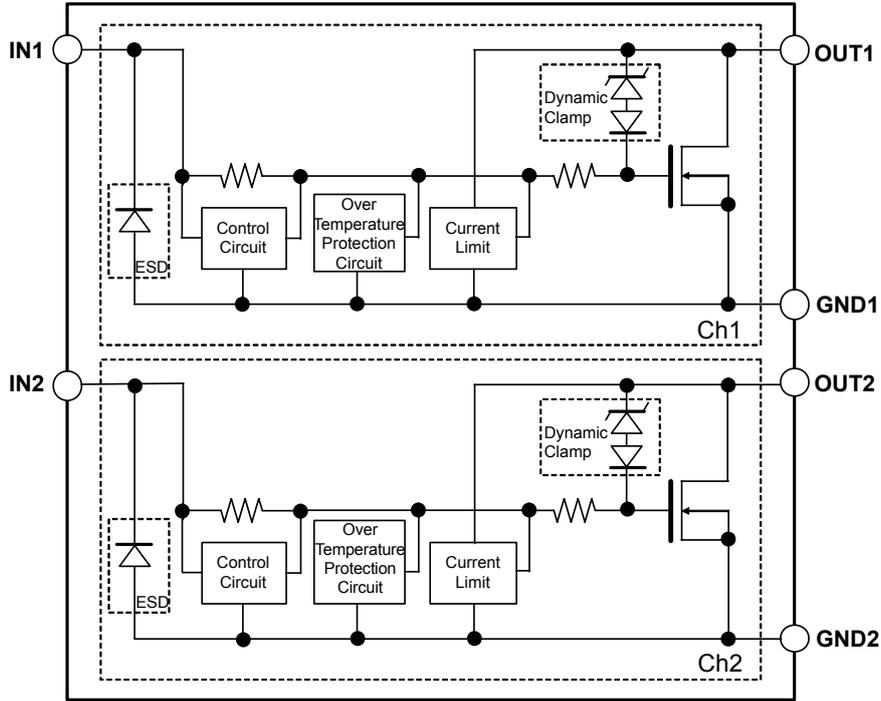
<R> QUALITY GRADE

Part Number	Quality Grade
μPD166100GR-E1-AZ	Special
μPD166100GR-E2-AZ	Special
μPD166101GR-E1-AZ	Special
μPD166101GR-E2-AZ	Special

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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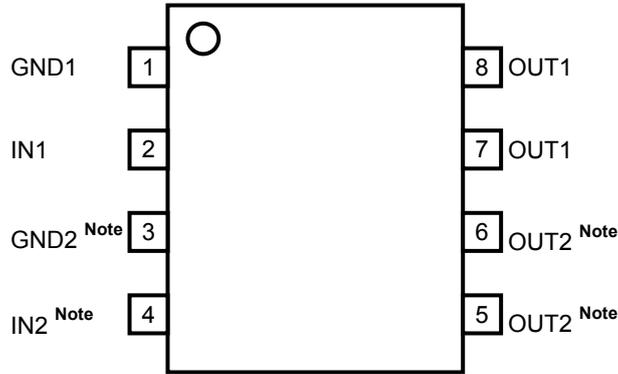
BLOCK DIAGRAM



Remark μPD166100: Ch1 only

PIN CONFIGURATION (Top View)

- Power SOP 8
μPD166100GR, μPD166101GR



Pin No.	Symbol	Function
1	GND1	Connected to Ground
2	IN1	Input terminal1 (active level is high)
3	GND2 ^{Note}	Connected to Ground
4	IN2 ^{Note}	Input terminal2 (active level is high)
5	OUT2 ^{Note}	Output terminal2
6	OUT2 ^{Note}	Output terminal2
7	OUT1	Output terminal1
8	OUT1	Output terminal1

Note μPD166100: Pin No.3 to 6 are N.C.

ABSOLUTE MAXIMUM RATING (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Rating	Unit	
Output voltage	V _{OUT}	V _{IN} = 0 V, DC	40	V	
Input voltage	V _{IN}		7	V	
Negative input current	I _{IL}		-10	mA	
Output current	I _{OUT(DC)}	V _{IN} = 5 V	SELF LIMITED	A/UNIT	
Total power dissipation	P _D ^{Note}	μ PD166100	On-State	1.5	W
		μ PD166101	2ch On-State	2	
Channel temperature	T _{ch}		150	°C	
Storage temperature	T _{stg}		-55 to +150	°C	

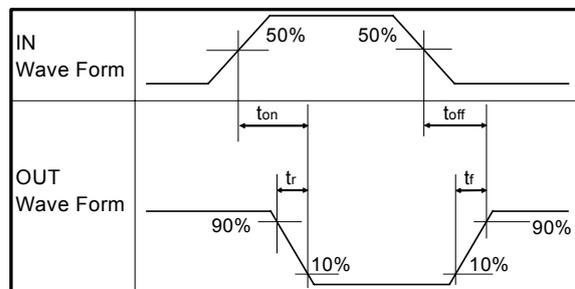
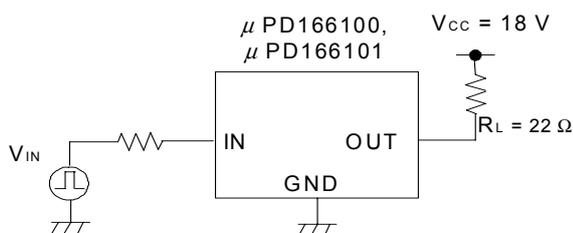
Note Mounted on ceramic substrate of 20 cm x 20 cm x 1.1 mm

ELECTRICAL CHARACTERISTICS (T_{ch} = 25°C unless otherwise specified)

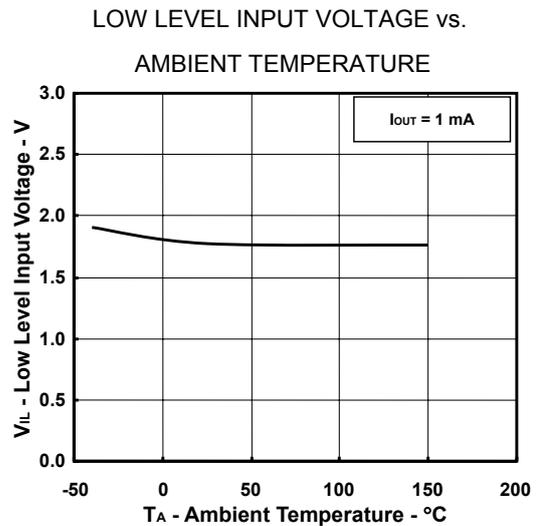
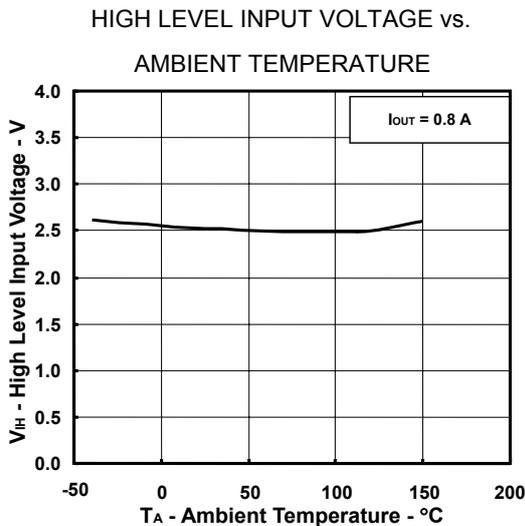
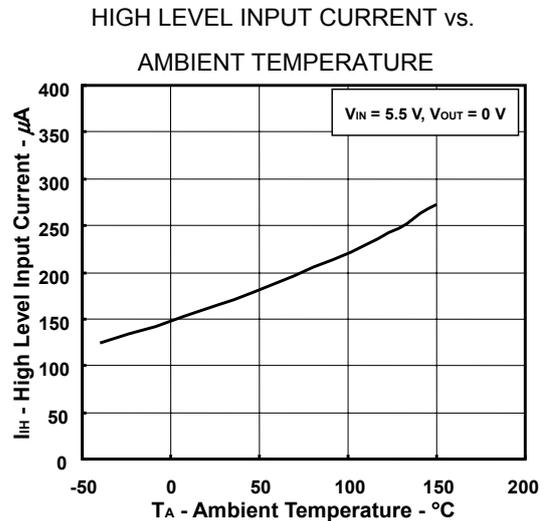
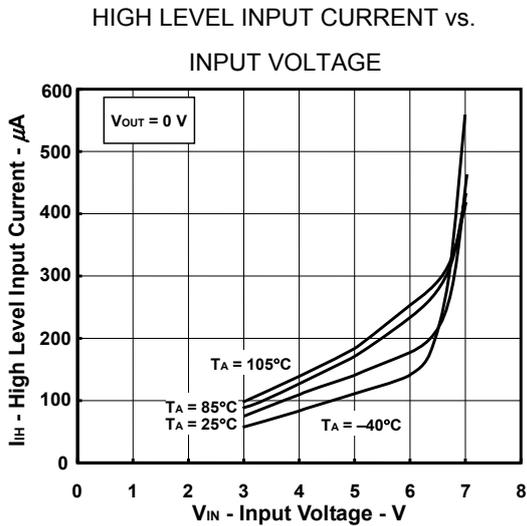
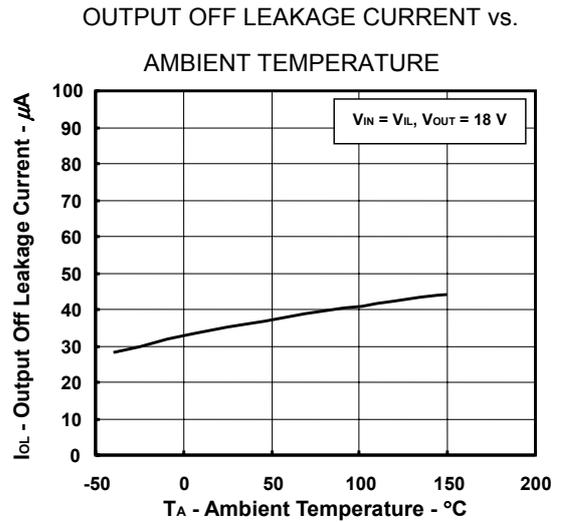
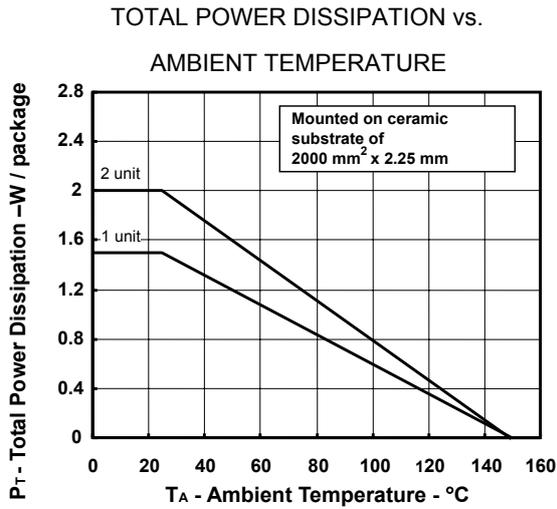
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output clamping voltage	V _{OUT}	I _{OUT} = 1 mA, V _{IN} = 0 V	40		60	V
Output Off leakage current	I _{OL}	V _{IN} = V _{IL} , V _{OUT} = 20 V			100	μA
High Level Input current	I _{IH}	V _{IN} = 5.5 V, V _{OUT} = 0 V			300	μA
Low Level Input current	I _{IL}	V _{IN} = 0 V, V _{OUT} = 20 V	-10		10	μA
High Level Input voltage	V _{IH}	I _{OUT} = 0.8 A, V _{OUT} = 0.2 V	3			V
Low Level Input voltage	V _{IL}	V _{OUT} = 10 V, I _{OUT} = 1 mA			1.5	V
ON-state resistance	R _{DS(ON)}	V _{IN} = 5 V, I _{OUT} = 0.8 A			160	mΩ
		V _{IN} = 3 V, I _{OUT} = 0.8 A			195	mΩ
Turn-on time	t _{on}	V _{CC} = 18 V, R _L = 22 Ω,			120	μs
Rise time	t _r	V _{IN} = 0 to 5 V,			80	μs
Turn-off time	t _{off}	R _{IN} = 10 Ω			200	μs
Fall time	t _f				80	μs
Thermal shutdown detection temperature ^{Note}	T _{HI}	V _{IN} = 5 V	150			°C
Current limit	I _S	V _{IN} = 3 V	1			A
Input frequency	f _{IN}				1	kHz

Note The low side switch is shutdown if the channel temperature exceeds thermal shutdown temperature. It will automatically restart after the channel temperature has cooled down than thermal shutdown temperature.

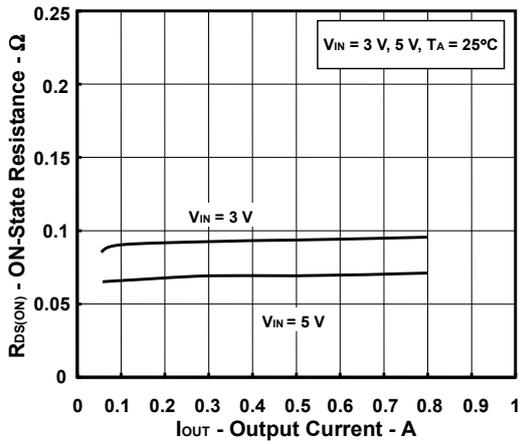
TEST CIRCUIT



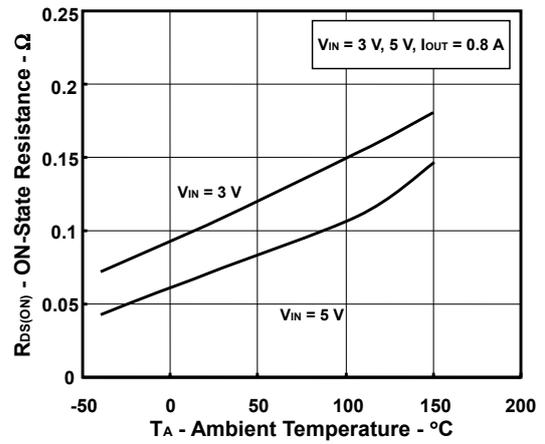
TYPICAL CHARACTERISTICS



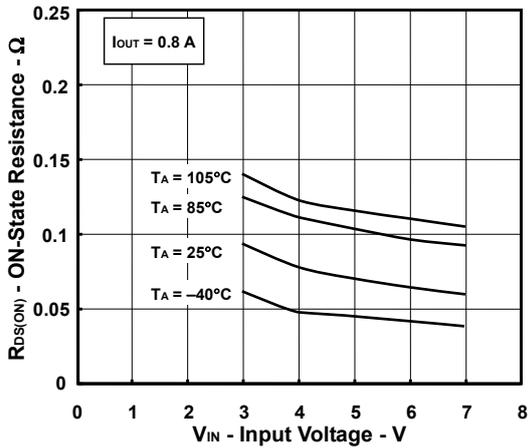
ON-STATE RESISTANCE vs.
OUTPUT CURRENT



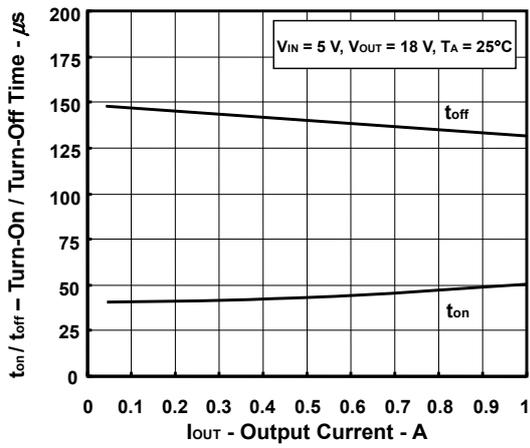
ON-STATE RESISTANCE vs.
AMBIENT TEMPERATURE



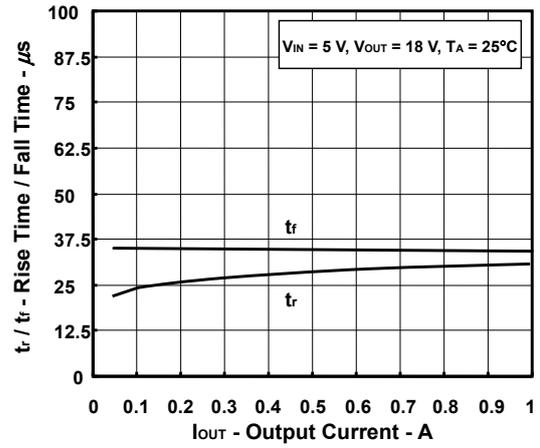
ON-STATE RESISTANCE vs.
INPUT VOLTAGE



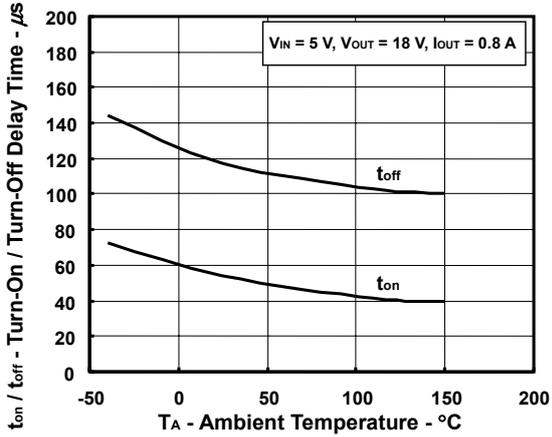
TURN-ON / TURN-OFF DELAY TIME vs.
OUTPUT CURRENT



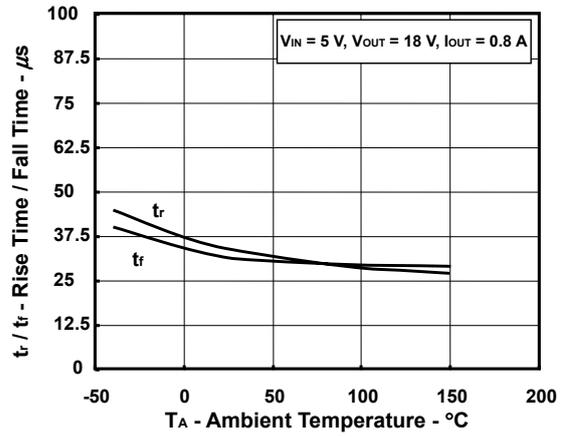
RISE TIME / FALL TIME vs.
OUTPUT CURRENT



TURN-ON / TURN-OFF DELAY TIME vs.
AMBIENT TEMPERATURE

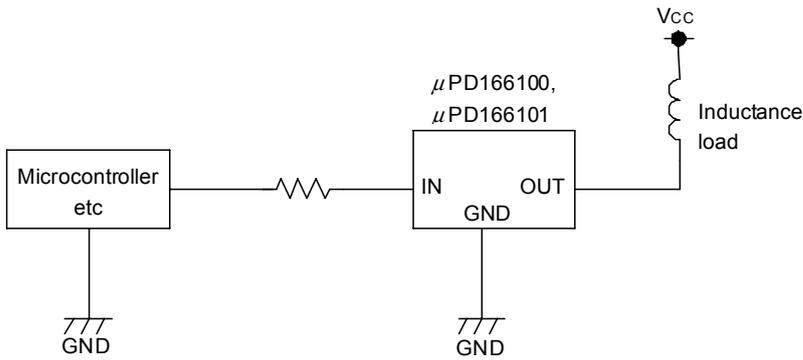


RISE TIME / FALL TIME vs.
AMBIENT TEMPERATURE

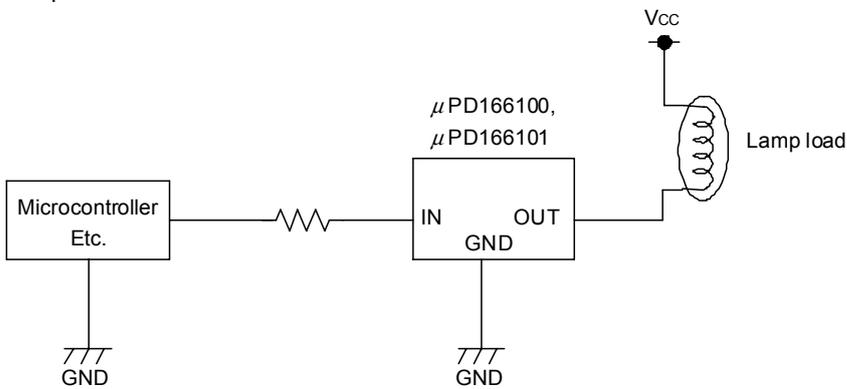


APPLICATION CIRCUIT EXAMPLE

(1) Inductance load



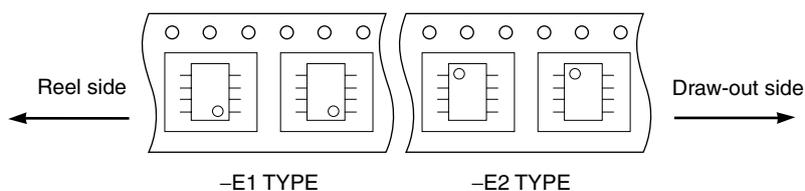
(2) Lamp load



Caution This circuit diagram is a connection example, and it is not the one to mass-produce it.

<R> TAPING INFORMATION

There are two types (E1, E2) of directions of the device in the career tape.

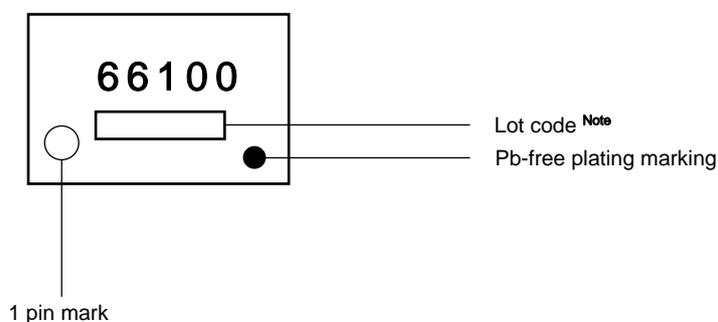


<R> MARKING INFORMATION

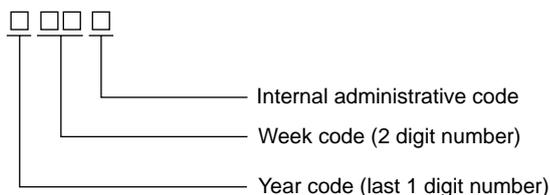
This figure indicates the marking items and arrangement. However, details of the letterform, the size and the position aren't indicated.

- μ PD166100GR, μ PD166101GR

Example) μ PD166100GR



Note Composition of the lot code



<R> **RECOMMENDED SOLDERING CONDITIONS**

The μPD166100, 166101 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

μ PD166100GR-E1-AZ ^{Note}, μ PD166100GR-E2-AZ ^{Note}: Power SOP 8

μ PD166101GR-E1-AZ ^{Note}, μ PD166101GR-E2-AZ ^{Note}: Power SOP 8

Process	Conditions	Symbol
Infrared Ray Reflow	Peak temperature: 235°C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210°C or higher), Maximum number of reflow processes: 3 times or less.	IR35-00-3
Partial Heating Method	Pin temperature: 350°C or below, Heat time: 3 seconds or less (Per each side of the device).	P350

Note Pb-free (This product does not contain Pb in the external electrode.)

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

Remark Flux: Rosin-based flux with low chlorine content (chlorine 0.2 Wt% or below) is recommended.

<R> REVISION HISTORY

Revision	Major changes since last version	Page
1 st edition	Released 1 st edition March 2005	
2 nd edition	Released 2 nd edition December 2008	
	Revised Ordering information	1
	Add Taping information, Marking information	8
	Revised Recommended soldering conditions	9
	Add Revision history	10

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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