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Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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96-Bit AC-PDP DRIVER

The μ PD16334 is a high-voltage CMOS driver designed for flat display panels such as PDPs, VFDs and ELs. It consists of a 96-bit bi-directional shift register, 96-bit latch and high-voltage CMOS driver. The logic block is designed to operate using a 5-V power supply/3.3-V interface enabling direct connection to a gate array or a microcontroller. In addition, the μ PD16334 achieves low power dissipation by employing the CMOS structure while having a high withstand voltage output (80 V, 50 mA).

FEATURES

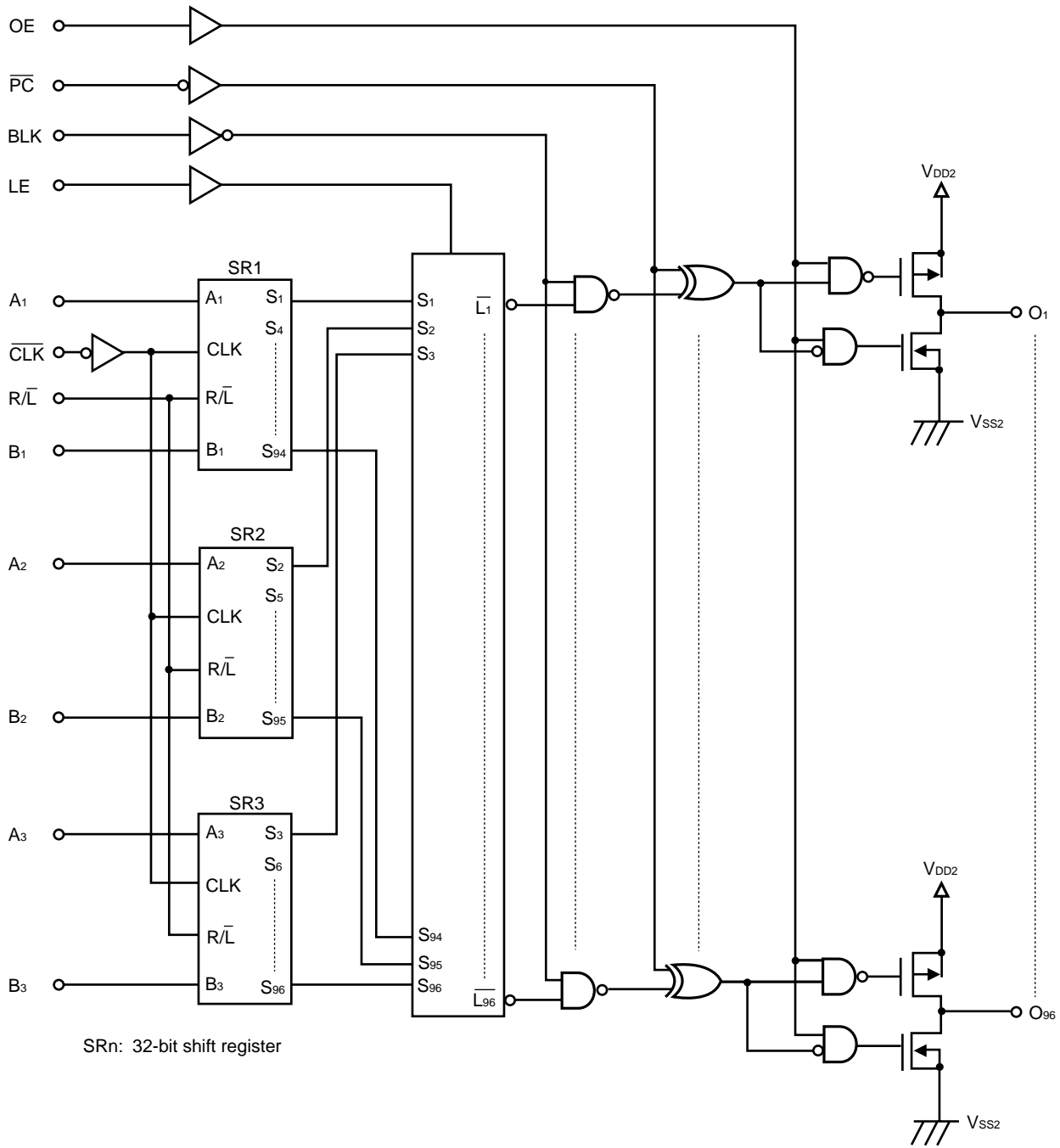
- Selectable by IBS pin; three 32-bit bi-directional shift register circuits configuration or six 16-bit bi-directional shift register circuits configuration
- Data control with transfer clock (external) and latch
- High-speed data transfer ($f_{max.} = 25$ MHz min. at data fetch)
($f_{max.} = 15$ MHz min. at cascade connection)
- High withstand output voltage (80 V, 50 mA_{MAX.})
- 3.3 V CMOS input interface
- High withstand voltage CMOS structure
- Capable of reversing all driver outputs by \overline{PC} pin

ORDERING INFORMATION

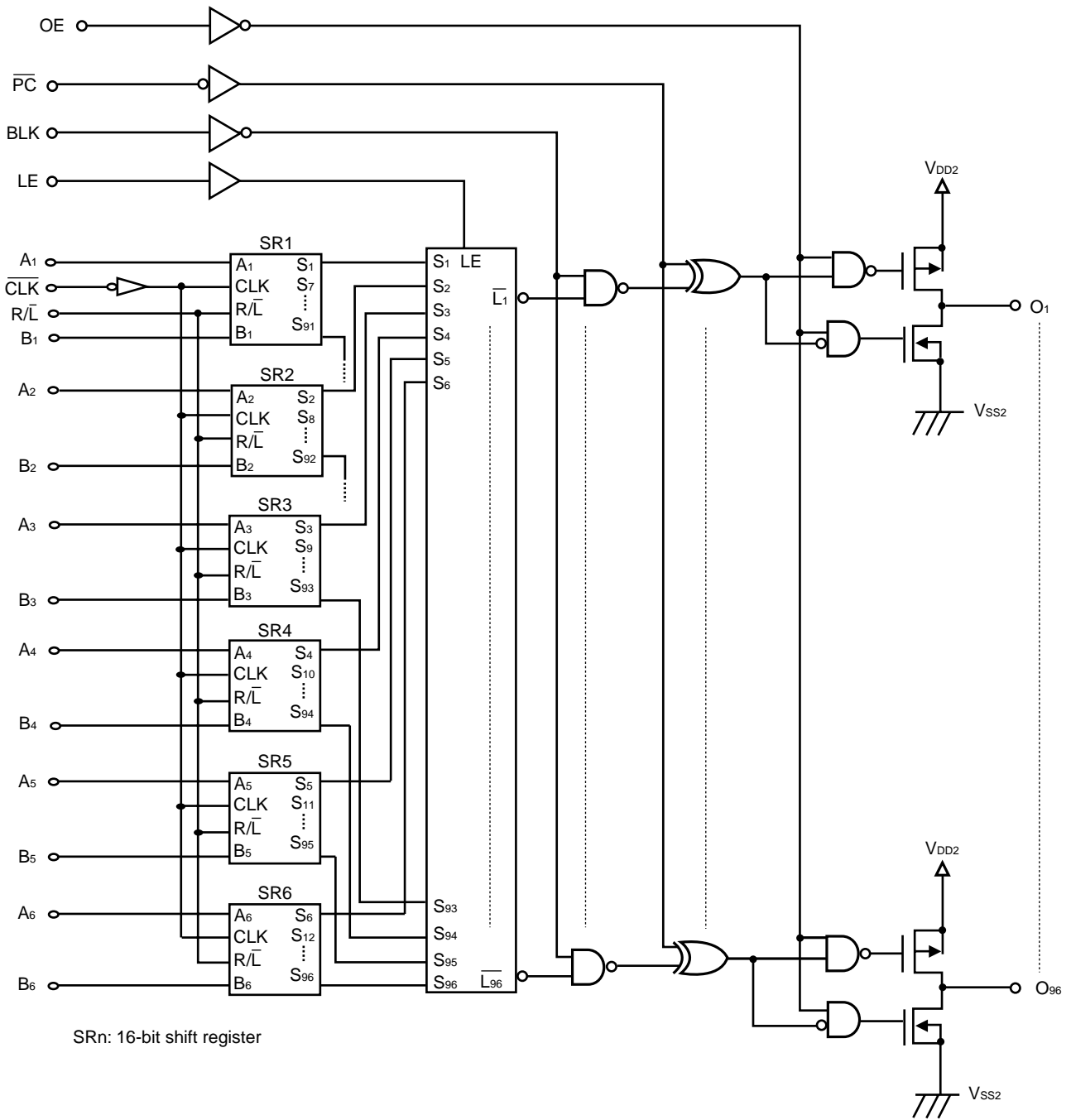
Part Number	Package
μ PD16334	COB*

* Please consult with an NEC sales representative about COB.

BLOCK DIAGRAM (IBS = H, 3-BIT INPUT, 32-BIT LENGTH SHIFT REGISTER)



BLOCK DIAGRAM (IBS = L, 6-BIT INPUT, 16-BIT LENGTH SHIFT REGISTER)



PIN DESCRIPTION

Symbol	Pin Name	Description
PC	Polarity change input	$\overline{PC} = L$: All driver output invert
BLK	Blank input	BLK = H : All output = H or L
LE	Latch enable input	Automatically executes latch by setting high at rising edge of the clock
OE	Output enable	Make output high impedance by input H
A ₁ to A ₃ (6)	RIGHT data input/output (Note)	When $R/\overline{L}=H$ (values in parentheses are for 6-bit input) A ₁ to A ₃ (6) : Input B ₁ to B ₃ (6) : Output
B ₁ to B ₃ (6)	LEFT data input/output (Note)	When $R/\overline{L}=L$ (values in parentheses are for 6-bit input) A ₁ to A ₃ (6) : Output B ₁ to B ₃ (6) : Input
CLK	Clock input	Shift executed on fall
R/ \overline{L}	Shift control input	Right shift mode when $R/\overline{L}= H$ SR ₁ : A ₁ → S ₁ ...S ₉₄ → B ₁ (Same direction for SR ₂ to SR ₆) Left shift mode when $R/\overline{L}= L$ SR ₁ : B ₁ → S ₉₄ ...S ₁ → A ₁ (Same direction for SR ₂ to SR ₆)
IBS	Input mode switch	H: 32-bit length shift register, 3-bit input L: 16-bit length shift register, 6-bit input
O ₁ to O ₉₆	High withstand voltage output	80 V, 50 mA _{MAX.}
V _{DD1}	Power supply for logic block	5 V ± 10 %
V _{DD2}	Power supply for driver block	10 to 70 V
V _{SS1}	Logic GND	Connect to system GND
V _{SS2}	Driver GND	Connect to system GND

Note When input mode is 3-bit, set unused input and output pins “L” level.

TRUTH TABLE 1 (Shift Register Block)

Input		Output		Shift Register
R/ \overline{L}	CLK	A	B	
H	↓	Input	Output ^{Note1}	Right shift execution
H	H or L		Output	Hold
L	↓	Output ^{Note2}	Input	Left shift execution
L	H or L	Output		Hold

Notes 1. The data of S₉₁ to S₉₃ (S₈₅ to S₉₀) shifts to S₉₄ to S₉₆ (S₉₁ to S₉₆) and is output from B₁ to B₃ (B₁ to B₆) at the falling edge of the clock, respectively. (Values in parentheses are for 6-bit input)

2. The data of S₄ to S₆ (S₇ to S₁₂) shifts to S₁ to S₃ (S₁ to S₆) and is output from A₁ to A₃ (A₁ to A₆) at the falling edge of the clock, respectively (Values in parentheses are for 6-bit input)

TRUTH TABLE 2 (Latch Block)

LE	CLK	Output State of Latch Block (\overline{L}_n)
H	↑	Latch S _n data and hold output data
	↓	Hold latch data
L	X	Hold latch data

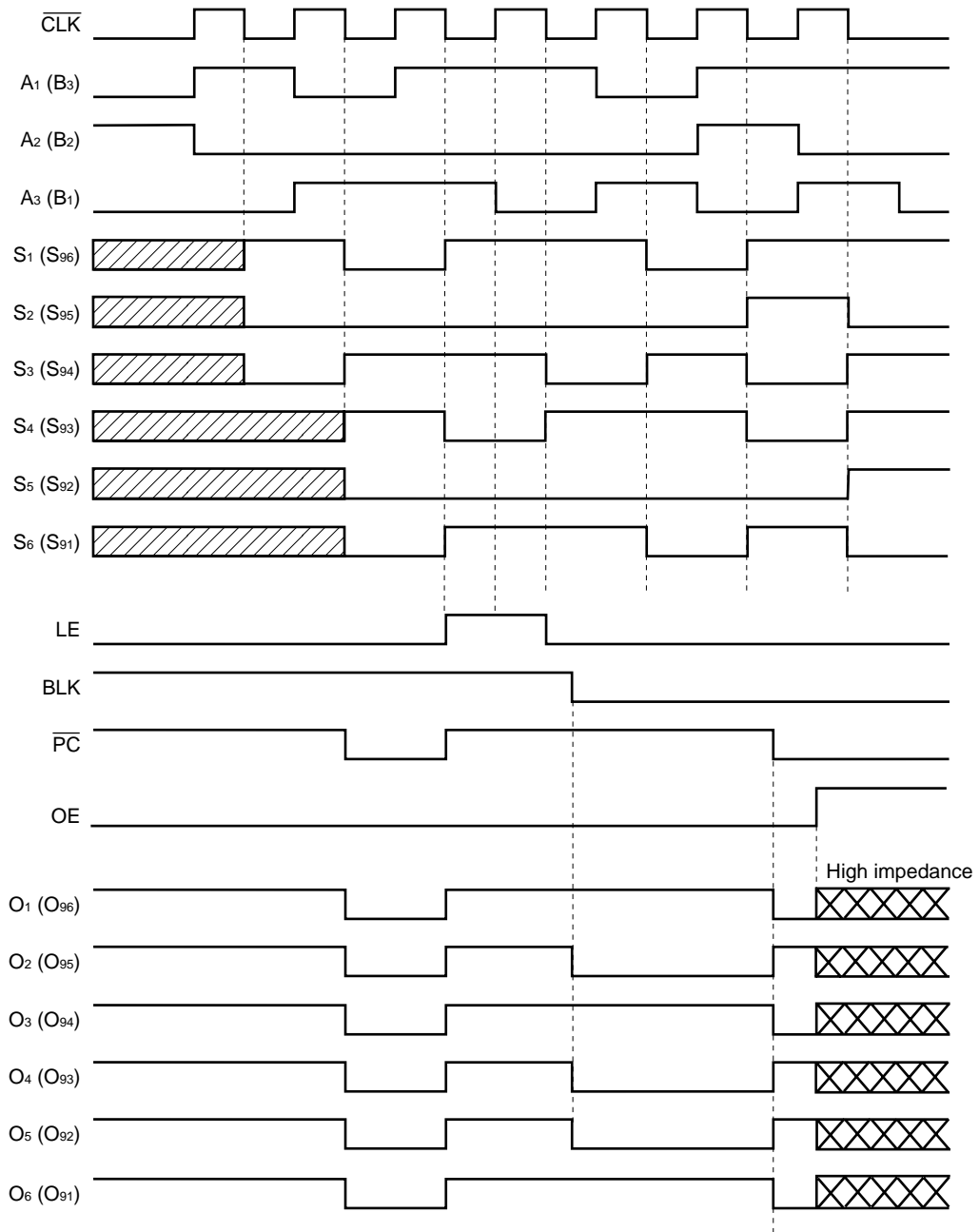
TRUTH TABLE 3 (Driver Block)

\overline{L}_n	BLK	PC	OE	Output State of Driver Block
X	H	H	L	H (All driver outputs: H)
X	H	L	L	L (All driver outputs: L)
X	L	H	L	Output latch data (\overline{L}_n)
X	L	L	L	Output inverted latch data (\overline{L}_n)
X	X	X	H	Set output impedance high

X: H or L, H: High level, L: Low level

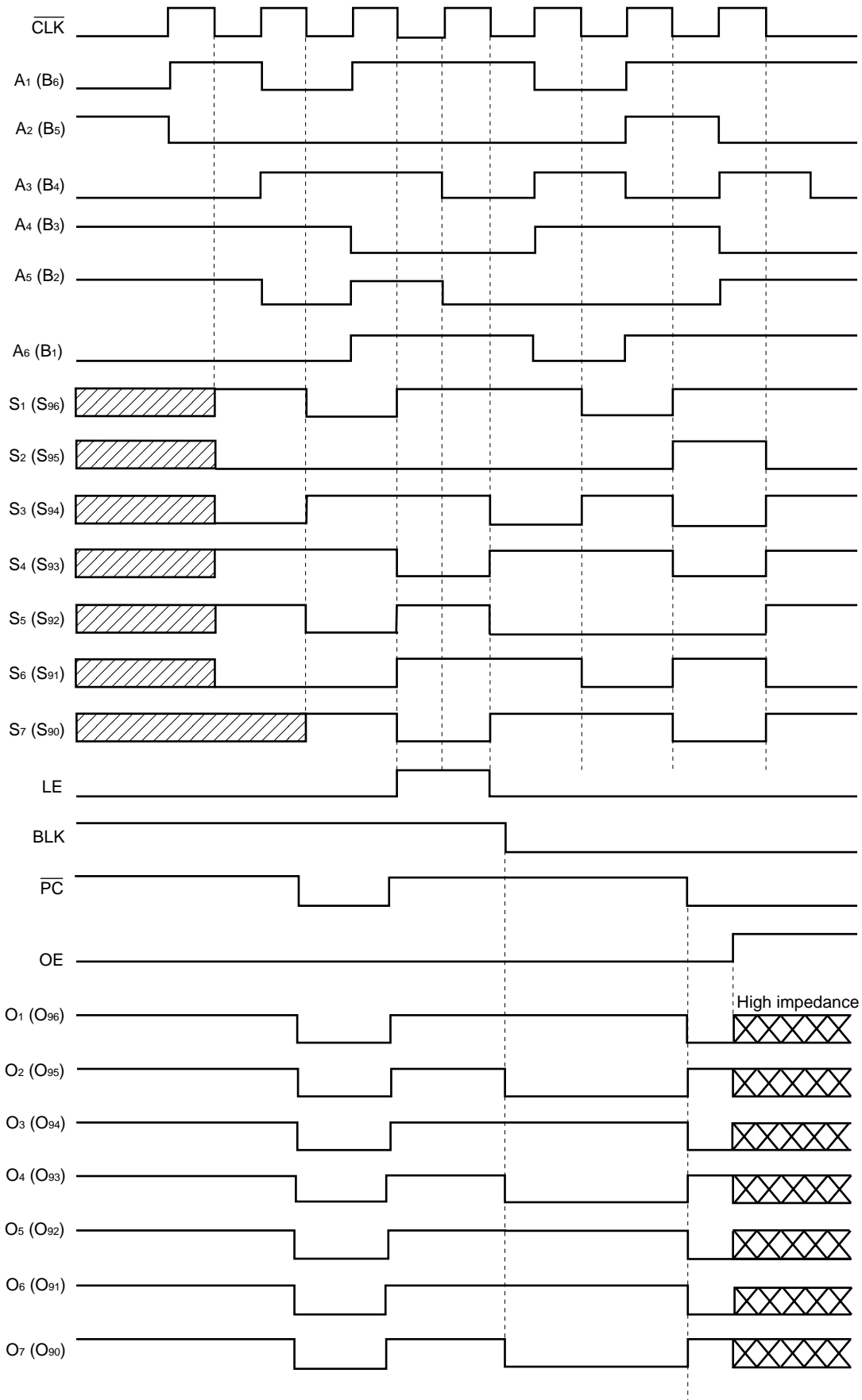
TIMING CHART (WHEN IBS="H": 3-BIT INPUT, RIGHT SHIFT)

Values in parentheses in the following chart are when R/L=L.



TIMING CHART (WHEN IBS="L": 6-BIT INPUT, RIGHT SHIFT)

Values in parentheses in the following chart are when R/L=L.



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic Block Supply Voltage	V _{DD1}	-0.5 to +7.0	V
Driver Block Supply Voltage	V _{DD2}	-0.5 to +80	V
Logic Block Input Voltage	V _I	-0.5 to V _{DD1} + 0.5	V
Driver Block Output Current	I _{O2}	50	mA
Junction Temperature	T _j	+125	°C
Storage Temperature	T _{stg.}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Block Supply Voltage	V _{DD1}	4.75	5.0	5.25	V
Driver Block Supply Voltage	V _{DD2}	10		70	V
High-Level Input Voltage	V _{IH}	2.7		V _{DD1}	V
Low-Level Input Voltage	V _{IL}	0		0.6	V
Driver Output Current	I _{OH2}			-40	mA
	I _{OL2}			+40	mA

Caution In order to prevent latch-up breakage, be sure to enter the power to V_{DD1}, logic signal and V_{DD2} in that order, and turn off the power in the reverse order, keep this order also during a transition period.

ELECTRICAL SPECIFICATIONS (T_A = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-Level Output Voltage	V _{OH1}	Logic, I _{OH1} = -1.0 mA	0.9 • V _{DD1}		V _{DD1}	V
Low-Level Output Voltage	V _{OL1}	Logic, I _{OL1} = 1.0 mA	0		0.1 V _{DD1}	V
High-Level Output Voltage	V _{OH21}	O ₁ to O ₉₆ , I _{OH2} = -1 mA	69			V
	V _{OH22}	O ₁ to O ₉₆ , I _{OH2} = -10 mA	65			V
Low-Level Output Voltage	V _{OL21}	O ₁ to O ₉₆ , I _{OL2} = 5 mA			1.0	V
	V _{OL22}	O ₁ to O ₉₆ , I _{OL2} = 40 mA			10	V
Input Leakage Current	I _{IL}	V _I = V _{DD1} or V _{SS1}			±1.0	μA
High-Level Input Voltage	V _{IH}	V _{DD1} = 4.75 to 5.25 V	2.7			V
Low-Level Input Voltage	V _{IL}	V _{DD1} = 4.75 to 5.25 V			0.6	V
Static Current Dissipation	I _{DD1}	Logic, T _A = -40 to +85 °C			10 ^{Note}	mA
	I _{DD1}	Logic, T _A = 25 °C			10 ^{Note}	mA
	I _{DD2}	Driver, T _A = -40 to +85 °C			1000	μA
	I _{DD2}	Driver, T _A = 25 °C			100	μA

Note When all inputs are high-level (V_{IH} = 2.7 V to V_{DD1}, the R/L and IBS pins are fixed to V_I = V_{SS1} or V_{DD1})

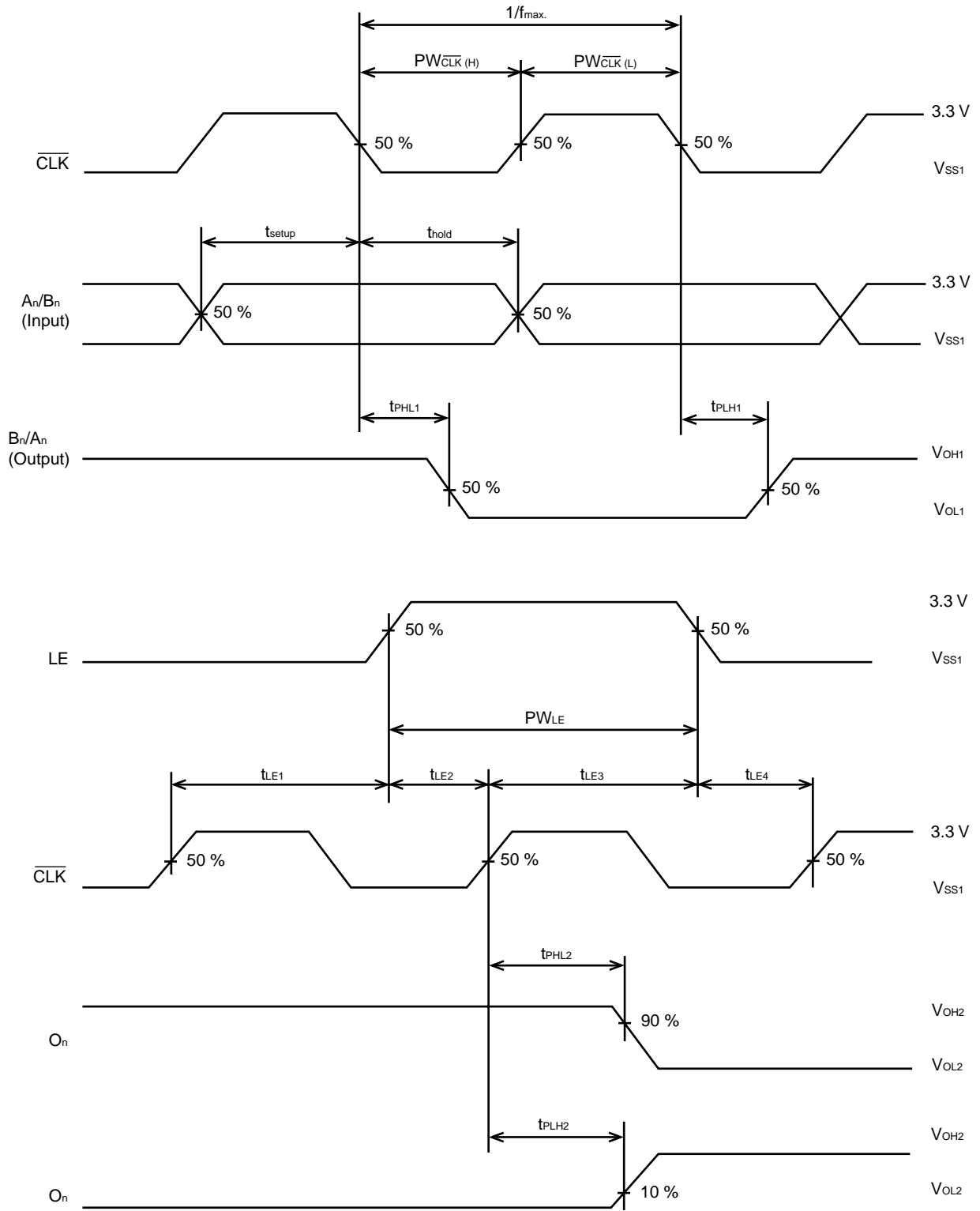
SWITCHING CHARACTERISTICS (T_A = 25 °C, V_{DD1} = 5 V, V_{DD2} = 70 V, V_{SS1} = V_{SS2} = 0 V, Logic C_L = 15 pF, Driver C_L = 50 pF, t_r = t_f = 6.0 ns)

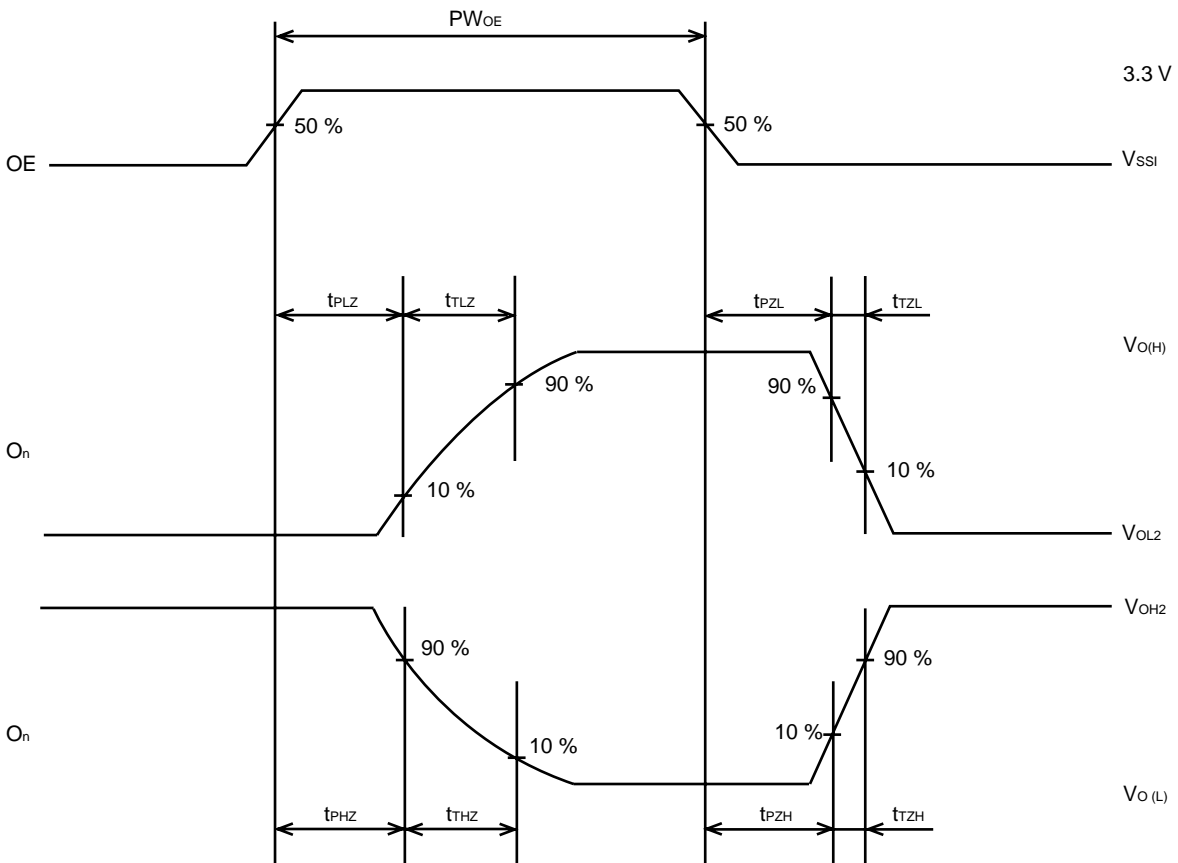
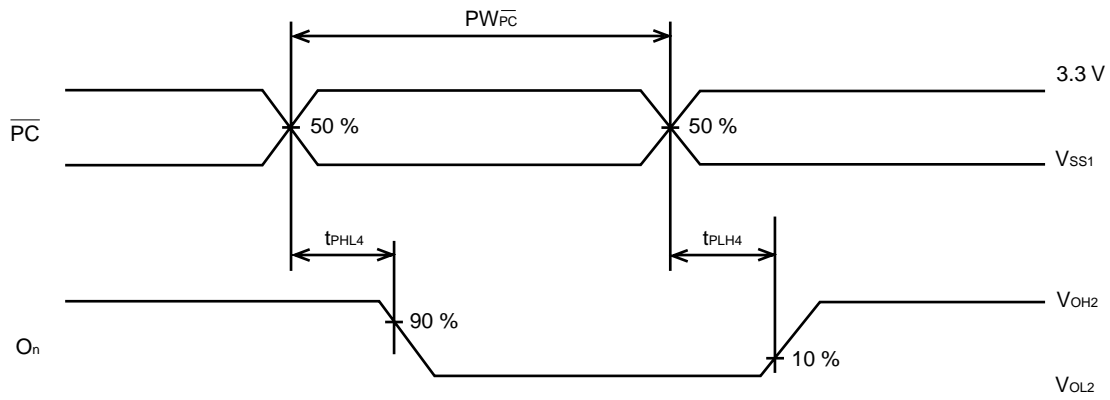
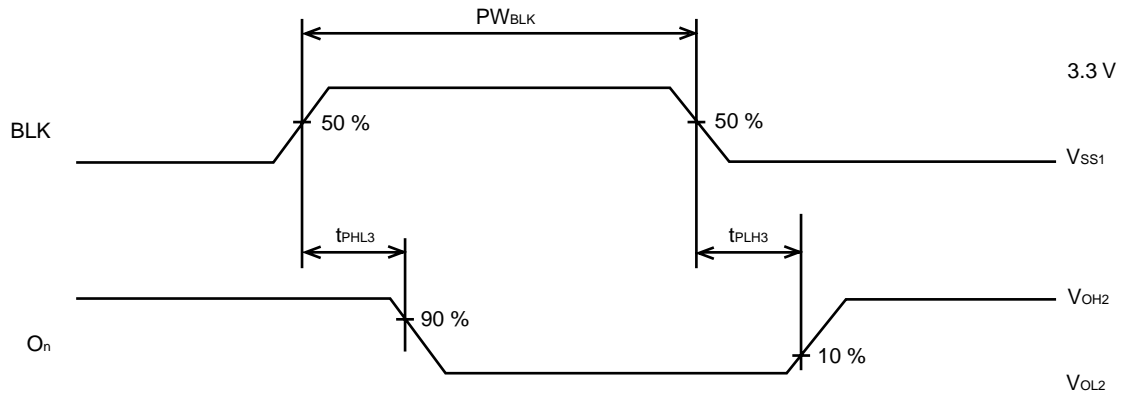
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transmission Delay time	t _{PHL1}	$\overline{\text{CLK}} \downarrow \rightarrow \text{A/B}$			55	ns
	t _{PLH1}				55	ns
	t _{PHL2}	$\overline{\text{CLK}} \uparrow (\text{LE} = \text{H}) \rightarrow \text{O}_1 \text{ to } \text{O}_{96}$			180	ns
	t _{PLH2}				180	ns
	t _{PHL3}	$\text{BLK} \rightarrow \text{O}_1 \text{ to } \text{O}_{96}$			165	ns
	t _{PLH3}				165	ns
	t _{PHL4}	$\overline{\text{PC}} \rightarrow \text{O}_1 \text{ to } \text{O}_{96}$			160	ns
	t _{PLH4}				160	ns
	t _{PHZ}	$\text{OE} \rightarrow \text{O}_1 \text{ to } \text{O}_{96}$			300	ns
	t _{PZH}	$\text{RL} = 10 \text{ k}\Omega$			180	ns
	t _{PLZ}				300	ns
	t _{PZL}				180	ns
Rise Time	t _{TLH}	$\text{O}_1 \text{ to } \text{O}_{96}$			150	ns
	t _{TLZ}	$\text{RL} = 10 \text{ k}\Omega$			3	μs
	t _{TZH}	$\text{O}_1 \text{ to } \text{O}_{96}$			150	ns
Fall Time	t _{THL}	$\text{O}_1 \text{ to } \text{O}_{96}$			150	ns
	t _{THZ}	$\text{RL} = 10 \text{ k}\Omega$			3	μs
	t _{TZL}	$\text{O}_1 \text{ to } \text{O}_{96}$			150	ns
Maximum Clock Frequency	f _{max.}	When data is read, duty 50 %	25			MHz
		cascade connection, Duty 50 %	15			MHz
Input Capacitance	C _i				15	pF

TIMING REQUIREMENT (T_A = -40 to +85 °C, V_{DD1} = 4.75 to 5.25 V, V_{SS1,2} = 0 V, t_r = t_f = 6.0 ns)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW _{$\overline{\text{CLK}}$}		20			ns
Latch Enable Pulse Width	PW _{LE}		30			ns
Blank Pulse Width	PW _{BLK}		200			ns
$\overline{\text{PC}}$ Pulse Width	PW _{$\overline{\text{PC}}$}		200			ns
OE Pulse Width	PW _{OE}	$\text{RL} = 10 \text{ k}\Omega$	3.3			μs
Data Setup Time	t _{setup}		10			ns
Data Hold Time	t _{hold}		10			ns
Latch Enable Time 1	t _{LE1}		25			ns
Latch Enable Time 2	t _{LE2}		5			ns
Latch Enable Time 3	t _{LE3}		25			ns
Latch Enable Time 4	t _{LE4}		5			ns

SWITCHING CHARACTERISTICS WAVEFORM





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