

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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64-BIT AC-PDP DRIVER

The μ PD16327 is a high breakdown voltage CMOS driver for flat display panels such as PDP, VFD and EL. It consists of 64-bit bidirectional shift registers (16 bits \times 4 circuits), a 64-bit latch, and a high breakdown voltage CMOS driver. The logic block operates on a 5 V power supply, designed to be connected directly to a microcomputer (CMOS level input). The driver block comprises 100 V, 40 mA $_{MAX}$. high breakdown voltage output, and both the logic block and driver block consist of CMOS, allowing operation with low power consumption.

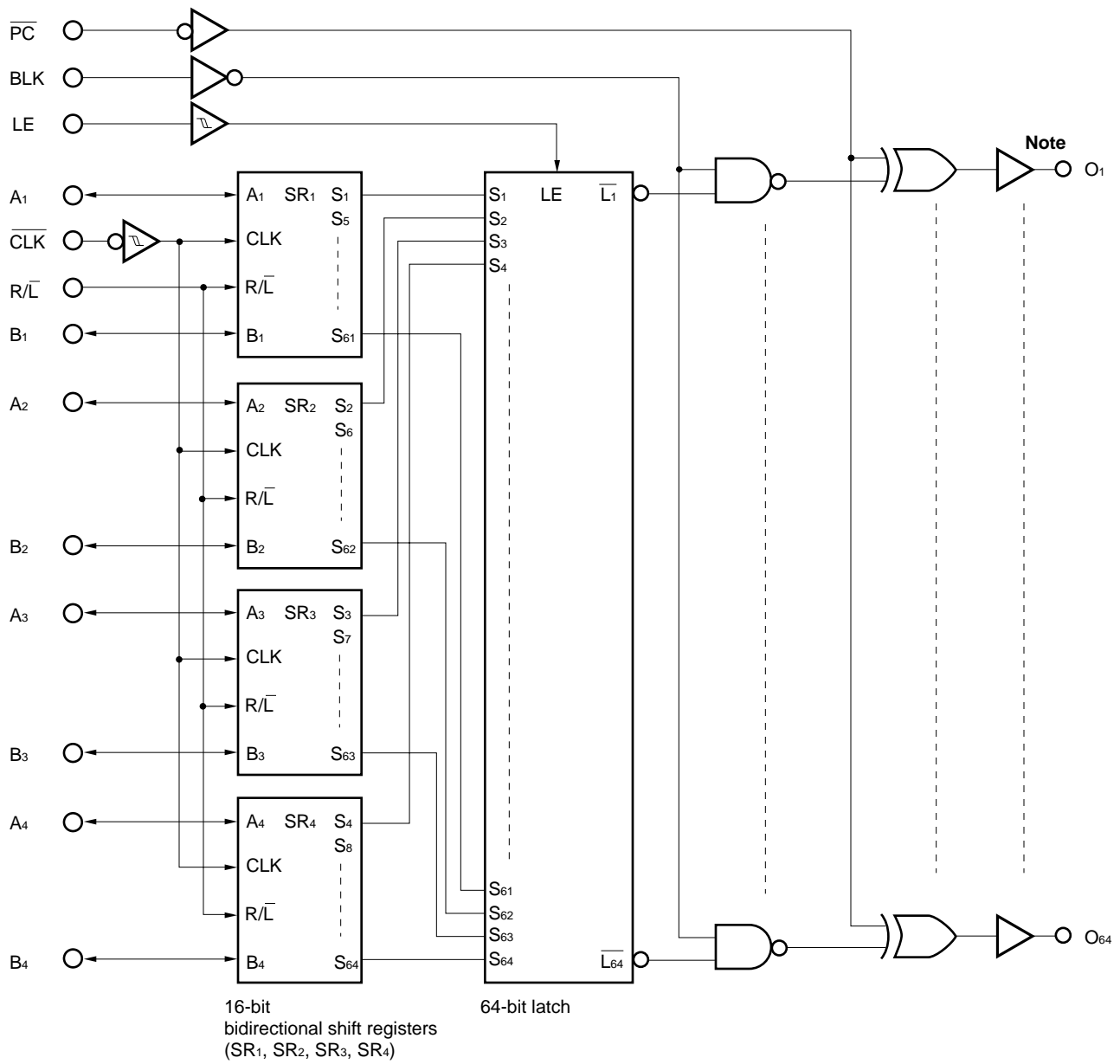
FEATURES

- 4 circuits of 16-bit bidirectional shift registers on chip
- Data control by transfer lock (external) and latch
- High-speed data transfer capability ($f_{max.} = 20$ MHz $_{MIN.}$: With cascading)
- Wide operating temperature range ($T_A = -40$ to 85 °C)
- High breakdown voltage (100 V, 40 mA $_{MAX.}$)
- High breakdown voltage CMOS structure
- \overline{PC} pin allows polarity of all driver outputs to be inverted.

ORDERING INFORMATION

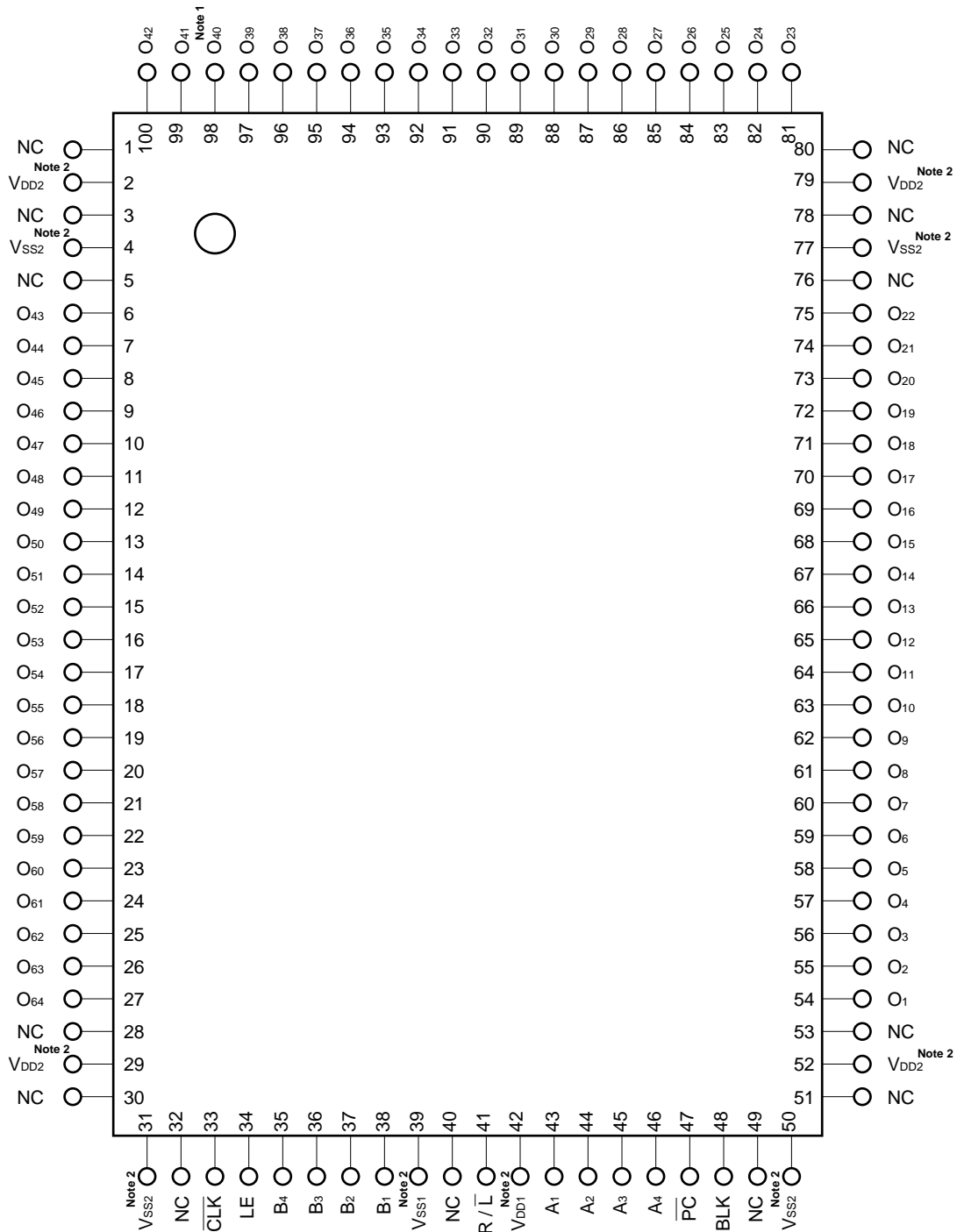
Part Number	Package
μ PD16327GF-3BA	100-pin plastic QFP

BLOCK DIAGRAM



Note High breakdown voltage CMOS driver 100 V ± 40 mA MAX.

PIN CONFIGURATION (Top View)



- Notes**
1. Be sure to use all pins V_{DD1} , V_{DD2} , V_{SS1} and V_{SS2} . Use V_{SS1} and V_{SS2} at the same potential.
 2. Pin 40 is connected to the lead frame, and therefore be sure to leave it open.

Remark In order to prevent latch-up breakage, be sure to enter the power to V_{DD1} , logic signal, and V_{DD2} , in that order, and turn off the power in the reverse order. Keep this order also during a transition period.

PIN DESCRIPTION

Pin Symbol	Pin Name	Pin Number	Description
\overline{PC}	Polarity inverted input	47	$\overline{PC} = L$: Polarity of all outputs inverted
BLK	Blanking input	48	BLK = H: All outputs = H or L
LE	Latch enable input	34	Latch is automatically executed by being driven high upon a clock rise.
A ₁ to A ₄	RIGHT data input/output	43-46	When $R/\overline{L} = H$, A ₁ to A ₄ : Input B ₁ to B ₄ : Output
B ₁ to B ₄	LEFT data input/output	38-35	When $R/\overline{L} = L$, A ₁ to A ₄ : Output B ₁ to B ₄ : Input
\overline{CLK}	Clock input	33	Shift is executed on a fall.
R/\overline{L}	Shift control input	41	H: Right shift mode SR ₁ : A ₁ → S ₁ ... S ₆₁ → B ₁ (SR ₂ , SR ₃ , SR ₄ also same direction) L: Left shift mode SR ₁ : B ₁ → S ₆₁ ... S ₁ → A ₁ (SR ₂ , SR ₃ , SR ₄ also same direction)
O ₁ to O ₆₄	High breakdown voltage output	54-75, 82-99, 5-28	100 V, 40 mA MAX.
V _{DD1}	Logic block power supply	42	5 V ± 10 %
V _{DD2}	Driver block power supply	2, 30, 51, 79	30 to 150 V
V _{SS1}	Logic ground	39	Connected to system GND
V _{SS2}	Driver ground	4, 32, 49, 77	Connected to system GND
NC	Free pins	1, 3, 5, 29, 31, 40 50, 52, 76, 78, 80 81, 100	Non-connection Be sure to leave pin 40 open.

TRUTH TABLE 1 (SHIFT REGISTER BLOCK)

Input		Output		Shift Register
R/ \overline{L}	\overline{CLK}	A	B	
H	↓	Input	Output ^{Note 1}	Execution of right shift
H	H or L		Output	Retained
L	↓	Output ^{Note 2}	Input	Execution of left shift
L	H or L	Output		Retained

Notes 1. On a clock fall, the data items of S₅₇, S₅₈, S₅₉ and S₆₀ are shifted to S₆₁, S₆₂, S₆₃ and S₆₄, and output from B₆₁, B₆₂, B₆₃ and B₆₄, respectively.

2. On a clock fall, the data items of S₅, S₆, S₇ and S₈ are shifted to S₁, S₂, S₃ and S₄, and output from A₁, A₂, A₃ and A₄, respectively.

TRUTH TABLE 2 (LATCH BLOCK)

LE	$\overline{\text{CLK}}$	Output state of latch block ($\overline{\text{L}}_n$)
H	↑	Latches S_n data and retains output data.
	↓	Retains latch data.
L	×	Retains latch data.

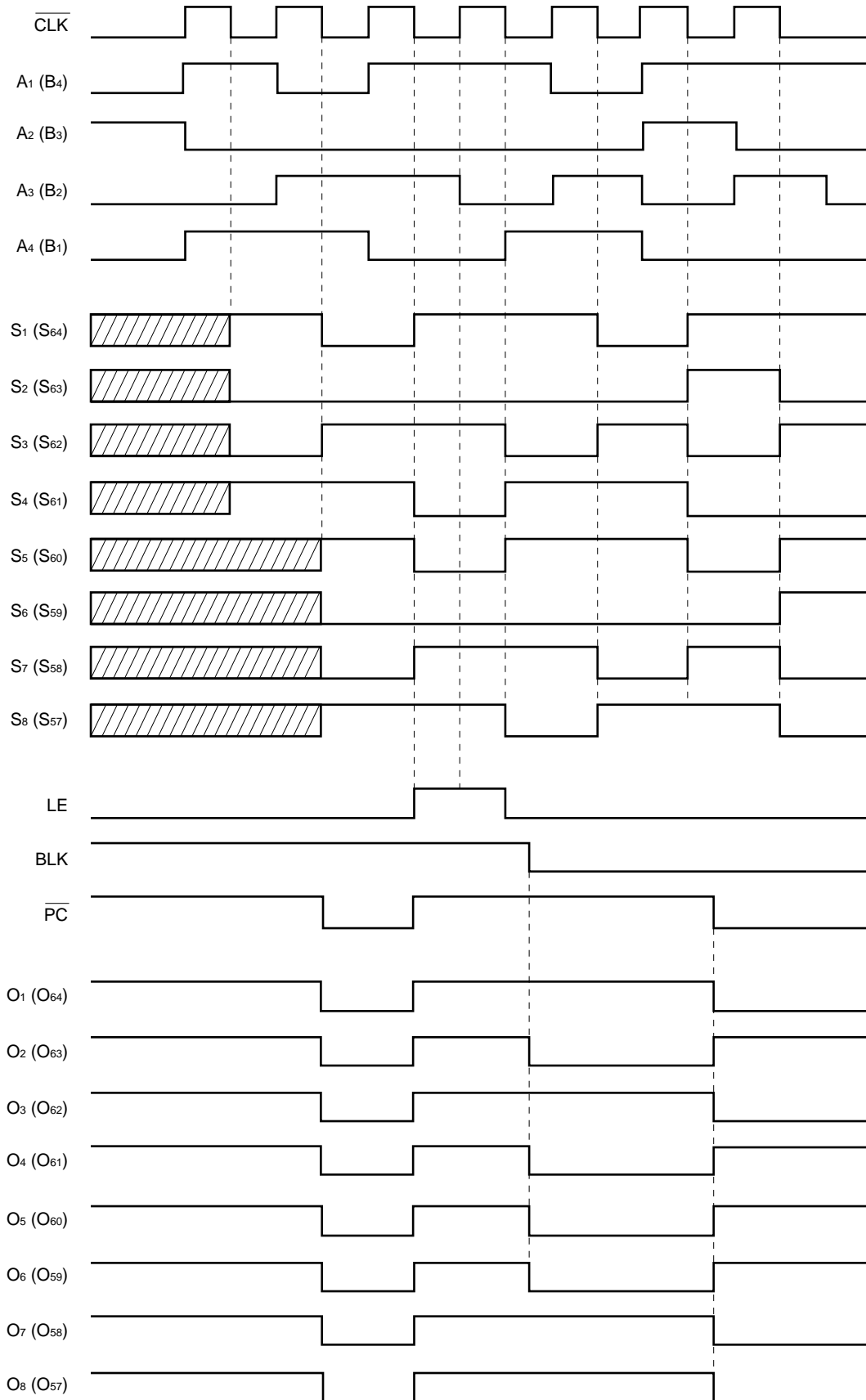
TRUTH TABLE 3 (DRIVER BLOCK)

$\overline{\text{L}}_n$	BLK	$\overline{\text{PC}}$	Driver output state
×	H	H	H (all driver outputs: H)
×	H	L	L (all driver outputs: L)
×	L	H	Outputs latch data ($\overline{\text{L}}_n$).
×	L	L	Outputs latch data ($\overline{\text{L}}_n$) with polarity inverted.

Remark X = H or L, H = high level, L = low level

TIMING CHART (RIGHT SHIFT)

() applies when $R/\bar{L} = L$.



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Item	Symbol	Rating	Unit
Logic block supply voltage	V _{DD1}	-0.5 to +7.0	V
Driver block supply voltage	V _{DD2}	-0.5 to +100	V
Logic block input voltage	V _I	-0.5 to V _{DD1} + 0.5	V
Driver block output current	I _{O2}	40	mA
Input current	I _I	±25	mA
Package allowable power dissipation	P _D	1300 ^{Note}	mW
Operating ambient temperature	T _A	-40 to +85 °C	°C
Storage temperature	T _{stg.}	-65 to +150 °C	°C

Note When T_A ≥ 25 °C, load should be alleviated at a rate of -13.0 mW/°C.

RECOMMENDED OPERATING RANGE (T_A = -40 to +85 °C, V_{SS1} = V_{SS2} = 0 V)

Item	Symbol	MIN.	TYP.	MAX.	Unit
Logic block supply voltage	V _{DD1}	4.5	5.0	5.5	V
Driver block supply voltage	V _{DD2}	30		90	V
Input voltage high	V _{IH}	0.7·V _{DD1}		V _{DD1}	V
Input voltage low	V _{IL}	0		0.2·V _{DD1}	V
Driver output current	I _{OH2}			-30	mA
	I _{OL2}			+30	mA

ELECTRICAL SPECIFICATIONS (T_A = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 90 V, V_{SS1} = V_{SS2} = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage high	V _{OH1}	Logic, I _{OH1} = -1.0 mA	0.9·V _{DD1}		V _{DD1}	V
Output voltage low	V _{OL1}	Logic, I _{OL1} = 1.0 mA	0		0.1·V _{DD1}	V
Output voltage high	V _{OH21}	O ₁ to O ₆₄ , I _{OH2} = -10 mA	83			V
	V _{OH22}	O ₁ to O ₆₄ , I _{OH2} = -30 mA	70			V
Output voltage low	V _{OL21}	O ₁ to O ₆₄ , I _{OL2} = 10 mA			5.0	V
	V _{OL22}	O ₁ to O ₆₄ , I _{OL2} = 30 mA			15	V
Input leakage current	I _{IL}	V _I = V _{DD1} or V _{SS1}			±1.0	μA
Input voltage high	V _{IH}		0.7·V _{DD1}			V
Input voltage low	V _{IL}				0.2·V _{DD1}	V
Static consumption current	I _{DD1}	Logic, T _A = -40 to +85 °C			100	μA
	I _{DD1}	Logic, T _A = 25 °C			10	μA
	I _{DD2}	Driver, T _A = -40 to +85 °C			1000	μA
	I _{DD2}	Driver, T _A = 25 °C			100	μA

Phase-out/Discontinued

SWITCHING CHARACTERISTICS ($T_A = 25\text{ °C}$, $V_{DD1} = 5.0\text{ V}$, $V_{DD2} = 90\text{ V}$, $V_{SS1} = V_{SS2} = 0\text{ V}$,
logic $C_L = 15\text{ pF}$, driver $C_L = 50\text{ pF}$, $t_r = t_f = 6.0\text{ ns}$)

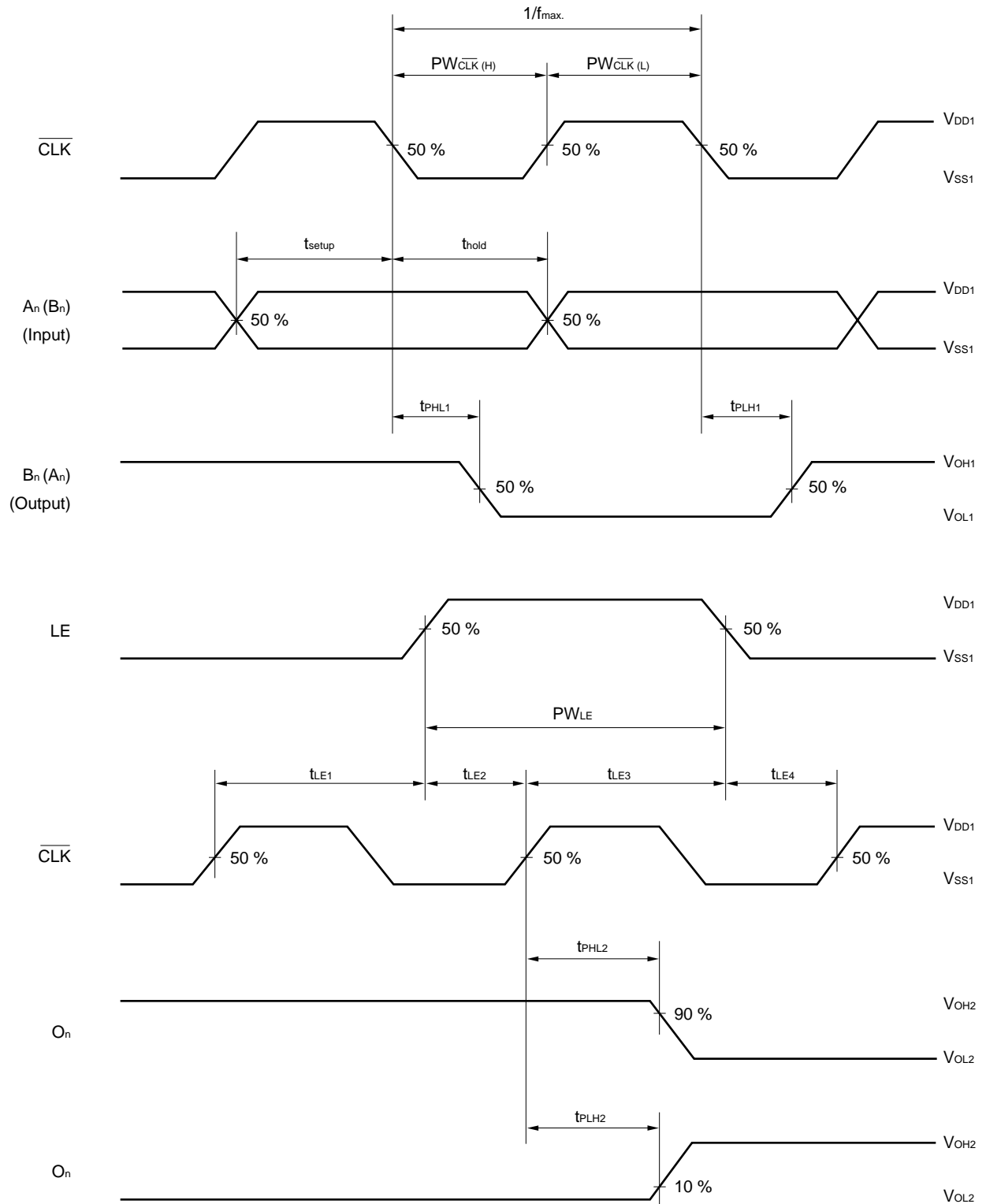
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transmission delay time	t _{PHL1}	$\overline{\text{CLK}} \downarrow \rightarrow \text{A/B}$			40	ns
	t _{PLH1}				40	ns
	t _{PHL2}	$\overline{\text{CLK}} \uparrow (\text{LE} = \text{H}) \rightarrow \text{O}_1 \text{ to } \text{O}_{64}$			180	ns
	t _{PLH2}				180	ns
	t _{PHL3}	$\text{BLK} \rightarrow \text{O}_1 \text{ to } \text{O}_{64}$			165	ns
	t _{PLH3}				165	ns
	t _{PHL4}	$\overline{\text{PC}} \rightarrow \text{O}_1 \text{ to } \text{O}_{64}$			160	ns
	t _{PLH4}				160	ns
Rise time	t _{TLH}	$\text{O}_1 \text{ to } \text{O}_{64}$			200	ns
Fall time	t _{THL}	$\text{O}_1 \text{ to } \text{O}_{64}$			200	ns
Maximum clock frequency	f _{max.}	Data fetch, Duty = 50 % $T_A = -40 \text{ to } 85\text{ °C}$ $V_{DD1} = 4.5 \text{ to } 5.5\text{ V}$	25			MHz
		With cascading, Duty = 50 % $T_A = -40 \text{ to } 85\text{ °C}$ $V_{DD1} = 4.5 \text{ to } 5.5\text{ V}$	20			MHz
Input capacitance	C _i				15	pF

TIMING REQUIREMENTS ($T_A = -40 \text{ to } +85\text{ °C}$, $V_{DD1} = 4.5 \text{ to } 5.5\text{ V}$, $V_{SS1} = V_{SS2} = 0\text{ V}$,
 $t_r = t_f = 6.0\text{ ns}$)

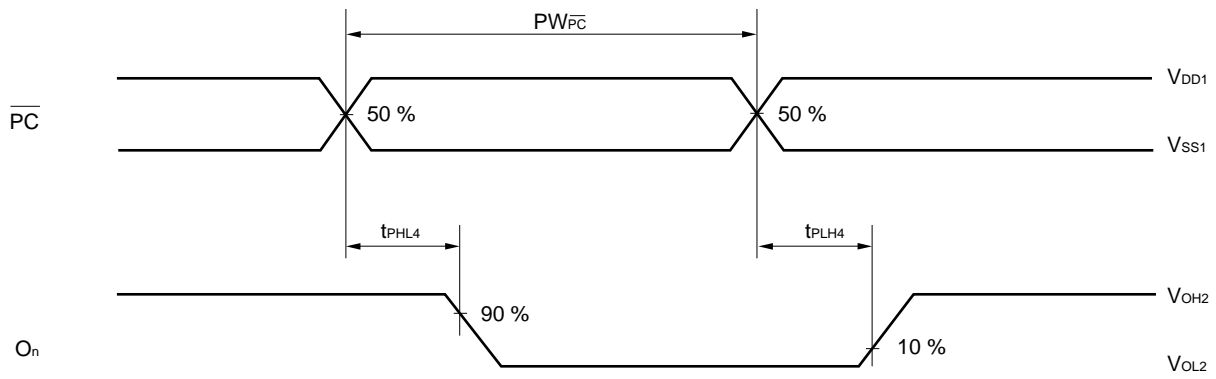
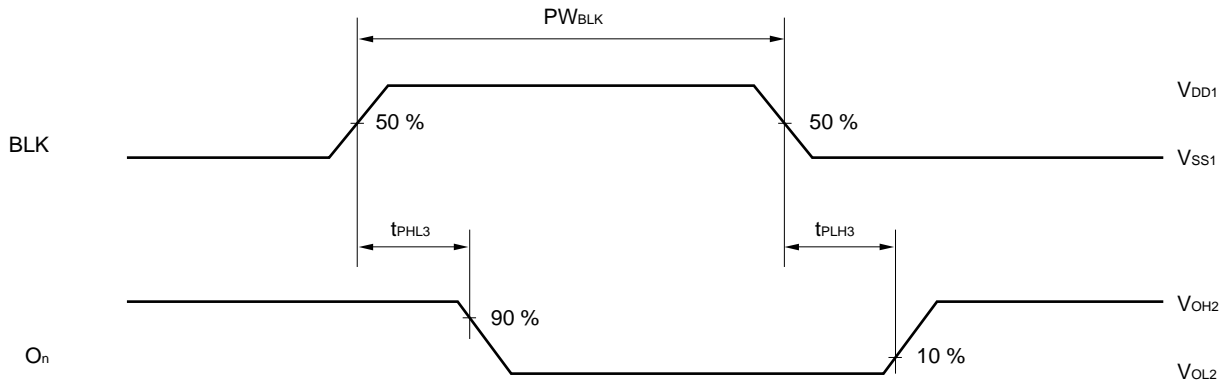
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW _{$\overline{\text{CLK}}$}		20			ns
Latch enable pulse width	PW _{LE}		30			ns
Blank pulse width	PW _{BLK}		500			ns
$\overline{\text{PC}}$ pulse width	PW _{$\overline{\text{PC}}$}		500			ns
Data setup time	t _{setup}		10			ns
Data hold time	t _{hold}		10			ns
Latch enable time 1	t _{LE1}		20			ns
Latch enable time 2	t _{LE2}		10			ns
Latch enable time 3	t _{LE3}		20			ns
Latch enable time 4	t _{LE4}		10			ns

SWITCHING CHARACTERISTIC WAVEFORM (R/L = H)

() applies when R/L = L.



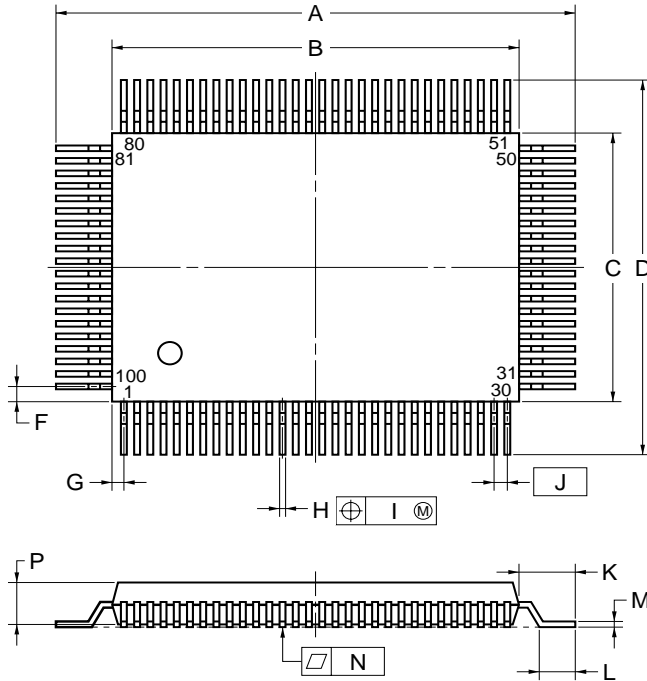
Phase-out/Discontinued



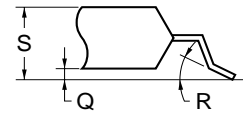
PACKAGE DRAWINGS

100 PIN PLASTIC QFP (14×20)

100 PIN PLASTIC QFP (14×20)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

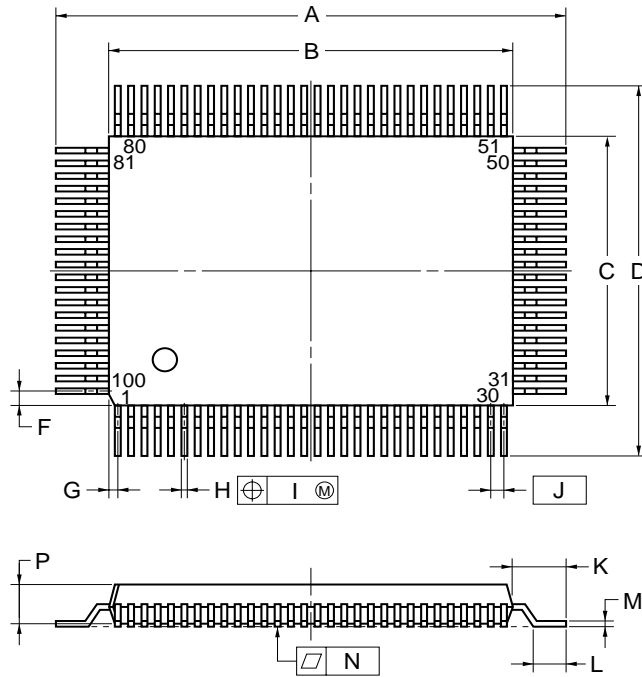
ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	0.795 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	0.012 ^{+0.004} _{-0.005}
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	0.071 ^{+0.008} _{-0.009}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P100GF-65-3BA-3

PACKAGE DRAWINGS

100 PIN PLASTIC QFP (14×20)

100 PIN PLASTIC QFP (14×20)



NOTE
 Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.2	0.913 ^{+0.009} _{-0.008}
B	20.0±0.2	0.787 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.2±0.2	0.677±0.008
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	0.012 ^{+0.004} _{-0.005}
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S100GF-65-3BA-3

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended below.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

SURFACE MOUNT TYPE

For details of recommended soldering conditions, refer to the information document “**Semiconductor Device Mounting Technology Manual**” (C10535E).

μ PD16327GF-3BA

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230 °C, Duration: 30 sec. MAX. (at 210 °C or above), Number of times: Once, Time limit: None ^{Note}	IR30-00-1
VPS	Package peak temperature: 215 °C, Duration: 40 sec. MAX. (at 200 °C or above), Number of times: Once, Time limit: None ^{Note}	VP15-00-1
Pin partial heating	Pin partial temperature: 300 °C MAX., Duration: 10 sec. MAX., Time limit: None ^{Note}	

Note For the storage period after dry-pack decapsulation, storage conditions are max. 25 °C, 65 % RH.

Caution Use of more than one soldering method should be avoided (except in the case of pin partial heating).

REFERENCES

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)
Quality Grades on NEC Semiconductor Devices (C11531E)

[MEMO]

[MEMO]

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