

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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240/244-OUTPUT TFT-LCD SOURCE DRIVER WITH TIMING GENERATOR (COMPATIBLE WITH 64-GRAY SCALES)

DESCRIPTION

The μPD161831 is a source driver for LIPS TFTs with on-chip timing generator and featuring 240/244 outputs. Data input as 6-bit x 3-dot digital data is output as 64 γ -corrected values using an internal D/A converter, achieving 260,000-color (full-color) display.

FEATURES

- CMOS level input
- 240/244 outputs (R, G, B output)
- Input of 6 bits (gray-scale data) by 3 dots
- Capable of outputting 64 values by means of 5 external power modules and a D/A converter
- Output dynamic range: $V_{SS} + 0.05\text{ V}$ to $V_S - 0.05\text{ V}$
- High-speed data transfer: $f_{CLK} = 20\text{ MHz MAX.}$ (during 2-times data transfer when operating at $V_{CC} = 2.5\text{ V}$. During 1-time data transfer 10 MHz MAX.)
- High-speed data transfer: $f_{CLK} = 16\text{ MHz MAX.}$ (during 2-times data transfer when operating at $V_{CC} = 2.2\text{ V}$. During 1-time data transfer 8 MHz MAX.)
- On-chip power supplies (driver power supply, gate top power supply, gate bottom power supply)
- Logic power supply voltage (V_{CC}): 2.2 to 3.6 V
- DC/DC reference power supply (V_{DC}): 2.5 to 3.6 V
- On-chip timing generator (Outputs R, G, B switching signal to panel. Outputs gate control signal.)
- On-chip 8-bit serial interface (applied to SPI)

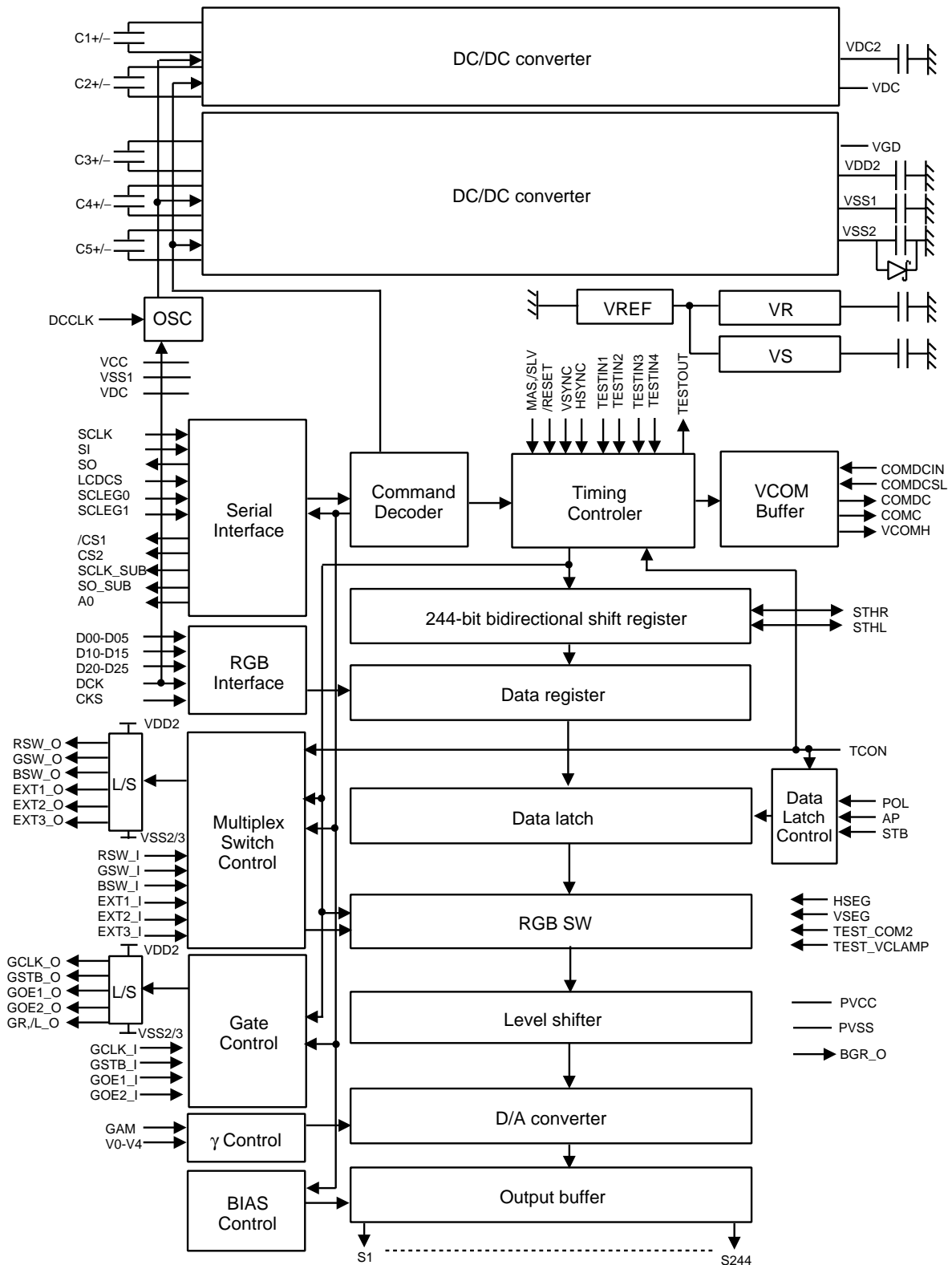
ORDERING INFORMATION

Part Number	Package
μPD161831P	Chip

Remark Purchasing the above chip entail the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

★ 1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (Pad Layout)

Chip size: T.B.D.

Bump size: INPUT/VCOM/TEST/DUMMY: $50 \times 75 \mu\text{m}^2$

OUTPUT: $35 \times 100 \mu\text{m}^2$

Remark T.B.D.: To be determined.

Alignment Mark (Unit: μm)

		X Coordinate	Y Coordinate
Alignment1	Aluminum (core)	10768.0	441.0
	Bump (core)	10768.0	366.0
Alignment2	Aluminum (core)	-10768.0	441.0
	Bump (core)	-10768.0	366.0

Remark The figures are rounded off in $0.5 \mu\text{m}$ units.

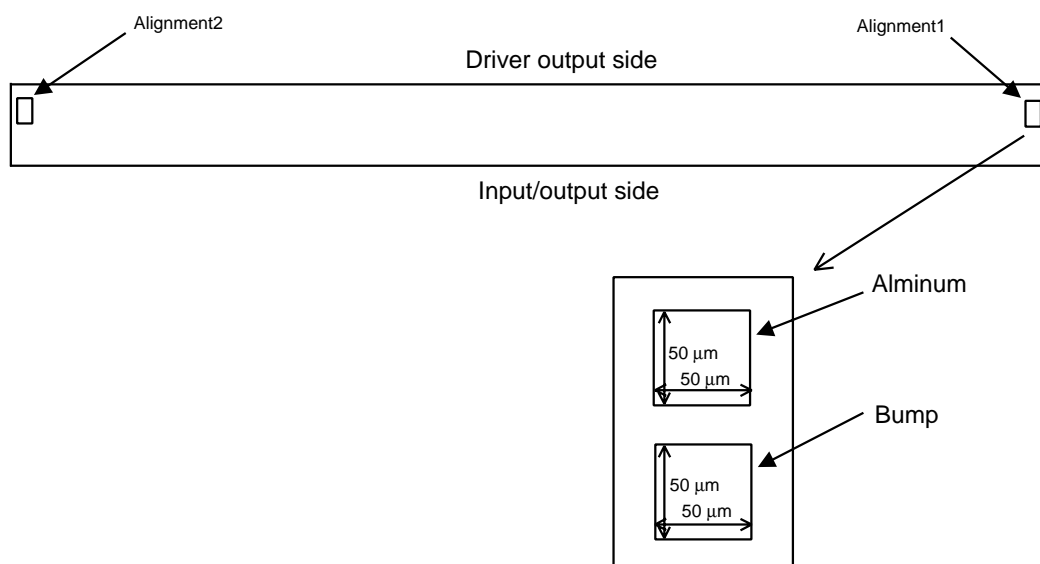


Table 2-1. Pad Layout (1/2)

No.	PAD Name	X [μm]	Y [μm]	No.	PAD Name	X [μm]	Y [μm]	No.	PAD Name	X [μm]	Y [μm]	No.	PAD Name	X [μm]	Y [μm]
1	Dummy	10797.00	594.99	71	S178	5820.00	594.99	141	S108	1620.00	594.99	211	S38	-2580.00	594.99
2	Dummy	10737.00	594.99	72	S177	5760.00	594.99	142	S107	1560.00	594.99	212	S37	-2640.00	594.99
3	Dummy	10677.00	594.99	73	S176	5700.00	594.99	143	S106	1500.00	594.99	213	S36	-2700.00	594.99
4	Dummy	9840.00	594.99	74	S175	5640.00	594.99	144	S105	1440.00	594.99	214	S35	-2760.00	594.99
5	S244	9780.00	594.99	75	S174	5580.00	594.99	145	S104	1380.00	594.99	215	S34	-2820.00	594.99
6	S243	9720.00	594.99	76	S173	5520.00	594.99	146	S103	1320.00	594.99	216	S33	-2880.00	594.99
7	S242	9660.00	594.99	77	S172	5460.00	594.99	147	S102	1260.00	594.99	217	S32	-2940.00	594.99
8	S241	9600.00	594.99	78	S171	5400.00	594.99	148	S101	1200.00	594.99	218	S31	-3000.00	594.99
9	S240	9540.00	594.99	79	S170	5340.00	594.99	149	S100	1140.00	594.99	219	S30	-3060.00	594.99
10	S239	9480.00	594.99	80	S169	5280.00	594.99	150	S99	1080.00	594.99	220	S29	-3120.00	594.99
11	S238	9420.00	594.99	81	S168	5220.00	594.99	151	S98	1020.00	594.99	221	S28	-3180.00	594.99
12	S237	9360.00	594.99	82	S167	5160.00	594.99	152	S97	960.00	594.99	222	S27	-3240.00	594.99
13	S236	9300.00	594.99	83	S166	5100.00	594.99	153	S96	900.00	594.99	223	S26	-3300.00	594.99
14	S235	9240.00	594.99	84	S165	5040.00	594.99	154	S95	840.00	594.99	224	S25	-3360.00	594.99
15	S234	9180.00	594.99	85	S164	4980.00	594.99	155	S94	780.00	594.99	225	S24	-3420.00	594.99
16	S233	9120.00	594.99	86	S163	4920.00	594.99	156	S93	720.00	594.99	226	S23	-3480.00	594.99
17	S232	9060.00	594.99	87	S162	4860.00	594.99	157	S92	660.00	594.99	227	S22	-3540.00	594.99
18	S231	9000.00	594.99	88	S161	4800.00	594.99	158	S91	600.00	594.99	228	S21	-3600.00	594.99
19	S230	8940.00	594.99	89	S160	4740.00	594.99	159	S90	540.00	594.99	229	S20	-3660.00	594.99
20	S229	8880.00	594.99	90	S159	4680.00	594.99	160	S89	480.00	594.99	230	S19	-3720.00	594.99
21	S228	8820.00	594.99	91	S158	4620.00	594.99	161	S88	420.00	594.99	231	S18	-3780.00	594.99
22	S227	8760.00	594.99	92	S157	4560.00	594.99	162	S87	360.00	594.99	232	S17	-3840.00	594.99
23	S226	8700.00	594.99	93	S156	4500.00	594.99	163	S86	300.00	594.99	233	S16	-3900.00	594.99
24	S225	8640.00	594.99	94	S155	4440.00	594.99	164	S85	240.00	594.99	234	S15	-3960.00	594.99
25	S224	8580.00	594.99	95	S154	4380.00	594.99	165	S84	180.00	594.99	235	S14	-4020.00	594.99
26	S223	8520.00	594.99	96	S153	4320.00	594.99	166	S83	120.00	594.99	236	S13	-4080.00	594.99
27	S222	8460.00	594.99	97	S152	4260.00	594.99	167	S82	60.00	594.99	237	S12	-4140.00	594.99
28	S221	8400.00	594.99	98	S151	4200.00	594.99	168	S81	0.00	594.99	238	S11	-4200.00	594.99
29	S220	8340.00	594.99	99	S150	4140.00	594.99	169	S80	-60.00	594.99	239	S10	-4260.00	594.99
30	S219	8280.00	594.99	100	S149	4080.00	594.99	170	S79	-120.00	594.99	240	S9	-4320.00	594.99
31	S218	8220.00	594.99	101	S148	4020.00	594.99	171	S78	-180.00	594.99	241	S8	-4380.00	594.99
32	S217	8160.00	594.99	102	S147	3960.00	594.99	172	S77	-240.00	594.99	242	S7	-4440.00	594.99
33	S216	8100.00	594.99	103	S146	3900.00	594.99	173	S76	-300.00	594.99	243	S6	-4500.00	594.99
34	S215	8040.00	594.99	104	S145	3840.00	594.99	174	S75	-360.00	594.99	244	S5	-4560.00	594.99
35	S214	7980.00	594.99	105	S144	3780.00	594.99	175	S74	-420.00	594.99	245	S4	-4620.00	594.99
36	S213	7920.00	594.99	106	S143	3720.00	594.99	176	S73	-480.00	594.99	246	S3	-4680.00	594.99
37	S212	7860.00	594.99	107	S142	3660.00	594.99	177	S72	-540.00	594.99	247	S2	-4740.00	594.99
38	S211	7800.00	594.99	108	S141	3600.00	594.99	178	S71	-600.00	594.99	248	S1	-4800.00	594.99
39	S210	7740.00	594.99	109	S140	3540.00	594.99	179	S70	-660.00	594.99	249	Dummy	-4860.00	594.99
40	S209	7680.00	594.99	110	S139	3480.00	594.99	180	S69	-720.00	594.99	250	Dummy	-4920.00	594.99
41	S208	7620.00	594.99	111	S138	3420.00	594.99	181	S68	-780.00	594.99	251	Dummy	-4980.00	594.99
42	S207	7560.00	594.99	112	S137	3360.00	594.99	182	S67	-840.00	594.99	252	Dummy	-5040.00	594.99
43	S206	7500.00	594.99	113	S136	3300.00	594.99	183	S66	-900.00	594.99	253	Dummy	-5100.00	594.99
44	S205	7440.00	594.99	114	S135	3240.00	594.99	184	S65	-960.00	594.99	254	Dummy	-5160.00	594.99
45	S204	7380.00	594.99	115	S134	3180.00	594.99	185	S64	-1020.00	594.99	255	Dummy	-5220.00	594.99
46	S203	7320.00	594.99	116	S133	3120.00	594.99	186	S63	-1080.00	594.99	256	Dummy	-5280.00	594.99
47	S202	7260.00	594.99	117	S132	3060.00	594.99	187	S62	-1140.00	594.99	257	Dummy	-5340.00	594.99
48	S201	7200.00	594.99	118	S131	3000.00	594.99	188	S61	-1200.00	594.99	258	Dummy	-5400.00	594.99
49	S200	7140.00	594.99	119	S130	2940.00	594.99	189	S60	-1260.00	594.99	259	Dummy	-5460.00	594.99
50	S199	7080.00	594.99	120	S129	2880.00	594.99	190	S59	-1320.00	594.99	260	Dummy	-5520.00	594.99
51	S198	7020.00	594.99	121	S128	2820.00	594.99	191	S58	-1380.00	594.99	261	Dummy	-5580.00	594.99
52	S197	6960.00	594.99	122	S127	2760.00	594.99	192	S57	-1440.00	594.99	262	Dummy	-5640.00	594.99
53	S196	6900.00	594.99	123	S126	2700.00	594.99	193	S56	-1500.00	594.99	263	Dummy	-5700.00	594.99
54	S195	6840.00	594.99	124	S125	2640.00	594.99	194	S55	-1560.00	594.99	264	Dummy	-5760.00	594.99
55	S194	6780.00	594.99	125	S124	2580.00	594.99	195	S54	-1620.00	594.99	265	Dummy	-5820.00	594.99
56	S193	6720.00	594.99	126	S123	2520.00	594.99	196	S53	-1680.00	594.99	266	Dummy	-5880.00	594.99
57	S192	6660.00	594.99	127	S122	2460.00	594.99	197	S52	-1740.00	594.99	267	Dummy	-5940.00	594.99
58	S191	6600.00	594.99	128	S121	2400.00	594.99	198	S51	-1800.00	594.99	268	Dummy	-6000.00	594.99
59	S190	6540.00	594.99	129	S120	2340.00	594.99	199	S50	-1860.00	594.99	269	Dummy	-6060.00	594.99
60	S189	6480.00	594.99	130	S119	2280.00	594.99	200	S49	-1920.00	594.99	270	Dummy	-6120.00	594.99
61	S188	6420.00	594.99	131	S118	2220.00	594.99	201	S48	-1980.00	594.99	271	Dummy	-6180.00	594.99
62	S187	6360.00	594.99	132	S117	2160.00	594.99	202	S47	-2040.00	594.99	272	Dummy	-6240.00	594.99
63	S186	6300.00	594.99	133	S116	2100.00	594.99	203	S46	-2100.00	594.99	273	Dummy	-6300.00	594.99
64	S185	6240.00	594.99	134	S115	2040.00	594.99	204	S45	-2160.00	594.99	274	Dummy	-6360.00	594.99
65	S184	6180.00	594.99	135	S114	1980.00	594.99	205	S44	-2220.00	594.99	275	Dummy	-6420.00	594.99
66	S183	6120.00	594.99	136	S113	1920.00	594.99	206	S43	-2280.00	594.99	276	Dummy	-6480.00	594.99
67	S182	6060.00	594.99	137	S112	1860.00	594.99	207	S42	-2340.00	594.99	277	Dummy	-6540.00	594.99
68	S181	6000.00	594.99	138	S111	1800.00	594.99	208	S41	-2400.00	594.99	278	Dummy	-6600.00	594.99
69	S180	5940.00	594.99	139	S110	1740.00	594.99	209	S40	-2460.00	594.99	279	Dummy	-6660.00	594.99
70	S179	5880.00	594.99	140	S109	1680.00	594.99	210	S39	-2520.00	594.99	280	Dummy	-6720.00	594.99

Table 2-1. Pad Layout (2/2)

No.	PADName	X[μm]	Y[μm]	No.	PADName	X[μm]	Y[μm]	No.	PADName	X[μm]	Y[μm]	No.	PADName	X[μm]	Y[μm]
281	Dummy	-6780.00	594.99	351	VDC	-7880.04	-607.50	421	Dummy	-2080.26	-607.50	491	D25	4594.17	-607.50
282	Dummy	-6840.00	594.99	352	VDC2	-7780.05	-607.50	422	Dummy	-1980.27	-607.50	492	D24	4694.16	-607.50
283	BSW O	-6900.00	594.99	353	VDC2	-7705.05	-607.50	423	Dummy	-1880.28	-607.50	493	D23	4794.15	-607.50
284	BSW O	-6960.00	594.99	354	VDC2	-7630.05	-607.50	424	Dummy	-1780.29	-607.50	494	D22	4894.14	-607.50
285	GSW O	-7080.00	594.99	355	VDC2	-7555.05	-607.50	425	Dummy	-1680.30	-607.50	495	D21	4994.13	-607.50
286	GSW O	-7140.00	594.99	356	VDC2	-7480.05	-607.50	426	Dummy	-1580.31	-607.50	496	D20	5094.12	-607.50
287	RSW O	-7260.00	594.99	357	VDC2	-7405.05	-607.50	427	VOC	-1480.32	-607.50	497	D15	5194.11	-607.50
288	RSW O	-7320.00	594.99	358	VDC2	-7330.05	-607.50	428	VCC	-1405.32	-607.50	498	D14	5294.10	-607.50
289	EXT3 O	-7440.00	594.99	359	C1+	-7230.06	-607.50	429	VOC	-1330.32	-607.50	499	D13	5394.09	-607.50
290	EXT3 O	-7500.00	594.99	360	C1+	-7155.06	-607.50	430	VCC	-1255.32	-607.50	500	D12	5494.08	-607.50
291	EXT2 O	-7620.00	594.99	361	C1+	-7080.06	-607.50	431	VSS	-1155.33	-607.50	501	D11	5594.07	-607.50
292	EXT2 O	-7680.00	594.99	362	C1+	-7005.06	-607.50	432	VSS	-1080.33	-607.50	502	D10	5694.06	-607.50
293	EXT1 O	-7800.00	594.99	363	C1+	-6930.06	-607.50	433	VSS	-1005.33	-607.50	503	D05	5794.05	-607.50
294	EXT1 O	-7860.00	594.99	364	C1+	-6855.06	-607.50	434	VSS	-930.33	-607.50	504	D04	5894.04	-607.50
295	VSS2	-7980.00	594.99	365	C1+	-6780.06	-607.50	435	VSS	-855.33	-607.50	505	D03	5994.03	-607.50
296	VSS2	-8040.00	594.99	366	C1-	-6680.07	-607.50	436	STHR	-755.34	-607.50	506	D02	6094.02	-607.50
297	VSS2	-8100.00	594.99	367	C1-	-6605.07	-607.50	437	GOE2 I	-655.35	-607.50	507	D01	6194.01	-607.50
298	VSS2	-8160.00	594.99	368	C1-	-6530.07	-607.50	438	GOE1 I	-555.36	-607.50	508	D00	6294.00	-607.50
299	VSS1	-8280.00	594.99	369	C1-	-6455.07	-607.50	439	GSTB I	-455.37	-607.50	509	STHL	6393.99	-607.50
300	VSS1	-8340.00	594.99	370	C1-	-6380.07	-607.50	440	GCLK I	-355.38	-607.50	510	STHL	6468.99	-607.50
301	VSS1	-8400.00	594.99	371	C1-	-6305.07	-607.50	441	STB	-255.39	-607.50	511	TESTOUT	6568.98	-607.50
302	VSS1	-8460.00	594.99	372	C1-	-6230.07	-607.50	442	AP	-155.40	-607.50	512	TESTIN4	6668.97	-607.50
303	VDD2	-8580.00	594.99	373	C2+	-6130.08	-607.50	443	POL	-55.41	-607.50	513	TESTIN3	6768.96	-607.50
304	VDD2	-8640.00	594.99	374	C2+	-6055.08	-607.50	444	TOON	44.58	-607.50	514	TESTIN2	6868.95	-607.50
305	VDD2	-8700.00	594.99	375	C2+	-5980.08	-607.50	445	PVCC	144.57	-607.50	515	TESTIN1	6968.94	-607.50
306	VDD2	-8760.00	594.99	376	C2+	-5905.08	-607.50	446	OSEL	244.56	-607.50	516	V4	7068.93	-607.50
307	GOE2 O	-8880.00	594.99	377	C2+	-5830.08	-607.50	447	VCSL	344.55	-607.50	517	V4	7143.93	-607.50
308	GOE2 O	-8940.00	594.99	378	C2+	-5755.08	-607.50	448	GAM	444.54	-607.50	518	V3	7243.92	-607.50
309	GOE2 O	-9000.00	594.99	379	C2+	-5680.08	-607.50	449	MAS/SLV	544.53	-607.50	519	V3	7318.92	-607.50
310	GOE2 O	-9060.00	594.99	380	C2-	-5580.09	-607.50	450	SOLEGI	644.52	-607.50	520	V2	7418.91	-607.50
311	GOE1 O	-9180.00	594.99	381	C2-	-5505.09	-607.50	451	SOLEGO	744.51	-607.50	521	V2	7493.91	-607.50
312	GOE1 O	-9240.00	594.99	382	C2-	-5430.09	-607.50	452	OKS	844.50	-607.50	522	V1	7593.90	-607.50
313	GR/L O	-9360.00	594.99	383	C2-	-5355.09	-607.50	453	HSEG	944.49	-607.50	523	V1	7668.90	-607.50
314	GR/L O	-9420.00	594.99	384	C2-	-5280.09	-607.50	454	VSEG	1044.48	-607.50	524	V0	7768.89	-607.50
315	GCLK O	-9540.00	594.99	385	C2-	-5205.09	-607.50	455	PVSS	1144.47	-607.50	525	V0	7843.89	-607.50
316	GCLK O	-9600.00	594.99	386	C2-	-5130.09	-607.50	456	EXT3 I	1244.46	-607.50	526	Dummy	7943.88	-607.50
317	GSTB O	-9720.00	594.99	387	C3+	-5030.10	-607.50	457	EXT2 I	1344.45	-607.50	527	Dummy	8043.87	-607.50
318	GSTB O	-9780.00	594.99	388	C3+	-4955.10	-607.50	458	EXT1 I	1444.44	-607.50	528	Dummy	8143.86	-607.50
319	Dummy	-9840.00	594.99	389	C3+	-4880.10	-607.50	459	BSW I	1544.43	-607.50	529	Dummy	8243.85	-607.50
320	Dummy	-10677.00	594.99	390	C3-	-4780.11	-607.50	460	GSW I	1644.42	-607.50	530	Dummy	8343.84	-607.50
321	Dummy	-10737.00	594.99	391	C3-	-4705.11	-607.50	461	RSW I	1744.41	-607.50	531	Dummy	8443.83	-607.50
322	Dummy	-10797.00	594.99	392	C3-	-4630.11	-607.50	462	Dummy	1844.40	-607.50	532	Dummy	8543.82	-607.50
323	Dummy	-10788.00	-607.50	393	C4+	-4530.12	-607.50	463	Dummy	1944.39	-607.50	533	COMDCSL	8643.81	-607.50
324	Dummy	-10688.01	-607.50	394	C4+	-4455.12	-607.50	464	Dummy	2044.38	-607.50	534	COMDCIN	8743.80	-607.50
325	Dummy	-10588.02	-607.50	395	C4+	-4380.12	-607.50	465	Dummy	2144.37	-607.50	535	COMDCIN	8818.80	-607.50
326	Dummy	-9879.99	-607.50	396	C4-	-4280.13	-607.50	466	Dummy	2244.36	-607.50	536	VCOMH	8918.79	-607.50
327	VSS	-9780.00	-607.50	397	C4-	-4205.13	-607.50	467	/RESET	2344.35	-607.50	537	VCOMH	8993.79	-607.50
328	VSS	-9705.00	-607.50	398	C4-	-4130.13	-607.50	468	A0	2444.34	-607.50	538	VCOMH	9068.79	-607.50
329	VSS	-9630.00	-607.50	399	C5+	-4030.14	-607.50	469	CS2	2544.33	-607.50	539	VCOMH	9143.79	-607.50
330	VSS	-9555.00	-607.50	400	C5+	-3955.14	-607.50	470	CS1	2644.32	-607.50	540	COMDC	9243.78	-607.50
331	VSS	-9480.00	-607.50	401	C5+	-3880.14	-607.50	471	SCLK SUB	2744.31	-607.50	541	COMDC	9318.78	-607.50
332	VS	-9380.01	-607.50	402	C5-	-3780.15	-607.50	472	SOSUB	2844.30	-607.50	542	COMC	9418.77	-607.50
333	VS	-9305.01	-607.50	403	C5-	-3705.15	-607.50	473	LDCS	2944.29	-607.50	543	COMC	9493.77	-607.50
334	VS	-9230.01	-607.50	404	C5-	-3630.15	-607.50	474	LDCS	3019.29	-607.50	544	COMC	9568.77	-607.50
335	VS	-9155.01	-607.50	405	DOCLK	-3530.16	-607.50	475	SCLK	3119.28	-607.50	545	COMC	9643.77	-607.50
336	VS	-9080.01	-607.50	406	VDD2	-3430.17	-607.50	476	SCLK	3194.28	-607.50	546	COMC	9718.77	-607.50
337	VGD	-8980.02	-607.50	407	VDD2	-3355.17	-607.50	477	SI	3294.27	-607.50	547	Dummy	9818.76	-607.50
338	VGD	-8905.02	-607.50	408	VSS1	-3255.18	-607.50	478	SI	3369.27	-607.50	548	Dummy	10588.02	-607.50
339	VGD	-8830.02	-607.50	409	VSS1	-3180.18	-607.50	479	SO	3469.26	-607.50	549	Dummy	10688.01	-607.50
340	VGD	-8755.02	-607.50	410	VSS2	-3080.19	-607.50	480	SO	3544.26	-607.50	550	Dummy	10788.00	-607.50
341	VR	-8655.03	-607.50	411	VSS2	-3005.19	-607.50	481	VSYN	3644.25	-607.50				
342	VR	-8580.03	-607.50	412	TEST_VCLAMP	-2905.20	-607.50	482	HSYN	3744.24	-607.50				
343	VR	-8505.03	-607.50	413	TEST_VCLAMP	-2830.20	-607.50	483	HSYN	3819.24	-607.50				
344	VR	-8430.03	-607.50	414	TEST_COM2	-2730.21	-607.50	484	DCK	3919.23	-607.50				
345	VDC	-8330.04	-607.50	415	TEST_COM2	-2655.21	-607.50	485	DCK	3994.23	-607.50				
346	VDC	-8255.04	-607.50	416	BGR O	-2555.22	-607.50	486	Dummy	4094.22	-607.50				
347	VDC	-8180.04	-607.50	417	MVS	-2455.23	-607.50	487	Dummy	4194.21	-607.50				
348	VDC	-8105.04	-607.50	418	MVS	-2380.23	-607.50	488	Dummy	4294.20	-607.50				
349	VDC	-8030.04	-607.50	419	Dummy	-2280.24	-607.50	489	Dummy	4394.19	-607.50				
350	VDC	-7955.04	-607.50	420	Dummy	-2180.25	-607.50	490	Dummy	4494.18	-607.50				

3. PIN FUNCTIONS

3.1 Source Driver Control Pins

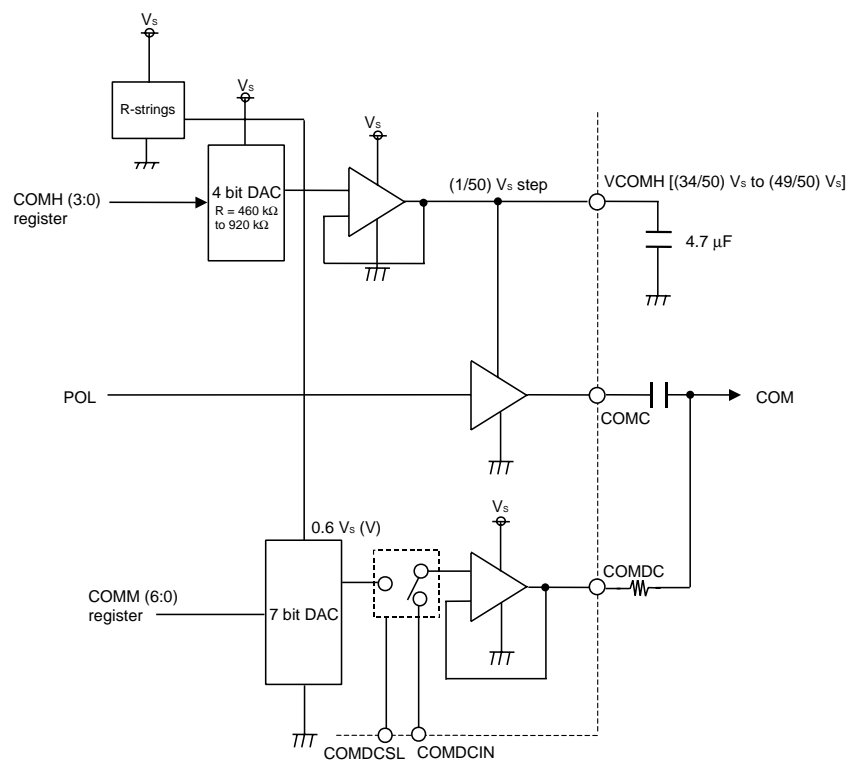
(1/2)

Pin Symbol	Pin Name	Pin Number	I/O	Description
S ₁ to S ₂₄₄	Driver output	248 to 5	Output	The D/A converted 64-gray-scale analog voltage is output. OSEL = L: S ₁ to S ₂₄₄ OSEL = H: S ₃ to S ₂₄₂
OSEL	Driver output count switching	446	Input	The output count can be selected. When OSEL = H, the unused pins S ₁ , S ₂ , S ₂₄₃ , S ₂₄₄ always become Hi-Z (high impedance). OSEL = L: 244 outputs OSEL = H: 240 outputs
DCK	Dot clock	484, 485	Input	Dot clock signal
CKS	Dot clock inversion	452	Input	Inverts the active level of the dot clock. CKS = L: Low active CKS = H: High active
HSYNC	Horizontal sync signal	482, 483	Input	Horizontal sync signal input pin. <u>Do not input a width wider than the horizontal period as the width of the HSYNC active level.</u>
VSYNC	Vertical sync signal	481	Input	Vertical sync signal input pin.
HSEG	HSYNC polarity selection	453	Input	Selects the active level of the HSYNC signal. HSEG = L: Low active HSEG = H: High active
VSEG	VSYSN polarity selection	454	Input	Selects the active level of the VSYNC signal. VSEG = L: Low active VSEG = H: High active
D ₀₀ to D ₀₅	Display data input	508 to 503	Input	The display data is input with a width of 18 bits, the gray scale data (6 bits) by 3 dots (1 pixels). D _{x0} : LSB, D _{x5} : MSB
D ₁₀ to D ₁₅		502 to 497		
D ₂₀ to D ₂₅		496 to 491		
SCLK	Serial clock input	475, 476	Input	Clock pin of serial interface.
SO	Serial data output	479, 480	Output	Data output pin of serial interface.
SI	Serial data input	477, 478	Input	Data input pin of serial interface.
LCDCS	Serial interface chip select	473, 474	Input	Chip select pin of serial interface.
SCLEG0, SCLEG1	Serial clock mode selection	451, 450	Input	Mode select pin of serial clock. For details, refer to 4. REGISTERS for explanation in serial interface .
VCSEL	COM amplitude output fixing signal	447	Input	Fixes the VCOM output to L. When not using the VCOM output, set VCSEL to L. VCSEL = L: VCOM output fixed to L VCSEL = H: VCOM signal output in accordance with POL signal
GAM	External γ-usage selection	448	Input	When the γ-correction power supply is input externally, switch GAM to H. If two or more chips are used, be sure to input the γ - correction power supply externally. Figure 3-1 shows VCOM application example. GAM = L: External γ-correction power supply not input GAM = H: External γ-correction power supply input

(2/2)

Pin Symbol	Pin Name	Pin Name	I/O	Description
MAS, /SLV	Master slave control	449	Input	When the timing generator is used and 2 chips are connected in cascade, selects use either as master IC or slave IC. When the timing generator is not used, either leave this pin or input a high level. MAS, /SLV = L: Use as slave MAS, /SLV = H: Use as master
V ₀ -V ₄	γ-corrected power supplies	525 to 516	Input	These pins input the γ-corrected power supplies from outside, the relationship below must be observed. Also, be sure to stabilize the gray-scale-level power supply during gray-scale voltage output. $V_{SS} \leq V_4 \leq V_3 \leq V_2 \leq V_1 \leq V_0 \leq V_S$
VCOMH	Amplitude voltage	536 to 539	Output	Outputs the voltage set with the amplitude voltage adjustment D/A converter.
COMC	Square wave signal output	542 to 546	Output	Outputs the square wave signal obtained through common modulation of V _{p-p} voltage 0 V-VCOMH.
COMDC	Common center voltage output	540, 541	Output	Outputs the common center voltage.
COMDCIN	Common center voltage external input	534, 535	Input	Input pin used to input the common center voltage from external. Valid when COMDCSL = H.
COMDCSL	Common center voltage external input switch	533	Input	Inputs a H level as the common voltage when the voltage input from the COMDCIN pin is used.
TCON	Timing generator use/non-use selection	444	Input	This pin is used to select whether or not to use the timing generator. TCON = L: Timing generator used TCON = H: Timing generator not used
/RESET	Reset	467	Input	Reset pin. This is the active low signal.

Figure 3-1. VCOM Application Example



3.2 Gate Scan Control Pins

Pin Symbol	Pin Name	Pin Name	I/O	Description
GCLK_O	Gate CLK output	315, 316	Output	Pin for CLK output to the gate control circuit.
GSTB_O	Gate STB output	317, 318	Output	Pin for strobe signal fed to gate control circuit
GOE1_O	Gate OE1 output	311, 312	Output	Pin for OE1 output to gate control circuit
GOE2_O	Gate OE2 output	307 to 310	Output	Pin for OE2 output to gate control circuit
GCLK_I	Gate CLK input	440	Input	Input the CLK signal to the gate control circuit, when the timing generator function is not used. The signal input to this pin is output from the GCLK_O via a level shifter.
GSTB_I	Gate STB input	439	Input	Input the STB signal to the gate control circuit, when the timing generator function is not used. The signal input to this pin is output from the GSTB_O via a level shifter.
GOE1_I	Gate OE1 input	438	Input	Input the OE1 signal to the gate control circuit, when the timing generator function is not used. The signal input to this pin is output from the GOE1_O via a level shifter.
GOE2_I	Gate OE2 input	437	Input	Input the OE2 signal to the gate control circuit, when the timing generator function is not used. The signal input to this pin is output from the GOE2_O via a level shifter.
GR,/L_O	Gate R,/L output	313, 314	Output	Pin that outputs R,/L to the gate control circuit.

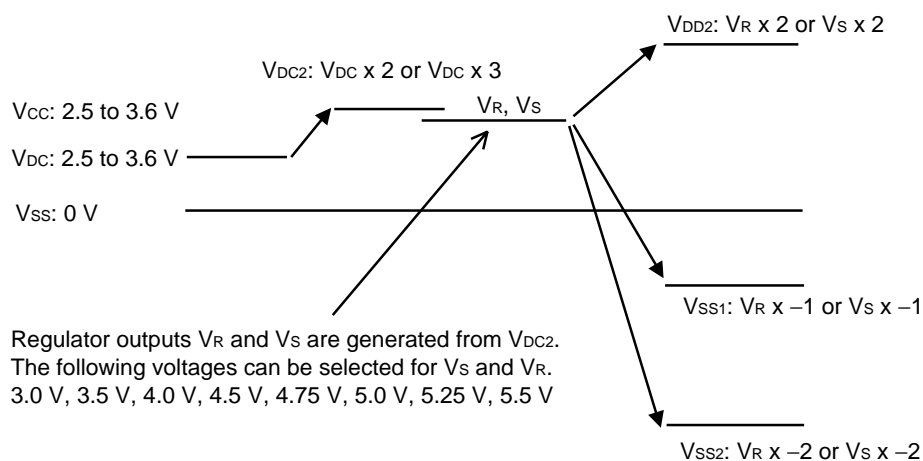
3.3 Control Pin for Multiplex Switch, etc.

Pin Symbol	Pin Name	Pin Name	I/O	Description
RSW_O	Multiplex control signal output	287, 288	Output	Output pin that controls the multiplex switch on the panel.
GSW_O		285, 286	Output	
BSW_O		283, 284	Output	
EXT1_O	Extension control signal output	293, 294	Output	Extension output pin that controls the circuit on the panel.
EXT2_O		291, 292	Output	
EXT3_O		289, 290	Output	
RSW_I	Multiplex control signal input	461	Input	Pin for inputting the signal that controls the multiplex switch on the panel, when the timing generator function is not used. The signal input to this pin is output from the RSW_O pin via a level shifter.
GSW_I		460	Input	Pin for inputting the signal that controls the multiplex switch on the panel, when the timing generator function is not used. The signal input to this pin is output from the GSW_O pin via a level shifter.
BSW_I		459	Input	Pin for inputting the signal that controls the multiplex switch on the panel, when the timing generator function is not used. The signal input to this pin is output from the BSW_O pin via a level shifter.
EXT1_I	Extension control signal input	458	Input	Pin for inputting the extension signal that controls the circuit on the panel, when the timing generator function is not used. The signal input to this pin is output from the EXT1_O pin via the level shifter.
EXT2_I		457	Input	Pin for inputting the extension signal that controls the circuit on the panel, when the timing generator function is not used. The signal input to this pin is output from the EXT2_O pin via the level shifter.
EXT3_I		456	Input	Pin for inputting the extension signal that controls the circuit on the panel, when the timing generator function is not used. The signal input to this pin is output from the EXT3_O pin via the level shifter.

3.4 Power Supply Function Control Pin

Pin Symbol	Pin Name	Pin Name	I/O	Description
C1+/-, C2+/-, C3+/-, C4+/-, C5+/-	Booster capacitor connection	359 to 404	—	Connect the boost capacitor of the DC/DC converter to this pin. Booster ratio is difference on the way of using condenser connection. For details, refer to figure 3–3.
V _{DC2}	DC/DC converter output	352 to 358	—	DC/DC converter boost output ($V_{DC} \times 2$ or $V_{DC} \times 3$). This output is the V _s and V _R amplifier power supply. The V _{DC2} boot step is selected with the V _{CD2} bit. V _{CD2} bit = 0: $V_{DC} \times 2$ V _{CD2} bit = 1: $V_{DC} \times 3$
V _s	Source power supply output	336 to 332	—	Source voltage output pin. The V _s output voltage can be changed through the VSEL0 to VSEL2.
MV _s	External resistance input	417, 418	Input	An external resistance can be input to set any output voltage. EXRV bit = 0: Leave open (Internal resistor selection) EXRV bit = 1: Connect external resistor.
V _R	Reference power supply output	341 to 344	—	Gate reference power supply output pin. The V _R output voltage can be changed through the VRSEL to VRSEL2 setting.
V _{DD2}	DC/DC converter output	303 to 306, 406, 407	—	DC/DC converter boost output ($V_{GD} \times 2$)
V _{SS1}	DC/DC converter output	299 to 302, 408 to 411	—	DC/DC converter boost output ($V_{GD} \times -1$)
V _{SS2}	DC/DC converter output	295 to 298	—	DC/DC converter boost output ($V_{GD} \times -2$)
V _{DC}	Reference power supply input for source power supply voltage	345 to 351	—	Extension pin used to control circuit on panel.
V _{GD}	Reference power supply input for gate power supply voltage	337 to 340	—	Extension pin used to control circuit on panel.
DCCLK	Boost clock input	405	Input	Pin used to input boost clock of DC/DC converter.

Figure 3–2. DC/DC Converter Boost Configuration



★ Figure 3–3. Relationship between Condenser Connection for Booster and Booster Ratio

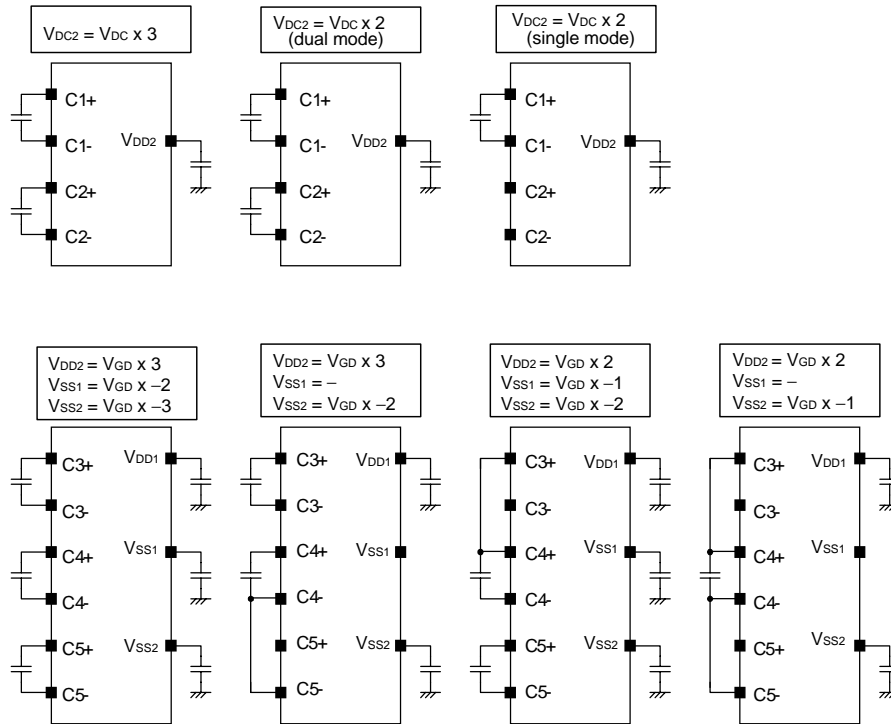
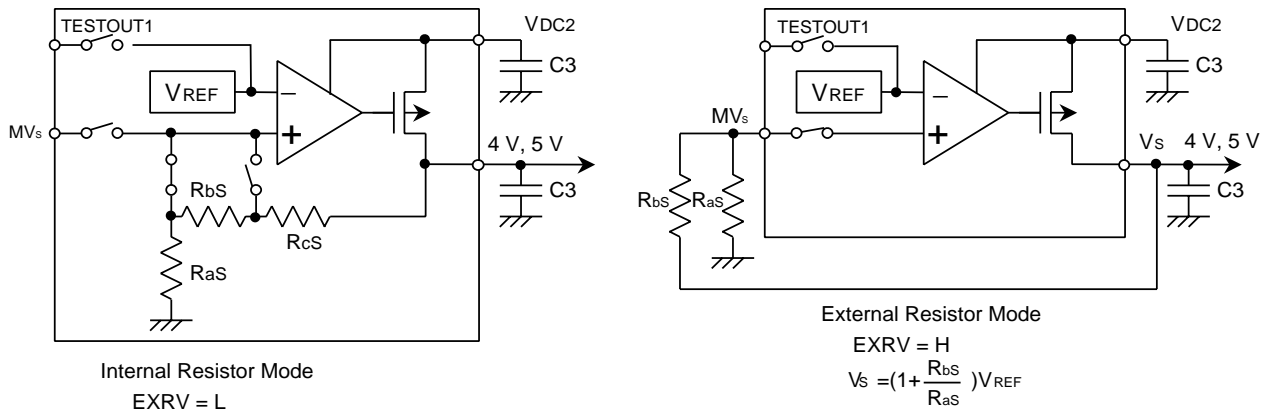


Figure 3–4. Vs, Amp. Circuit Configuration



3.5 Control Pins when Timing Generator Function Not Used, and Other Pins

Pin Symbol	Pin Name	Pin Name	I/O	Description
STHR	Right shift start pulse I/O	436	I/O	Start pulse I/O pin during cascade connection. When an H level is read at the rising edge of CLK, fetching of display data starts. In the case of right shift, STHR = input and STHL = output. In the case of left shift, STHL = input and STHR = output.
STHL	Left shift start pulse I/O	509, 510	I/O	
STB	Latch input	441	Input	This is the timing signal at which the contents of the data register are latched. When an H level is read at the rising edge of CLK, the contents of the data register are latched and transferred to the D/A converter, and an analog voltage is output according to the display data. Even after STB fetch, do not stop CLK because the internal operation is performed using CLK. At the rising edge of STB, the content of the shift register are cleared. After one pulse is input at startup, the operation becomes normal. At the rising edge of STB, the output switch is switched OFF. For the STB input timing, refer to 5. TIMING GENERATOR NON-USE FUNCTION .
AP	Output SW ON/OFF	442	Input	Switches the BIAS circuit ON/OFF and the output switch and amplifier ON. The period during which AP is H is the amplifier circuit setting period and the liquid crystal drive period. At the falling edge of AP, the amplifier output and output switch go ON and liquid crystal driving starts. At the rising edge of STB, the output switch is switched to OFF and the output becomes Hi-Z.
POL	Polarity inversion signal	443	Input	Inverts the output polarity. At the rising edge of RSEL, the polarity inversion signal data is fetched internally. The γ -resistor is switched according to the positive and negative polarity. POL = L: Negative polarity (common high output) POL = H: Positive polarity (common low output)

3.6 Back Panel LCD Controller Driver Control Pins

Pin Symbol	Pin Name	Pin Name	I/O	Description
/CS1	Back panel LCD chip select	470	Output	Active-low chip select signal to the back panel LCD controller driver.
CS2	Back panel LCD chip select	469	Output	Active-high chip select signal to the back panel LCD controller driver.
SCLK_SUB	Serial clock to the back panel LCD	471	Output	Back panel LCD serial data output.
SO_SUB	Outputs serial data to the back panel LCD	472	Output	Outputs serial data to the back panel LCD controller driver.
A0	Back panel LCD data/command control	468	Output	Controls data/command to the back panel LCD controller driver.

3.7 Other Control Pins

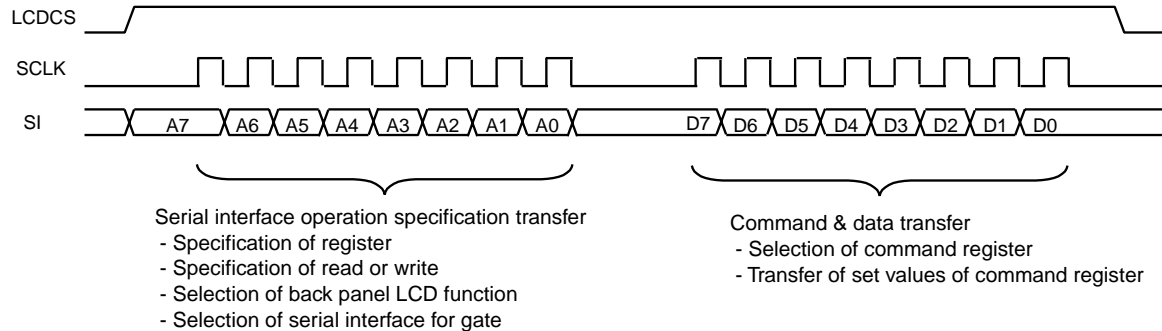
Pin Symbol	Pin Name	Pin Name	I/O	Description
TESTIN1 to TESTIN4	TEST input	515 to 512	Input	Keep this pin low-level or leave it open.
TESTOUT	TEST output	511	Output	Leave this pin open.
TEST_COM2	TEST output	414, 415	Output	Leave this pin open.
TEST_VCLAMP	TEST output	412, 413	Output	Leave this pin open.
★ BGR_O	Hand cap regulator output	416	Output	Leave this pin open.
★ PV _{cc}	Power supply for pull-up	445	–	This is pull-up power supply for mode setting pin.
★ PV _{ss}	Power supply for pull-down	456	–	This is pull-down power supply for mode setting pin.
V _{cc}	Logic supply voltage	427 to 430	–	2.2 to 3.6 V
V _{ss}	Driver ground	327 to 331. 431 to 435	–	Grounding
Dummy	Dummy	1 to 4, 249 to 282, 319 to 326, 419 to 426, 462 to 466, 486 to 490, 526 to 532	–	Dummy pin

Caution To avoid latch-up failure, the sequence when turning on the power must be V_{cc} → logic input → booster voltage for rising → gray-scale power supply (V₀-V₄), and the reverse sequence when turning off the power. Follow this sequence during shift periods as well.

4. REGISTERS

The μPD161831 can set a horizontal period and vertical period by using registers. The serial interface is used to specify a register and set values to it. Figure 4–1 shows a simplified timing chart of the serial interface.

Figure 4–1. Timing Chart of Serial Interface



This serial interface has an 8-bit configuration. Note that it is accessed twice in 8-bit units to set a register.

The first 8-bit data (A7 to A0 in figure 4–1) is transferred to the “serial interface operation specification register”.

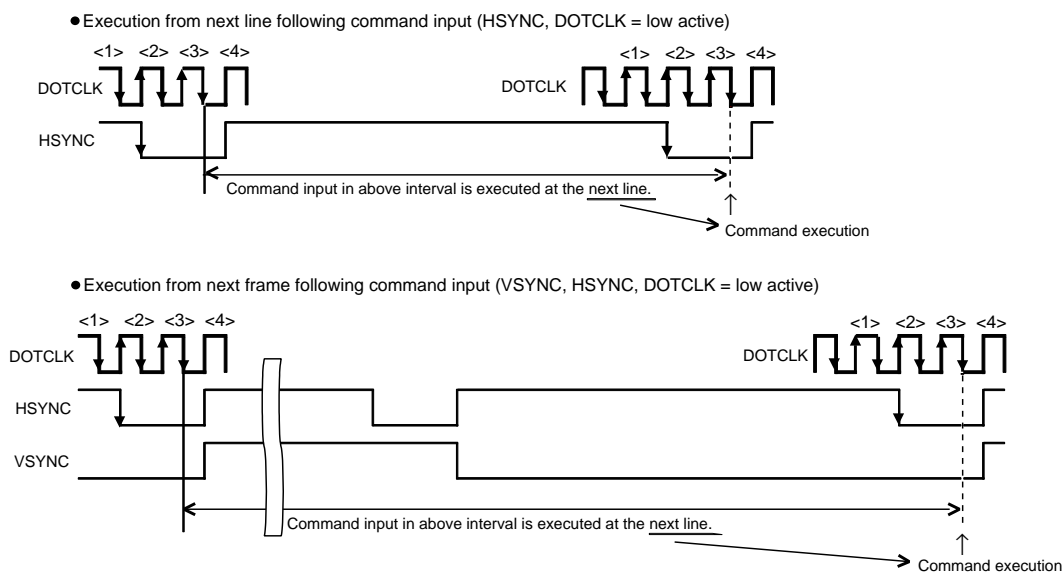
The serial interface operation specification register specifies the transfer operation of the next 8 bits (D7 to D0 in figure 4–1). The second 8-bit data selects a command register or transfers the set value of the command register.

In addition, while writing a setup in command register with the 8-bit transfer + 8-bit (A7 to A0 + D7 to D0) which selects command register or transferring of 8 bit + 8-bit transfer of readings (A7 to A0 + D7 to D0) (a total of 32 bits), continue making chip select (LCDCS) active.

Table 4–1 indicates the function of the serial interface operation specification register. Table 4–2 shows the register number and register name of each command register. Tables 4–3 and 4–5 to 4–24 describe the function of each command register.

When the timing generator is used, there are three execution patterns for each command: Immediate execution following setting, execution at the line following that where command was set, and execution at the frame following that where command was set. In the case of execution at the next line and execution at the next frame, the concrete command execution timing is as follows.

However, when the timing generator is not used, commands are executed at the first falling edge of DCK following command transmission.



4.1 Serial Interface Operation Specification Register

Table 4–1 shows the function of the serial interface operation specification register.

Table 4–1. Function of Serial Interface Operation Specification Register (A7 to A0)

No.	Bit Name	Function
A7	–	–
A6	μPD161831/back panel LCD select	<p>This bit specifies whether data D7 to D0 are data for a register of the μPD161831 or data for the back panel LCD. If D7 to D0 are data for the back panel LCD, the chip select pins for the back panel LCD (/CS1 = L, CS2 = H) are asserted, and data D7 to D0 are output to SUB_SO along with the clock output by SCLK_SUB.</p> <p>0: D7 to D0 are data for a μPD161831 register. 1: D7 to D0 are data for the back panel LCD controller driver.</p>
A5	Read/write select	<p>This bit selects whether the transfer of data D7 to D0 is for a read operation or a write operation. Note, however, that in a read operation, only the registers of the μPD161831 can be read. For the timing chart of the read operation, refer to 5. TIMING GENERATOR NON-USE FUNCTION.</p> <p>0: D7 to D0 are for a write operation. 1: D7 to D0 are for a read operation.</p>
A4	–	–
A3	–	–
A2	–	–
A1	–	–
A0	Command/data select	<p>This bit selects whether data D7 to D0 specify the register number of a command register or are set to a command register.</p> <p>If an access to the back panel LCD controller driver is selected (A6 = 1), the value of this bit is reflected on the A0 pin (when A0 = 0: Low output, when A0 = 1: High output).</p> <p>0: D7 to D0 specify a register number. 1: D7 to D0 are set to a register.</p>

4.2 Command Registers

4.2.1 Command register list

Table 4–2 lists the command registers.

However, each register is read default value when invalid data leads in unused of timing generator.

Table 4–2. Command Register List (1/2)

Register No.	D5 to D0						Register Name	Default Value	Timing Generator Function		Reset		Internal Set Timing
	D5	D4	D3	D2	D1	D0			Use	Not used	Command	Hard	
R0	0	0	0	0	0	0	65,000/260,000 color select	00H	O	–	O	–	F
R1	0	0	0	0	0	1	Horizontal period valid data input start timing	0AH	O	–	O	–	F
R2	0	0	0	0	1	0	Vertical period valid data input start timing	02H	O	–	O	–	F
R3	0	0	0	0	1	1	Horizontal valid pixel data setting	00H	O	–	O	–	C
R4	0	0	0	1	0	0	Standby	00H	O	O	O	–	F
R5	0	0	0	1	0	1	8-color mode	00H	O	O	O	–	L
R6	0	0	0	1	1	0	Setting	02H	O	Δ1	O	Note1	Note2
R7	–	–	–	–	–	–	Use prohibited (Not used)	–	–	–	–	–	–
R8	0	0	1	0	0	0	Amplifier drive period setting	0EH	O	–	O	–	C
R9	0	0	1	0	0	1	Quarter data function	00H	O	O	O	–	F
R10	0	0	1	0	1	1	Level shifter voltage setting	00H	O	O	O	–	C
R11	0	0	1	1	0	0	Common amplitude voltage adjustment D/A converter	0FH	O	O	O	–	C
R12	0	0	1	1	0	1	Common center voltage adjustment D/A converter	35H	O	O	O	–	C
R13, R14	–	–	–	–	–	–	Use prohibited (Not used)	–	–	–	–	–	–
R15	0	0	1	1	1	1	Command reset	00H	O	O	–	–	C
R16 to R23	–	–	–	–	–	–	Use prohibited (Not used)	–	–	–	–	–	–
R24	0	1	1	0	0	0	DC/DC operation setting	00H	O	O	O	O	C
R25	0	1	1	0	0	1	DC/DC step setting	16H	O	O	O	O	C
R26	0	1	1	0	1	0	DC/DC oscillation setting	15H	O	O	O	O	C
R27	0	1	1	0	1	1	Regulator output setting	2AH	O	O	O	O	C
R28	0	1	1	1	0	0	LPM setting	00H	O	O	O	O	C
R29 to R32	–	–	–	–	–	–	Use prohibited (Not used)	–	–	–	–	–	–
R33	1	0	0	0	0	1	DC/DC rise setting	00H	O	O	O	O	C
R34, R35	–	–	–	–	–	–	Use prohibited (Not used)	–	–	–	–	–	–

Remarks 1. O: Enabled, -: Disabled, Δ1: Only bit 3 disabled, Δ2: Only bit 7 enabled

2. The internal set timing is the timing at which the command is enabled.

C: Enabled when command is set

F: Enabled at beginning of frame

L: Enabled at beginning of line

Notes 1. Bit 0 is enabled when line is set. Bit 3 is enabled when frame is set. All other bits are enabled when command is set.

2. Bits 4 and 5 are enabled when hard reset is performed. All other bits are disabled.

Table 4–2. Command Register List (2/2)

Register No.	D5 to D0						Register Name	Default Value	Timing Generator Function		Reset		Internal Set Timing
	D5	D4	D3	D2	D1	D0			Use	Not used	Command	Hard	
R36	1	0	0	1	0	0	RSW_O start timing setting	0FH	O	–	O	–	C
R37	1	0	0	1	0	1	RSW_O end timing setting	1DH	O	–	O	–	C
R38	1	0	0	1	1	0	GSW_O start timing setting	1EH	O	–	O	–	C
R39	1	0	0	1	1	1	GSW_O end timing setting	2CH	O	–	O	–	C
R40	1	0	1	0	0	0	BSW_O start timing setting	2DH	O	–	O	–	C
R41	1	0	1	0	0	1	BSW_O end timing setting	3BH	O	–	O	–	C
R42	1	0	1	0	1	0	EXT1_O start timing setting	0AH	O	–	O	–	C
R43	1	0	1	0	1	1	EXT1_O end timing setting	0AH	O	–	O	–	C
R44	1	0	1	1	0	0	EXT2_O start timing setting	0AH	O	–	O	–	C
R45	1	0	1	1	0	1	EXT2_O end timing setting	0AH	O	–	O	–	C
R46	1	0	1	1	1	0	EXT3_O start timing setting	0AH	O	–	O	–	C
R47	1	0	1	1	1	1	EXT3_O end timing setting	0AH	O	–	O	–	C
R48	1	1	0	0	0	0	EXT1 to EXT3 function setting	80H	O	Δ2	O	–	C
R49	1	1	0	0	0	1	GOE1 start timing setting	04H	O	–	O	–	C
R50	1	1	0	0	1	0	GOE1 end timing setting	38H	O	–	O	–	C
R51	1	1	0	0	1	1	Dummy line setting	00H	O	–	O	–	F
R52, R53	–	–	–	–	–	–	Use prohibited (Not used)	–	–	–	–	–	–
R54	1	1	0	1	1	0	COM2, VCLAMP control	00H	O	O	O	O	C
R55	1	1	0	1	1	1	Test mode setting	00H	O	O	O	–	C
R56 to R255	–	–	–	–	–	–	Use prohibited (Not used)	–	–	–	–	–	–

Remarks 1. O: Enabled, -: Disabled, Δ1: Only bit 3 disabled, Δ2: Only bit 7 enabled

2. The internal set timing is the timing at which the command is enabled.

C: Enabled when command is set

F: Enabled at beginning of frame

L: Enabled at beginning of line

Notes 1. Bit 0 is enabled when line is set. Bit 3 is enabled when frame is set. All other bits are enabled when command is set.

2. Bits 4 and 5 are enabled when hard reset is performed. All other bits are disabled.

4.2.2 65,536/262,144 color select register

This register is used to select the number of colors (65,536 or 262,144 colors) of one pixel and specify the data transfer mode when 262,144 colors are selected.

If transferring 262,144 colors twice is selected, the time required to transfer the data of one pixel is two times longer than that of the first transfer (if the dot clock frequency is the same). To make the frame frequency for the first transfer and the second transfer the same, therefore, increase the dot clock frequency for the second transfer to twice that of the first transfer.

Note also that the setting of this register is reflected from the operation of the next frame after the register is set.

Table 4–3. 65,536/262,144 Color Select Register (R0)

Register Set Value	Function
00H	65,536 colors: 16-bit data is transferred once
01H Note	262,144 colors: 12-bit and 6-bit data are transferred twice.
02H Note	262,144 colors: 9-bit and 9-bit data are transferred twice.
03H	262,144 colors: 18-bit data is transferred once
04H-FFH	Use prohibited

Note The 65,536/262,144 color select register cannot be used in mode that do not use the timing generator.

The relationship between each data transfer mode and the display data input pins (D₀₅ to D₀₀, D₁₅ to D₁₀, and D₂₅ to D₂₀) is shown in the table below. The data input to D₀₅ to D₀₀ is output during the period while BSW_O is active, and the data input to D₂₅ to D₂₀ is output during the period while RSW_O is active.

However, **Red5**, **Green5**, **Blue5** in table 4–4 are the data lines needed to input in 8-color mode.

Table 4–4. Relationship Between Data Transfer Mode and Display Data Input Pins (“–” indicates that input data is invalid)

Display Data Input Pin	65,536 Colors	262,144 Colors				
		One transfer, 18-bit	Two transfers, 12-bit + 6-bit		Two transfers, 9-bit + 9-bit	
			First transfer	Second transfer	First transfer	Second transfer
D ₂₅	Red5	Red5	Red5	Blue5	Red5	Green2
D ₂₄	Red4	Red4	Red4	Blue4	Red4	Green1
D ₂₃	Red3	Red3	Red3	Blue3	Red3	Green0
D ₂₂	Red2	Red2	Red2	Blue2	Red2	Blue5
D ₂₁	Red1	Red1	Red1	Blue1	Red1	Blue4
D ₂₀	– Note	Red0	–	–	–	–
D ₁₅	Green5	Green5	Red0	Blue0	Red0	Blue3
D ₁₄	Green4	Green4	–	–	Green5	Blue2
D ₁₃	Green3	Green3	–	–	Green4	Blue1
D ₁₂	Green2	Green2	Green5	–	Green3	Blue0
D ₁₁	Green1	Green1	Green4	–	–	–
D ₁₀	Green0	Green0	Green3	–	–	–
D ₀₅	Blue5	Blue5	Green2	–	–	–
D ₀₄	Blue4	Blue4	Green1	–	–	–
D ₀₃	Blue3	Blue3	Green0	–	–	–
D ₀₂	Blue2	Blue2	–	–	–	–
D ₀₁	Blue1	Blue1	–	–	–	–
D ₀₀	– Note	Blue0	–	–	–	–

Note It is not necessary to input data to the D₂₀ and D₀₀ pins when 65,536 colors are selected, but amplifier output is performed on the assumption that data input to D₂₅ and D₀₅ is input to D₂₀ and D₀₀.

4.2.3 Horizontal period valid input start timing setting register

This register sets the timing to start inputting the valid data of the horizontal period in HSYNC and VSYNC mode.

It sets the number of dot clocks from the falling edge of the HSYNC signal until the input data becomes valid. If transferring display data twice is selected, set half the number of dot clocks actually needed. Note also that the setting of this register is reflected from the operation of the next frame after the register is set.

Table 4–5. Horizontal Period Valid Input Start Timing Setting Register (R1)

Register Set Value	Number of Dot Clocks
00H	4 clocks
01H	4 clocks
:	:
04H	4 clocks
05H	5 clocks
06H	6 clocks
07H	7 clocks
:	:
FDH	253 clocks
FEH	254 clocks
FFH	255 clocks

4.2.4 Vertical period valid input start timing setting register

This register sets the timing to start inputting the valid data of the vertical period in HSYNC and VSYNC mode.

It sets the number of HSYNC from the falling edge of the VSYNC signal until the input data becomes valid. Note also that the setting of this register is reflected from the operation of the next frame after the register is set.

Table 4–6. Vertical Period Valid Input Start Timing Setting Register (R2)

Register Set Value	Number of HSYNC Signals
00H	2
01H	2
02H	2
03H	3
04H	4
05H	5
06H	6
:	:
FDH	253
FEH	254
FFH	255

4.2.5 Horizontal Valid Pixel Data Register

This register sets the number of valid pixel data during the horizontal period in HSYNC and VSYNC mode. Note also that the setting of this register is reflected from the operation of the next frame after the register is set.

Table 4–7. Horizontal Valid Pixel Data Register (R3)

Register Set Value	Number of Valid Data
00H	240
01H	244
02H	480
03H	488

4.2.6 Standby register

This register is used to set or restore from a standby mode. The data set to bits 7 to 1 of this register is ignored.

When a standby command is input, the μPD161831 performs white display (source output, and V_{ss} level output by COMC) from the next frame following command output. Following the execution of this command, execute the regulator OFF command and the DC/DC converter OFF for the power supply function. Also when standby is canceled, doing the opposite of when standby is input, execute the normal operation command (R4 = "0") after setting both the DC/DC converter and the regulator to ON..

Table 4–8. Standby Register (R4)

Bit 0 Set Value	Mode
0	Normal operation mode
1	Standby mode

4.2.7 8-color mode register

This register is used to select the 8-color mode. The data set to bits 7 to 1 of this register is ignored. The data line that must be input in 8-color mode differs depending on the selection of the 65,000-color mode and 260,000-color transfer mode. For the actual data line to be used, refer to Table 4–4.

Note that the setting of this register is reflected from the operation of the next line after the register is set.

Table 4–9. 8-Color Mode Register (R5)

Bit 0 Set Value	Mode
0	65,000/260,000 colors (R0 register is valid)
1	8-color mode

4.2.8 Setting register

This register is used to set the low power mode and the direction of scanning. Data set to bits 6 and bit7 of these register are ignored.

Table 4–10. Setting Register (R6)

Bit Name	Mode
Bit 0	Adjusts the driver bias current of the μ PD161831 to enter the low power mode. Since the through rate of the operational amplifier inside the IC changes, be sure to carefully perform panel evaluation. Note that the setting of this bit is reflected from the operation of the next line after the register values are set. Bit 0 = 0: Driver output low power mode Bit 0 = 1: Normal mode
Bit 1	Selects the scanning direction by using the GRL_O and GSTB_O pins. This bit becomes valid as soon as it is set. <u>Therefore, it must be set after gate scanning of one frame has been completed and before scanning of the next frame is started.</u> The setting of this bit is reflected in the operation immediately after the register is set. Bit 1 = 0: Reverse scan (scanning from bottom to top, GRL_O = L output) Bit 1 = 1: Forward scan (scanning from top to bottom, GRL_O = H output)
Bit 2	Selects whether the display data input to the μ PD161831 is input from S ₃ to S ₂₄₂ , or vice versa. <240 output selection> Bit2 = 0: S ₂₄₂ → S ₃ Bit2 = 1: S ₃ → S ₂₄₂ <244 output selection> Bit2 = 0: S ₂₄₄ → S ₁ Bit2 = 1: S ₁ → S ₂₄₄ The relationship between the input data and output pin is as follows: The setting of this bit is reflected in the operation immediately after the register is set.
Bit 3	Selects whether the line or frame is inverted. In the 8-color mode, the power consumption can be further reduced by selecting frame inversion. The setting of this bit is reflected from the operation of the next line after the register is set. Bit 3 = 0: Line inversion Bit 3 = 1: Frame inversion
Bit 4	Performs GOE1 output control. When bit 4 = 0, a Low level is forcibly output to GOE1. Bit 4 = 0: Forcible output of low level to GOE1. Bit 4 = 1: Normal operation
Bit 5	Controls ON/OFF switching of square wave output from the COMC pin. Bit 5 = 0: Output V _{ss} level Bit 5 = 1: Output square wave
Bit 6, bit 7	Use prohibited

4.2.9 Amplifier drive period setting register

In the μPD161831, the amplifier drive period is set with the horizontal period address count (HCNT) as the driver output. The amplifier drive period set with this register is the drive period of R, G, and B, respectively, when division by 3 is performed. The amplifier drive start timing is the RGW_O, GSW_O, and BSW_O signal start timing. For detail, refer to figures 4–2 through 4–6.

Note that the setting of this register is reflected to the operation immediately after the register is set. The effective bits of this register are bit 0 to bit 4.

Figure 4–7 indicates how the amplifier of the μPD161831 is driven.

Table 4–11. Amplifier Drive Period Setting Register (R8)

Register Set Value	Horizontal Period Address Count
00H	0
01H	1
02H	2
03H	3
04H	4
:	:
1DH	29
1EH	30
1FH	31

Figure 4–2. Horizontal Period Amplifier Drive Timing and GCK/GOE1 Signal Output Timing
(When line inversion is set: When VSYNC signal is active)

μPD161831 display timing chart <line inversion, 240 outputs, VSYNC width = 1H, valid in horizontal period valid data input timing (R1) = 16, vertical period valid data input timing (R2) = 2, no dummy lines>
VSYNC (width = 1H) line

Display CLK address value (HCNT) is four times cycling in DOTCLK
Display CLK address value (HCNT) can be set up to 1-58 (0, 59, and 59 or more addresses prohibited).
When all 240 or more CLK are put in 1H period, it is added after display CLK address value (HCNT) 58 address.

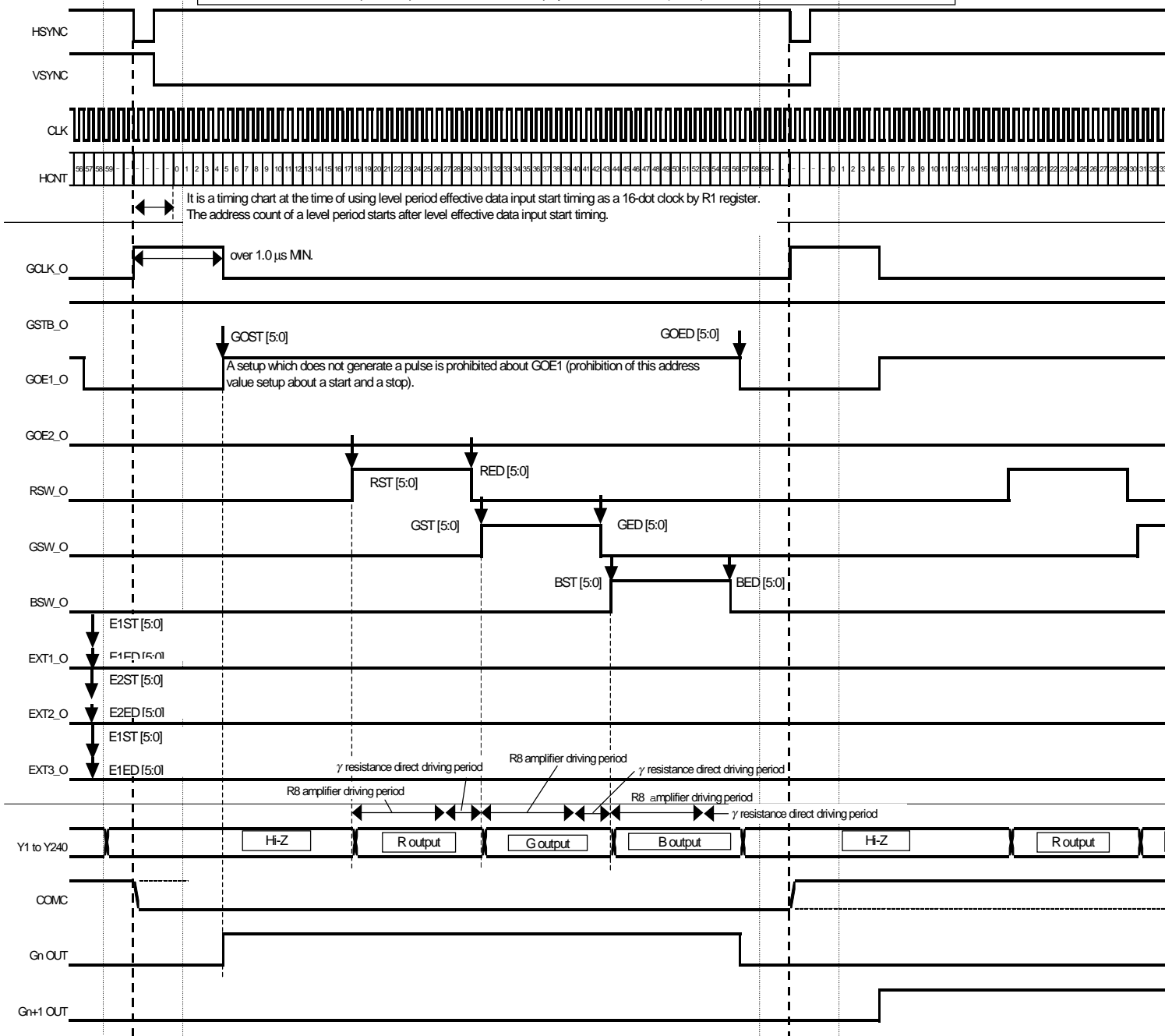


Figure 4–3. Horizontal Period Amplifier Drive Timing and GCK/GOE1 Signal Output Timing
(When line inversion is set: Line immediately after VSYNC to valid data input start line)

μ PD161831 display timing chart <line inversion, 240 outputs, VSYNC width = 1H, horizontal period valid data input timing (R1) = 16, vertical period valid data input timing (R2) = 2, no dummy line>
Line right after VSYNC to valid data input start line

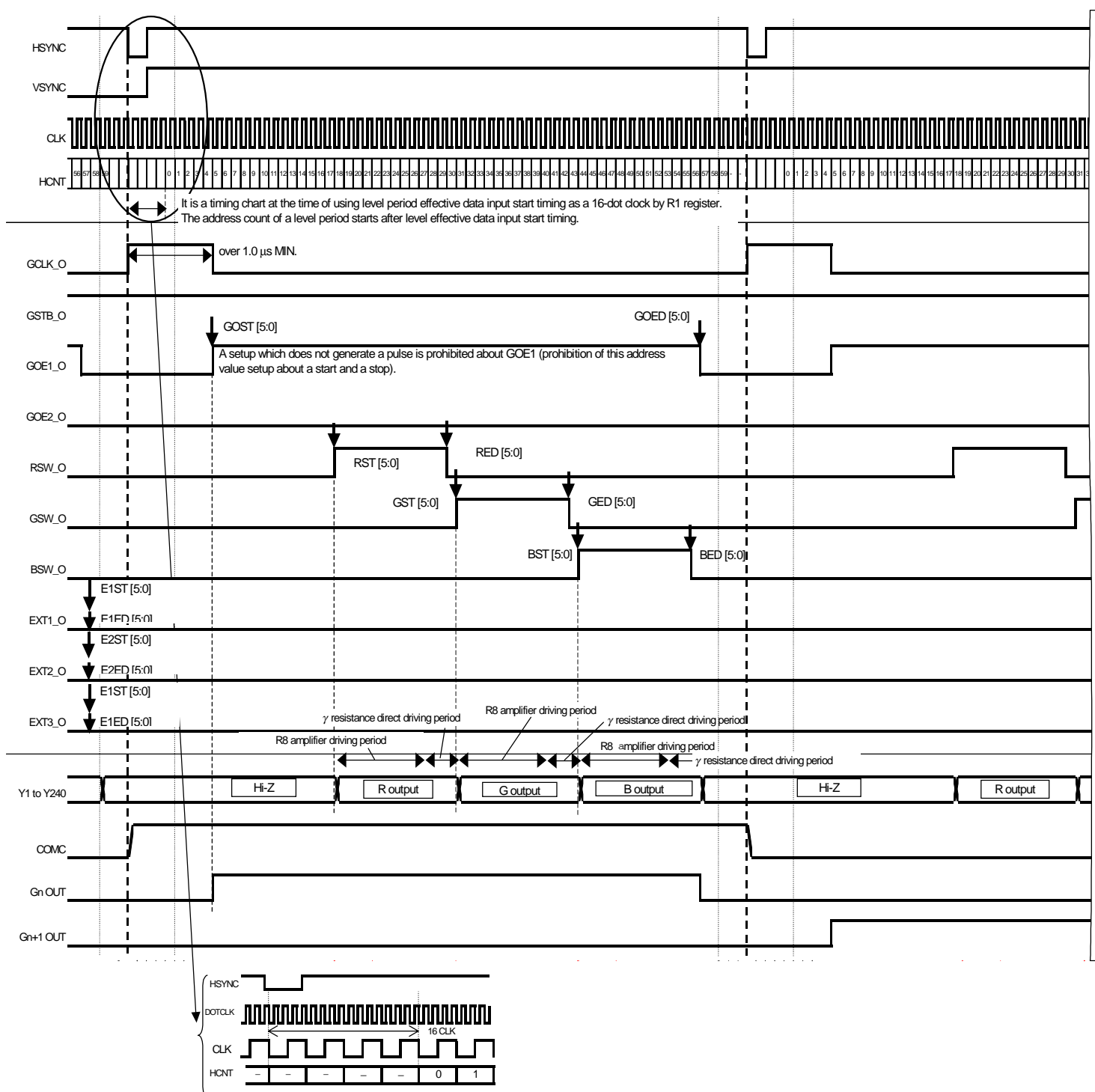
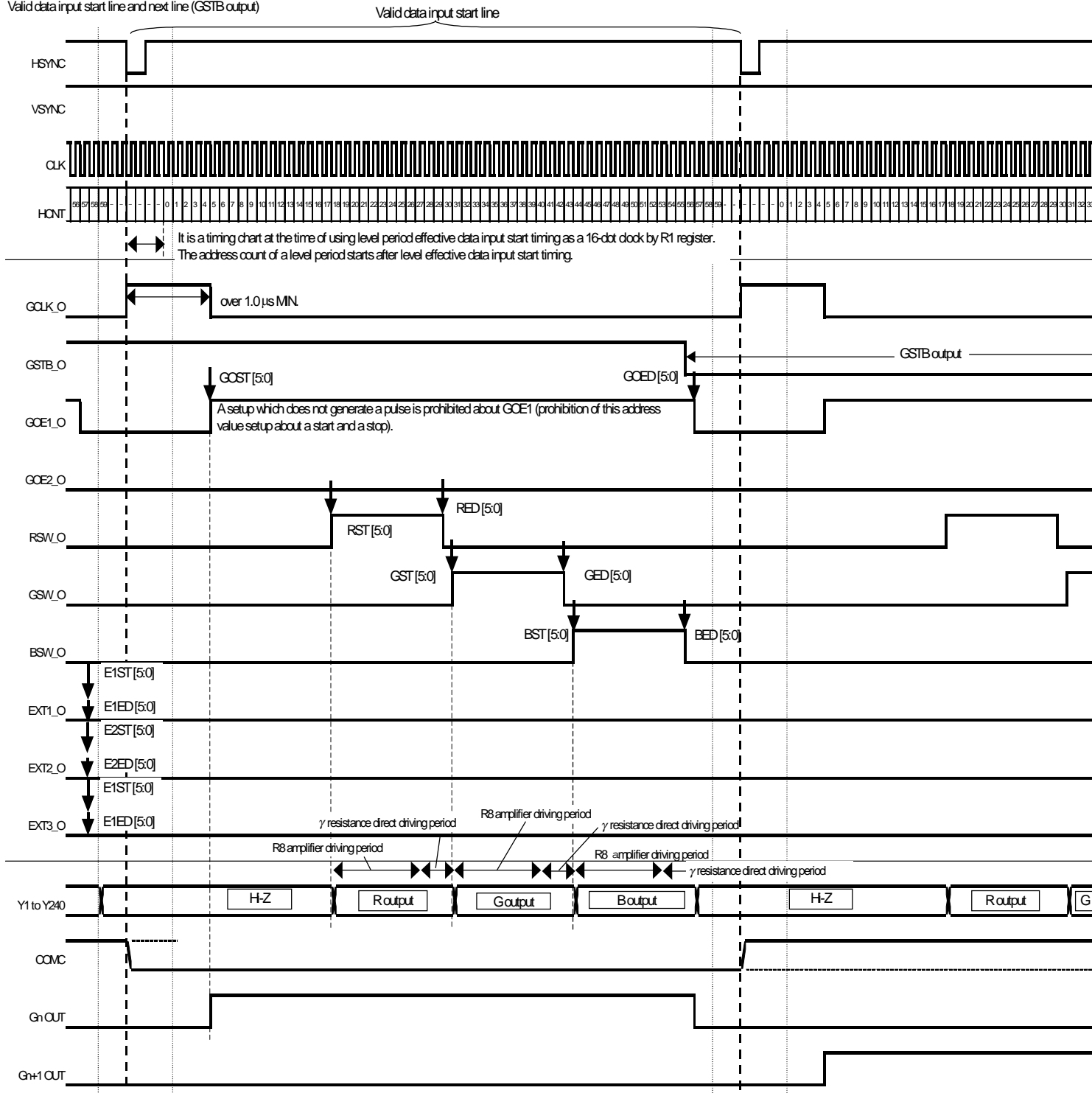


Figure 4-4. Horizontal Period Amplifier Drive Timing and GCK/GOE1 Signal Output Timing
(When line inversion is set: Laid data input start line to GSTB output line)

μPD161831 display timing chart <line inversion, 240 outputs, VSYNC width = 1H, horizontal period valid data input timing (R1) = 16, vertical period valid data input timing (R2) = 2, no dummy line>
Valid data input start line and next line (GSTB output)



**Figure 4-5. Horizontal Period Amplifier Drive Timing and GCK/GOE1 Signal Output Timing
(When frame inversion is set, positive polarity)**

μPD161831 display timing chart (frame inversion/positive polarity, 240 output)

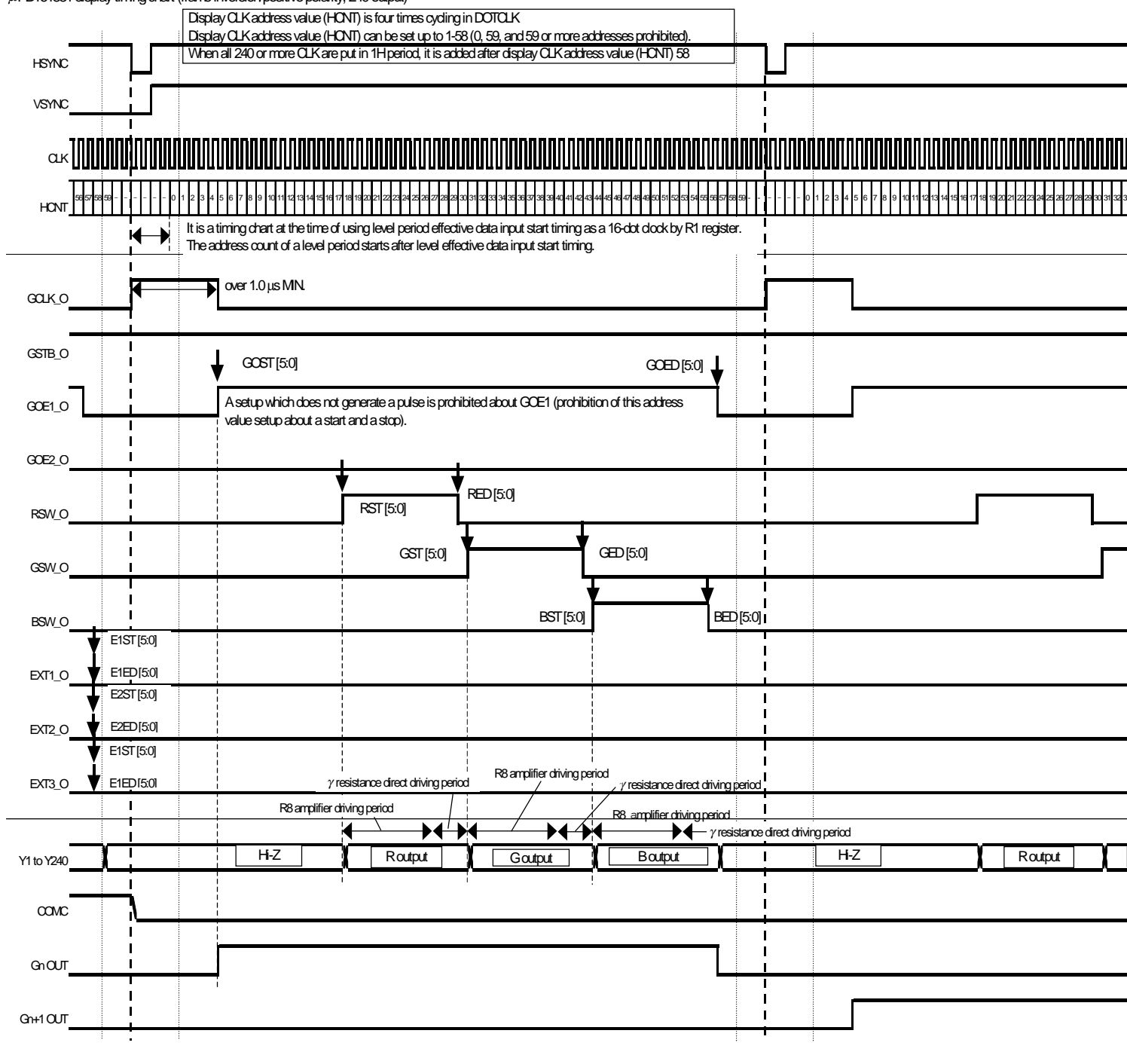
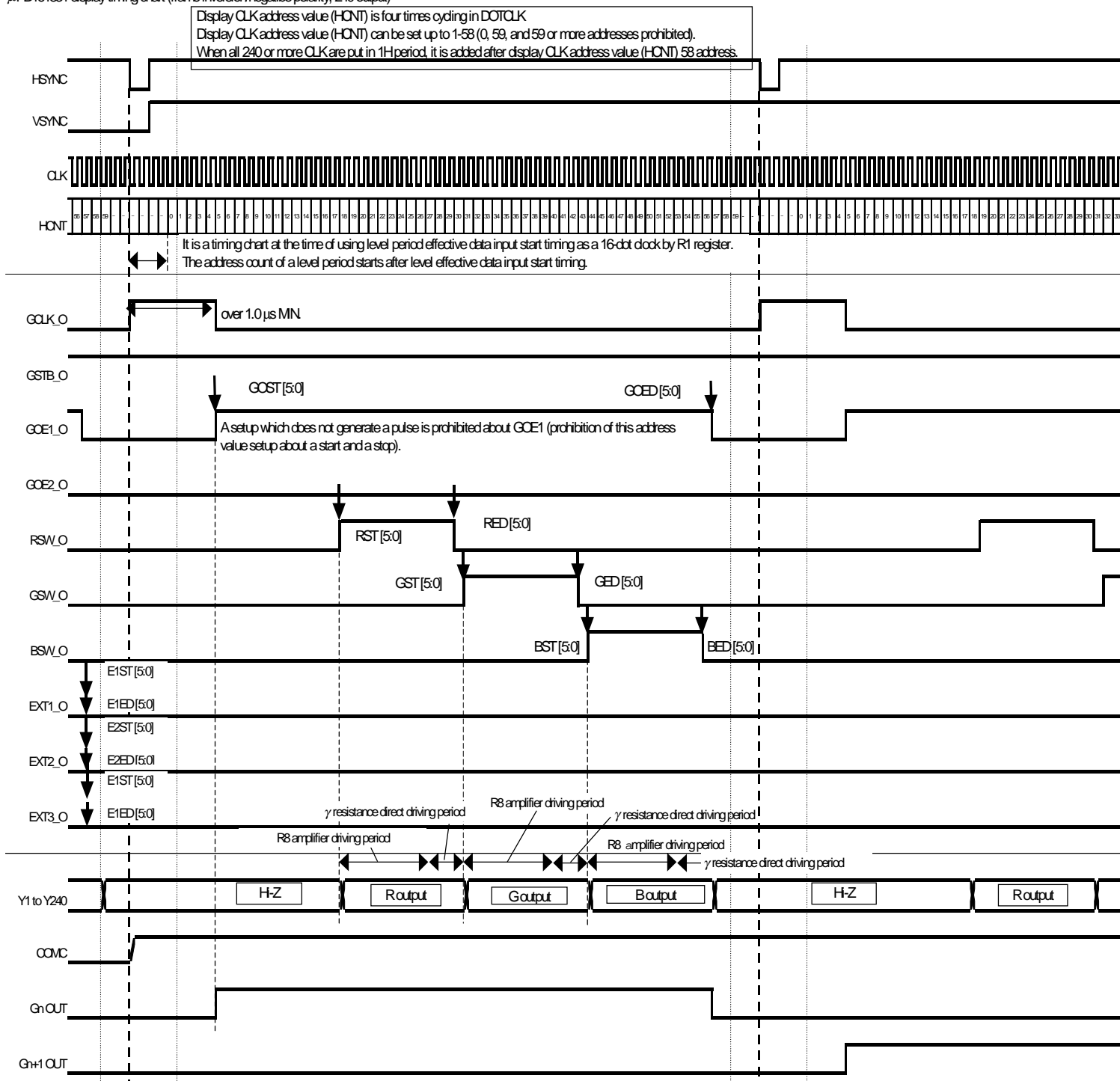


Figure 4-6. Horizontal Period Amplifier Drive Timing and GCK/GOE1 Signal Output Timing
(When frame inversion is set, negative polarity)

μPD161831 display timing chart (frame inversion/negative polarity, 240 output)



The LCD driver circuit of the μPD161831 consists of “ γ resistor”, “ γ select switch”, “D/A converter”, and “output stage”, as shown below. The following amplifier drive period can be selected by using R8, the amplifier drive period setting register.

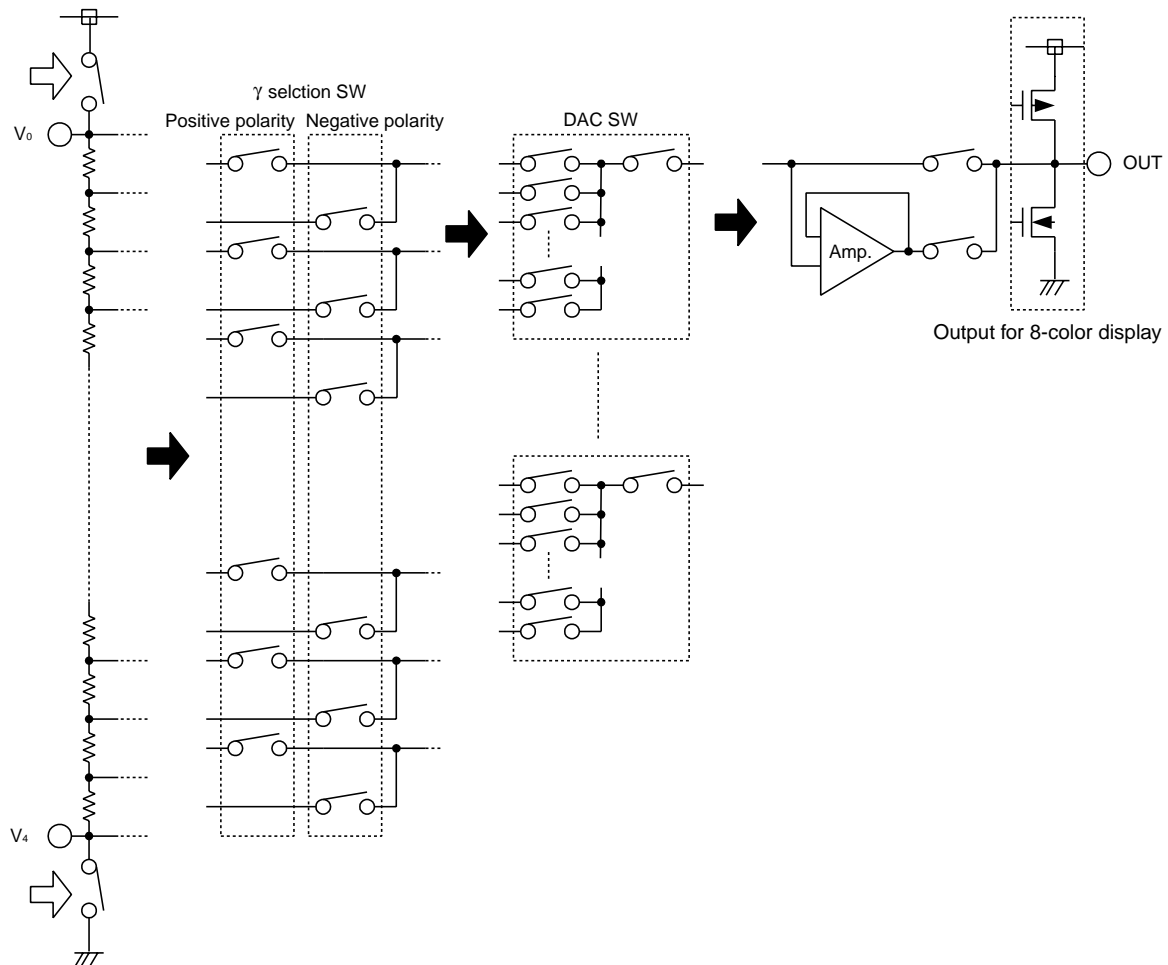
γ resistor : String resistor for γ curve

γ select switch: Selects γ curve during positive pole or negative pole driving

D/A converter: Selects the output voltage level from display data.

Output stage : Consists of a driving amplifier, a switch for voltage hold driving, and an inverter for 8-color display.

Figure 4-7. Output circuit image of Amplifier Drive Operation



4.2.10 Quarter data function register

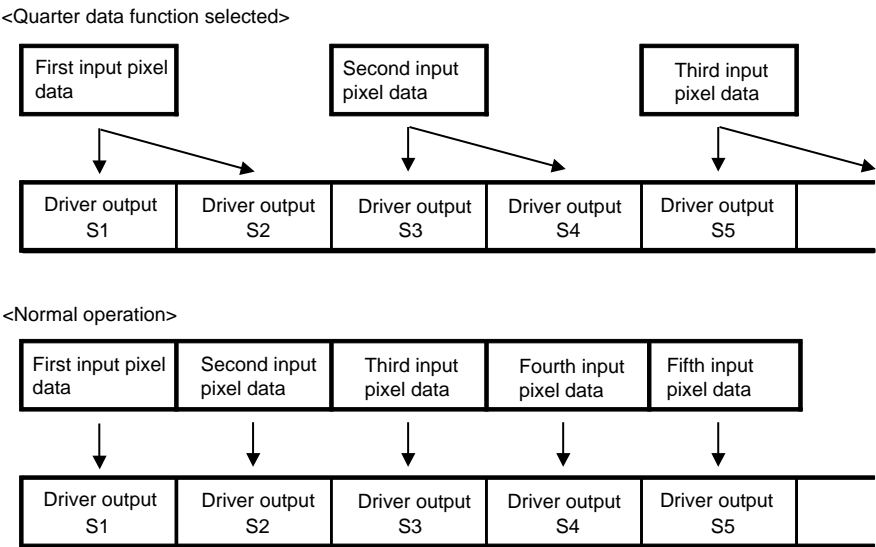
The quarter data function is selected with the bit 0 setting.

Table 4–12. Quarter Data Function Register (R9)

Bit 0	Mode
0	Normal operation
1	Quarter data function operation

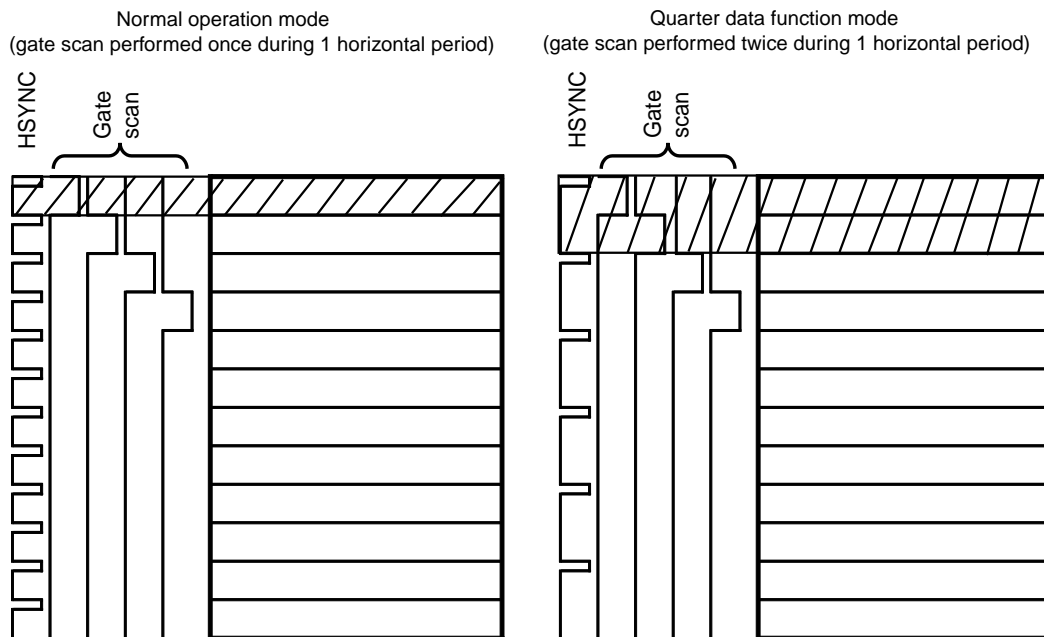
When the quarter data function is selected, one pixel of input data is also used as the neighboring 1 pixel of data. The data that is next input externally becomes the pixel data after the neighboring 1-pixel data mentioned above.

Figure 4–8. Quarter Data Function



Moreover, when the quarter data function is selected, 2-lines' worth of data output are gate scanned during the horizontal period corresponding to 1 line.

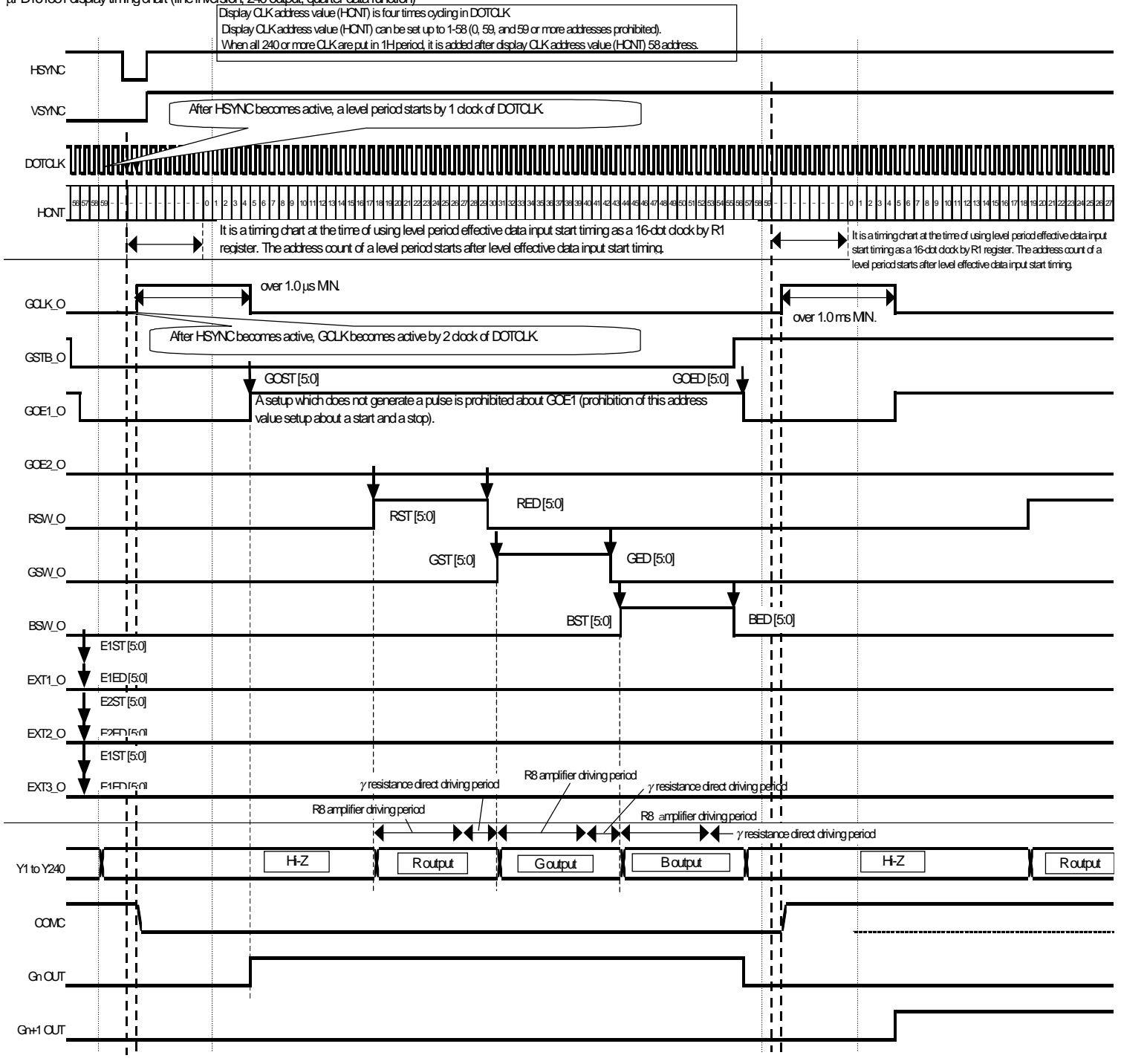
Figure 4-9. Gate Scan Operation when Quarter Data Function is Selected



The horizontal period timing is as follows.

Figure 4–10. Horizontal Period Timing Chart when Quarter Data Function is Selected

μPD161831 display timing chart (line inversion, 240 output, quarter data function)



As an image, in order to perform display of 240 outputs x 320 lines during normal operation, 240 outputs x 640 lines of data are input, but when the quarter data function is selected, in order to perform display of 240 outputs x 320 lines, just 120 outputs x 160 lines of data can be input.

While display is less fine compared to during normal operation, the input data is just one fourth the amount during normal operation, and transfer data can be reduced during moving picture display.

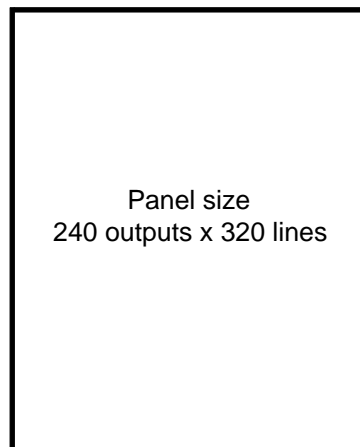
<Normal operation>

Amount of data required to display 1 screen
= 240 outputs x 320 lines



<Quarter data function selected>

Amount of data required to display 1 screen
= 120 outputs x 160 lines



4.2.11 Level shifter voltage setting register

Then negative voltage level of the level shifter is set by setting bit 0 and bit1.

The circuit block of the level shifter is divided into the gate control signal side (GCLK_O, GSTB_O, GOE1_O, GOE2_O) and the driver output related signal side (RSW_O, GSW_O, BSW_O, EXT1_O to EXT3_O), and the negative voltage side voltage level can be selected individually for the gate control signal side and the driver output related signal side between either V_{SS1} and V_{SS2} with the R11 register.

The data set to bit 1 and bit 2 is ignored. Note that the setting of this register is reflected to the operation immediately after the register is set.

Table 4–13. Level Shifter Voltage Setting Register (R10)

Bit Name	Mode
Bit 0	Sets the voltage level on the negative voltage side of the gate output control signals (GCLK_O, GSTB_O, GOE1_O, GOE2_O). Bit 0 = 0: V _{SS2} level Bit 0 = 1: V _{SS1} level
Bit 1	Sets the voltage level on the negative voltage side of the driver output related signals (RSW_O, GSW_O, BSW_O, EXT1_O to EXT3_O) Bit 1 = 0: V _{SS2} level Bit 1 = 1: V _{SS1} level

4.2.12 Common amplitude voltage adjustment D/A converter register

The common amplitude voltage can be selected by setting bit 0 to bit 3 of the R11 register.

The voltage between $(34/50) \cdot V_s$ and $(49/50) \cdot V_s$ is divided by the 4-bit D/A converter. Note that the setting of this register is reflected to the operation immediately after the register is set.

4.2.13 Common center voltage adjustment D/A converter register

The common center voltage can be selected by setting bit 0 to bit 6 of the R12 register. The voltage between 0 (V) and $0.6 \cdot V_s$ (V) is divided by the 7-bit D/A converter. Note that the setting of this register is reflected to the operation immediately after the register is set.

4.2.14 Command reset register

Bit 0 of this register is used to initialize the command register. Data set to bit 1 to bit 7 is ignored. Command reset is automatically cleared after it is set. The setting of this bit is reflected in the operation immediately after the register is set.

Table 4–14. Command Reset Register (R15)

Bit 0	Mode
0	Normal operation
1	Command reset

4.2.15 DC/DC operation setting register

The register is used to switch ON/OFF the DC/DC converter controls and switch ON/OFF boosting of each power supply.

Table 4–15. DC/DC Operation Setting Register (R24)

Bit Name	Mode
Bit 0 <DCON>	Controls ON/OFF in DC/DC converter. Bit 0 = 0: DC/DC converter OFF Bit 0 = 1: DC/DC converter ON
Bit 1	Use prohibited
Bit 2 <VD2ON>	Control ON/OFF in V_{DD2} booster. Bit 2 = 0: V_{DD2} booster OFF Bit 2 = 1: V_{DD2} booster ON
Bit 3 <VDC2ON>	Control ON/OFF in V_{DC2} booster. Bit 3 = 0: V_{DC2} booster OFF Bit 3 = 1: V_{DC2} booster ON
Bit 4 <VS1ON>	Control ON/OFF in V_{SS1} booster. Bit 4 = 0: V_{SS1} booster OFF Bit 4 = 1: V_{SS1} booster ON
Bit 5 <VS2ON>	Control ON/OFF in V_{SS2} booster. Bit 5 = 0: V_{SS2} booster OFF Bit 5 = 1: V_{SS2} booster ON
Bit 6 <RGONR>	Control ON/OFF in V_R regulator. Bit 6 = 0: V_R regulator OFF Bit 6 = 1: V_R regulator ON
Bit 7	Use prohibited

4.2.16 DC/DC step setting register

This register is used to set the boost step, etc., of the DC/DC converter.

Table 4-16. DC/DC Step Setting Register (R25)

Bit Name	Mode
Bit 0: V _{CD2}	Selects the number of boost steps for V _{DC2} . V _{CD2} = 0: V _{DC2} = V _{DC} × 2 V _{CD2} = 1: V _{DC2} = V _{DC} × 3
Bit 1: V _{Ms}	Selects the boost mode for V _{DC2} . V _{Ms} = 0: Single boosting mode V _{Ms} = 1: Dual boosting mode
Bit 2: VRSEL0 Bit 3: VRSEL1 Bit 4: VRSEL2	Selects the V _R regulator's output voltage. <VRSEL0 = 0, VRSEL1 = 0, VRSEL2 = 0>: V _R = 3.0 V <VRSEL0 = 1, VRSEL1 = 0, VRSEL2 = 0>: V _R = 3.5 V <VRSEL0 = 0, VRSEL1 = 1, VRSEL2 = 0>: V _R = 4.0 V <VRSEL0 = 1, VRSEL1 = 1, VRSEL2 = 0>: V _R = 4.5 V <VRSEL0 = 0, VRSEL1 = 0, VRSEL2 = 1>: V _R = 4.75 V <VRSEL0 = 1, VRSEL1 = 0, VRSEL2 = 1>: V _R = 5.0 V <VRSEL0 = 0, VRSEL1 = 1, VRSEL2 = 1>: V _R = 5.25 V <VRSEL0 = 1, VRSEL1 = 1, VRSEL2 = 1>: V _R = 5.5 V
Bit 5 to bit7	Use prohibited

4.2.17 DC/DC oscillation setting register

This register is used to set the boost frequency, etc., of the DC/DC converter.

Table 4-17. DC/DC oscillation setting register (R26)

Bit Name	Mode												
Bit 0: FS0 Bit 1: FS1	Selects the V _{DC2} boost frequency when other an the power supply function low-power mode is selected. <FS0 = 0, FS1 = 0>: f _{osc} /2, <FS0 = 1, FS1 = 0>: f _{osc} /4 <FS0 = 0, FS1 = 1>: f _{osc} /8, <FS0 = 1, FS1 = 1>: f _{osc} /16												
Bit 2: FS2 Bit 3: FS3	Selects the V _{DD2} , V _{SS1} , V _{SS2} boost frequency when other than the low-power supply function power mode is selected. <FS2 = 0, FS3 = 0>: f _{osc} /2, <FS2 = 1, FS3 = 0>: f _{osc} /4 <FS2 = 0, FS3 = 1>: f _{osc} /8, <FS2 = 1, FS3 = 1>: f _{osc} /16												
Bit 4: CLS0 Bit 5: CLS1 Bit 6: CLS2	Selects the internal oscillation frequency of the DC/DC converter function. <CLS0 = 0, CLS1 = 0, CLS2 = 0>: f _{osc} = 12.5 kHz, DCCLK: Open <CLS0 = 1, CLS1 = 0, CLS2 = 0>: f _{osc} = 15 kHz, DCCLK: Open <CLS0 = 0, CLS1 = 1, CLS2 = 0>: f _{osc} = 20 kHz, DCCLK: Open <CLS0 = 1, CLS1 = 1, CLS2 = 0>: External clock DCCLK input mode <CLS0 = 0, CLS1 = 0, CLS2 = 1>: External clock DCK 128 cycle mode <CLS0 = 1, CLS1 = 0, CLS2 = 1>: External clock DCK 256 cycle mode												
Bit 7: FUP	Selects the internal oscillation frequency of the DC/DC converter function. <table><tr><td></td><td>Internal Oscillation</td><td>External DCK 128 Cycles</td><td>External DCK 256 Cycles</td></tr><tr><td>FUP = 0</td><td>f_{osc}</td><td>DCK/128</td><td>DCK/256</td></tr><tr><td>FUP = 1</td><td>f_{osc} x 2</td><td>DCK/64</td><td>DCK/128</td></tr></table>		Internal Oscillation	External DCK 128 Cycles	External DCK 256 Cycles	FUP = 0	f _{osc}	DCK/128	DCK/256	FUP = 1	f _{osc} x 2	DCK/64	DCK/128
	Internal Oscillation	External DCK 128 Cycles	External DCK 256 Cycles										
FUP = 0	f _{osc}	DCK/128	DCK/256										
FUP = 1	f _{osc} x 2	DCK/64	DCK/128										

4.2.18 Regulator output setting register

This register is used to switch the regulator ON/OFF, set the output voltage, etc.

Table 4–18. Regulator Output Setting Register (R27)

Bit Name	Mode
Bit 0: RGON	Controls V_S regulator ON/OFF. RGON = 0: V_S regulator OFF RGON = 1: V_S regulator ON
Bit 1: VSEL0 Bit 2: VSEL1 Bit 3: VSEL2	Selects the V_S regulator output voltage. <VSEL0 = 0, VSEL1 = 0, VSEL2 = 0>: V_S = 3.0 V <VSEL0 = 1, VSEL1 = 0, VSEL2 = 0>: V_S = 3.5 V <VSEL0 = 0, VSEL1 = 1, VSEL2 = 0>: V_S = 4.0 V <VSEL0 = 1, VSEL1 = 1, VSEL2 = 0>: V_S = 4.5 V <VSEL0 = 0, VSEL1 = 0, VSEL2 = 1>: V_S = 4.75 V <VSEL0 = 1, VSEL1 = 0, VSEL2 = 1>: V_S = 5.0 V <VSEL0 = 0, VSEL1 = 1, VSEL2 = 1>: V_S = 5.25 V <VSEL0 = 1, VSEL1 = 1, VSEL2 = 1>: V_S = 5.5 V
Bit 4: EXRV	Selects whether to use an external resistor for the V_S regulator. EXRV = 0: Internal resistor mode EXRV = 1: Connect external resistor to MV_S and set voltage to any desired value.
Bit 5: ACS0 Bit 6: ACS1	Selects the V_R and V_S amplifier current. <ACS0 = 0, ACS1 = 0>: Amp. current = 5 μA <ACS0 = 1, ACS1 = 0>: Amp. current = 10 μA <ACS0 = 0, ACS1 = 1>: Amp. current = 15 μA <ACS0 = 1, ACS1 = 1>: Amp. current = 30 μA
Bit 7	Use prohibited

4.2.19 Power supply function LPM setting register

This register is used to set the power supply function low-power mode, etc.

Table 4–19. Power Supply Function LPM Setting Register (R28)

Bit Name	Mode
Bit 0: LPM	Controls the power supply function low-power mode LPM = 0: Normal mode LPM = 1: Low power mode
Bit 1: LFS0 Bit 2: LFS1	Selects the V_{DC2} boost frequency when the power supply function low-power mode is selected. <LFS0 = 0, LFS1 = 0>: $f_{osc}/8$, <LFS0 = 1, LFS1 = 0>: $f_{osc}/16$ <LFS0 = 0, LFS1 = 1>: $f_{osc}/32$, <LFS0 = 1, LFS1 = 1>: $f_{osc}/64$
Bit 3: LFS2 Bit 4: LFS3	Selects the V_{DD2} , V_{SS1} , and V_{SS2} boost frequency when the power supply function low-power mode is selected. <LFS2 = 0, LFS3 = 0>: $f_{osc}/8$, <LFS2 = 1, LFS3 = 0>: $f_{osc}/16$ <LFS2 = 0, LFS3 = 1>: $f_{osc}/32$, <LFS2 = 1, LFS3 = 1>: $f_{osc}/64$
Bit 5: LACS0 Bit 6: LACS1	Selects the V_R and V_S amplifier current. <LACS0 = 0, LACS1 = 0>: Amp. current = 1.25 μA <LACS0 = 1, LACS1 = 0>: Amp. current = 2.5 μA <LACS0 = 0, LACS1 = 1>: Amp. current = 5.0 μA <LACS0 = 1, LACS1 = 1>: Amp. current = 7.5 μA
Bit 7	Use prohibited

4.2.20 DC/DC startup setting register

This register is used to set the DC/DC startup time, startup mode, etc.

Table 4–20. DC/DC startup Setting Register (R33)

Bit Name	Mode
Bit 0: PUPT0 Bit 1: PUPT1	Sets the V_{DC2} , V_{DD2} , V_{SS1} , and V_{SS2} ON time at DC/DC startup. This bit is effective only when $PONM = 1$. For the startup time, refer to table 4–21.
Bit 2: DUPF0 Bit 3: DUPF1	Sets the DC/DC operating frequency at DC/DC startup. This bit is effective only when bit 5 ($PONM$) = 0 and bit 4 (PON) = 1 are set. <DUPF0 = 0, DUPF1 = 0>: $f_{osc}/8$, <DUPF0 = 1, DUPF1 = 0>: $f_{osc}/16$ <DUPF0 = 0, DUPF1 = 1>: $f_{osc}/32$, <DUPF0 = 1, DUPF1 = 1>: $f_{osc}/64$
Bit 4: PON	Selects the operating frequency at V_{DC2} , V_{DD2} , V_{SS1} , and V_{SS2} rise at startup. $PONM = 0$ is only valid. $PON = 0$: Normal operation $PON = 1$: Rising operation
Bit 5: PONM	Selects the DC/DC startup operation's internal sequence and external sequence. $PONM = 0$: External sequence $PONM = 1$: Internal sequence
Bit 6, bit7	Use prohibited

Table 4–21. DC/DC Rising Time Selection

PONM	PON	PUPT0	PUPT1	VDC2ON	RGONR	VS1/2ON	VD2ON	Remark
1	X	0	0	$16/f_{osc}$	$2048/f_{osc}$	$1.5 \times 2048/f_{osc}$	$2.5 \times 2048/f_{osc}$	Use internal sequence
1	X	1	0	$16/f_{osc}$	$256/f_{osc}$	$1.5 \times 256/f_{osc}$	$2.5 \times 256/f_{osc}$	Use internal sequence
1	X	0	1	$16/f_{osc}$	$512/f_{osc}$	$1.5 \times 512/f_{osc}$	$2.5 \times 512/f_{osc}$	Use internal sequence
1	X	1	1	$16/f_{osc}$	$1024/f_{osc}$	$1.5 \times 1024/f_{osc}$	$2.5 \times 1024/f_{osc}$	Use internal sequence
0	1	X	X	External input	External input	External input	External input	Use external sequence
0	0	X	X					Normal mode

Remark X: 0 or 1

4.2.21 Driver output related control signal registers (R36 to R47)

These registers set the start timing and the end timing of the active period of the RSW_O, GSW_O, BSW_O, EXT1_O to EXT3_O signals, with the clock obtained by dividing a 1-line horizontal period by 4 as the reference (reference clock of 60 clocks in the case of 1 line consisting of 240 pixels of data). The effective bits of these registers are bit 0 to bit 5, respectively. (Values up to 01H to 3BH can be set.)

4.2.22 EXT1 to EXT3 function setting register

EXT1_O outputs each line signal at the timing set with R42 and R43, but for EXTR2_O and EXT3_O, the output cycle can be selected depending on the positive polarity and negative polarity of the common. Table 4–22 shows the concrete details.

Moreover, the RSW_O, BSW_O, GSW_O inverted signals can be selected for EXT1_O to EXT3_O.

Table 4–22. EXT1 to EXT3 Function Setting Register (R48)

Bit Name	Mode
Bit 0	Sets the EXT2_O output during line inversion. Bit 0 = 0: Outputs every line Bit 0 = 1: Outputs only line when common is positive.
Bit 1	Sets the EXT2_O output during frame inversion. Bit 1 = 0: Outputs every line Bit 1 = 1: Outputs only the first display line for frames when the common is positive.
Bit 2	Sets the EXT3_O output during line inversion. Bit 2 = 0: Output every line Bit 2 = 1: Output only lines when the common is negative.
Bit 3	Sets the EXT3_O output during frame inversion. Bit 3 = 0: Output every line Bit 3 = 1: Outputs only the first display line for frames when the common is negative.
Bit 4 to bit 6	Use prohibited
Bit 7	Selects the mode for outputting the RSW_O, GSW_O, and BSW_O inverted signals from EXT1_O to EXT3_O. Bit 7 = 0: Executes the operation set to bit 0 to bit 3. Bit 7 = 1: Outputs the RSW_O, GSW_O, and BSW_O inverted signals from EXT1_O to EXT3_O. EXT1_O = /RSW_O, EXT2_O = /GSW_O, EXT3_O = /BSW_O

4.2.23 GOE1 signal setting registers (R49, R50)

These registers set the start timing (R49) and the end timing (R50) of the active period of the GOE1_O signal, with the clock obtained by dividing the 1-line horizontal period by 4 as the reference (reference clock of 60 clocks in the case of 1 line consisting of 240 pixels of data).

4.2.24 Dummy line setting register (R51)

This register is used to set whether to perform dummy output to the first line of a frame. In the case of a dummy line, the data input in the immediately preceding line is output. Refer to figure 4–11 and figure 4–12.

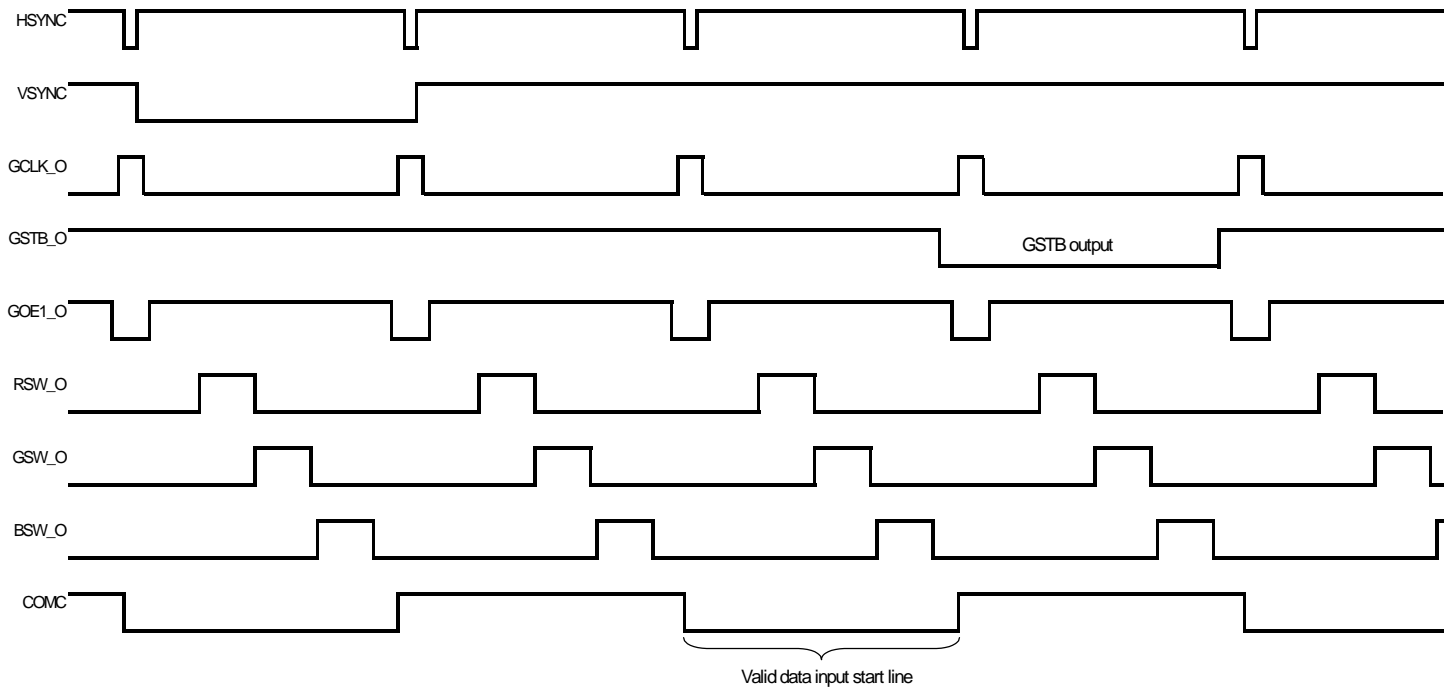
Table 4–23. Dummy Line Setting Register (R51)

Bit 0	Mode
0	Dummy line
1	No dummy line

Figure 4–11. Vertical Period GSTB (Top: No dummy line, bottom: Dummy line)

μPD161831 display timing chart <line inversion, 240 output, VSYNC width = 1H, vertical period valid data input timing (R2) = 2>

1) no dummy line



2) dummy line

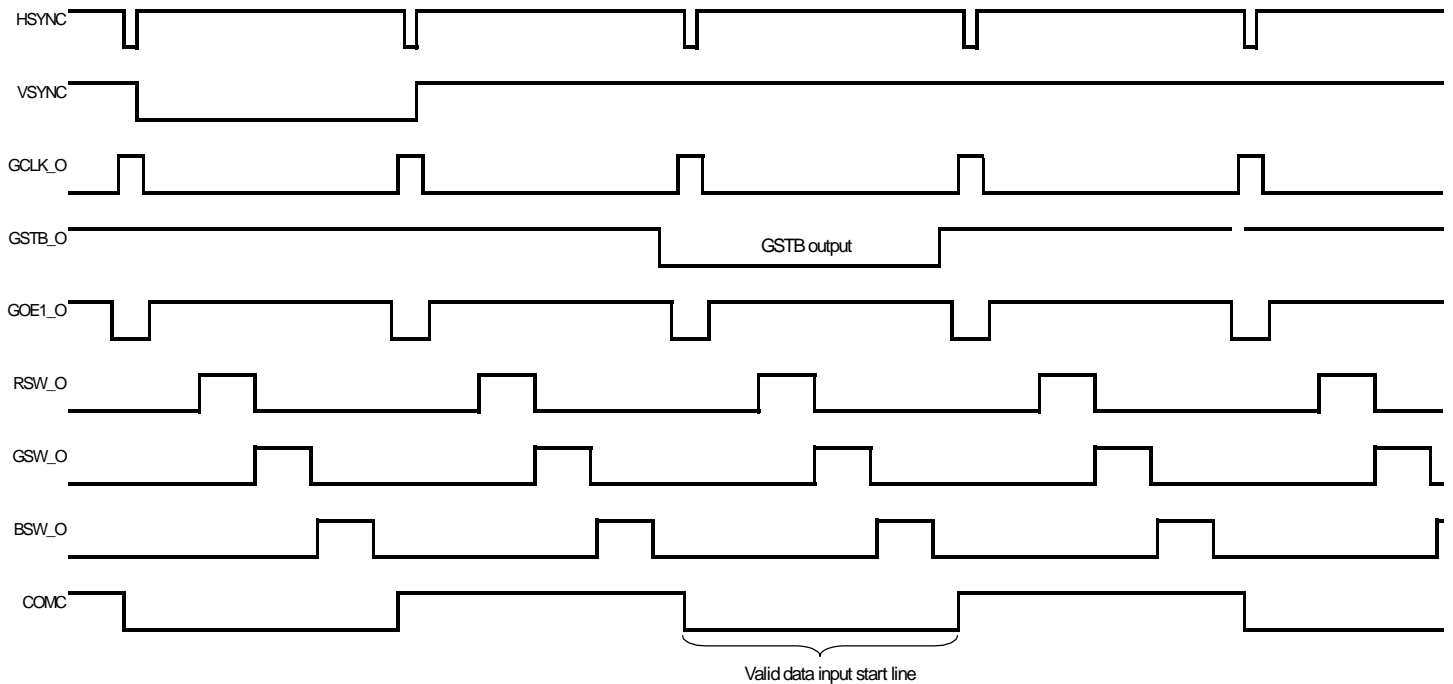
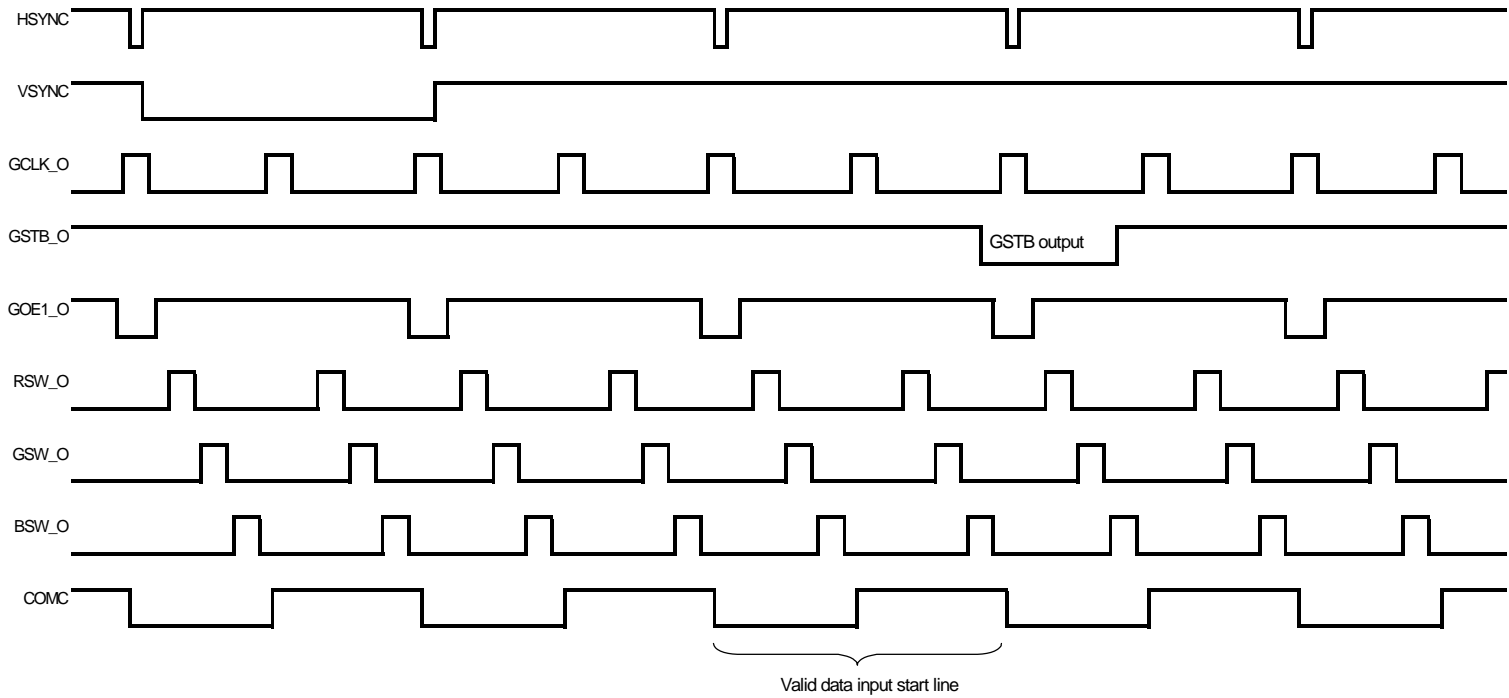


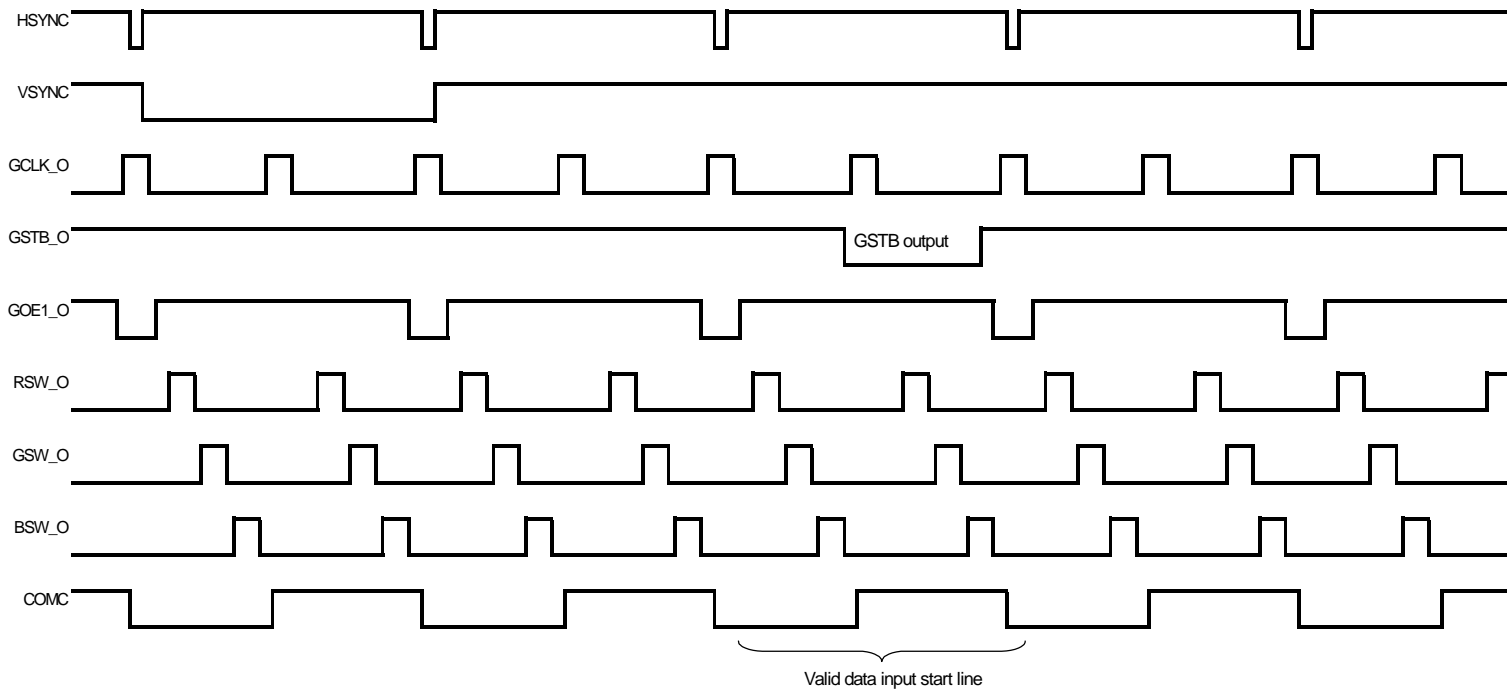
Figure 4–12. Vertical Period GSTB (Top: No dummy line, bottom: Dummy line)

μPD161831 display timing chart <line inversion, 240 output, quarter data function, VSYNC width = 1H, vertical period valid data input timing (R2) = 2>

1) no dummy line



2) dummy line



5. TIMING GENERATOR NON-USE FUNCTION

Operation using an external signal without using the on-chip timing generator function is possible by setting the TCON pin (TCON = H).

When the timing generator non-use function is selected, data input is performed using the following pins. The concrete timing chart is shown on the following.

- DCK: Dot clock
- D00 to D05, D10 to D15, D20 to D25: Data bus
- STHR, STHL: Data input start pulse
- STB: Data latch input
- AP: Amplifier drive period control
- POL: Polarity inversion signal

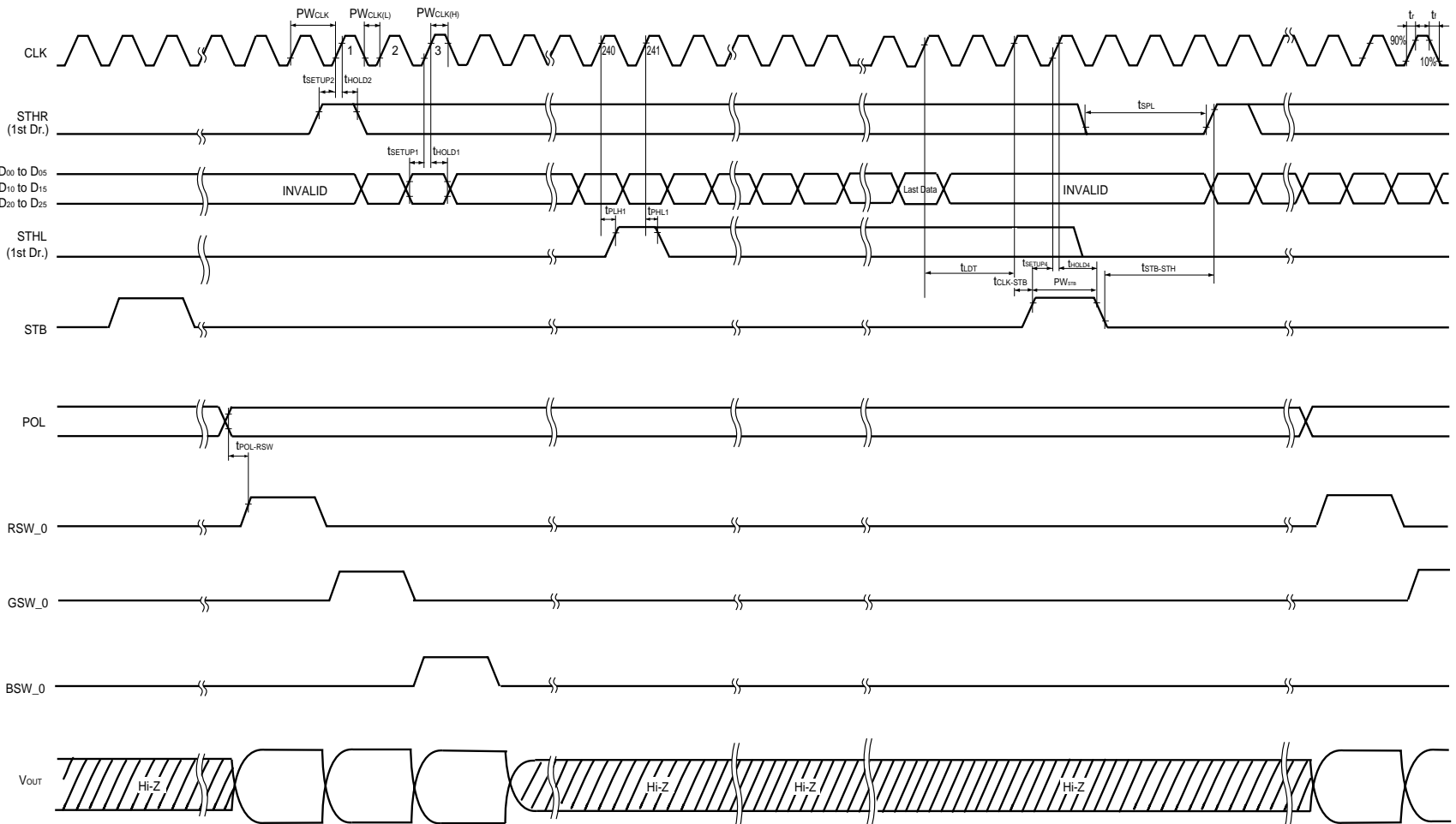
However, the serial interface can be used, and the common and power supply settings performed with the serial interface.

Moreover, when the timing generator non-use function is selected, instead of generating signals through the on-chip timing generator for GCLK_O, GSTB_O, GOE1_O, GOE2_O, RSW_O, GSW_O, BSW_O, and EXT1_O to EXT3_O signals, the signals input from the GCLK_I, GSTB_I, GOE1_I, GOE2_I, RSW_I, GSW_I, BSW_I, and EXT1_I to EXT3_I are output via a level shifter.

The signals input to RSW_I, GSW_I, and BSW_I are also used as the amplifier output timing.

The level shifter circuit block is divided into the gate control signal side and the driver output related signal side, and it is possible to individually select the negative voltage side voltage level individually from V_{SS2} and V_{SS3} at the gate control signal side and the driver output-related signal side. (Refer to 4.2.12 Common amplitude voltage adjustment D/A converter register.)

Figure 5-1. Data Input Timing Chart When Timing Generator Non-Use Function is Selected (R6, Bit 2 = H)
(Unless otherwise specified, $V_{IH} = 0.7 V_{DD1}$, $V_{IL} = 0.3 V_{DD1}$)



6. INTERFACE

6.1 RGB Interface

The RGB interface has the following two modes:

- HSYNC, VSYNC mode

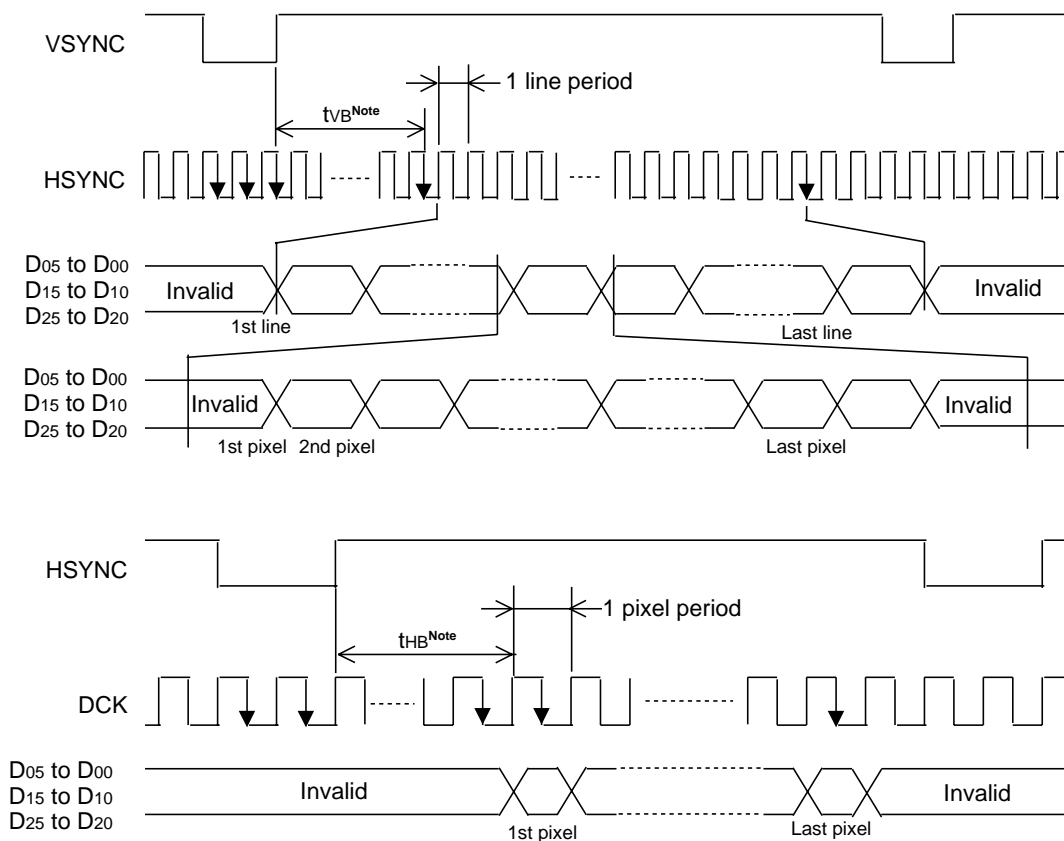
Each mode is explained below.

6.1.1 HSYNC, VSYNC mode

This mode is used to input display data from the DCK, HSYNC, VSYNC, D₀₅ to D₀₀, D₁₅ to D₁₀, and D₂₅ to D₂₀ pins. In this mode, the value set to the R3 register is valid as the number of valid data in the horizontal period. Figure 6–1 shows the timing chart.

Input at least 1 dot clock for the front porch period.

Figure 6–1. Timing Chart in HSYNC, VSYNC Mode (When CKS = L, HSEG = L, VSES = L)



Note t_{VB} = vertical back porch period
 t_{HB} = horizontal back porch period

6.2 Serial Interface

The μPD161831 uses an 8-bit serial interface to set registers related to the horizontal period and vertical period from the MCU, and control the timing of outputting strobe signals to the gate driver.

In addition, the back panel LCD controller driver can also be controlled.

6.2.1 Serial interface between MCU and μPD161831

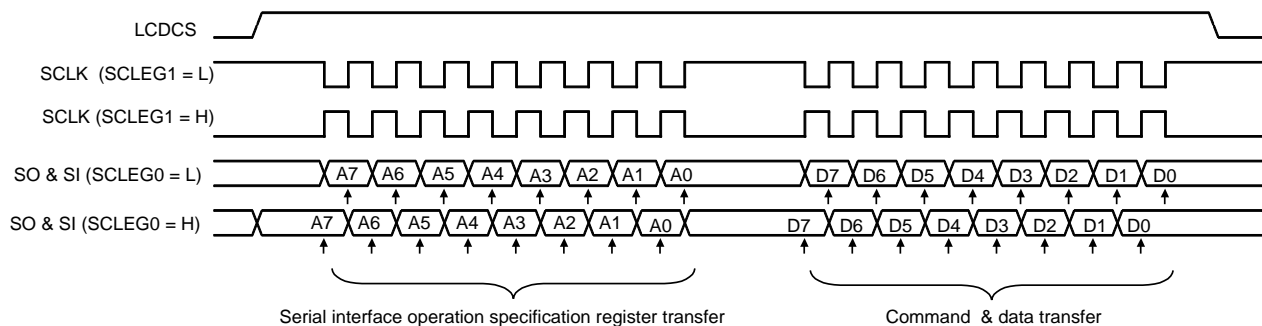
The serial interface between MCU and μPD161831 can acknowledge serial data input (SI), serial clock input (SCLK), and serial data output (SO) if the chip select signal (LCDCS) is active (LCDS = H). This interface supports SPI, and its relationship with the valid edge of the serial clock and the active level of the serial clock can be set by using the SCLEG0 and SCLEG1 pins.

Table 6–1. Relationship between Serial Clock and Data

Pin Name		Active Level of Serial Clock	Input Timing of Serial Data	Output Timing of Serial Data
SCLEG1	SCLEG0			
L	L	Low level	Rising edge of serial clock	Falling edge of serial clock
L	H	Low level	Falling edge of serial clock	Rising edge of serial clock
H	L	High level	Falling edge of serial clock	Rising edge of serial clock
H	H	High level	Rising edge of serial clock	Falling edge of serial clock

Figure 6–2 shows the signal chart of the serial interface.

Figure 6–2. Serial Interface Signal Chart



Remarks 1. “↑” indicates the timing of reading data.

2. If the chip is not active, the shift register and counter are reset to the default status.
3. When wiring SCL, the influence of terminal reflection and external noise due to the wiring length must be taken into consideration. It is recommended to confirm the operation on the actual system.

Figures 6–3 and 6–4 show the relationship between the read/write operation and the SCLEG0 and SCLEG1 pins setting.

A read or write operation is specified by a command. When a read operation is specified by a command (A5 bit = 1), the 8-bit data transferred next is read. Figure 6–4 gives a specific example. Be aware that the SO pin becomes Hi-Z at all times other than when data is output.

Figure 6–3. Serial Interface Signal Chart (Write sequence)

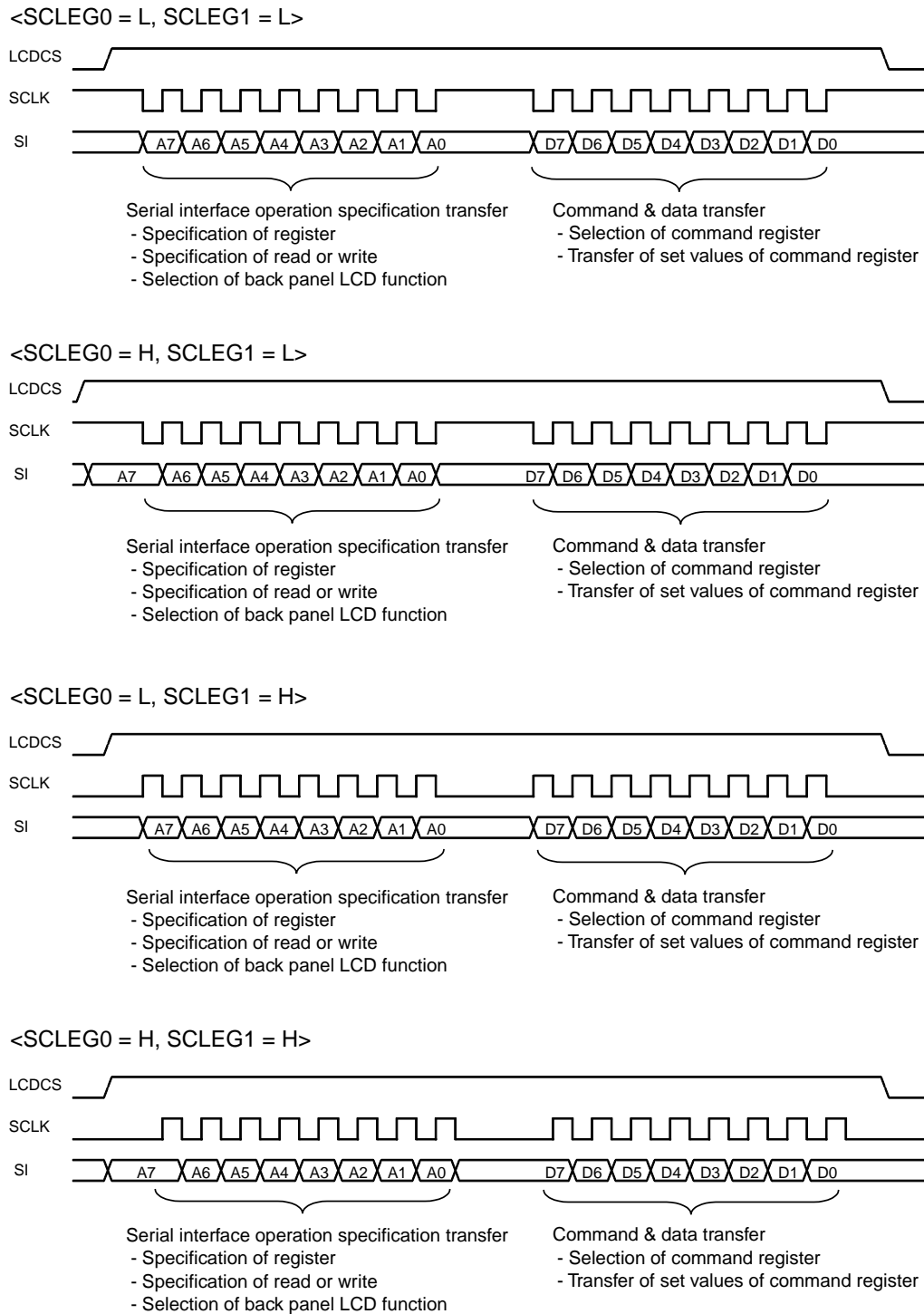
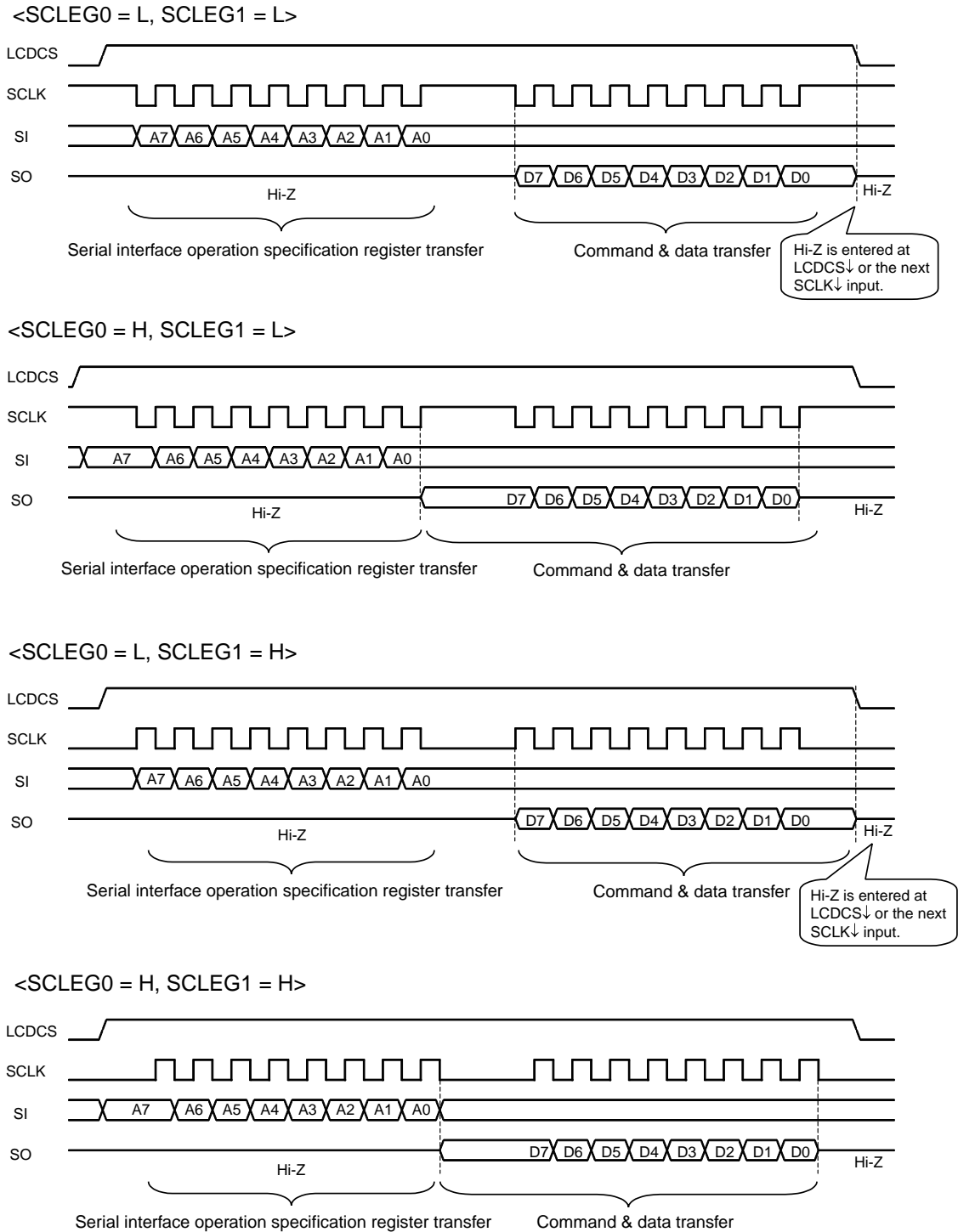


Figure 6-4. Serial Interface Signal Chart (Read Sequence)



6.2.2 Serial interface between μPD161831 and back panel LCD Controller Driver

This 8-bit serial interface is used to control the back panel LCD.

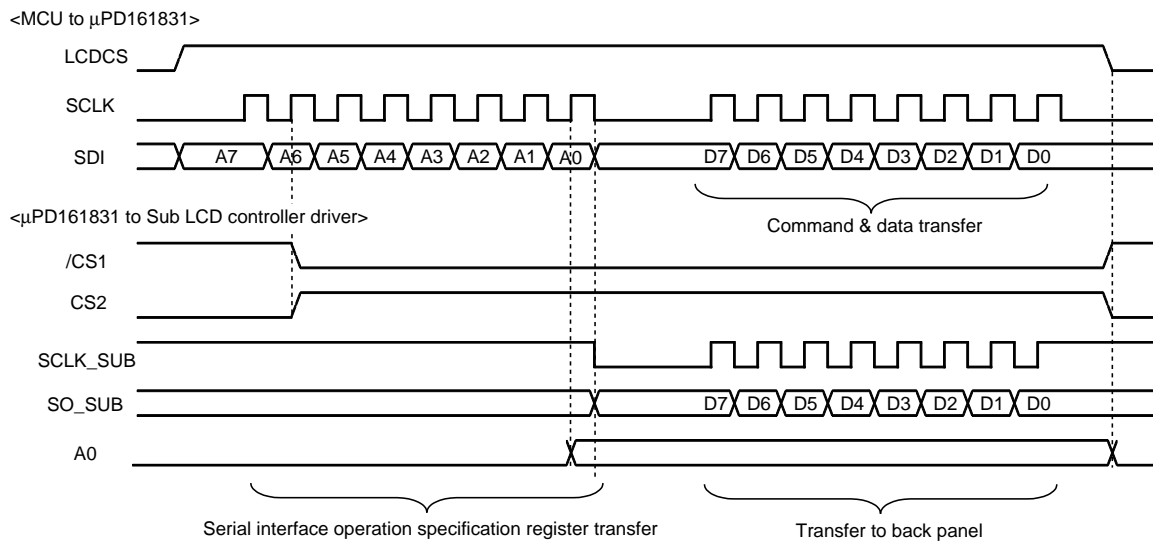
When a function to transfer data to the back panel LCD is selected by a command (A6 bit = 1), the chip select signals (/CS1 and CS2) for the back panel LCD are asserted. When data is input from the SCLK and SI pins to transfer parameters and data, the polarity of the back panel LCD clock (SCLK_SUB) is the low level (high-level start) and data is output from the back panel serial data output line (SO_SUB) at the falling edge of the clock, regardless of the polarity and edge specification of the clock input to SCLK.

Bit A0 of the command can be used to specify the level to be output to the A0 pin. If “command specification” is specified by the A0 bit (A0 bit = 0), the A0 pin outputs a low level when the data of the parameter & data register is transferred. If “parameter setting” is specified by the A0 bit (A0 bit = 1), the A0 pin outputs a high level when the data of the parameter & data register is transferred.

This interface can be used even in the standby mode.

The transfer operation is illustrated below.

Figure 6–5. Serial Interface Signal Chart (Access to Back Panel LCD, SCLEG0 = SCLEG1 = H)



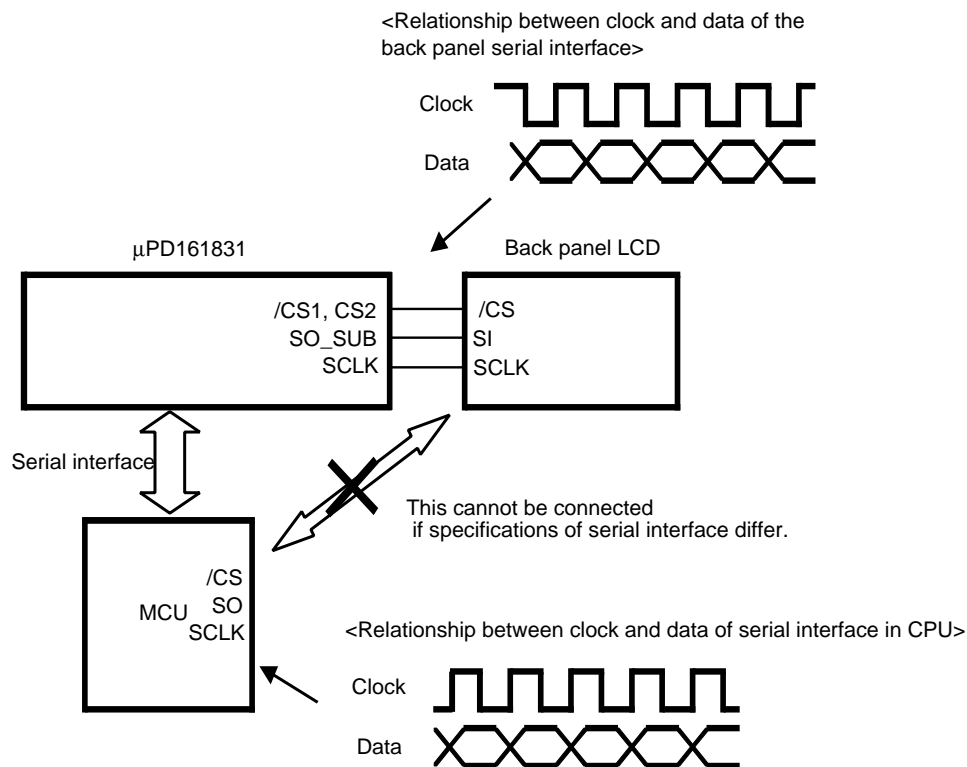
This interface is effective in the following cases:

- When an access to the back panel LCD controller driver is to be (or must be) made by the serial interface.
- If the specifications of the internal serial interface of the MCU in the set differ from the specifications of the back panel LCD controller driver.

(Even if the serial interface of the MCU does not start when the serial clock is high, output data at the falling edge of the clock, and input data at the rising edge of the clock (frequently used specifications), the serial interface of the μPD161831 supports SPI and any input).

An example where the back panel serial interface is necessary is given below.

Figure 6–6. Example Where Back Panel Serial Interface Is Necessary



7. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

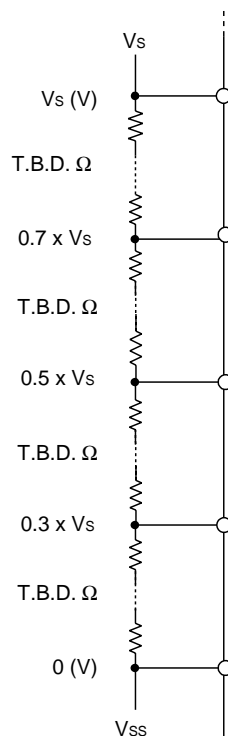
The μPD161831 includes a γ resistor for normally-black support. The relationship between the input data and the output voltage is shown in figure 7–2.

Any 3 major points V_1 - V_3 from the LCD panel γ -characteristics curve can be used as the external power supplies. The relation V_0 - V_4 external power supplies and γ correction resistance is shown in table 7–1, figure 7–1.

Table 7–1. Relationship between External Power Supplies and γ Correct Voltage and Resistance

Pin Name	Voltage (V)	Resistance (Ω)
V_0	V_s	T.B.D.
V_1	$0.7 \times V_s$	T.B.D.
V_2	$0.5 \times V_s$	T.B.D.
V_3	$0.3 \times V_s$	T.B.D.
V_4	0	T.B.D.

Figure 7–1. Relationship between External Power Supplies and γ Correction Resistance



External power supply pins V_0 - V_4 can be customized at any place of the γ correction voltage. The string resistance between V_{ss} - V_s that generates the γ correction voltage is divided by 250, from which the desired voltage can be selected and the γ correction voltage can be customized. In addition, positive or negative polarity can also be selected for each γ correction voltage.

Table 7–2. Relationship between Input Data and Output Voltage Value
T.B.D.

Figure 7–2. Relationship between Positive/Negative Polarity and Data Output

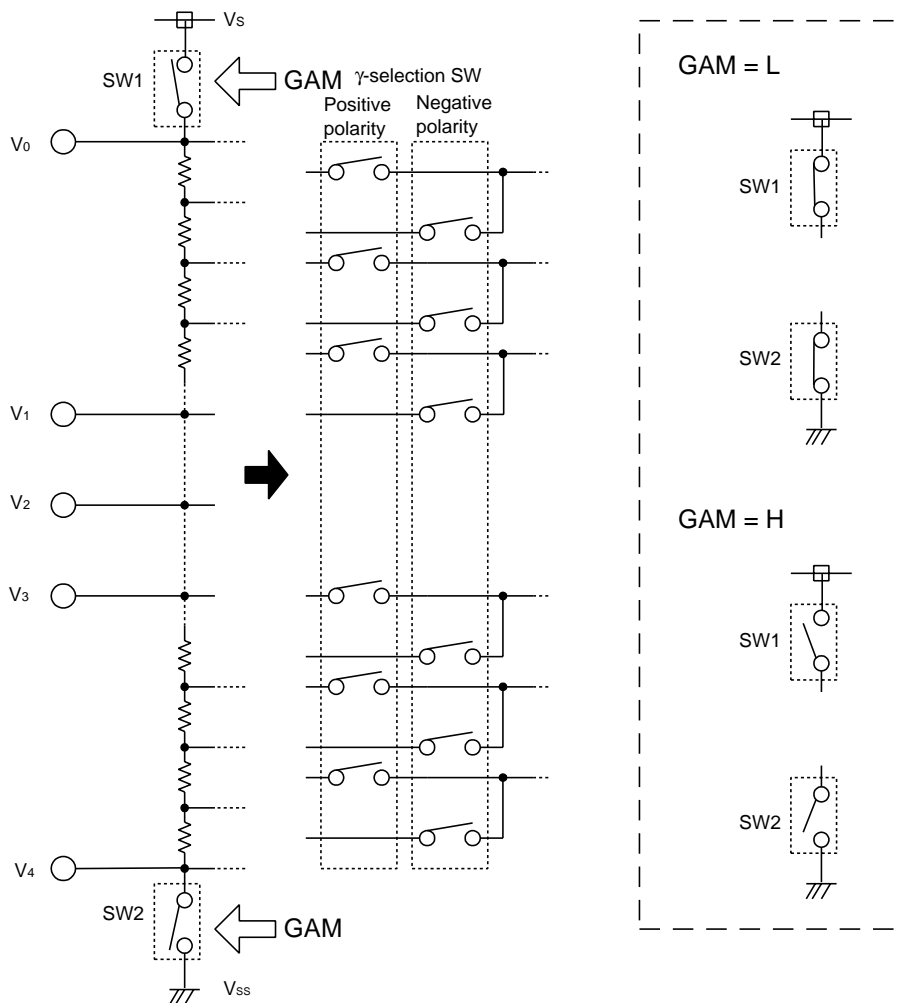
T.B.D.

8. CONNECTION OF γ CORRECTION RESISTOR TO POWER SUPPLY AND GND PINS

Connection of the γ correction resistors of the μPD161831, γ correction resistor power supplies (V_0 - V_4) is shown below.

Depending on the setting of the GAM pin, the maximum and minimum potential of the γ correction resistors can be changed between V_S - V_{SS} and V_0 - V_4 .

Figure 8-1. GAM Pin Function

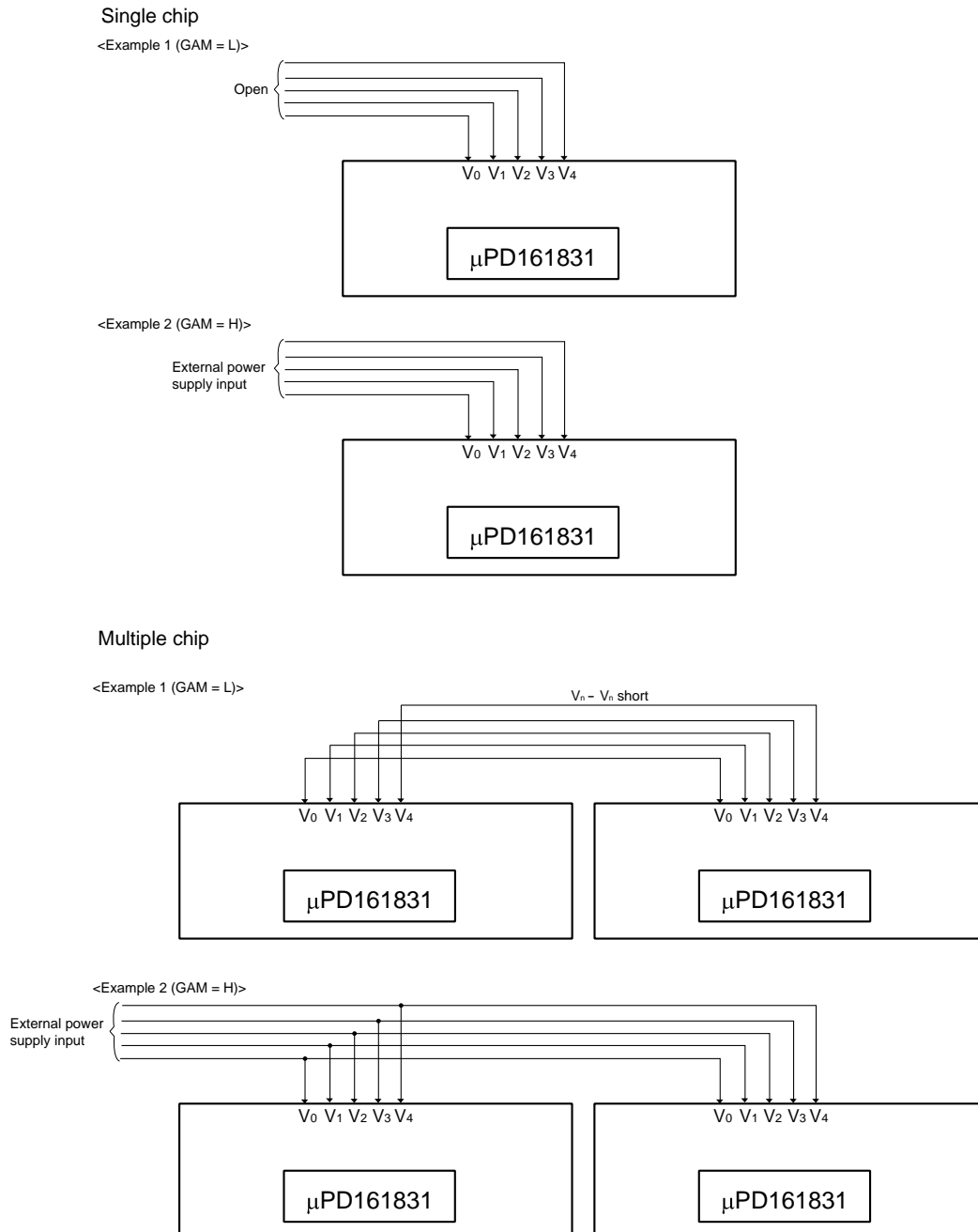


9. γ -CORRECTION POWER SUPPLY CONNECTION EXAMPLE

The μ PD161831 enables customization of the γ -correction power supply on both the positive and negative polarity sides (For details, refer to 7. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE).

Consequently, a γ -correction power supply does not have to be input externally when a single source-driver chip is being used in the panel.

Figure 9–1. γ -Correction Power-Supply Connection Example



10. RESET

The μPD161831 can be reset by hardware (/RESET pin) or a command (R15 register).

A hardware reset resets all the functions, including the registers except serial interface. A command reset initializes only the registers. Be sure to execute a hardware reset and command reset immediately after power application.

Each reset is explained below.

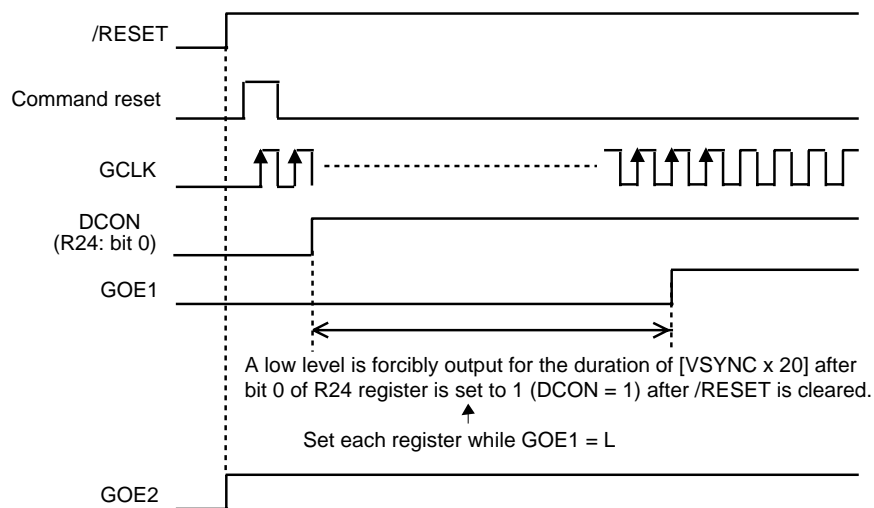
10.1 Hardware Reset

When a hardware reset is input (/RESET = L), reset is performed for the registers listed in table 4–2 and the on-chip hardware function. (Initialization of the serial interface counter is performed from LCDCS.) Therefore, even when the timing generator non-use mode is selected, be sure to input a hardware reset.

While the hardware reset signal is being input (/RESET = L → H) and during the period of “VSYNC x 20” after bit 0 of the R24 register has been set to 1 (DCON = 1) after the reset was cleared, all the gate outputs are set to OFF, and the charge on the TFT panel pixels is decreased to 0.

Figure 10–1 shows the timing between when the hardware reset signal is input and when display output is produced.

Figure 10–1. From Input of Hardware Reset to Display Output



When bit 4 of the R4 register = 0, GOE1 output continues to be low level even after the “VSYNC x 20” period has elapsed after bit 0 of the R24 register is set to 1 (DCON = 1).

Moreover, if bit 4 of the R4 register is set to “1” before the “VSYNC x 20” period elapses after bit 0 of the R24 register has been set to (DCON = 1), low output is performed from the GOE1 pin until the “VSYNC x 20” time has elapsed.

10.2 Command Reset

A command reset (R15 register) only initializes the registers.

11. GOE1 AND GOE2 SIGNALS

The output of the GOE1 and GOE2 signals changes according to the setting of the DCON signal and the input of /RESET and standby.

-GOE1: After DCON is set to 1 (bit 0 of R24 register is set to 1), the GOE1 signal outputs a low level for a period of “VSYNC x 20”, and output of all the gates is switched off.

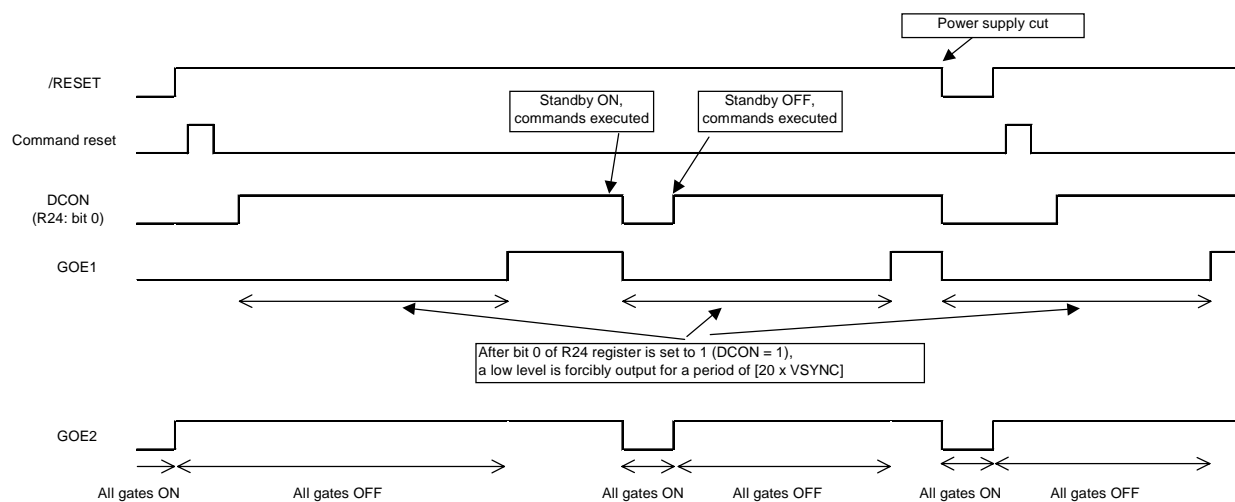
(All gates are off at power application.)

-GOE2: In standby mode, when DCON = 0, GOE2 outputs a low level and output of all the gates is switched on.

(In standby mode, the charge of the panel is discharged.)

Refer to figure 11–1 below for details.

Figure 11–1. GOE1 and GOE2 Signal Output



Regarding the GOE1 signal, the above-described function does not work when the timing generator function is not used, and output enable/disable for the GOE1 signal following reset release can be controlled only with the R6 register.

12. POWER SUPPLY ON/OFF SEQUENCE

T.B.D.

13. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ($V_{SS1} = V_{SS2} = 0\text{ V}$)

Parameter	Symbol	Rating	Unit
Logic part supply voltage	V_{CC}	-0.3 to +4.5	V
Driver part supply voltage	V_S	-0.3 to +6.0	V
Input voltage	V_I	-0.3 to $V_{CC} + 0.3$	V
Output voltage	V_O	-0.3 to $V_{CC} + 0.3$	V
Operating ambient temperature	T_A	-40 to +85	°C
Storage temperature	T_{stg}	-55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range ($T_A = -40\text{ to }+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic part supply voltage	V_{CC}		2.2		3.6	V
Driver part supply voltage	V_S		4.5	5.0	5.5	V
Booster reference power supply	V_{DC}		2.5		3.6	V
High-level input voltage	V_{IH}		0.7 V_{CC}		V_{CC}	V
Low-Level input voltage	V_{IL}		0		0.3 V_{CC}	V
γ -corrected voltage	V_0 - V_4		V_{SS}		V_S	V
Clock frequency	f_{CLK}	$V_{CC} = 2.5\text{ to }5.5\text{ V}$			20	MHz
		$V_{CC} = 2.2\text{ to }5.5\text{ V}$			16	MHz

★ Electrical Characteristics (T_A = -40 to +85°C, V_{CC} = 2.2 to 3.6 V, V_S = 5.0 V ± 0.5 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input leak current	I _{IH}				1.0	μA
	I _{IL}	Except TESTIN1, TESTIN2	-1.0			μA
Input current	I _{IH2}	TESTIN1, TESTIN2		1.5	5.0	μA
High-level output voltage	V _{OH}	Except COMC, I _{OH} = -0.1 mA	V _{CC} - 0.5			V
Low-level output voltage	V _{OL}	Except COMC, I _{OL} = +0.1 mA			0.5	V
High-level output voltage	V _{OH2}	COMC, I _{OH} = -1.0 mA	T.B.D.			V
Low-level output voltage	V _{OL2}	COMC, I _{OL} = +1.0 mA			T.B.D.	V
γ-correction power-supply static current consumption	I _γ	V ₀ = 5.0 V, V ₄ = 0 V (GAM = L)	115	230	460	μA
Driver output current (Amp. drive)	I _{VOH1}	V _S = 5.0 V, V _{OUT} = V _X - 1.0 V ^{Note1} Input data: 1FH		T.B.D.	T.B.D.	mA
	I _{VOL1}	V _S = 5.0 V, V _{OUT} = V _X + 1.0 V ^{Note1} Input data: 20H	T.B.D.	T.B.D.		mA
Driver output voltage (8-color display mode)	V _{OH3}	V _S = 5.0 V, I _o = -100 μA	T.B.D.			V
	V _{OL3}	V _S = 5.0 V, I _o = +100 μA			T.B.D.	V
Output voltage deviation	ΔV _o			±10	±20	mV
Output voltage range	V _o	RGB data: 00H to 3FH	V _{SS} + 0.05		V _S - 0.05	V
COMDC output impedance	R _{COMDC}	I _o = -40 μA			T.B.D.	Ω
V _{REF} input voltage range	V _{REFIN}					V
V _{DD1} boost voltage	V _{DD1}	I _{DD1} = +300 μA	1.7 V _S		2.0 V _S	V
V _{DC2} boost voltage 1	V _{DC2}	V _{DC2} = L (x2 boost), I _{DC} = +1.0 mA	1.9 V _{DC}		2.0 V _{DC}	V
V _{DC2} boost voltage 2	V _{DC2}	V _{DC2} = L (x3 boost), I _{DC} = +1.0 mA	2.8 V _{DC}		3.0 V _{DC}	V
V _{SS2} boost voltage	V _{SS2}	I _{SS2} = -300 μA	-1.0 V _S		-0.8 V _S	V
V _{SS3} boost voltage	V _{SS3}	I _{SS3} = -300 μA	-3.0 V _S		-2.7 V _S	V
V _{DD1} output resistance	R _{VDD1}	I _{DD1} = +300 μA	1.5	3.0	5.0	kΩ
V _{DC2} output resistance 1	R _{VDC21}	V _{DC2} = L (x2 boost), I _{DC} = +1.0 mA	50	100	200	Ω
V _{DC2} output resistance 2	R _{VDC22}	V _{DC2} = L (x3 boost), I _{DC} = +1.0 mA	100	200	400	Ω
V _{SS2} output resistance	R _{VSS2}	I _{SS2} = -300 μA	1	2	3	kΩ
V _{SS3} output resistance	R _{VSS3}	I _{SS3} = -300 μA	1.5	3.0	5.0	kΩ
V _S output voltage	V _S	No load	4.5	5.0	5.5	V
V _R output voltage	V _R	No load	4.5	5.0	5.5	V
V _S output resistance	R _{V_S}	V _{DC2} = 6.0 V, I _S = +1.0 mA, V _S = 5.0 V		30	60	Ω
V _R output resistance	R _{V_R}	V _{DC2} = 6.0 V, I _R = +1.0 mA, V _S = 5.0 V		T.B.D.	T.B.D.	Ω
Logic part static current consumption	I _{CC1}	No load, standby mode			10	μA
Logic part dynamic current consumption	I _{CC2}	No load ^{Note2}		0.6	0.9	mA
Driver part static current consumption	I _{DC1}	No load, V _{DC} = 2.8 V, standby mode		T.B.D.	T.B.D.	μA
Driver part dynamic current consumption	I _{DC2}	No load, V _{DC} = 2.8 V, V _S = 5.0 V ^{Note2}		2.6	T.B.D.	mA
		No load, V _{DC} = 2.8 V, V _S = 5.0 V ^{Note2} , 8-color mode		1.3	T.B.D.	mA

Notes 1. V_X refers to the output voltage of analog output pins S₁ to S₂₄₀.

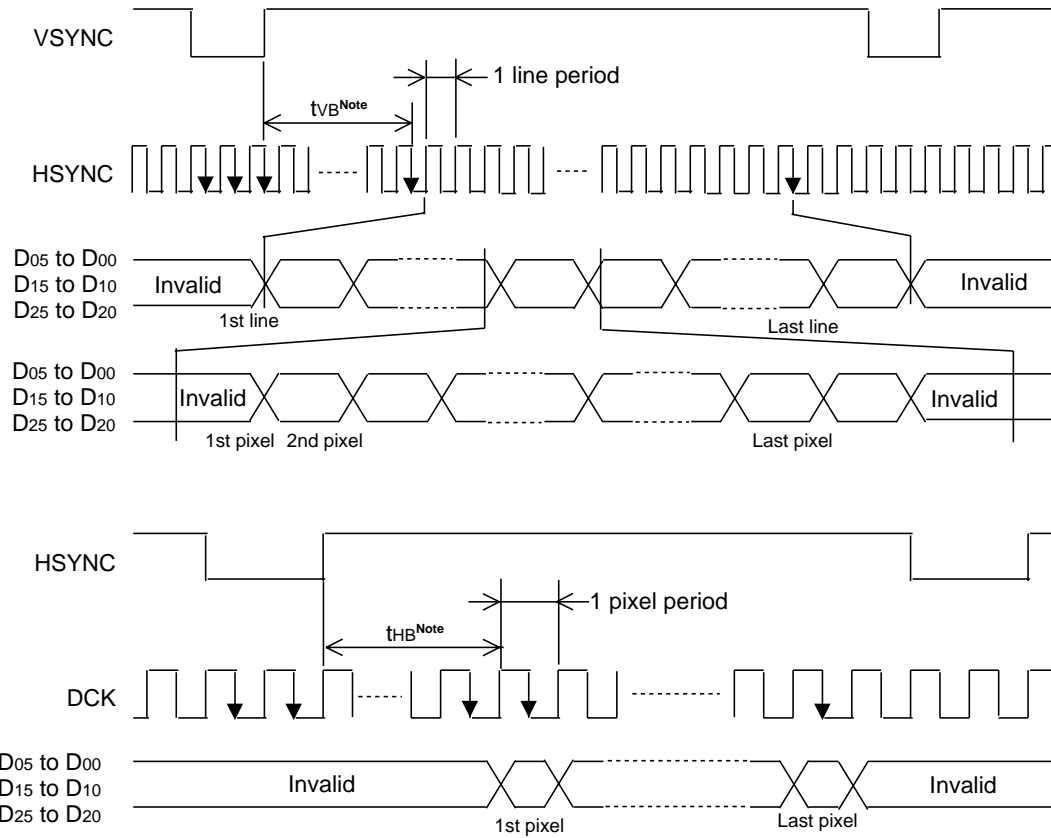
V_{OUT} refers to the voltage applied to analog output pins S₁ to S₂₄₀.

- 2.** f_{CLK} = 15 MHz, STB cycle = 52 μs, AP pulse width (each multiplexer switch amplifier driving time) = 10 μs, BA = L (low power mode)

Switching Characteristics ($T_A = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.2$ to 3.6 V , $V_S = 5.0\text{ V} \pm 0.5\text{ V}$, $V_{SS} = 0\text{ V}$)

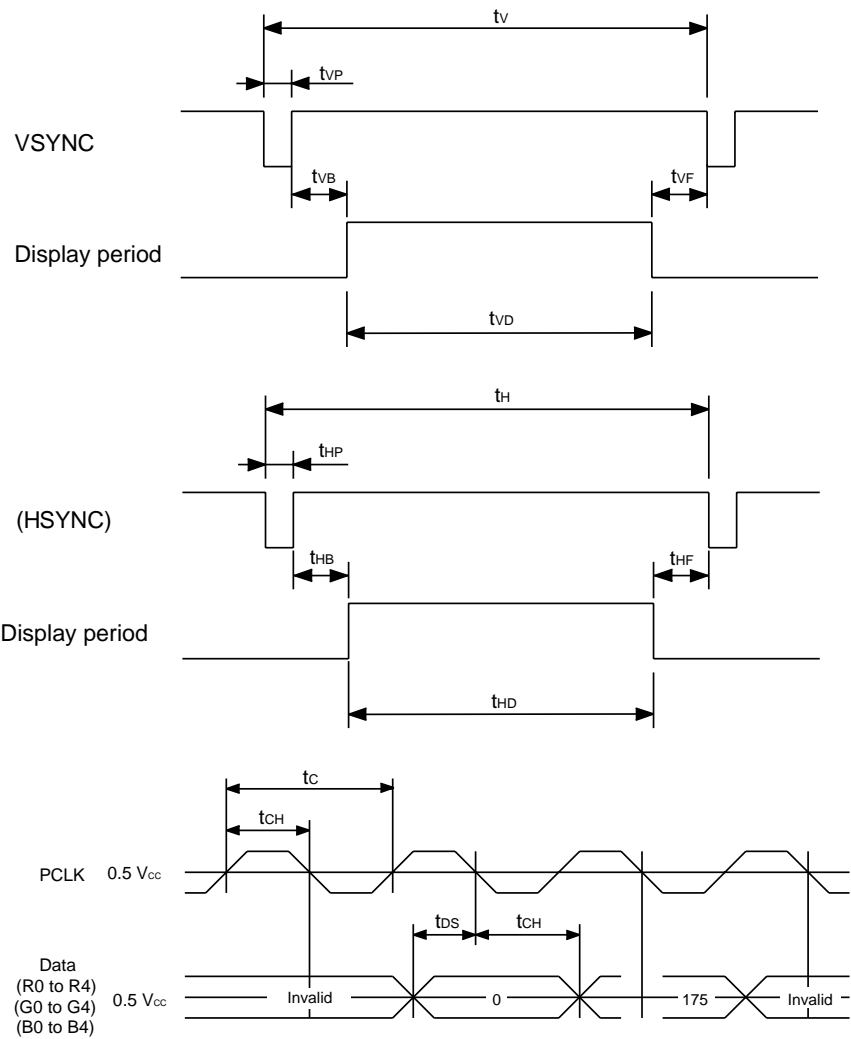
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start pulse delay time	t_{PLH1}	$C_L = 15\text{ pF}$			30	ns
Driver output delay time (High power mode, with load)	t_{PLH2H}	$C_L = 30\text{ pF}$, $AP\uparrow \rightarrow V_{OUT} - 100\text{ mV}$, or $V_{OUT} + 100\text{ mV}$			12	μs
	t_{PHL2H}				12	μs
Driver output delay time (Low power mode, with load)	t_{PLH2L}	$C_L = 30\text{ pF}$, $AP\uparrow \rightarrow V_{OUT} - 100\text{ mV}$, or $V_{OUT} + 100\text{ mV}$			15	μs
	t_{PHL2L}				15	μs
High capacitance	C_{I1}	$V_0 - V_4$, $T_A = 25^\circ\text{C}$		5	15	pF
	C_{I2}	Except for $V_0 - V_4$, $T_A = 25^\circ\text{C}$		10	15	pF
DC/DC oscillation frequency	f_{DCDC}	$FS0 = FS1 = H$	10	15	20	kHz
DCCLK input frequency	f_{DCCLK}			15	50	kHz

RGB interface (1/2)



Note tvB = vertical back porch period
tHB = horizontal back porch period

RGB interface (2/2)

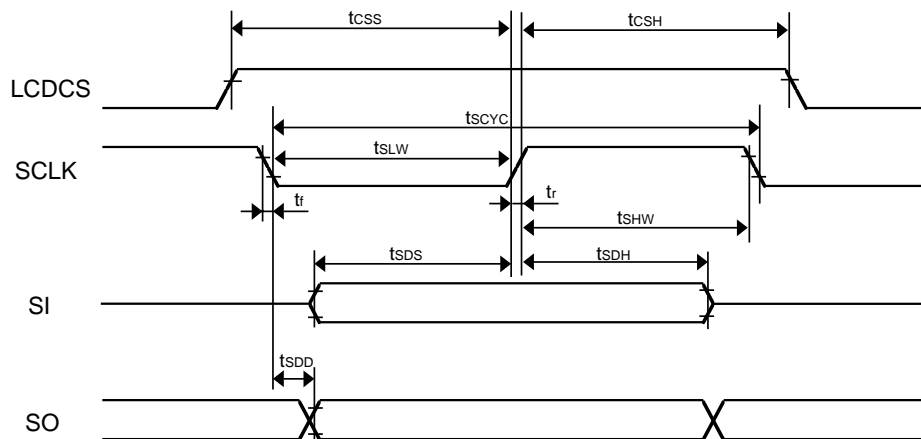


$T_A = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.2$ to 3.6 V, $V_S = 5.0$ V \pm 0.5 V, $V_{SS} = 0$ V

Name			Symbol	MIN.	TYP.	MAX.	Unit	Remark
Clock	Frequency	V _{CC} ≥ 2.5 V	1/t _c	T.B.D.	5.0	10.0	MHz	200 ns (TYP.)
		V _{CC} ≥ 2.2 V	1/t _c	T.B.D.	5.0	8.0	MHz	200 ns (TYP.)
	Duty		t _{CH} /t _c	T.B.D.	0.5	0.6	—	—
	Rise/Fall		t _{CRF}	—	—	T.B.D.	ns	—
Horizontal signal	Cycle		t _H	—	50.51	—	μs	19.8 kHz (TYP.)
				—	252	—	CLK	
	Display period		t _{HD}	240			CLK	—
	Front porch		t _{HF}	1.0	3.0	—	CLK	—
	Pulse width		t _{HP}	2.0	5.0	—	CLK	—
	Back porch		t _{HB}	2.0	4.0	—	CLK	—
	t _{HP} + t _{HB} (Quarter data function not used)			4.0	T.B.D.	T.B.D.	CLK	—
	t _{HP} + t _{HB} (Quarter data function used)			10.0	T.B.D.	T.B.D.	CLK	—
	HSYNC setup time		t _{HSS}	T.B.D.	—	—	ns	—
	HSYNC hold time		t _{HSH}	T.B.D.	—	—	ns	—
Vertical signal	Cycle		t _V	—	16.67	—	ms	60.0 Hz (TYP.)
				T.B.D.	330	T.B.D.	H	
	Front porch		t _{VF}	1.0	2.0	—	H	—
	Pulse width		t _{VP}	1.0	5.0	—	H	—
	Back porch		t _{VB}	1.0	3.0	—	H	—
	t _{VF} + t _{VP} + t _{VB}			4.0	10.0	—	H	—
	VSYNC setup time		t _{VSS}	T.B.D.	—	—	ns	—
	VSYNC hold time		t _{VSH}	T.B.D.	—	—	ns	—
Data	Clock – data timing		t _{DH}	T.B.D.	—	—	ns	—
	Data – clock timing		t _{DS}	T.B.D.	—	—	ns	—

Serial Interface

- Serial interface between MCU and μPD161831 (when SCLEG0 = SCLEG1 = H)



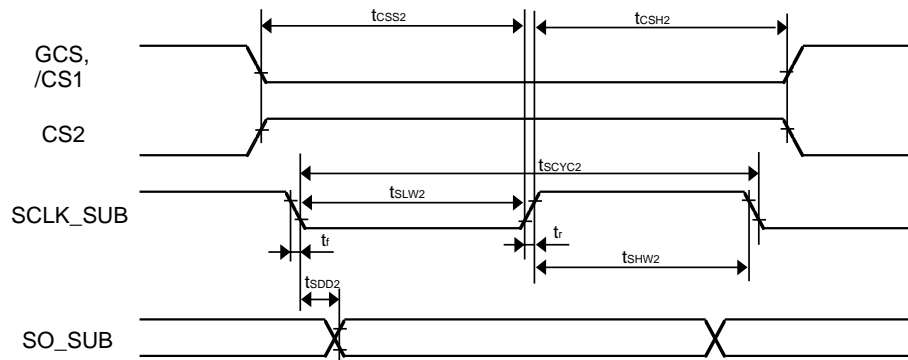
$T_A = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.2$ to 3.6 V, $V_S = 5.0$ V \pm 0.5 V, $V_{SS} = 0$ V

Parameter	Symbol	Condition	MIN.	TYP. ^{Note}	MAX.	Unit
Serial clock cycle	tscyc		150			ns
SCLK_SUB high-level pulse width	tSHW		60			ns
SCLK_SUB low-level pulse width	tSLW		60			ns
Data setup time	tSDS		60			ns
Data hold time	tSDH		60			ns
CS – SCL time	tcSS		90			ns
	tcSH		90			ns
SCLK↓ → SO output delay time	tSDD		T.B.D.			ns

Note TYP. values are reference values when $T_A = 25^\circ\text{C}$.

- Remarks**
- The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.
 - All timing is rated based on 20 to 80% of V_{CC} .

• Serial interface between μPD161831 and back panel



$T_A = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.2$ to 3.6 V, $V_S = 5.0$ V \pm 0.5 V, $V_{SS} = 0$ V

Parameter	Symbol	Condition	MIN.	TYP. ^{Note}	MAX.	Unit
Serial clock cycle	tSCYC2		T.B.D.			ns
SCLK_SUB high-level pulse width	tSHW2		T.B.D.			ns
SCLK_SUB low-level pulse width	tSLW2		T.B.D.			ns
CS – SCLK_SUB time	tCSS2		T.B.D.			ns
	tCSH2		T.B.D.			ns
SCLK_SUB↓ → SO_SUB output delay time	tSDD2		T.B.D.			ns

Note TYP. values are reference values when $T_A = 25^\circ\text{C}$.

- Remarks**
1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.
 2. All timing is rated based on 20 to 80% of V_{CC} .

Timing Requirements When not Using Timing Generator

T.B.D.

Timing Requirements ($T_A = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.2$ to 3.6 V, $V_{SS} = 0$ V, $t_r = t_f = 10$ ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW_{CLK}		100			ns
Clock pulse high time	$PW_{CLK(H)}$		30			ns
Clock pulse low time	$PW_{CLK(L)}$		30			ns
Data setup time	t_{SETUP1}		20			ns
Data hold time	t_{HOLD1}		20			ns
Start pulse setup time	t_{SETUP2}		20			ns
Start pulse hold time	t_{HOLD2}		20			ns
Start pulse low time	t_{SPL}		3			CLK
Last data timing	t_{LDT}		2			CLK
CLK – STB time	$t_{CLK-STB}$	$CLK\uparrow \rightarrow STB\uparrow$	20			ns
STB pulse width	PW_{STB}		40			ns
Start pulse rising time	$t_{STB-STH}$	$STB\uparrow \rightarrow STH\uparrow$	3			CLK
STB setup time	t_{SETUP4}		20			ns
STB hold time	t_{HOLD4}		20			ns
POL – RSW_O \uparrow time	$t_{POL-RSW}$		T.B.D.			ns
AP pulse width (High power mode)	PW_{APH}		T.B.D.			μ s
AP pulse width (Low power mode)	PW_{APL}	STB cycle = 40 μ s, $C_L = 30$ pF	T.B.D.			μ s

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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