To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS INTEGRATED CIRCUIT

μPD161830

240-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

DESCRIPTION

The μPD161830 is a source driver for TFT-LCDs supporting 64 gray-scale display and can operate with a supply voltage of 2.5 V for the logic block and 5.0 V for the driver block. Data input as 6-bit x 3-dot digital data is output as 64 γ-corrected values using an internal D/A converter and 5 external power modules, thus achieving a 260,000-color (full-color) display.

FEATURES

- CMOS level input
- 240 outputs
- Input of 6 bits (gray-scale data) by 3 dots
- Capable of outputting 64 values by means of 5 external power modules and a D/A converter
- Output dynamic range: V_{SS2} to V_{DD2}
- High-speed data transfer: f_{CLK} = 15 MHz MAX. (internal data transfer speed when operating at V_{DD1} = 2.5 V)
- Level inversion γ-correction power supply is possible
- Logic power supply voltage (V_{DD1}): 2.2 to 3.6 V
- Driver power supply voltage (V_{DD2}): 4.5 to 5.5 V

ORDERING INFORMATION

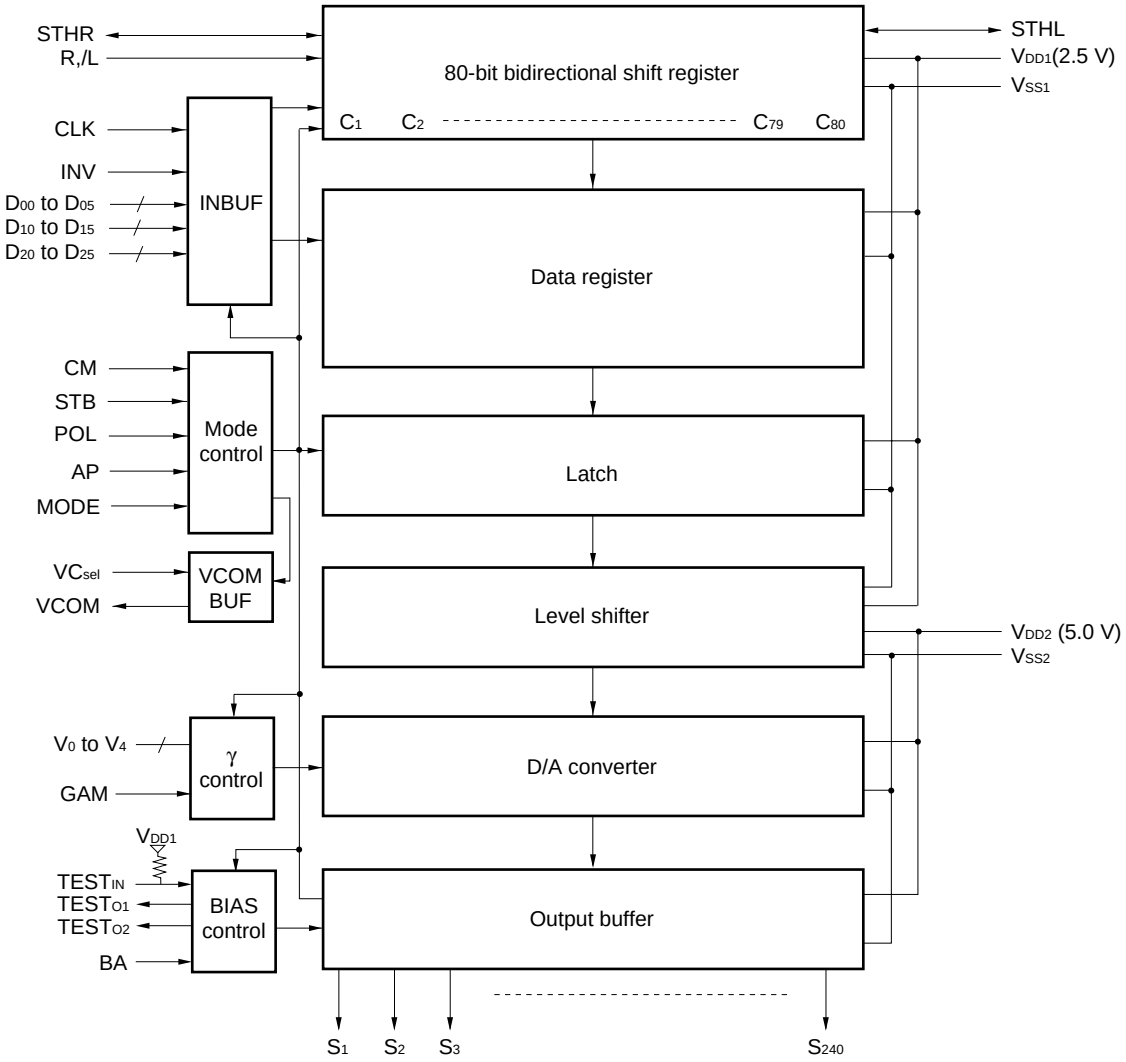
Part Number	Package
μPD161830P	Chip

Remark Purchasing the above chip entail the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

Document No. S16240EJ2V0PM00 (2nd edition)
Date Published July 2002 NS CP (K)
Printed in Japan

The mark ★ shows major revised points.

1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (Pad Layout)

Chip size: 15.84 x 1.11 mm^2

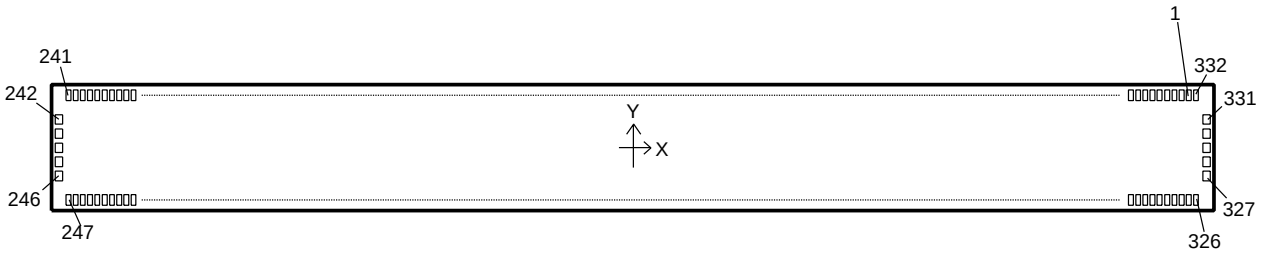
Bump size (Input/VCOM/test/dummy): 80 x 86 μm^2

Bump size (Output): 29 x 103 μm^2

Alignment Mark (μm)

X: 7716.45 Y: 347.04

X: –7716.45 Y: 347.04



Alignment mark shape (unit: μm)

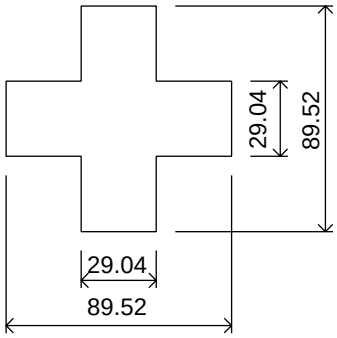


Table 2–1. Pad Layout (1/2)

No.	Name	X [μm]	Y [μm]
1	S1	7170.000	396.480
2	S2	7110.000	396.480
3	S3	7050.000	396.480
4	S4	6990.000	396.480
5	S5	6930.000	396.480
6	S6	6870.000	396.480
7	S7	6810.000	396.480
8	S8	6750.000	396.480
9	S9	6690.000	396.480
10	S10	6630.000	396.480
11	S11	6570.000	396.480
12	S12	6510.000	396.480
13	S13	6450.000	396.480
14	S14	6390.000	396.480
15	S15	6330.000	396.480
16	S16	6270.000	396.480
17	S17	6210.000	396.480
18	S18	6150.000	396.480
19	S19	6090.000	396.480
20	S20	6030.000	396.480
21	S21	5970.000	396.480
22	S22	5910.000	396.480
23	S23	5850.000	396.480
24	S24	5790.000	396.480
25	S25	5730.000	396.480
26	S26	5670.000	396.480
27	S27	5610.000	396.480
28	S28	5550.000	396.480
29	S29	5490.000	396.480
30	S30	5430.000	396.480
31	S31	5370.000	396.480
32	S32	5310.000	396.480
33	S33	5250.000	396.480
34	S34	5190.000	396.480
35	S35	5130.000	396.480
36	S36	5070.000	396.480
37	S37	5010.000	396.480
38	S38	4950.000	396.480
39	S39	4890.000	396.480
40	S40	4830.000	396.480
41	S41	4770.000	396.480
42	S42	4710.000	396.480
43	S43	4650.000	396.480
44	S44	4590.000	396.480
45	S45	4530.000	396.480
46	S46	4470.000	396.480
47	S47	4410.000	396.480
48	S48	4350.000	396.480
49	S49	4290.000	396.480
50	S50	4230.000	396.480
51	S51	4170.000	396.480
52	S52	4110.000	396.480
53	S53	4050.000	396.480
54	S54	3990.000	396.480
55	S55	3930.000	396.480
56	S56	3870.000	396.480
57	S57	3810.000	396.480
58	S58	3750.000	396.480
59	S59	3690.000	396.480
60	S60	3630.000	396.480
61	S61	3570.000	396.480
62	S62	3510.000	396.480
63	S63	3450.000	396.480
64	S64	3390.000	396.480
65	S65	3330.000	396.480
66	S66	3270.000	396.480
67	S67	3210.000	396.480
68	S68	3150.000	396.480
69	S69	3090.000	396.480
70	S70	3030.000	396.480
71	S71	2970.000	396.480
72	S72	2910.000	396.480
73	S73	2850.000	396.480
74	S74	2790.000	396.480
75	S75	2730.000	396.480
76	S76	2670.000	396.480
77	S77	2610.000	396.480
78	S78	2550.000	396.480
79	S79	2490.000	396.480
80	S80	2430.000	396.480
81	S81	2370.000	396.480
82	S82	2310.000	396.480
83	S83	2250.000	396.480
84	S84	2190.000	396.480
85	S85	2130.000	396.480
86	S86	2070.000	396.480
87	S87	2010.000	396.480
88	S88	1950.000	396.480
89	S89	1890.000	396.480
90	S90	1830.000	396.480
91	S91	1770.000	396.480
92	S92	1710.000	396.480
93	S93	1650.000	396.480
94	S94	1590.000	396.480
95	S95	1530.000	396.480
96	S96	1470.000	396.480
97	S97	1410.000	396.480
98	S98	1350.000	396.480
99	S99	1290.000	396.480
100	S100	1230.000	396.480
101	S101	1170.000	396.480
102	S102	1110.000	396.480
103	S103	1050.000	396.480
104	S104	990.000	396.480
105	S105	930.000	396.480
106	S106	870.000	396.480
107	S107	810.000	396.480
108	S108	750.000	396.480
109	S109	690.000	396.480
110	S110	630.000	396.480
111	S111	570.000	396.480
112	S112	510.000	396.480
113	S113	450.000	396.480
114	S114	390.000	396.480
115	S115	330.000	396.480
116	S116	270.000	396.480
117	S117	210.000	396.480
118	S118	150.000	396.480
119	S119	90.000	396.480
120	S120	30.000	396.480
121	S121	-30.000	396.480
122	S122	-90.000	396.480
123	S123	-150.000	396.480
124	S124	-210.000	396.480
125	S125	-270.000	396.480
126	S126	-330.000	396.480
127	S127	-390.000	396.480
128	S128	-450.000	396.480
129	S129	-510.000	396.480
130	S130	-570.000	396.480
131	S131	-630.000	396.480
132	S132	-690.000	396.480
133	S133	-750.000	396.480
134	S134	-810.000	396.480
135	S135	-870.000	396.480
136	S136	-930.000	396.480
137	S137	-990.000	396.480
138	S138	-1050.000	396.480
139	S139	-1110.000	396.480
140	S140	-1170.000	396.480
141	S141	-1230.000	396.480
142	S142	-1290.000	396.480
143	S143	-1350.000	396.480
144	S144	-1410.000	396.480
145	S145	-1470.000	396.480
146	S146	-1530.000	396.480
147	S147	-1590.000	396.480
148	S148	-1650.000	396.480
149	S149	-1710.000	396.480
150	S150	-1770.000	396.480
151	S151	-1830.000	396.480
152	S152	-1890.000	396.480
153	S153	-1950.000	396.480
154	S154	-2010.000	396.480
155	S155	-2070.000	396.480
156	S156	-2130.000	396.480
157	S157	-2190.000	396.480
158	S158	-2250.000	396.480
159	S159	-2310.000	396.480
160	S160	-2370.000	396.480
161	S161	-2430.000	396.480
162	S162	-2490.000	396.480
163	S163	-2550.000	396.480
164	S164	-2610.000	396.480
165	S165	-2670.000	396.480
166	S166	-2730.000	396.480
167	S167	-2790.000	396.480
168	S168	-2850.000	396.480
169	S169	-2910.000	396.480
170	S170	-2970.000	396.480
171	S171	-3030.000	396.480
172	S172	-3090.000	396.480
173	S173	-3150.000	396.480
174	S174	-3210.000	396.480
175	S175	-3270.000	396.480
176	S176	-3330.000	396.480
177	S177	-3390.000	396.480
178	S178	-3450.000	396.480
179	S179	-3510.000	396.480
180	S180	-3570.000	396.480

Table 2–1. Pad Layout (2/2)

No.	Name	X [μm]	Y [μm]
181	S181	-3630.000	396.480
182	S182	-3690.000	396.480
183	S183	-3750.000	396.480
184	S184	-3810.000	396.480
185	S185	-3870.000	396.480
186	S186	-3930.000	396.480
187	S187	-3990.000	396.480
188	S188	-4050.000	396.480
189	S189	-4110.000	396.480
190	S190	-4170.000	396.480
191	S191	-4230.000	396.480
192	S192	-4290.000	396.480
193	S193	-4350.000	396.480
194	S194	-4410.000	396.480
195	S195	-4470.000	396.480
196	S196	-4530.000	396.480
197	S197	-4590.000	396.480
198	S198	-4650.000	396.480
199	S199	-4710.000	396.480
200	S200	-4770.000	396.480
201	S201	-4830.000	396.480
202	S202	-4890.000	396.480
203	S203	-4950.000	396.480
204	S204	-5010.000	396.480
205	S205	-5070.000	396.480
206	S206	-5130.000	396.480
207	S207	-5190.000	396.480
208	S208	-5250.000	396.480
209	S209	-5310.000	396.480
210	S210	-5370.000	396.480
211	S211	-5430.000	396.480
212	S212	-5490.000	396.480
213	S213	-5550.000	396.480
214	S214	-5610.000	396.480
215	S215	-5670.000	396.480
216	S216	-5730.000	396.480
217	S217	-5790.000	396.480
218	S218	-5850.000	396.480
219	S219	-5910.000	396.480
220	S220	-5970.000	396.480
221	S221	-6030.000	396.480
222	S222	-6090.000	396.480
223	S223	-6150.000	396.480
224	S224	-6210.000	396.480
225	S225	-6270.000	396.480
226	S226	-6330.000	396.480
227	S227	-6390.000	396.480
228	S228	-6450.000	396.480
229	S229	-6510.000	396.480
230	S230	-6570.000	396.480
231	S231	-6630.000	396.480
232	S232	-6690.000	396.480
233	S233	-6750.000	396.480
234	S234	-6810.000	396.480
235	S235	-6870.000	396.480
236	S236	-6930.000	396.480
237	S237	-6990.000	396.480
238	S238	-7050.000	396.480
239	S239	-7110.000	396.480
240	S240	-7170.000	396.480
241	DUMMY1	-7311.420	407.010
242	DUMMY2	-7772.010	164.880
243	DUMMY3	-7772.010	64.860
244	DUMMY4	-7772.010	-35.160
245	DUMMY5	-7772.010	-135.180
246	DUMMY6	-7772.010	-235.200
247	DUMMY7	-7654.530	-407.010
248	VCOM	-7479.510	-407.010
249	STHL	-7229.490	-407.010
250	DUMMY8	-7054.440	-407.010
251	VDD2	-6793.050	-407.010
252	VDD2	-6693.090	-407.010
253	VDD2	-6593.130	-407.010
254	VDD1	-6331.710	-407.010
255	VDD1	-6231.750	-407.010
256	VDD1	-6131.790	-407.010
257	VSS1	-5878.440	-407.010
258	VSS1	-5778.480	-407.010
259	VSS1	-5678.520	-407.010
260	VSS2	-5428.500	-407.010
261	VSS2	-5328.540	-407.010
262	VSS2	-5228.580	-407.010
263	VCSEL	-4975.260	-407.010
264	R,/L	-4725.240	-407.010
265	MODE	-4475.220	-407.010
266	BA	-4225.200	-407.010
267	GAM	-3975.180	-407.010
268	CM	-3725.160	-407.010
269	POL	-3475.140	-407.010
270	AP	-3225.120	-407.010
271	STB	-2975.100	-407.010
272	D25	-2725.080	-407.010
273	D24	-2475.060	-407.010
274	D23	-2225.040	-407.010
275	D22	-1975.020	-407.010
276	D21	-1725.000	-407.010
277	D20	-1474.980	-407.010
278	CLK	-1224.960	-407.010
279	DUMMY9	-1049.910	-407.010
280	V4	-874.860	-407.010
281	V4	-774.900	-407.010
282	V4	-674.940	-407.010
283	V3	-424.920	-407.010
284	V3	-324.960	-407.010
285	V3	-225.000	-407.010
286	V2	25.080	-407.010
287	V2	125.040	-407.010
288	V2	225.000	-407.010
289	V1	475.020	-407.010
290	V1	574.980	-407.010
291	V1	674.940	-407.010
292	V0	925.020	-407.010
293	V0	1024.980	-407.010
294	V0	1124.940	-407.010
295	DUMMY10	1299.990	-407.010
296	INV	1475.010	-407.010
297	D15	1725.030	-407.010
298	D14	1975.050	-407.010
299	D13	2225.070	-407.010
300	D12	2475.090	-407.010
301	D11	2725.110	-407.010
302	D10	2975.130	-407.010
303	D05	3225.150	-407.010
304	D04	3475.170	-407.010
305	D03	3725.190	-407.010
306	D02	3975.210	-407.010
307	D01	4225.230	-407.010
308	D00	4475.250	-407.010
309	TESTO1	4725.270	-407.010
310	TESTO2	4975.290	-407.010
311	TESTIN	5225.310	-407.010
312	VDD1	5475.360	-407.010
313	VDD1	5575.320	-407.010
314	VDD1	5675.280	-407.010
315	VSS1	5853.630	-407.010
316	VSS1	5953.590	-407.010
317	VSS1	6053.550	-407.010
318	VSS2	6303.570	-407.010
319	VSS2	6403.530	-407.010
320	VSS2	6503.490	-407.010
321	VDD2	6843.180	-407.010
322	VDD2	6943.140	-407.010
323	VDD2	7043.100	-407.010
324	DUMMY11	7304.490	-407.010
325	STHR	7479.540	-407.010
326	DUMMY12	7654.560	-407.010
327	DUMMY13	7772.010	-235.200
328	DUMMY14	7772.010	-135.180
329	DUMMY15	7772.010	-35.160
330	DUMMY16	7772.010	64.860
331	DUMMY17	7772.010	164.880
332	DUMMY18	7311.420	407.010

3. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	Pad No.	I/O	Description
S_1 to S_{240}	Driver output	1 to 240	Output	The D/A converted 64-gray-scale analog voltage is output.
D_{00} to D_{05}	Display data input	308 to 303	Input	The display data is input with a width of 18 bits, viz., the gray scale data (6 bits) by 3 dots (1 pixels). D_{X0}: LSB, D_{X5}: MSB
D_{10} to D_{15}		302 to 297		
D_{20} to D_{25}		277 to 272		
R,/L	Shift direction control input	264	Input	These refer to the shift direction control input. The shift directions of the shift registers are as follows. R,/L = L (left shift): STHL (input), $S_{240} \rightarrow S_1 \rightarrow$ STHR (output) R,/L = H (right shift) : STHR (input), $S_1 \rightarrow S_{240} \rightarrow$ STHL (output)
STHR	Right shift start pulse input/output	325	I/O	These refer to the start pulse I/O pins when driver ICs are connected in cascade. Fetching of display data starts when H is read at the rising edge of CLK. R,/L = L (left shift): STHL input, STHR output R,/L = H (right shift): STHR input, STHL output
STHL	Left shift start pulse input/output	249	I/O	
CLK	Shift clock input	278	Input	This pin is the shift clock input of the shift register. Display data is captured into the data register at the rising edge. The start pulse output enters high level at the rising edge of the 80 th clock following the start pulse input, and becomes the start pulse of the next level driver. The 81th clock of the first driver becomes the start pulse input of the next driver
STB	Latch input	271	Input	A timing signal that latches the contents of the data register. When an H level is read at the rising edge of CLK, the contents of the data register are latched and transferred to the D/A converter, and analog voltage corresponding to the display data is output. Also, because the internal operation via CLK continues even after the STB latch, do not stop CLK. The contents of the shift register are cleared at the rising edge of STB. Following a 1-pulse input at startup, this IC will operate normally. Note that the output switch is turned off at the rising edge of STB. For the STB input timing, refer to **Switching Characteristics Waveform.**
POL	Polarity inversion signal	269	Input	This pin inverts the output polarity. The polarity inversion signal data is captured at the rising edge of STB. The γ-resistor is switched in accordance with the positive/negative polarity. POL = L: Negative polarity POL = H: Positive polarity
INV	Data inversion	296	Input	This pin inverts the input data. Input data in synchronization with the shift clock. INV = L: Normal input INV = H: Data inversion input
VCOM	COM amplitude output	248	Output	This pin inverts the signal input from the POL pin and outputs it following conversion to the V_{DD2} potential at the rising edge of STB. When the VCOM output is not used, VC_{sel} must be fixed to L.
VC_{sel}	COM amplitude output fixing signal	263	Input	The VCOM output is fixed to L. When the VCOM output is not used, VC_{sel} needs to be fixed to L. VC_{sel} = L: VCOM output fixed to L VC_{sel} = H: VCOM signal output in correspondence with POL signal
CM	8-color display mode switching	268	Input	The operating mode is switched to 8-color mode. Input data MSB leads display data. In this mode, turn off the γ-resistor, amplifier, and BIAS circuit. However, when the γ-correction power supply is input externally, the γ-circuit current will flow continuously. CM = L: Normal display mode CM = H: 8-color display mode

(2/2)

Pin Symbol	Pin Name	Pad No.	I/O	Description
AP	Output SW ON/OFF	270	Input	MODE = L This pin turns ON/OFF the BIAS circuit and turns on the output SW and amplifier. When AP is H, the amplifier is set and the LCD is driving. The amplifier output and output SW are turned on at the rising edge of AP, starting the LCD drive. Note that the output SW is turned off at the rising edge of STB and the output becomes Hi-Z (Hi-Z: High impedance). For details, refer to **4.1 Drive Timing by MODE and AP Signal.** For the AP input timing, refer to **Switching Characteristics Waveform.** MODE = H A sauce driver output circuit is changed to an amplifier output by grand fixation. For details, refer to **4.1 Drive Timing by MODE and AP Signal.**
GAM	External γ-usage selection	267	Input	When the γ-correction power supply is input externally, switch GAM to H. If two or more chips are used, be sure to input the γ-correction power supply externally. Figure 4–4 shows an input example of the γ-correction power supply. GAM = L: External γ-correction power supply not input (open) GAM = H: External γ-correction power supply input
MODE	Driver output functional change	265	Input	The drive mode of the sauce driver output by AP pin is set up as follows. For details, please refer to **4.1 Drive Timing by MODE and AP Signal.** MODE = L: Normal drive mode MODE = H: Grand output drive mode
V_0 to V_4	γ-corrected power supplies	294 to 280	–	These pins input the γ-corrected power supplies from outside, the relationship below must be observed. Also, be sure to stabilize the gray-scale-level power supply during gray-scale voltage output. $V_{SS2} \leq V_4 \leq V_3 \leq V_2 \leq V_1 \leq V_0 \leq V_{DD2}$
BA	BIAS current adjustment function	266	Input	This pin adjusts the BIAS current and through rate of amplifier inside IC. Select either the high power mode or low power mode. In addition, as compared with the time of the low power mode, twice about as many bias current as this flows at the time of high power mode. BA = L: Low power mode BA = H: high power mode
$TEST_{IN}$	TEST input pin	311	Input	Set to H or leave open
$TEST_{O1}$, $TEST_{O2}$	TEST output pin	309, 310	Output	Leave open.
V_{DD1}	Logic power supply	254 to 256, 312 to 314	–	2.2 to 3.6 V
V_{DD2}	Driver power supply	251 to 253, 321 to 323	–	4.5 to 5.5 V
V_{SS1}	Logic ground	257 to 259, 315 to 317	–	Ground
V_{SS2}	Driver ground	260 to 262, 318 to 320	–	Ground
Dummy1 to dummy18	Dummy	241 to 247, 250, 279, 295, 324, 326 to 332	–	This pin is dummy.

Caution To avoid latchup failure, the sequence when turning on the power must be V_{DD1} → logic input → V_{DD2} →gray-scale power supply (V_0 to V_4), and the reverse sequence when turning off the power. Follow this sequence during shift periods as well.

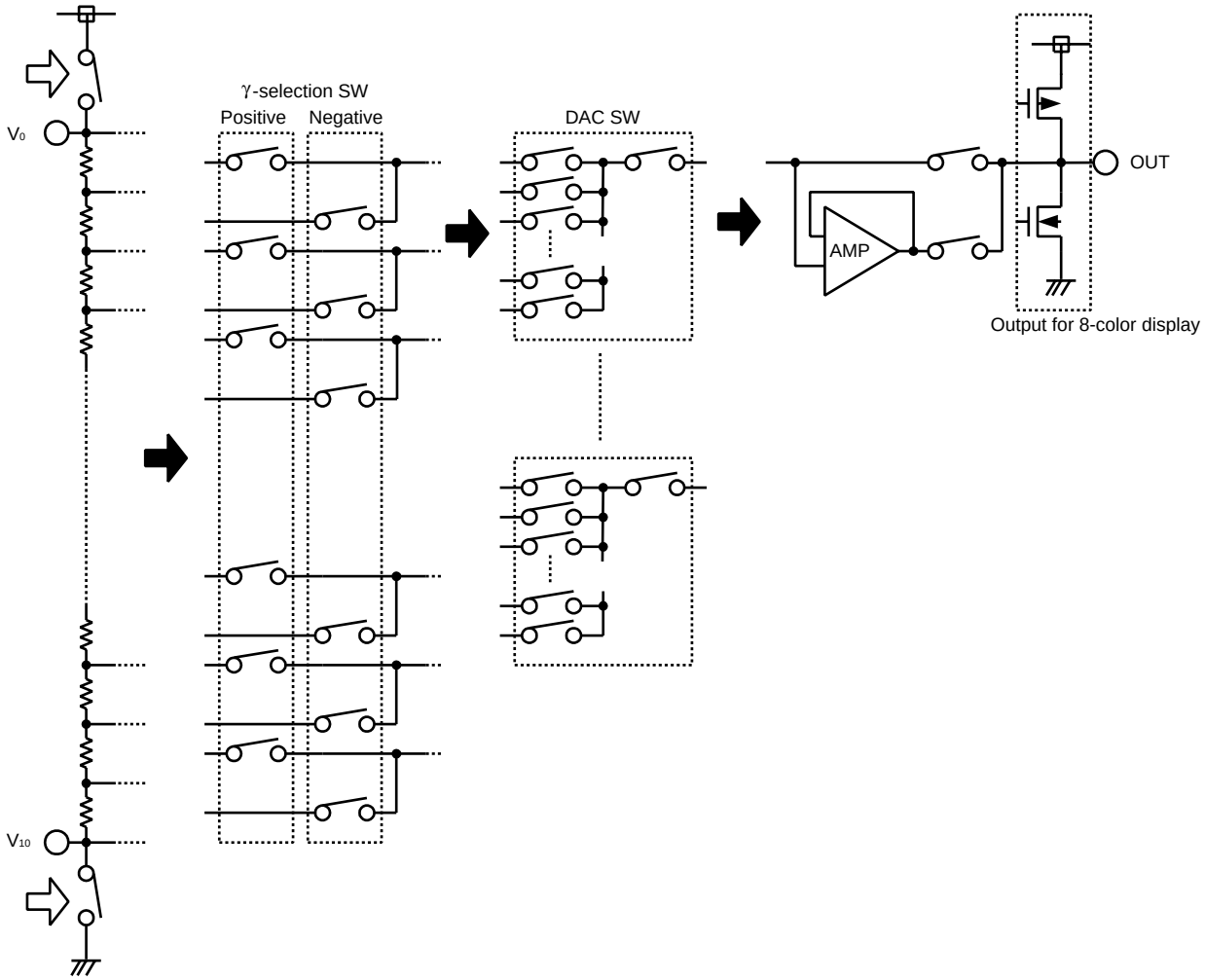
4. DISPLAY DRIVING CIRCUIT

The display driving circuit of μPD161830 consists of γ-resistance and γ-selection switch (SW) which are shown below, a D/A converter, and an output stage.

The function of each block is as follows.

γ-resistance : It is string resistance for γ-curve.
γ-selection switch (SW): Change γ-curve at the time of a positive and a negative drive.
D/A converter : Choose an output voltage level from display data.
Output stage : It consists of amplifier for a drive and a switch for a voltage maintenance drive, and an inverter for 8 color displays.

Figure 4–1. Output Circuit Image



4.1 Drive Timing by MODE and AP Signal

·MODE = L

Normal drive is selected when a MODE pin is set as L.

Based on output stage construction, AP pin, STB pin, CLK pin signal, and the relation of Sn (sauce output) state are shown in the next figure.

From 1 clock of a CLK signal to 4 clock is used for the output stage after a STB standup, it carries out decoding to the latch output voltage level of display data, and transmits to an output circuit.

The output circuit's having prevented from Sn pin output compulsorily the output of the level which is not decided as a Hi-Z state from the standup of a STB signal to the standup of a CLK signal 4 clock.

When AP pin is L input after 4 clock rises, as for Sn pin output, Hi-Z state is maintained, and an output circuit changes from the standup of AP pin input to an AMP drive state. Moreover, Sn pin outputs that the notes 1 which pull up to the voltage (display data) level which requires the potential of a TFT drain line, or are reduced[Note1].

When low power consumption is required, AMP pin is switched from H to L, after a voltage level attain to requirement voltage level L, output circuit stage operation is changed into SW drive[Note2], and it stabilizes a voltage level.

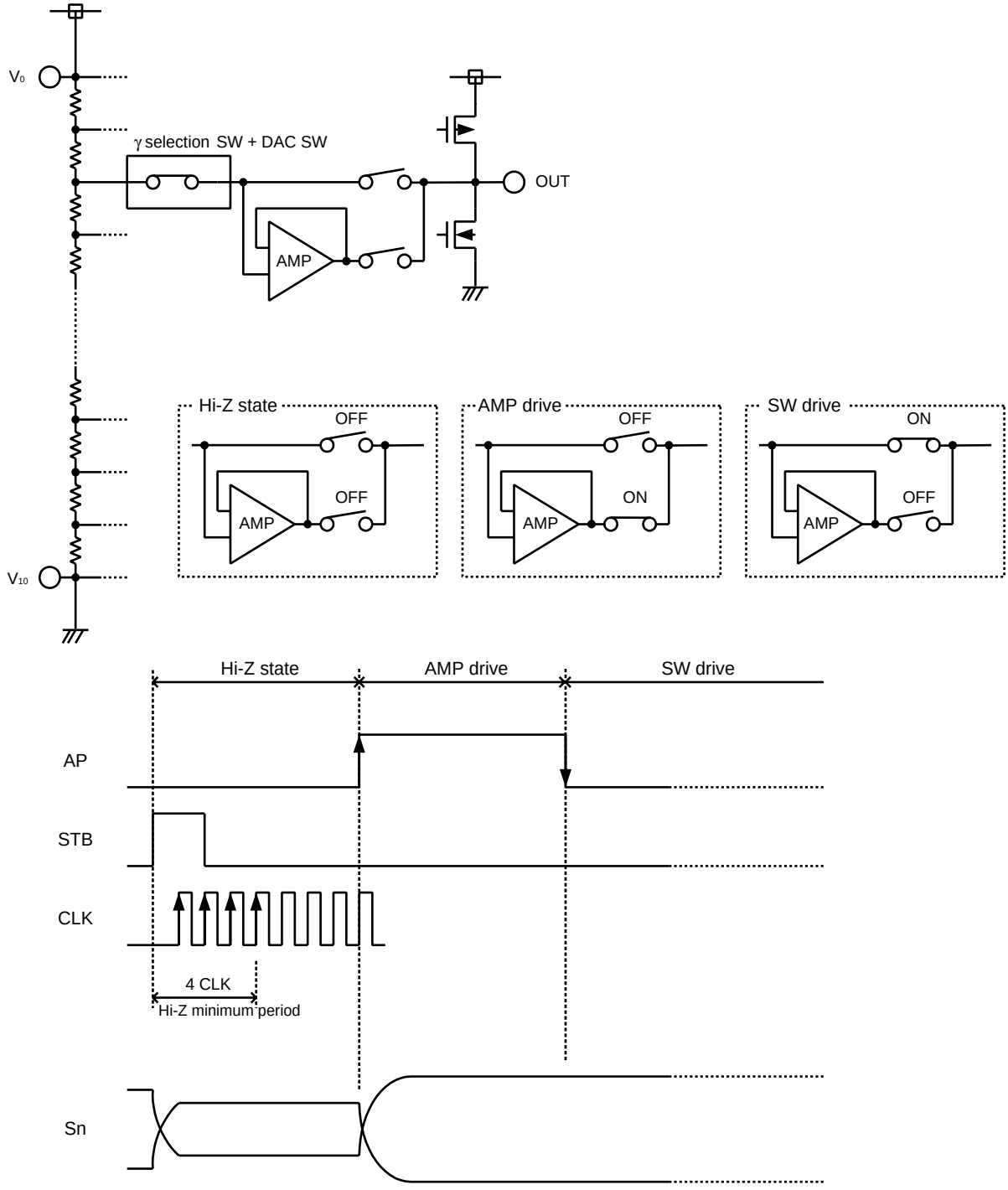
Since liquid crystal load is driven only by SW drive of γ-resistance direct file when referred to as AP = L before attainment of the level to demand, most time is needed for level attainment.

Since this timing (AP = H period) is dependent on the load conditions of liquid crystal, it is a real use TFT panel and fully needs to be evaluated.

Notes 1. When it is always set as AP = H, Sn pin starts an AMP drive automatically after the standup of 4 clock.

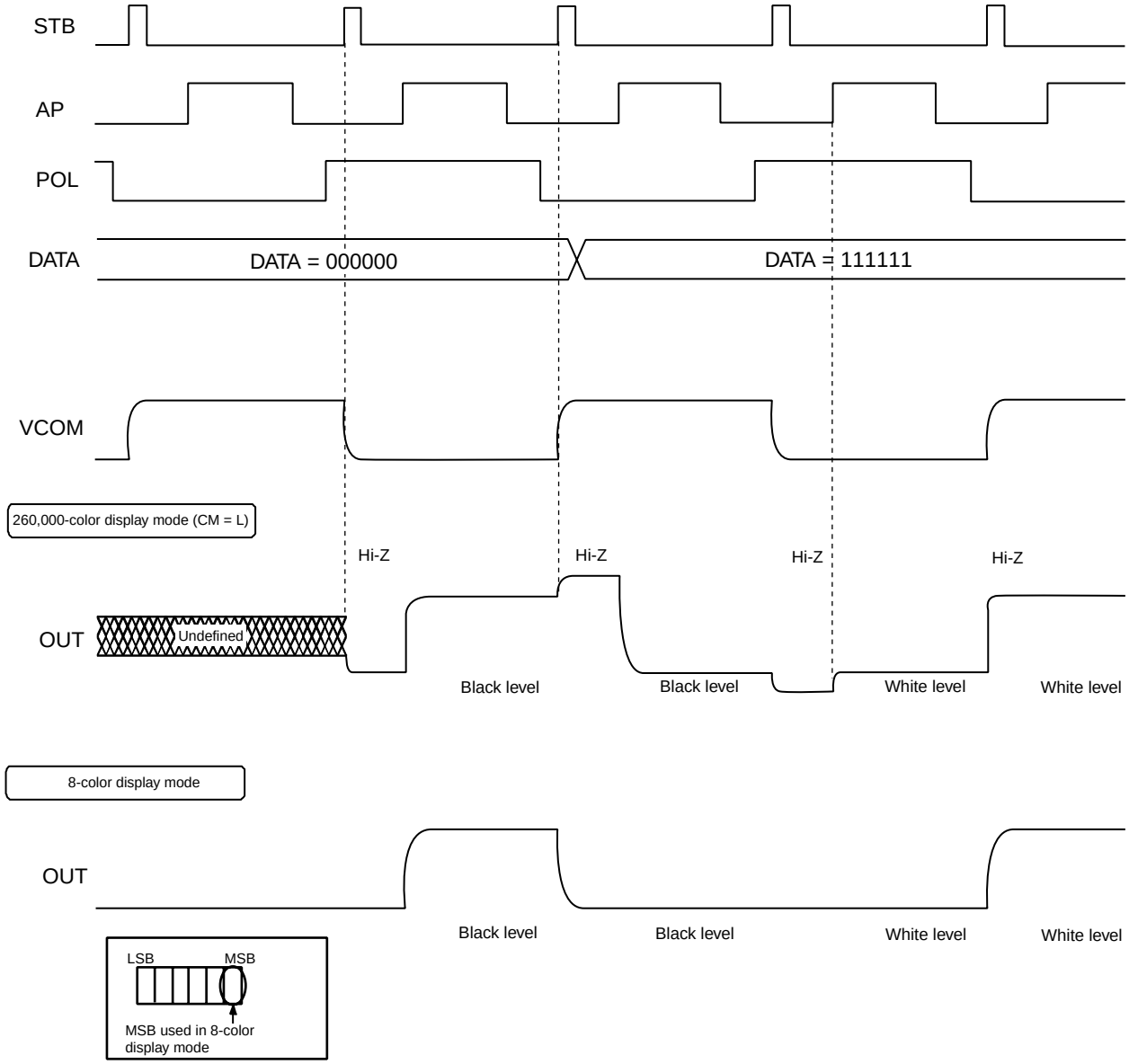
2. At the time of SW drive, stop the bias current of an output stage amplifier circuit, and stop the consumption current of the output stage.

Figure 4–2. Output Stage Operation Image



Examples of the input/output timing of each signal during white and black display in normal mode are shown below.

Figure 4–3. Timing Chart

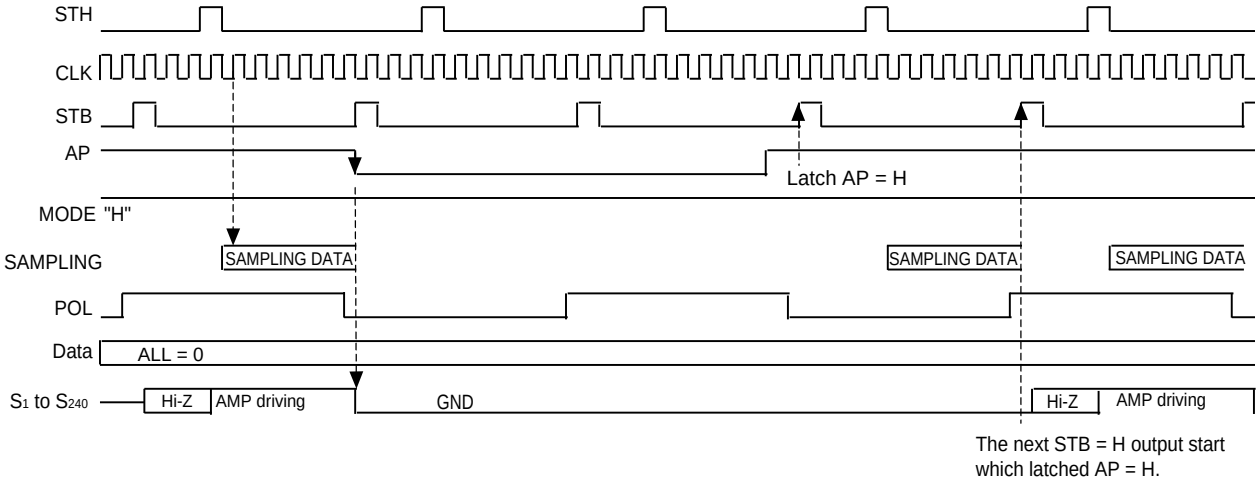


·MODE = H (GND output driving)

When a MODE pin is set as H, the output change function by AP pin is changed as follows.

AP Pin	Sn Pin (source output) Drive
L	GND output (V_{SS} fixed)
H	Normal AMP operation

As for sauce output, output is fixed to ground (V_{SS}) in falling of AP signal at the time of GND output drive (MODE = H). Moreover, the return to an APM drive usually returns from the next STB = H period which latched AP = H by the rising edge of STB signal. The relationship of the CLK signal at the time of a GND output drive, a STB signal, AP signal, and Sn state is shown as follows.

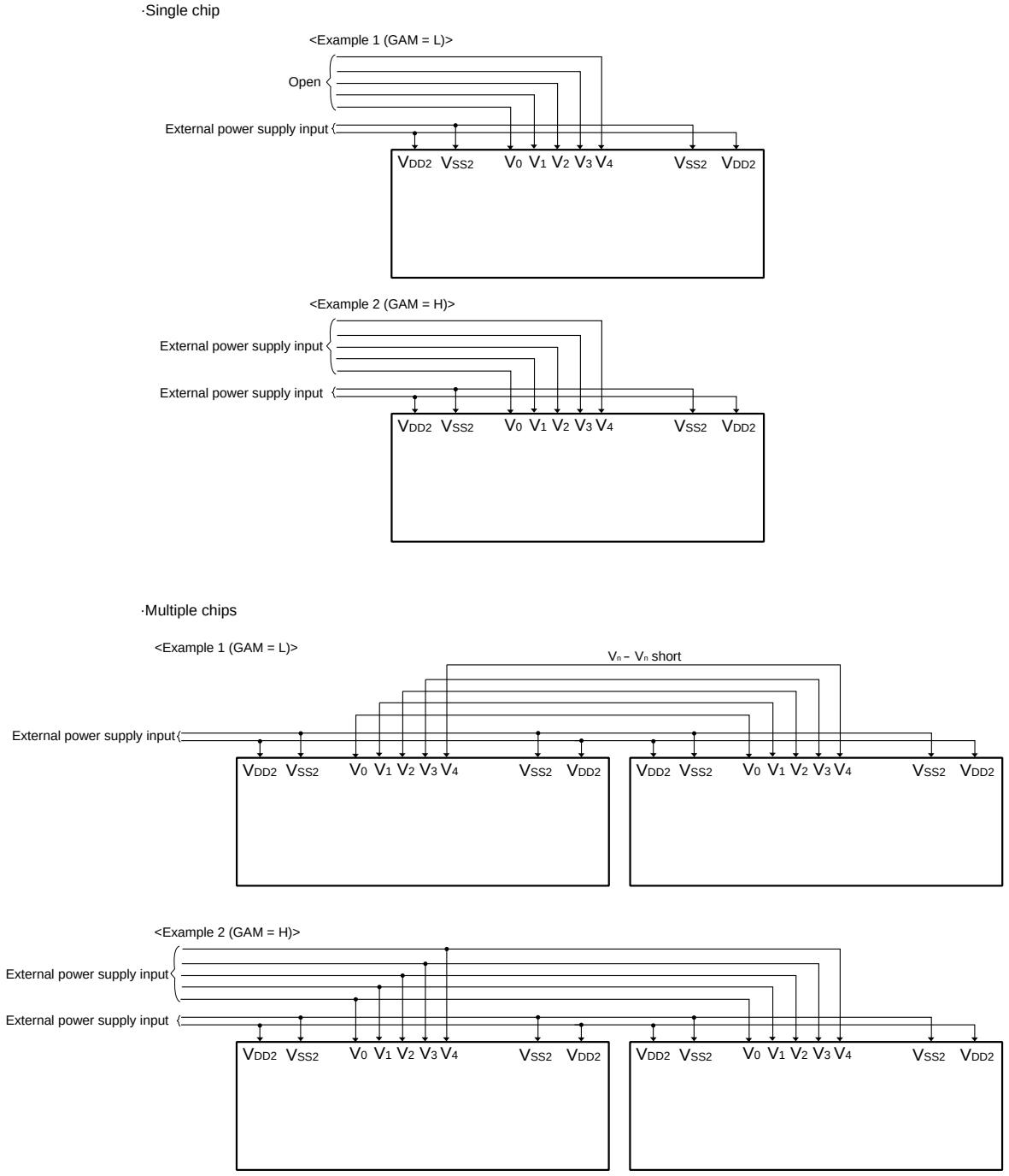


4.2 γ-Correction Power Supply Connection Example

The μPD161830 enables customization of the γ-correction power supply on both the positive and negative polarity sides (refer to **6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE**). Consequently, a γ-correction power supply does not have to be input externally when a single source-driver chip is being used in the panel.

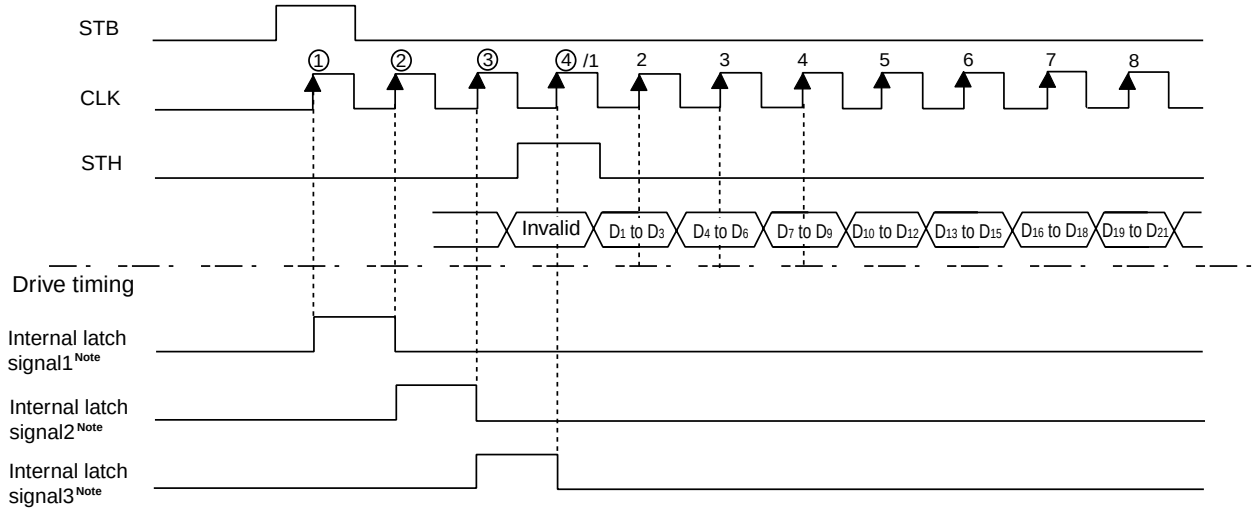
Multiple chips can also be used without having to input a γ-correction power supply externally because the error between the chips can be absorbed by shorting the γ-correction power supply pins, as shown in Figure 4–4.

Figure 4–4. γ-Correction Power-Supply Connection Example



4.3 CLK Signal Input

Input at least 4 clocks of the CLK signal after the rising of the STB signal.



Note Internal latch signal : It is the signal that do latch the display data put in data register in output latch circuit.

5. MODE EXPLANATION

Normal Mode/ 8-clor Display Mode

CM	POL	Data	Driver Output Status	Driver Output (in normally white)
H	H	MSB = H	8-color mode	White level display
		MSB = L		Black level display
	L	MSB = H		White level display
		MSB = L		Black level display
L	H	All bit = H	260,000-color mode	White level display
		All bit = L		Black level display
	L	All bit = H		White level display
		All bit = L		Black level display

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The relationship between input data and output voltage are shown in Table 6–2.

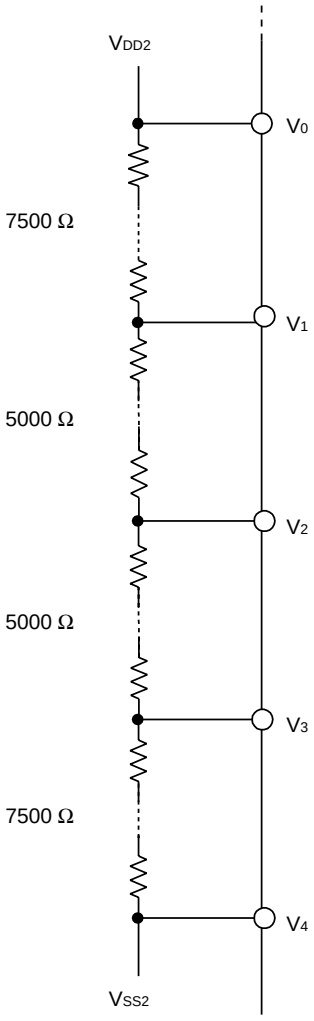
Any 3 major points V_1 to V_3 from the LCD panel γ-characteristics curve can be used as the external power supplies.

The relationship V_0 to V_4 external power supplies and γ-correction resistance is shown in Table 6–1, Figure 6–1.

Table 6–1. Relationship between External Power Supply Pins and γ-correction Resistance

Pin Name	Voltage (V)	Resistance (Ω)
V_0	5.0	0
V_1	3.5	7,500
V_2	2.5	12,500
V_3	1.5	17,500
V_4	0	25,000

Figure 6–1. Relationship between External Power Supply Pins and γ-correction Resistance



This external power supply pins (V_0 to V_4) can customize the γ-correction voltage by selecting the desired voltage from one of 250 divisions of the string resistor between V_{SS2} and V_{DD2}, which generated γ-correction voltage. Note that the voltage can be selected individually for both positive and negative polarity.

Table 6–2. Relationship of Input Data and Output Voltage in the μPD161830

T.B.D.

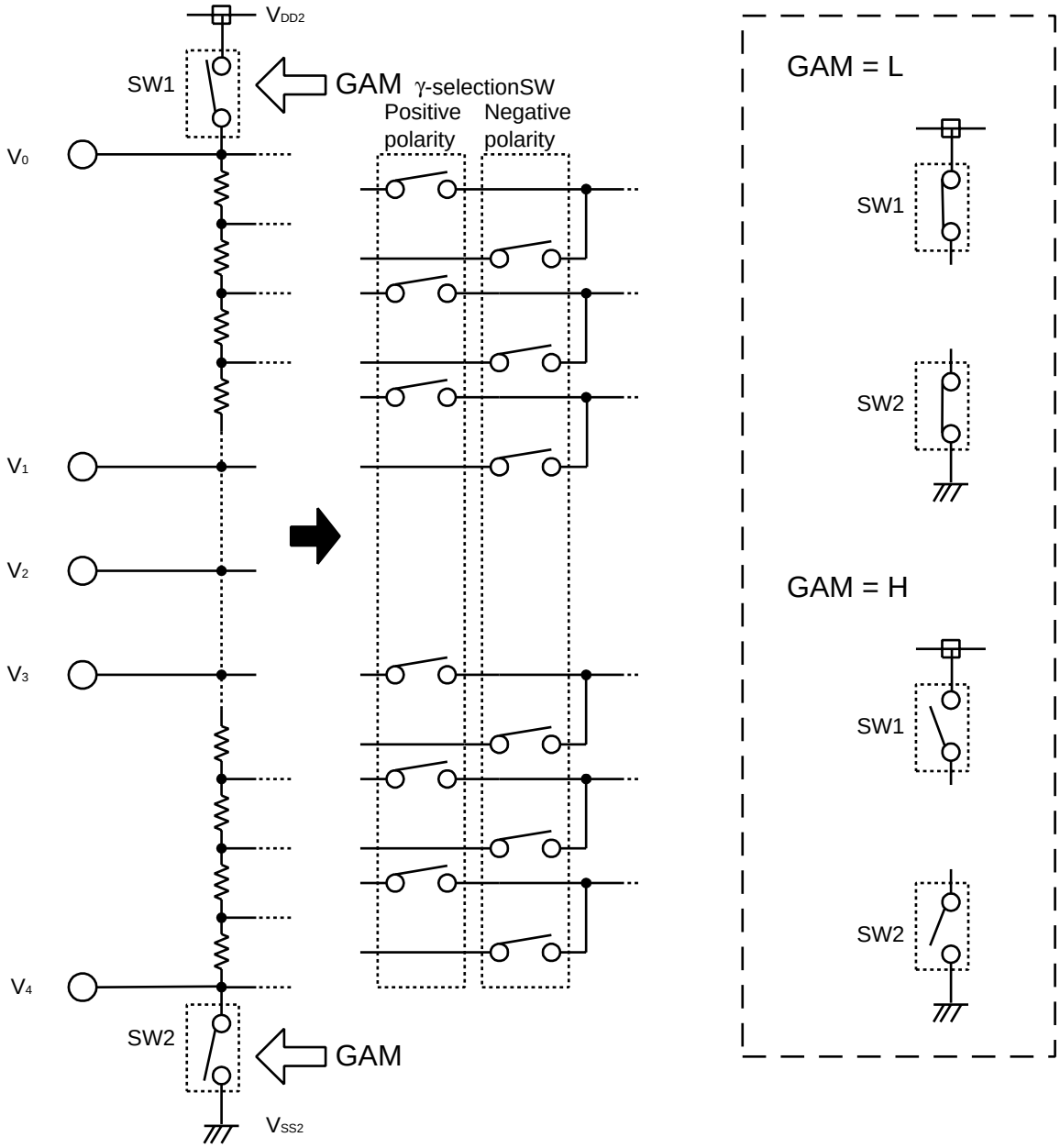
Remark T.B.D. (To be determined.)

6.1 Connection between γ-correction Resistance, Power Supply, and GND Pin

Connection of γ- compensation resistance power supply (V_0 to V_4) and a power supply pin (V_{DD2} and V_{SS2}) is indicated below to be γ- compensation resistance of μPD161830.

By setup of a GAM pin, as for γ-compensation resistance, connection changes the highest minimum potential between V_{DD2} to V_{SS2} or among V_0 to V_4.

Figure 6–2. GAM Pin Function



7. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 6 bits x RGBs (3 dots)

Input width: 18 bits (1-pixel data)

R,/L = H (Right shift)

Output	S_1	S_2	S_3	S_4	...	S_{239}	S_{240}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{00} to D_{05}	...	D_{10} to D_{15}	D_{20} to D_{25}

R,/L = L (Left shift)

Output	S_1	S_2	S_3	S_4	...	S_{239}	S_{240}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{00} to D_{05}	...	D_{10} to D_{15}	D_{20} to D_{25}

8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.3 to +4.5	V
Driver Part Supply Voltage	V_{DD2}	–0.3 to +6.0	V
Input Voltage	V_I	–0.3 to $V_{DD1,2}$ + 0.3	V
Output Voltage	V_O	–0.3 to $V_{DD1,2}$ + 0.3	V
Operating Ambient Temperature	T_A	–20 to +75	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –20 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}		2.2		3.6	V
Driver Part Supply Voltage	V_{DD2}		4.5	5.0	5.5	V
High-Level Input Voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}		0		0.3 V_{DD1}	V
γ-Corrected Voltage	V_0 to V_4		V_{SS2}		V_{DD2}	V
Clock Frequency	f_{CLK}				15	MHz

Electrical Characteristics (T_A = –20 to +75°C, V_{DD1} = 2.2 to 3.6 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Leak Current	I_{IL}	D_{00}-D_{05}, D_{10}-D_{15}, D_{20}-D_{25}, R,/L, STB, CLK, STHR(L), INV, CM, AP, BA, POL, GAM, VC_{sel}			±1.0	μA
Input Current	I_{IL2}	$TEST_{IN}$	10	40	200	μA
High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = –1.0 mA	V_{DD1} – 0.5			V
Low-Level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = +1.0 mA			0.5	V
VCOM Output Voltage	V_{OH2}	V_{DD2} = 5.0 V, I_O = –1.0 mA	V_{DD2} – 0.5			V
	V_{OL2}	V_{DD2} = 5.0 V, I_O = +1.0 mA			0.5	V
γ-Correction Power-supply Static Current Consumption	I_γ	V_0 = 5.0 V, V_4 = 0 V (when in γ-correction power mode)	100	200	400	μA
Driver Output Current (AMP drive)	I_{VOH1}	V_{DD2} = 5.0 V, V_{OUT} = V_X – 1.0 V **Note1** Input data: 1FH		–0.5	–0.15	mA
	I_{VOL1}	V_{DD2} = 5.0 V, V_{OUT} = V_X + 1.0 V **Note1** Input data: 20H	0.15	0.50		mA
Driver Output Current (Switch drive)	I_{VOH2}	V_{DD2} = 5.0 V, V_{OUT} = V_X – 1.0 V **Note1** Input data: 1FH		–50	–15	μA
	I_{VOL2}	V_{DD2} = 5.0 V, V_{OUT} = V_X + 1.0 V **Note1** Input data: 20H	15	40		μA
Driver Output Current (8-color display mode)	V_{VOH3}	V_{DD2} = 5.0 V, I_O = –50 μA	V_{DD2} – 0.5			V
	V_{VOL3}	V_{DD2} = 5.0 V, I_O = +50 μA			0.5	V
Output Voltage Deviation	ΔV_O	V_{DD1} = 2.5 V, V_{DD2} = 5.0 V, V_{OUT} = 2.5 V **Note1**		±10	±20	mV
Output Voltage Range	V_O	Input data: 00H to 3FH	V_{SS2} + 0.05		V_{DD2} – 0.05	V
Logic Part Dynamic Current Consumption	I_{DD1}	With no load **Note2**		0.4	0.8	mA
Driver Part Dynamic Current Consumption	I_{DD2}	V_{DD} = 5.0 V, with no load **Note2**		0.9	1.5	mA

Notes 1. V_X refers to the output voltage of analog output pins S_1 to S_{240}.

V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{240}.

2. f_{CLK} = 15 MHz, STB cycle = 60 μs, AP pulse width = 15 μs, BA=L (low power mode)

Switching Characteristics (T_A = –20 to +75°C, V_{DD1} = 2.2 to 3.6 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

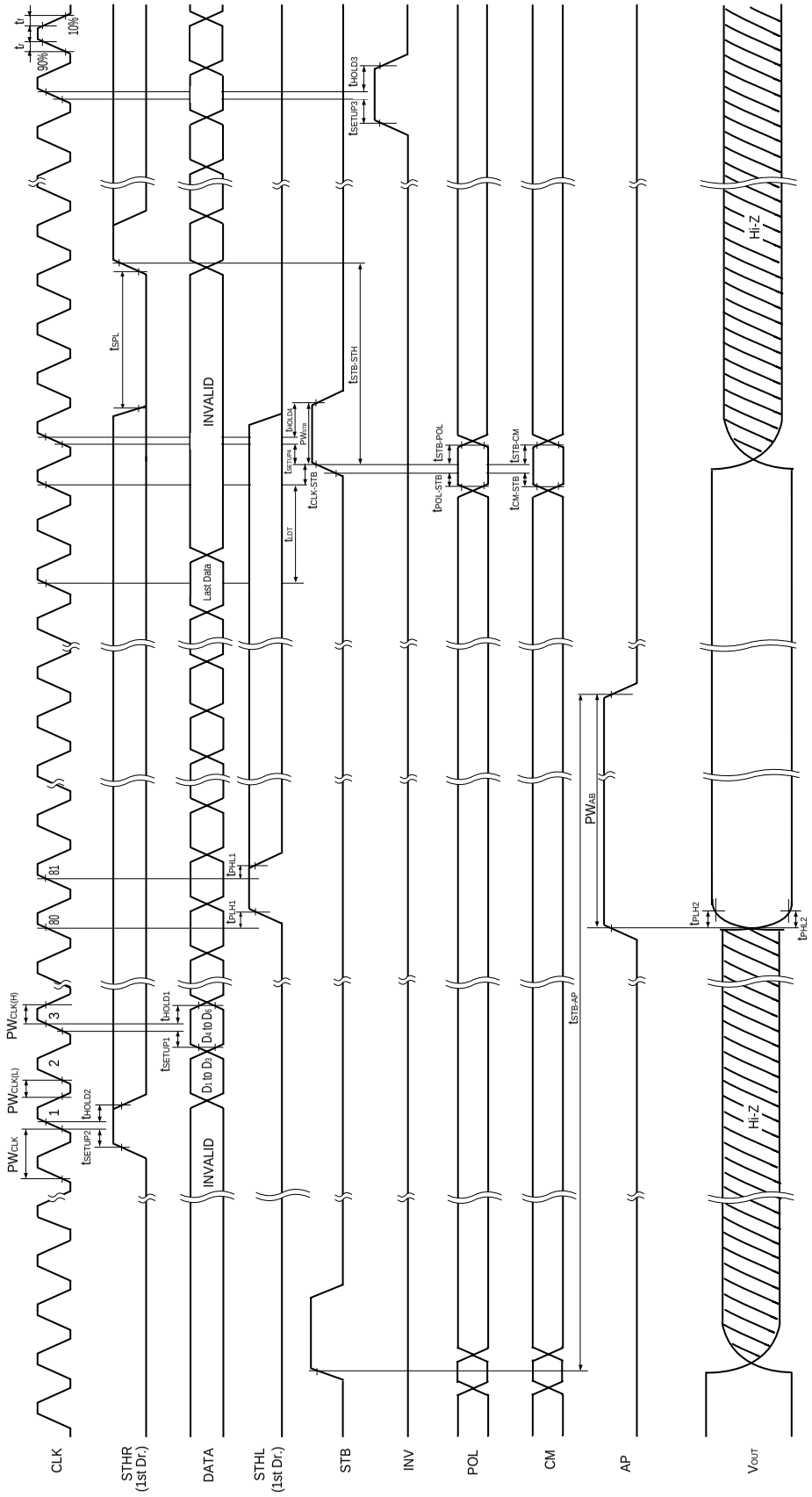
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 15 pF			25	ns
	t_{PHL1}				25	ns
Driver Output Delay Time	t_{PLH2H}	C_L = 30 pF			12	μs
(High power mode)	t_{PHL2H}	AP↑ →V_{OUT} – 100 mV or V_{OUT} + 100 mV			12	μs
Driver Output Delay Time	t_{PLH2L}	C_L = 30 pF			15	μs
(Low power mode)	t_{PHL2L}	AP↑ →V_{OUT} – 100 mV or V_{OUT} + 100 mV			15	μs
Input Capacitance	C_{I1}	V_0 to V_4, T_A = 25°C		5	15	pF
	C_{I2}	Excluded V_0 to V_4, T_A = 25°C		10	15	pF

Timing Requirements (T_A = –20 to +75°C, V_{DD1} = 2.2 to 3.6 V, V_{SS1} = 0 V, t_r = t_f = 10 ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		65			ns
Clock Pulse High Period	$PW_{CLK(H)}$		20			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		20			ns
Data Setup Time	t_{SETUP1}		20			ns
Data Hold Time	t_{HOLD1}		20			ns
Start Pulse Setup Time	t_{SETUP2}		20			ns
Start Pulse Hold Time	t_{HOLD2}		20			ns
Start Pulse Low Period	t_{SPL}		3			CLK
Last Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	CLK↑ →STB↑	20			ns
STB Pulse Width	PW_{STB}		40			ns
Start Pulse Rising Time	$t_{STB-STH}$	STB↑ →STH↑	3			CLK
INV Set-up Time	t_{SETUP3}		20			ns
INV Hold Time	t_{HOLD3}		20			ns
STB Set-up Time	t_{SETUP4}		20			ns
STB Hold Time	t_{HOLD4}		20			ns
POL-STB Time	$t_{POL-STB}$		0			ns
STB-POL Time	$t_{STB-POL}$		40			ns
CM-STB Time	t_{CM-STB}		0			ns
STB-CM Time	t_{STB-CM}		40			ns
STB-AP Time	t_{STB-AP}	STB↑ →AP↓	20			μs
AP Pulse Width (High power mode)	PW_{APH}		12			μs
AP Pulse Width (Low power mode)	PW_{APL}	STB cycle 40μs, C_L = 30 pF	15			μs
AP Set-up Time	t_{SETUP5}	STB↑, MODE = H	0			ns
AP Hold Time	t_{HOLD5}	STB↑, MODE = H	40			ns

★ **Switching Characteristic Waveform (R,/L= H)**

Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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