

# UPC824, UPC4074

## Low Noise J-FET Input Quad Operational Amplifier

### DESCRIPTION

The UPC824 and 4074 are low noise versions operational amplifier of UPC804 and 4084 series with the general-purpose J-FET input. Compared with the UPC804 and 4084 series, various characteristics such as input referred noise, input offset voltage and input bias current have been improved. It is therefore ideal for application circuits such as preamplifiers and active filters for measurement, audio and measurement where low noise, high input impedance and high-speed characteristics are important.

Depending on the operating ambient temperature, UPC824 is suitable for communication application while UPC4074 is suitable for general-purpose usage.

Along with this series of lineup, the dual type op-amp UPC822 and 4072 with same circuit configuration are also available.

### FEATURES

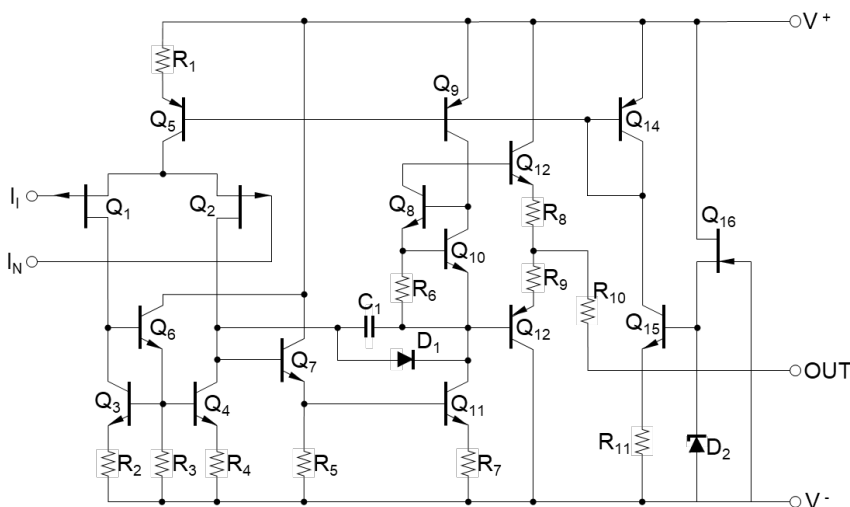
- Input Offset Voltage ±2 mV (TYP.)
- Input Bias Current 30 pA (TYP.)
- Slew Rate 13 V/μs (TYP.)
- Unity Gain Frequency 3 MHz (TYP.)
- Input Equivalent Noise Voltage Density 17 nV/√Hz (TYP.) (f = 1 kHz)
- Built-In Phase Compensation Circuit
- Built-In Output Short Circuit Protection
- Standard Quad op-amp terminal connection (pin compatible)

### ORDERING INFORMATION

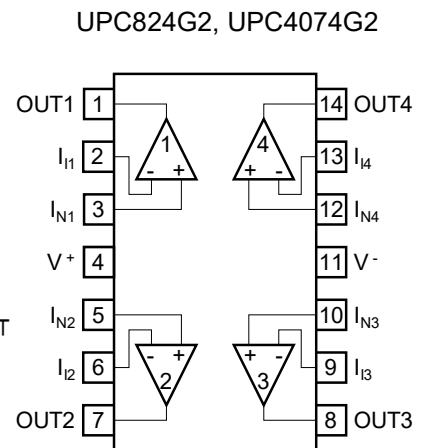
Order Name <sup>(1)</sup>	Package
UPC824G2-AP	14-Pin plastic SOP ( 5.72 mm (225 mil ) )
UPC4074G2-AP	14-Pin plastic SOP ( 5.72 mm (225 mil ) )

(1) Order names containing E1 or E2 indicate that the packaging format is embossed taping.  
Pin 1 of E1 is on draw-out side, and pin 1 of E2 is at take-up side.

### EQUIVALENT CIRCUIT (1/4 Circuit)



### PIN CONFIGURATION (Top View)



**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C)**

Parameter	Symbol	UPC824G2	UPC4074G2	Unit
Supply Voltage <sup>Note1</sup>	V <sup>+</sup> - V <sup>-</sup>	-0.3 to +36		V
Differential Input Voltage	V <sub>ID</sub>	±30		V
Input Voltage <sup>Note2</sup>	V <sub>I</sub>	V <sup>-</sup> -0.3 to V <sup>+</sup> +0.3		V
Output Applied Voltage <sup>Note3</sup>	V <sub>O</sub>	V <sup>-</sup> -0.3 to V <sup>+</sup> +0.3		V
Total Power Dissipation <sup>Note4</sup>	P <sub>T</sub>	550		mW
Output Short Circuit Duration <sup>Note5</sup>		Indefinite		s
Operating Ambient Temperature	T <sub>A</sub>	-40 to +85	-20 to+80	°C
Storage Temperature	T <sub>stg</sub>	-55 to +125		°C

- [Note]**
- Note that reverse connections of the power supply may damage the ICs.
  - The input terminal must be applied within the input voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp input voltage must operate within the electrical characteristics range of input common-mode voltage.
  - The output terminal must be applied within the output voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp output voltage must operate within the electrical characteristics range of maximum output voltage.
  - This is the value at T<sub>A</sub> ≤ +25 °C. De-rate value at -5.5 mW/°C when T<sub>A</sub> > 25 °C.
  - Please use below the total power dissipation and the de-rating value from Note 4.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	V <sup>±</sup>	±5		±16	V
Load Current	I <sub>O</sub>			±10	mA
Load Capacitance (When A <sub>v</sub> = +1)	C <sub>L</sub>			100	pF

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, V<sup>±</sup> = ±15 V)**

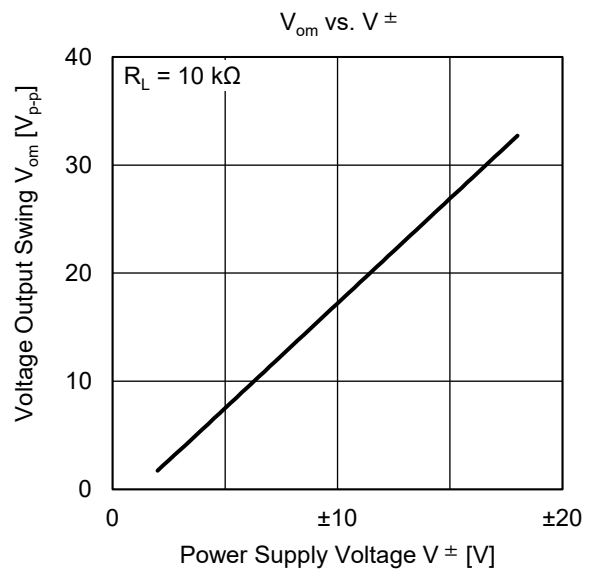
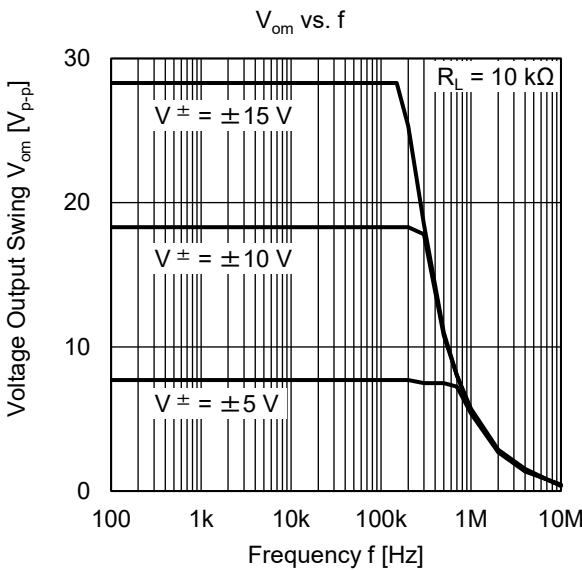
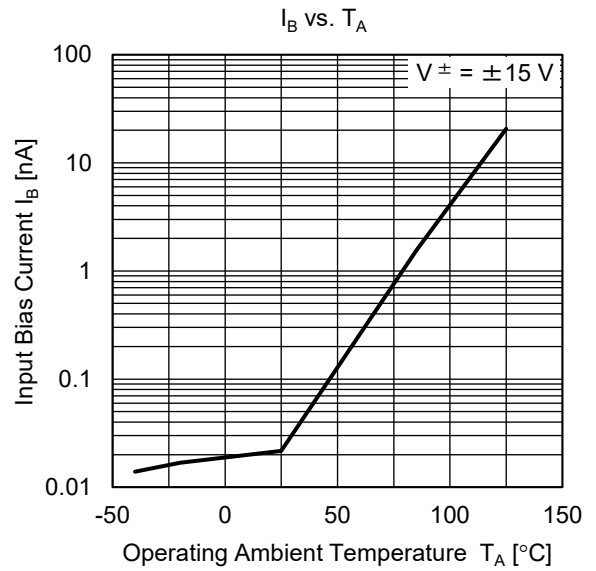
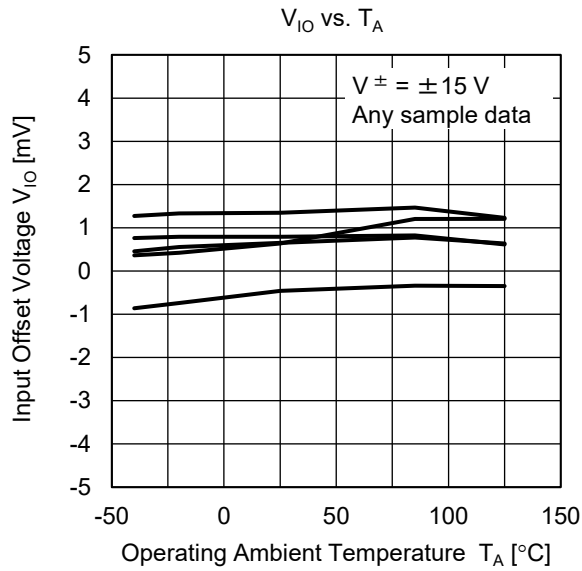
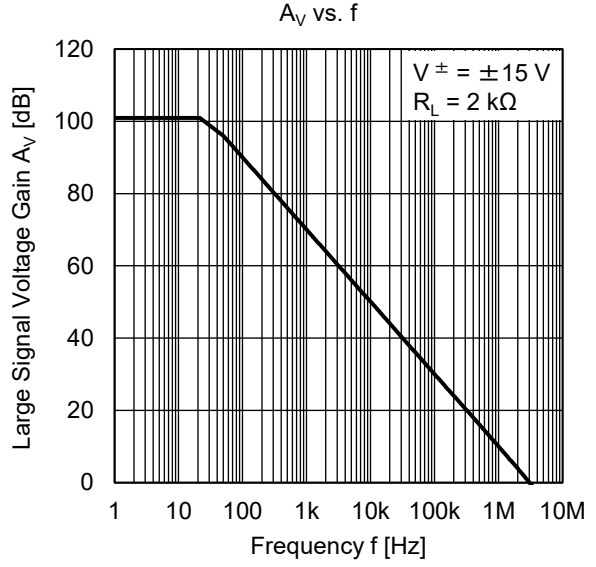
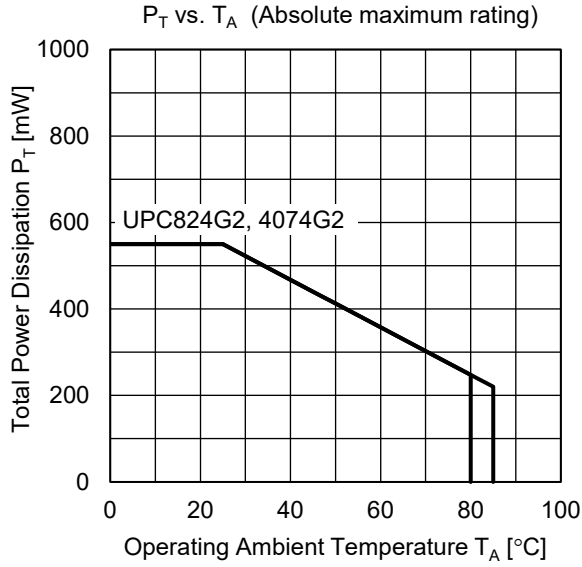
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Input Offset Voltage	V <sub>IO</sub>		±2	±10	mV	R <sub>S</sub> ≤ 50 Ω
Input Offset Current <sup>Note6</sup>	I <sub>IO</sub>		±5	±50	pA	
Input Bias Current <sup>Note6</sup>	I <sub>B</sub>		30	200	pA	
Large Signal Voltage Gain	A <sub>V</sub>	25000	200000			R <sub>L</sub> ≥ 2 kΩ, V <sub>O</sub> = ±10 V
Circuit Current <sup>Note7</sup>	I <sub>CC</sub>		8	10	mA	I <sub>O</sub> = 0 A
Common Mode Rejection Ratio	CMR	70	90		dB	
Supply Voltage Rejection Ratio	SVR	70	90		dB	
Voltage Output Swing	V <sub>om</sub>	±12	±13.5		V	R <sub>L</sub> ≥ 10 kΩ
Voltage Output Swing	V <sub>om</sub>	±10	±12		V	R <sub>L</sub> ≥ 2 kΩ
Input Common-Mode Voltage Range	V <sub>ICM</sub>	±10	+15 -13		V	
Slew Rate	SR		13		V/μs	A <sub>V</sub> = 1
Unity Gain Frequency	f <sub>unity</sub>		3		MHz	
Input Equivalent Noise Voltage	V <sub>n</sub>		4		μV <sub>r.m.s</sub>	R <sub>S</sub> = 100 Ω, f = 10 Hz to 10 kHz
Input Equivalent Noise Voltage Density	e <sub>n</sub>		17		nV/√Hz	R <sub>S</sub> = 100 Ω, f = 1 kHz
Channel Separation			120		dB	
Input Offset Voltage	V <sub>IO</sub>			±13	mV	R <sub>S</sub> ≤ 50 Ω, T <sub>A</sub> = -20 to +70 °C
Average V <sub>IO</sub> Temperature Drift	ΔV <sub>IO</sub> /ΔT		±10		μV/°C	T <sub>A</sub> = -20 to +70 °C
Input Offset Current <sup>Note6</sup>	I <sub>IO</sub>			±2	nA	T <sub>A</sub> = -20 to +70 °C
Input Bias Current <sup>Note6</sup>	I <sub>B</sub>			7	nA	T <sub>A</sub> = -20 to +70 °C

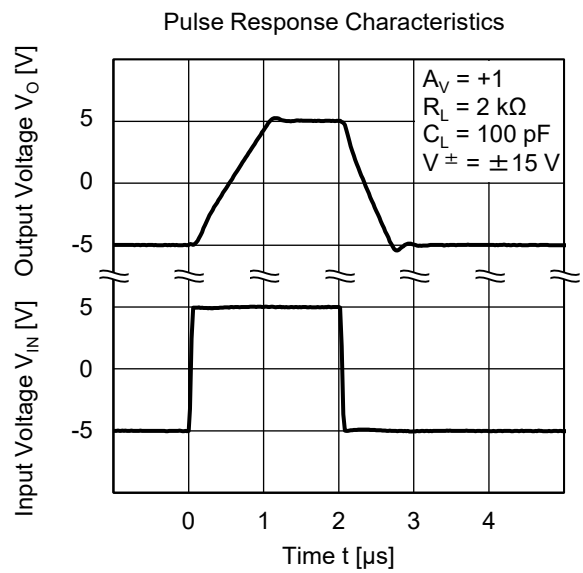
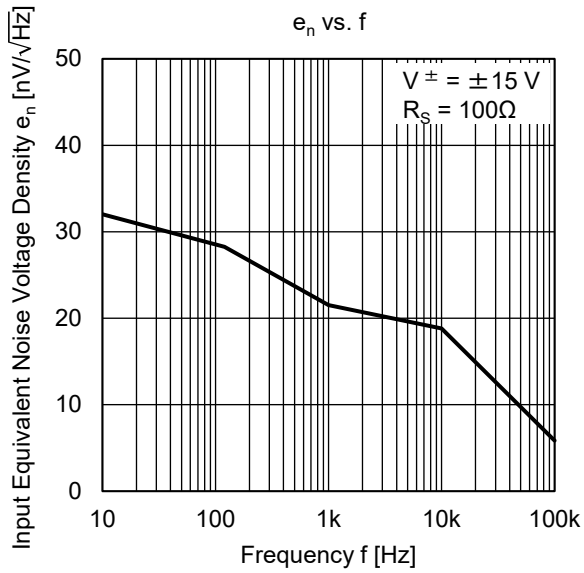
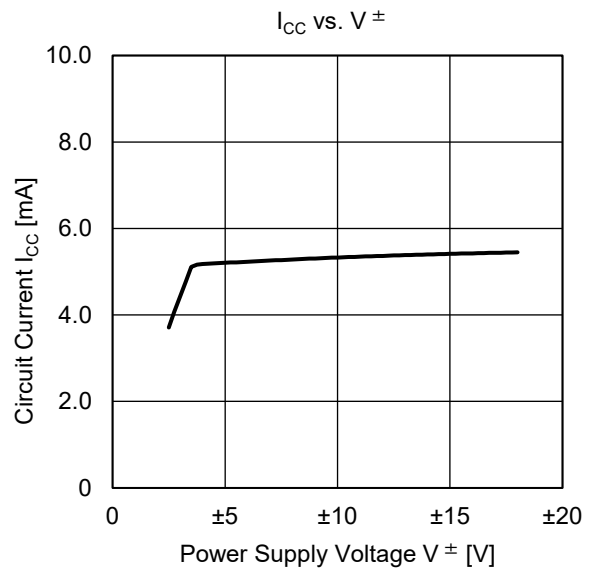
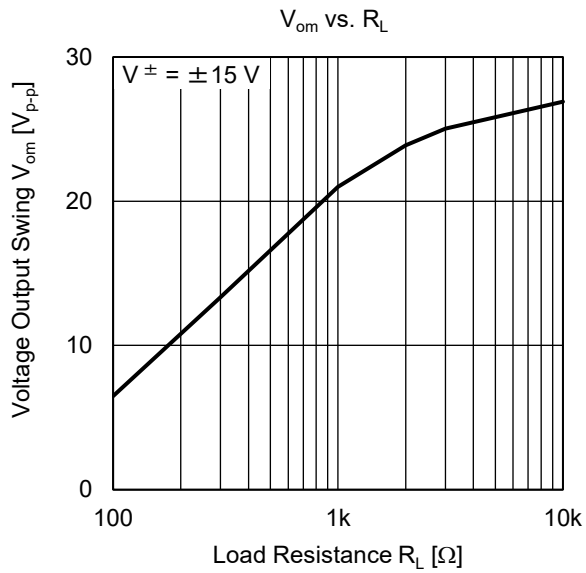
- 【Note】** 6. The direction of the input bias current is the same direction that flows into the IC because the first stage is composed of Pch J-FET. When T<sub>J</sub> = 25°C or higher, it increases exponentially with increase in temperature (please see I<sub>B</sub> - T<sub>A</sub> characteristics). During measurement, please kindly take care of T<sub>J</sub> ≐ T<sub>A</sub>.
7. It is the current that flows into the internal circuit. This current flows irrespective of the channel usage.

**Caution**

Since UPC824, 4074 have high input impedance characteristics, please be careful of insulation between the terminals on the board.

**ELECTRICAL CHARACTERISTICS CURVE (T<sub>A</sub> = 25 °C, TYP.)**



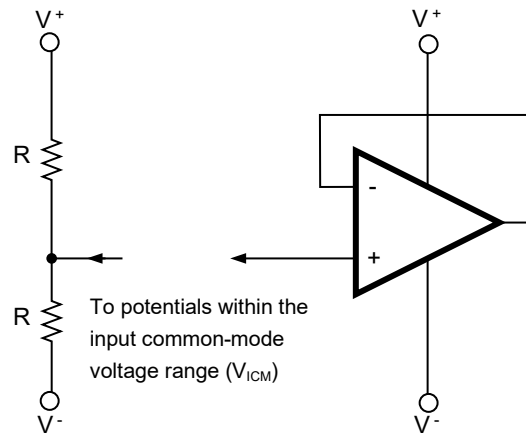


## USE WITH PRECAUTIONS

### Managing unused circuits

If there is an unused circuit, the following connection is recommended.

### Example of handling unused circuit



Note in this example, an intermediate voltage of  $V^+$  and  $V^-$  is applied.

- **Power Supply (Dual Power Supply / Single Power Supply)**

The op-amp operates when a predetermine voltage is applied between  $V^+$  to  $V^-$ . Therefore, while it operates from a single power supply ( $V^- = \text{GND}$ ), it is not possible to operate the input and output near GND. So please be careful of the input common-mode voltage range and maximum output voltage.

- **Ratings of input/output pin voltage**

When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the voltage of input pin is lower than  $V^-$ , or the voltage of output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- **Input common-mode voltage range**

When the supply voltage does not meet the condition of electrical characteristics, the input common-mode voltage range is as follows.

$$V_{ICM} \text{ (TYP.)}: V^- + 2 \text{ to } V^+ \text{ [V]} (T_A = 25^\circ\text{C})$$

During designing, do include some margin by considering characteristic variations, temperature characteristics etc.

- **Maximum Output Voltage**

When the supply voltage does not meet the condition of electrical characteristics, the TYP. value range of the maximum output voltage is as follows:

$$V_{om+} \text{ (TYP.)}: V^+ - 1.5 \text{ [V]} (T_A = 25^\circ\text{C}), V_{om-} \text{ (TYP.)}: V^- + 1.5 \text{ [V]} (T_A = 25^\circ\text{C})$$

During designing, do include some margin by considering characteristic variations, temperature characteristics and so on. In addition, also note that the output voltage range ( $V_{om+}$  to  $V_{om-}$ ) will become narrow when the output current increases.

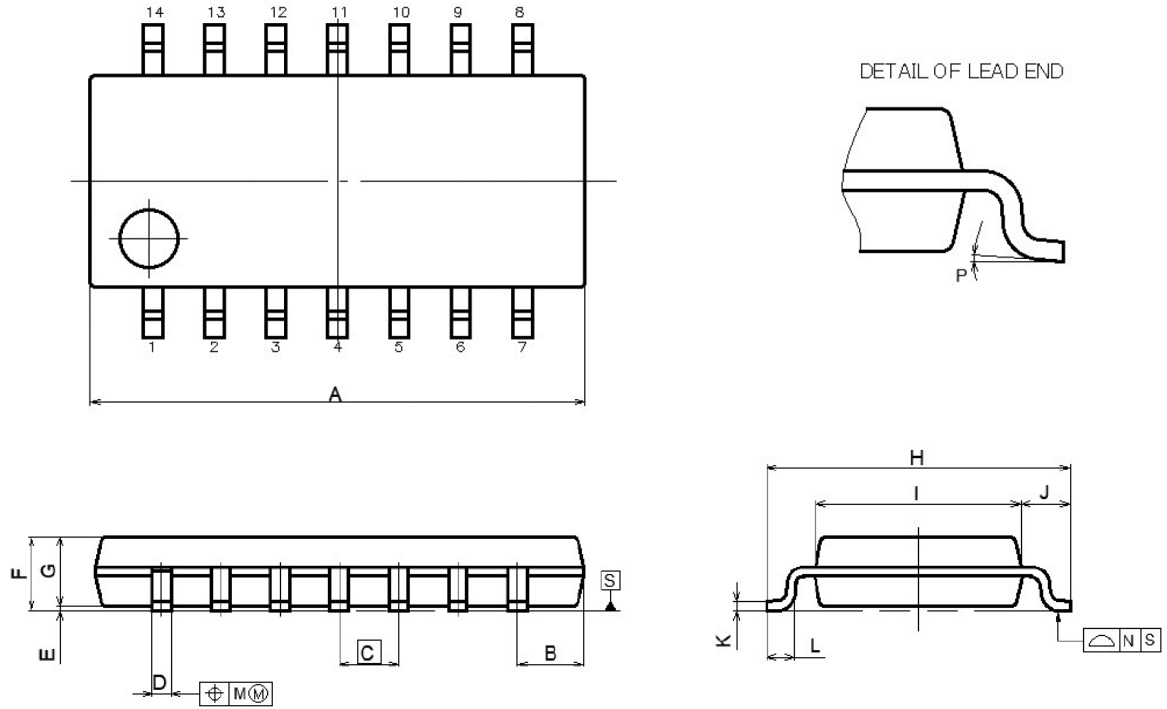
- **Handling of ICs**

When stress is added to the ICs due to warpage or bending of a board, the characteristic may fluctuate due to piezoelectric (piezo) effect. Therefore, pay attention to warpage or bending of a board.

**PACKAGE DRAWINGS**

14-PIN PLASTIC SOP

<b>JEITA Package code</b>	<b>RENESAS code</b>	<b>MASS (TYP.) [g]</b>
P-LSOP14-4.4×10.2-1.27	PLSP0014DB-A	0.17[g]



NOTE  
 EACH LEAD CENTERLINE IS LOCATED WITHIN 0.12 MM OF  
 ITS TRUE POSITION(T.P.) AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)

ITEM	DIMENSIONS
A	10.2±0.2
B	1.42MAX
C	1.27(T.P)
D	0.40±0.05
E	0.1±0.1
F	1.59±0.20
G	1.49±0.1
H	6.5±0.2
I	4.4±0.1
J	1.05±0.15
K	0.2±0.07
L	0.6±0.20
M	0.1MAX
N	0.1MAX
P	4°±4°

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