μPC4742MF-DAA

Single Power Supply, High Speed, Wide Band, Dual Operational Amplifier
Single Supply, SR = 7 V/μs, GBW = 3.5 MHz, V_{IO} = ±2 mV

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Description

The μPC4742MF-DAA is a high speed version of the operational amplifier, μPC358 for general single power supply use with high speed pulse response and high stabilization. A high speed PNP transistor is used in the circuit which improves the characteristics such as a slew rate, gain-bandwidth product, stabilization of the withstand load capacitance, with no crossover distortion compared to μPC358.

Therefore, μPC4742MF-DAA can be used in a wide range of application circuits for single power supply AC amplifier, active filters, line driver and an amplifier for light receiving element etc.

Features

- Slew Rate (A_V = +1): 7 V/μs (TYP.) (V^+ = +5 V, V^- = GND)
- Gain bandwidth Product (f = 100 kHz): 3.5 MHz (TYP.)
- Input offset voltage: ±2 mV (TYP.)
- Input offset current: ±6 nA (TYP.)
- A pin connection (pin compatible) of a standard dual operational
- Wide operating ambient temperature range : T_A = −40 to +85°C

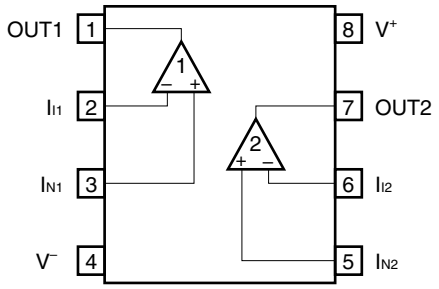
Ordering Information

Part Number	Package	Package Code (Previous Package Code)	Package Abbreviation	Supplying Form
μPC4742MF-DAA-E1-AT *1	8-pin plastic SOP (3.9 × 4.9)	PRSP0008DM-A (–)	MF	• 12 mm wide embossed taping • Pin 1 on draw-out side • 2500 p/reel

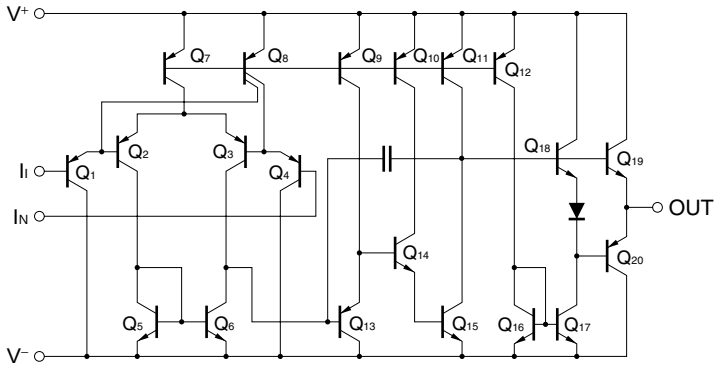
Note: *1. Pb-free (This product does not contain Pb in the external electrode and other parts.)

Caution: Do not use the products in applications such as the transportation equipment (a car, a train, a ship, etc.) where “Special quality grade” is required, because the products are placed in a quality grade “standard” to be required at general devices.

Pin Configuration (Top View)



Equivalent Circuit (for Each Circuit)



Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Ratings	Unit
Voltage between V^+ and V^- *1	$V^+ - V^-$	−0.3 to +36	V
Differential Input Voltage	V_{ID}	±36	V
Input Voltage *2	V_I	V^- − 0.3 to V^- + 36	V
Output Applied Voltage *3	V_O	V^- − 0.3 to V^+ + 0.3	V
Total Power Dissipation *4	P_T	440	mW
Output Short Circuit Duration (vs. GND) *5	t_S	Indefinite	s
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Notes: *1. Note that reverse connections of the power supply may damage ICs.

*2. The input voltage is allowed to input without damage or destruction independent of the magnitude of V^++. Either input signal is not allowed to go negative by more than 0.3 V. In addition, the input voltage that operates normally as an operational amplifier is within the Common Mode Input Voltage range of an electrical characteristic.

*3. A range where input voltage can be applied to an output pin externally with no deterioration or damage to the feature (characteristic). The input voltage can be applied regardless of the electric supply voltage. This specification which includes the transition state such as electric power ON/OFF must be kept.

*4. This is the value in $T_A \leq 56$°C of when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted. Derate at −6.4 mW/°C when $T_A > 56$°C. In the condition same as the above, Junction − ambient thermal resistance $R_{th(J-A)}$ = 156°C/W.

*5. Only as for $V^+ \leq 15$ V and any 1 channel. Please use the product within the derating condition or Total Power Dissipation, which are showed in Note 4.

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (Split)	$V^{\pm}$	±1.5		±16	V
Supply Voltage (V^- = GND)	V^+	+3	+5 to +30	+32	V
Output Current	I_O			±10	mA
Capacitive Load (A_V = +1)	C_L			1000 *1	pF

Note: *1. This is the value during a feedback resistance (R_f) = 0 Ω.

Electrical Characteristics (T_A = 25°C, $V^{\pm}$ = ±15 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Conditions
Input Offset Voltage	V_{IO}		±2	±4.5	mV	
Input Offset Current	I_{IO}		±6	±75	nA	
Input Bias Current *1	I_B		120	500	nA	
Large Signal Voltage Gain	A_V	25000	300000			R_L ≥ 2 kΩ, V_O = ±10 V
Supply Current *2	I_{CC}		4.3	5.5	mA	I_O = 0 A
Common Mode Rejection Ratio	CMR	70	86		dB	
Supply Voltage Rejection Ratio	SVR	70	93		dB	
Output Voltage Swing	V_{om}	±13.7	±14		V	R_L ≥ 10 kΩ
			−14.3			
		±13.5			V	R_L ≥ 2 kΩ
Common Model Input Voltage Range	V_{ICM}	V^-		V^+ − 1.8	V	
Slew Rate	SR		8.5		V/μs	A_V = +1 (rise)
Gain Band Width Product	GBW		3.5		MHz	f_O = 100 kHz
Channel Separation			120		dB	f = 20 Hz to 20 kHz

Notes: *1. The input bias current flows in the direction where the IC flows out because the first stage is configured with a PNP transistor.

*2. This is a current that flows in the internal circuit. This current will flow irrespective of the channel used.

Electrical Characteristics (T_A = 25°C, V^+ = +5 V, V^- = GND)

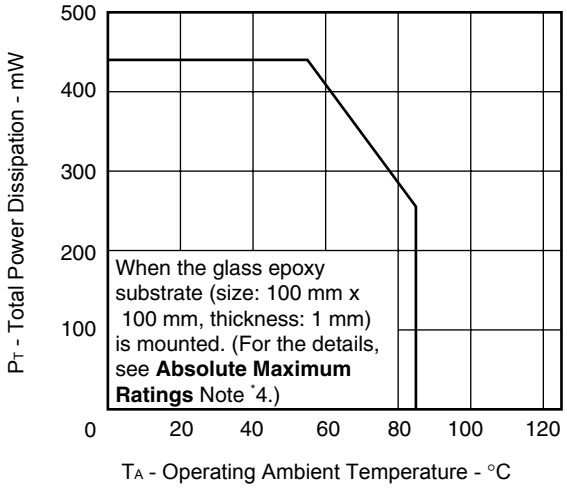
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Conditions
Input Offset Voltage	V_{IO}		±2	±5	mV	
Input Offset Current	I_{IO}		±6	±75	nA	
Input Bias Current *1	I_B		140	500	nA	
Large Signal Voltage Gain	A_V	25000	300000			R_L ≥ 2 kΩ
Supply Current *2	I_{CC}		3.3	4.5	mA	I_O = 0 A
Common Mode Rejection Ratio	CMR	70	80		dB	
Supply Voltage Rejection Ratio	SVR	70	95		dB	
Output Voltage Swing	V_{om}	3.7	4		V	R_L ≥ 2 kΩ (Connect to GND)
		0	0			
Common Model Input Voltage Range	V_{ICM}	0		V^+ − 1.8	V	
Output Source Current	$I_{O\ SOURCE}$	10	30		mA	$V_{IN\ (+)}$ = +1 V, $V_{IN\ (-)}$ = 0 V
Output Sink Current	$I_{O\ SINK}$	10	30		mA	$V_{IN\ (+)}$ = 0 V, $V_{IN\ (-)}$ = +1 V
Slew Rate	SR		7		V/μs	A_V = +1 (rise)

Notes: *1. The input bias current flows in the direction where the IC flows out because the first stage is configured with a PNP transistor.

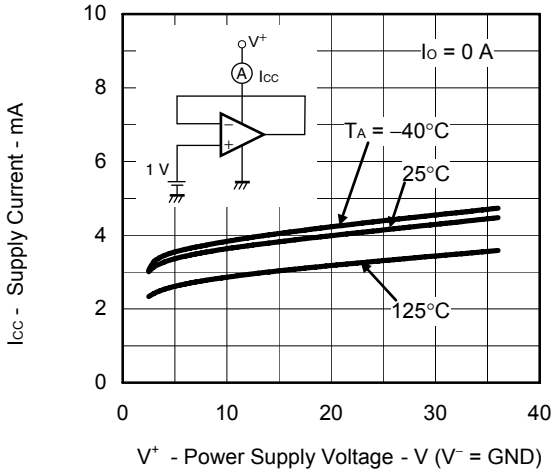
*2. This is a current that flows in the internal circuit. This current will flow irrespective of the channel used.

Typical Characteristics (T_A = 25°C, TYP.) (Reference value)

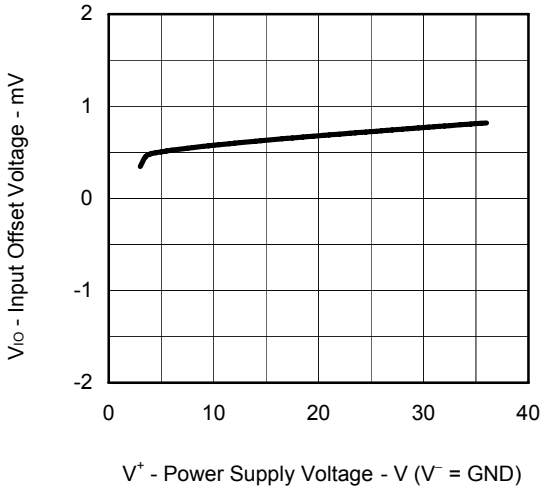
P_T vs. T_A



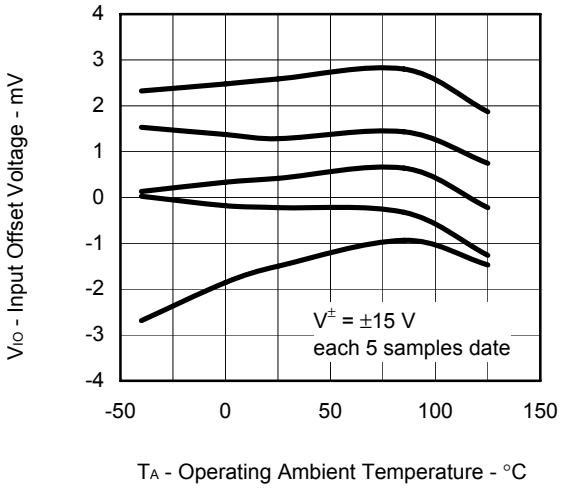
I_{CC} vs. V^+



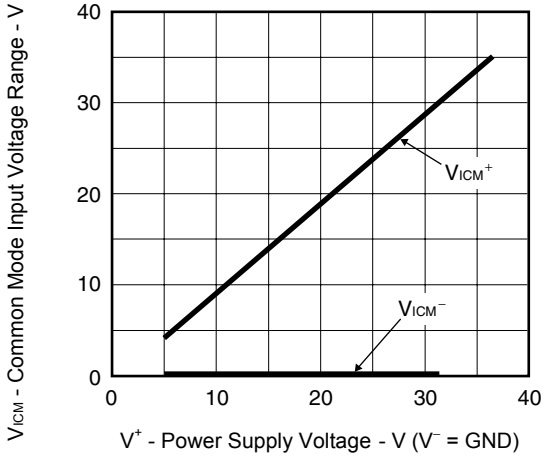
V_{IO} vs. V^+



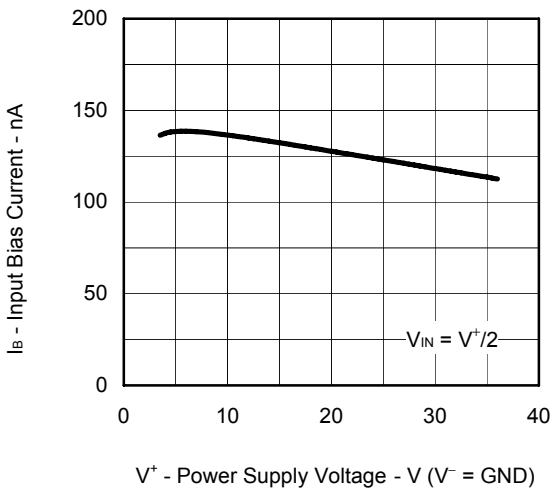
V_{IO} vs. T_A



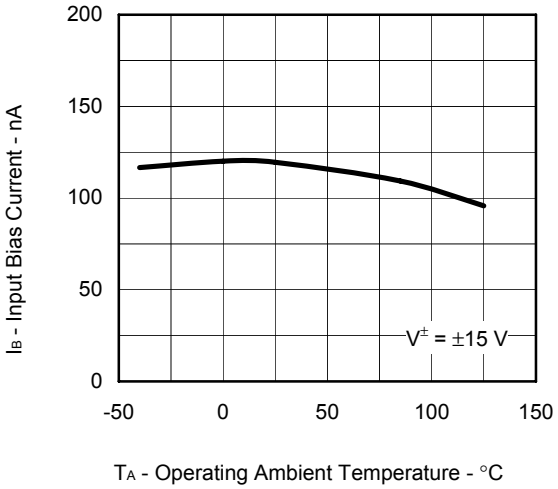
V_{ICM} vs. V^+



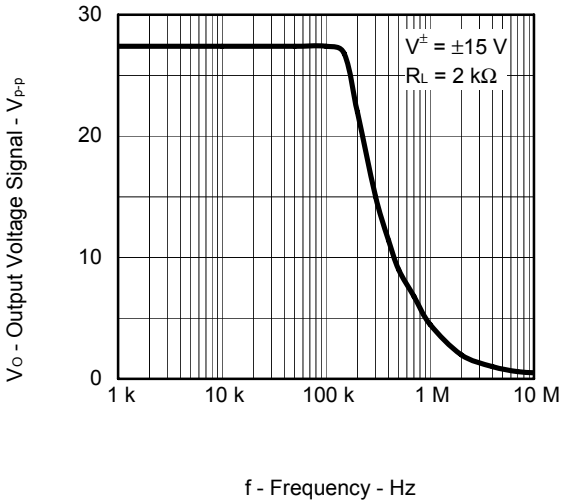
I_B vs. V^+



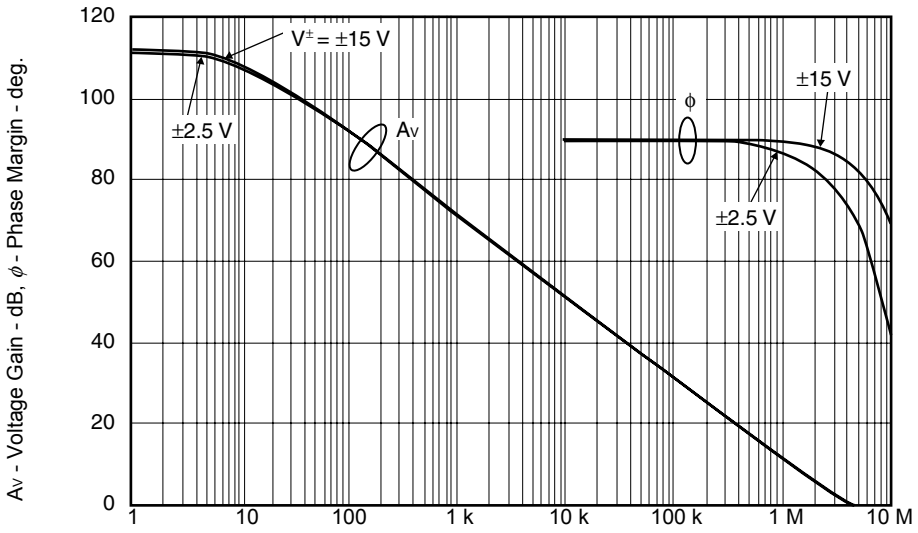
I_B vs. T_A



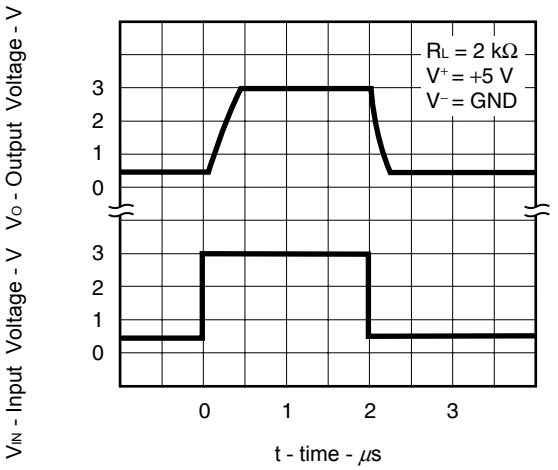
V_O vs. f



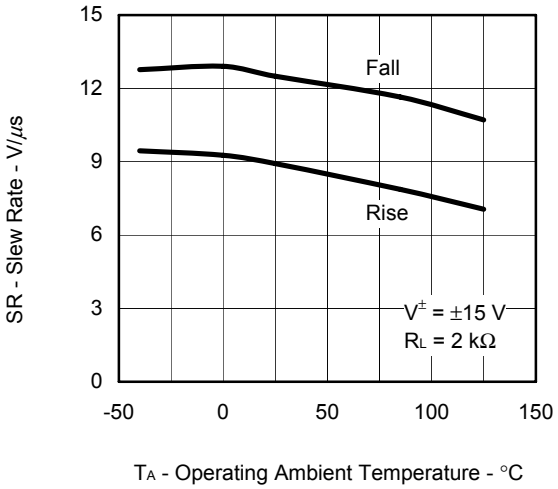
A_V, ϕ vs. f



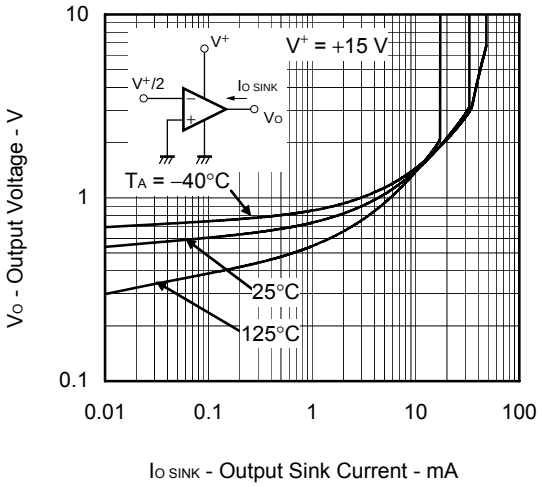
PULSE RESPONSE



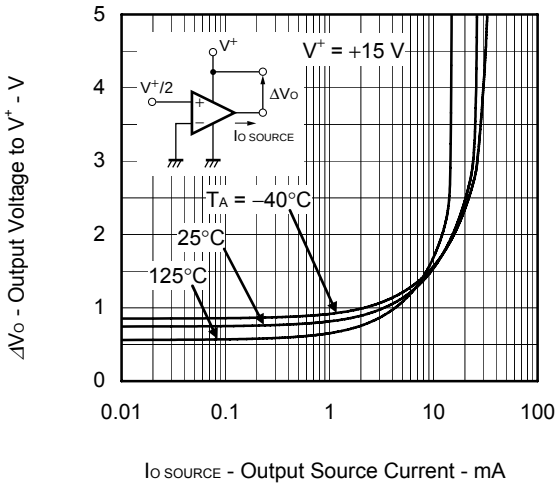
SR vs. T_A



V_O vs. $I_{O\ SINK}$



ΔV_O vs. $I_{O\ SOURCE}$

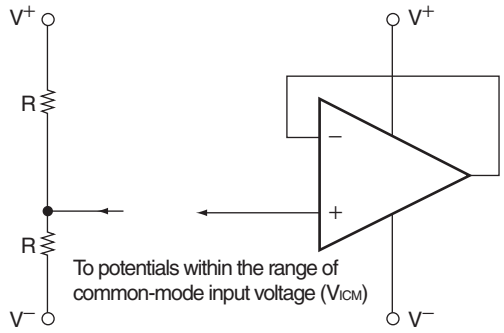


PRECAUTIONS FOR USE

- **The process of unused circuits**

If there is an unused circuit, the following connection is recommended.

Process example of unused circuits



Remark: A midpoint potential of V^+ and V^- is applied to this example.

- **Power supply used (Split/Single)**

  The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

- **Ratings of input/output pin voltage**

  When the voltage of input/output pin exceeds the absolute maximum rating, it may cause degradation of characteristics or damages, by a conduction of a parasitic diode within an IC. In addition, when the input pin may be lower than V^-, or the output pin may exceed the power supply voltage, it is recommended to make a clump circuit by a diode whose forward voltage is low (e.g.: Schottky diode) for protection.

- **Range of common-mode input voltage**

  When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.
  V_{ICM} (TYP.): V^- to $V^+ - 1.8$ (V) ($T_A = 25°C$)
  During designing, temperature characteristics for use with allowance.

- **The maximum output voltage**

  The range of the TYP. value of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:
  $V_{om}{}^+$ (TYP.): $V^+ - 1$ (V) ($T_A = 25°C$), $V_{om}{}^-$ (TYP.): $V^- + 0.7$ (V) ($T_A = 25°C$)
  During designing, consider variations in characteristics and temperature characteristics for use with allowance.
  In addition, also note that the output voltage range ($V_{om}{}^+ - V_{om}{}^-$) becomes narrow when an output current increases.

- **Operation of output**

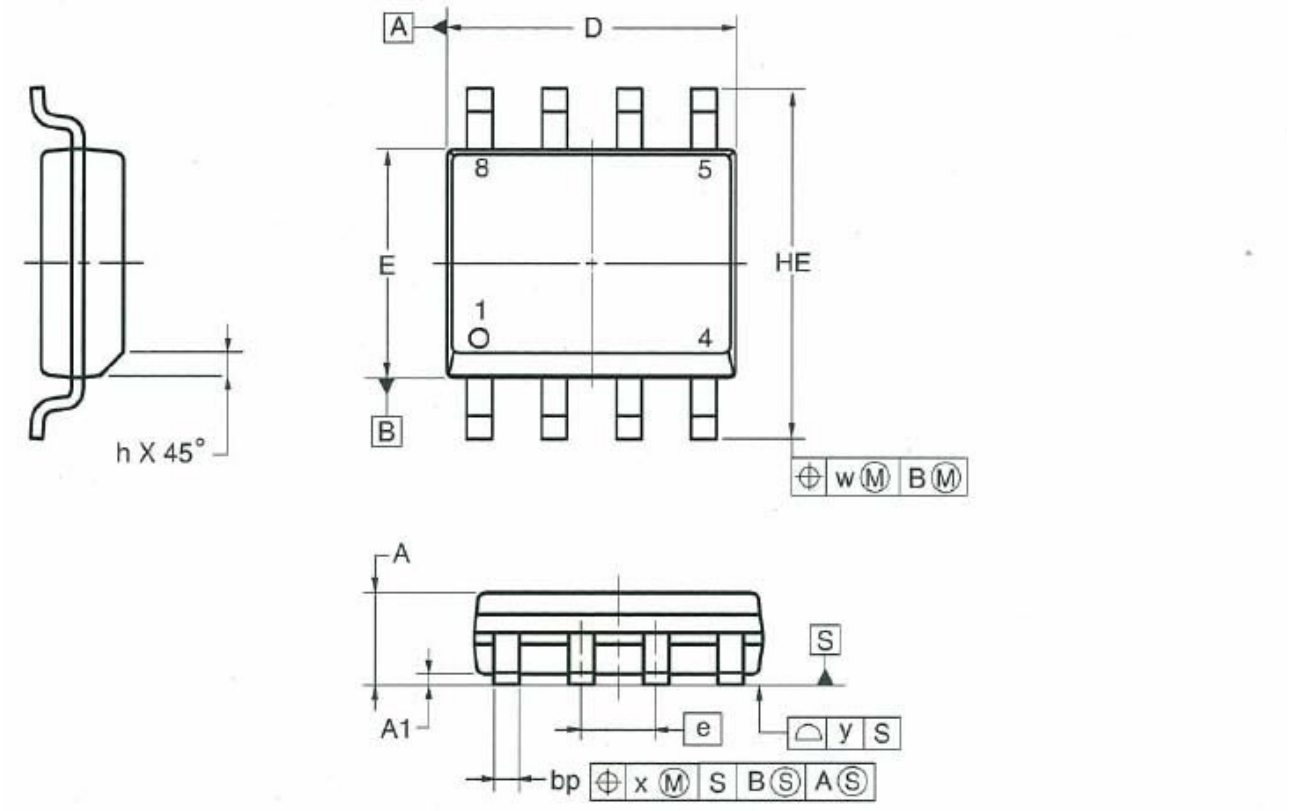
  This IC will not operate an output current sinking when the output voltage is $V^- + 0.7$ V and below. In this situation, an output voltage and its level approach to the V^- side can be improved by connecting the load resistance to an output pin / V^- intermediate by sinking current at the load resistance side. (The effect will differ depending on the flow of current in the load resistance.)

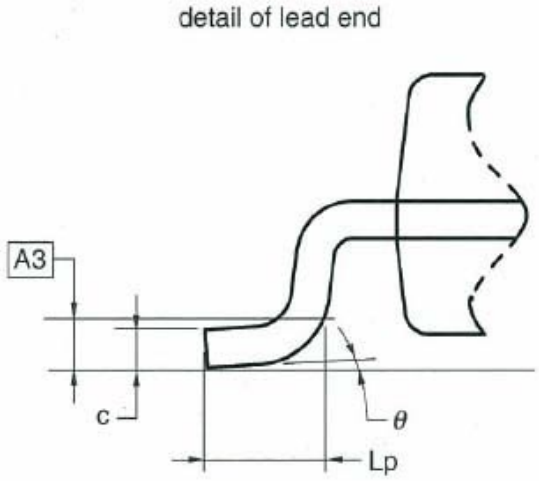
- **Handling of ICs**

  When stress is added to ICs due to warpage or bending of a board, the characteristic fluctuates due to piezoelectric effect. Therefore, pay attention to warpage or bending of a board.

Package Drawings

8-pin Plastic SOP (3.9 × 4.9)





(UNIT:mm)

ITEM	DIMENSIONS
D	4.80 to 5.00
E	3.80 to 4.00
HE	5.80 to 6.20
e	1.27
bp	0.35 to 0.49
A	1.35 to 1.75
A1	0.10 to 0.25
A3	0.25
c	0.19 to 0.25
Lp	0.40 to 1.25
h	0.25 to 0.50
w	0.25
x	0.25
y	0.10
θ	0° to 7°

Revision History	μPC4742MF-DAA Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Jul 25, 2012	–	First Edition Issued

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

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1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

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Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
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Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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