

# UPC4574GR-9LG

## Ultra Low-Noise, High Speed, Wide Band, Quad Operational Amplifier

### DESCRIPTION

UPC4574GR-9LG is a high performance version of general-purpose low-noise operational amplifier UPC458, 4741. Various characteristics such as band, slew rate, including input equivalent noise were greatly improve in comparison to UPC458 and 4741. It is also possible to operate the amplifier with stability for gain of 1 (total feedback or unity gain)

Therefore, it is ideal for application circuits such as audio preamplifiers, equalizers, tone controls, active filters.

In addition, special arrangement products with sorted DC items are available.

Under this product series, there is also a dual type UPC4570GR-9LG with equivalent characteristics

### FEATURES

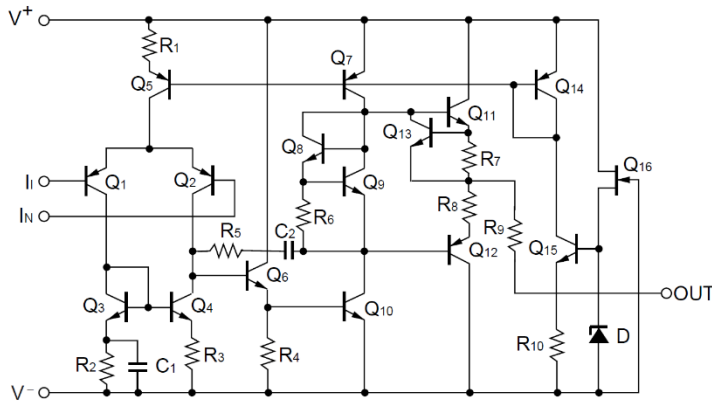
- Equivalent Input Noise Voltage (f = 1 kHz)                      5 nV/ $\sqrt{\text{Hz}}$  (TYP.)
- Total Harmonic Distortion Rate (f = 20 Hz ~ 20 kHz)      0.002 % (TYP.)
- Slew Rate    6 V/ $\mu\text{s}$  (TYP.)
- Gain Bandwidth Product GBW (f = 100 kHz)                      14 MHz (TYP.)
- Input Offset Voltage     $\pm 0.3$  mV (TYP.)
- Operating Ambient Temperature    -40 ~ +85 °C
- Internal Frequency Compensation
- The 14-pin TSSOP profile reduces the mounting area by approximately 50% compared to the standard SOP profile.

### ORDERING INFORMATION

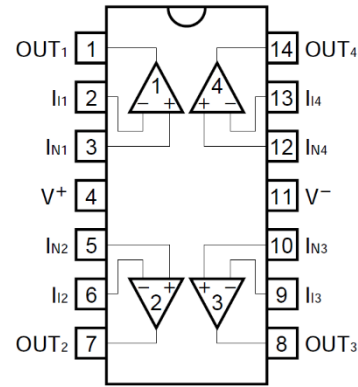
Order Name <sup>(1)</sup>	Selected Grade	Package
UPC4570GR-9LG-A	Standard	14-pin plastic TSSOP ( 5.72 mm ( 225 ) )
UPC4570GR(5)-9LG-A	DC parameter selection	14-pin plastic TSSOP ( 5.72 mm ( 225 ) )

(1) Order names containing E1 or E2 indicate that the packaging format is embossed taping.  
Pin 1 of E1 is on draw-out side, and pin 1 of E2 is at take-up side.

**EQUIVALENT CIRCUIT (1/4 Circuit)**



**PIN CONFIGURATION (Top View)**



**ABSOLUTE MAXIMUM RATINGS(T<sub>A</sub> = 25 °C)**

Parameter	Symbol	UPC4574GR-9LG UPC4574GR(5)-9LG	Unit
Power Supply Voltage <sup>Note 1</sup>	V <sup>+</sup> - V <sup>-</sup>	-0.3 ~ +36	V
Differential Input Voltage	V <sub>ID</sub>	±30	V
Input Voltage <sup>Note 2</sup>	V <sub>I</sub>	V <sup>-</sup> -0.3 ~ V <sup>+</sup> +0.3	V
Output Applied Voltage <sup>Note 3</sup>	V <sub>O</sub>	V <sup>-</sup> -0.3 ~ V <sup>+</sup> +0.3	V
Total Power Dissipation <sup>Note 4</sup>	P <sub>T</sub>	550	mW
Output Short Circuit Duration <sup>Note 5</sup>		10	s
Operating Ambient Temperature	T <sub>A</sub>	-40 ~ +85	°C
Storage Temperature	T <sub>stg</sub>	-55 ~ +125	°C

**[Note] 1.** Note that reverse connections of the power supply may damage the ICs.

**2.** The input terminal must be applied within the input voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp input voltage must operate within the electrical characteristics range of input common-mode voltage.

**3.** The output terminal must be applied within the output voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp output voltage must operate within the electrical characteristics range of maximum output voltage.

**4.** This is the value when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted.

Note that restrictions will be made to the following conditions for each product, and the de-rating ratio depending on the operating ambient temperature.

UPC4574GR-9LG : This is the value at T<sub>A</sub> ≤ 46 °C. Derate at -7.0 mW/°C when T<sub>A</sub> > 46 °C

**5.** A short circuit at the V<sup>+</sup> side may destroy the IC. Please use below the total loss and the de-rating of Note 4.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	V <sup>±</sup>	±4		±16	V
Output Current	I <sub>o</sub>			+10	mA
Source Resistance	R <sub>s</sub>			50	kΩ
Capacitive Load (A <sub>v</sub> = +1)	C <sub>L</sub>			100	pF

**ELECTRICAL CHARACTERISTICS**UPC4574GR-9LG ( $T_A = 25\text{ }^\circ\text{C}$ ,  $V^\pm = \pm 15\text{ V}$ )

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	$V_{IO}$		$\pm 0.3$	$\pm 5$	mV	$R_S \leq 50\ \Omega$
Input Offset Current	$I_{IO}$		$\pm 10$	$\pm 200$	nA	
Input Bias Current <sup>Note 6</sup>	$I_B$		500	1000	nA	
Large Signal Voltage Gain	$A_V$	30000	300000			$R_L \geq 2\ \text{k}\Omega$ , $V_O = \pm 10\ \text{V}$
Circuit Current <sup>Note 7</sup>	$I_{CC}$		8.5	12	mA	$I_O = 0\ \text{A}$
Common Mode Rejection Ratio	CMR	80	100		dB	
Supply Voltage Rejection Ratio	SVR	80	100		dB	
Output Voltage Swing	$V_{om}$	$\pm 12$	$\pm 13.4$		V	$R_L \geq 10\ \text{k}\Omega$
Output Voltage Swing	$V_{om}$	$\pm 10$	+12.8 -12.4		V	$R_L \geq 2\ \text{k}\Omega$
Common Mode Input Voltage Range	$V_{ICM}$	$\pm 12$	$\pm 14$		V	
Slew Rate	SR	4	6		V/ $\mu\text{s}$	$R_L \geq 2\ \text{k}\Omega$
Gain Bandwidth Product	GBW	10	14		MHz	$f_O = 100\ \text{kHz}$
Unity Gain Frequency	$f_{unity}$		7		MHz	open loop
Phase Margin	$\phi_{unity}$		50		Deg	open loop
Total Harmonic Distortion	THD		0.002		%	$V_O = 3\ V_{r.m.s.}$ , $f = 20\ \text{Hz} \sim 20\ \text{kHz}$ (Figure 1)
Equivalent Noise Input Voltage	$V_n$		1.2		$\mu\text{V}_{r.m.s.}$	RIAA (Figure 2)
Equivalent Noise Input Voltage	$V_n$		0.53	0.65	$\mu\text{V}_{r.m.s.}$	FLAT + JIS A, $R_S = 100\ \Omega$ (Figure 3)
Equivalent Noise Input Voltage Density	$e_n$		5.5		$\text{nV}/\sqrt{\text{Hz}}$	$f_O = 10\ \text{Hz}$ , $R_S = 100\ \Omega$
Equivalent Noise Input Voltage Density	$e_n$		5.0		$\text{nV}/\sqrt{\text{Hz}}$	$f_O = 1\ \text{kHz}$ , $R_S = 100\ \Omega$
Equivalent Noise Input Current Density	$i_n$		0.7		$\text{pA}/\sqrt{\text{Hz}}$	$f_O = 1\ \text{kHz}$
Channel Separation			120		dB	$f = 20\ \text{Hz} \sim 20\ \text{kHz}$

**[Note]** 6. The current flow direction of the input bias is out from the IC because the first stage of the IC composed of PNP transistor.

7. Current flowing through the internal circuit. This current flow regardless of the channel used.

**ELECTRICAL CHARACTERISTICS**UPC4574GR(5)-9LG ( $T_A = 25\text{ }^\circ\text{C}$ ,  $V^\pm = \pm 15\text{ V}$ )

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	$V_{IO}$		$\pm 0.3$	$\pm 1$	mV	$R_S \leq 50\ \Omega$
Input Offset Current	$I_{IO}$		$\pm 10$	$\pm 60$	nA	
Input Bias Current <sup>Note 6</sup>	$I_B$		500	650	nA	
Large Signal Voltage Gain	$A_V$	50000	300000			$R_L \geq 2\ \text{k}\Omega$ , $V_O = \pm 10\ \text{V}$
Circuit Current <sup>Note 7</sup>	$I_{CC}$		8.5	11	mA	$I_O = 0\ \text{A}$
Common Mode Rejection Ratio	CMR	85	100		dB	
Supply Voltage Rejection Ratio	SVR	85	100		dB	
Output Voltage Swing	$V_{om}$	$\pm 13$	$\pm 13.4$		V	$R_L \geq 10\ \text{k}\Omega$
Output Voltage Swing	$V_{om}$	$\pm 11.5$	+12.8 -12.4		V	$R_L \geq 2\ \text{k}\Omega$
Common Mode Input Voltage Range	$V_{ICM}$	$\pm 13$	$\pm 14$		V	
Slew Rate	SR	4	6		V/ $\mu\text{s}$	$R_L \geq 2\ \text{k}\Omega$
Gain Bandwidth Product	GBW	10	14		MHz	$f_O = 100\ \text{kHz}$
Unity Gain Frequency	$f_{unity}$		7		MHz	open loop
Phase Margin	$\phi_{unity}$		50		Deg	open loop
Total Harmonic Distortion	THD		0.002		%	$V_O = 3\ V_{r.m.s.}$ , $f = 20\ \text{Hz} \sim 20\ \text{kHz}$ (Figure 1)
Equivalent Noise Input Voltage	$V_n$		1.2		$\mu\text{V}_{r.m.s.}$	RIAA (Figure 2)
Equivalent Noise Input Voltage	$V_n$		0.53	0.65	$\mu\text{V}_{r.m.s.}$	FLAT + JIS A, $R_S = 100\ \Omega$ (Figure 3)
Equivalent Noise Input Voltage Density	$e_n$		5.5		$\text{nV}/\sqrt{\text{Hz}}$	$f_O = 10\ \text{Hz}$ , $R_S = 100\ \Omega$
Equivalent Noise Input Voltage Density	$e_n$		5.0		$\text{nV}/\sqrt{\text{Hz}}$	$f_O = 1\ \text{kHz}$ , $R_S = 100\ \Omega$
Equivalent Noise Input Current Density	$i_n$		0.7		$\text{pA}/\sqrt{\text{Hz}}$	$f_O = 1\ \text{kHz}$
Channel Separation			120		dB	$f = 20\ \text{Hz} \sim 20\ \text{kHz}$

**[Note]** 6. The current flow direction of the input bias is out from the IC because the first stage of the IC composed of PNP transistor.

7. Current flowing through the internal circuit. This current flow regardless of the channel used.

## MEASUREMENT CIRCUIT

Figure 1: Total Harmonic Distortion Measurement Circuit

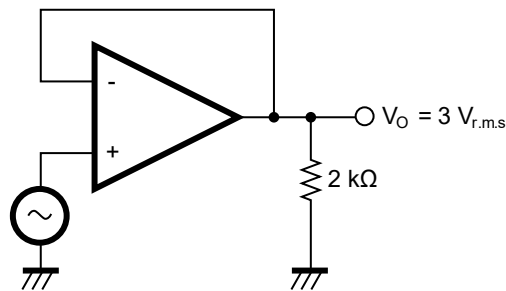


Figure 2: Noise Measurement Circuit (RIAA)

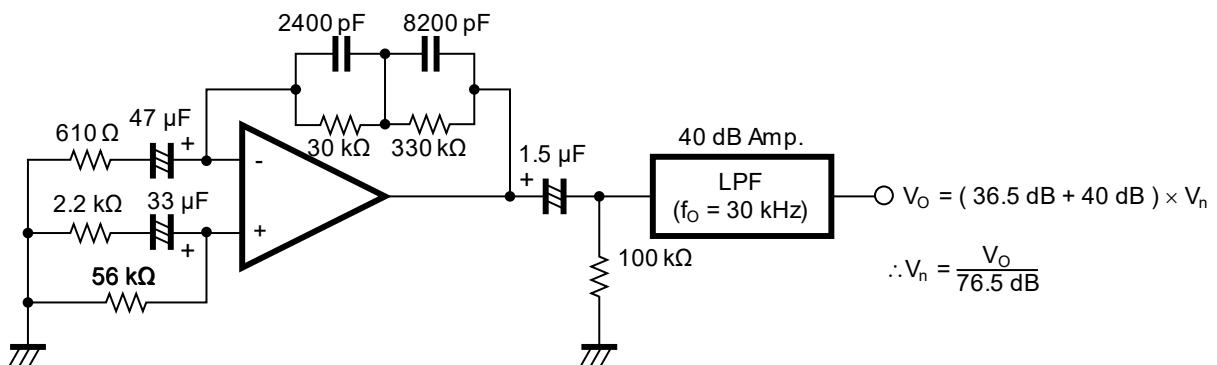
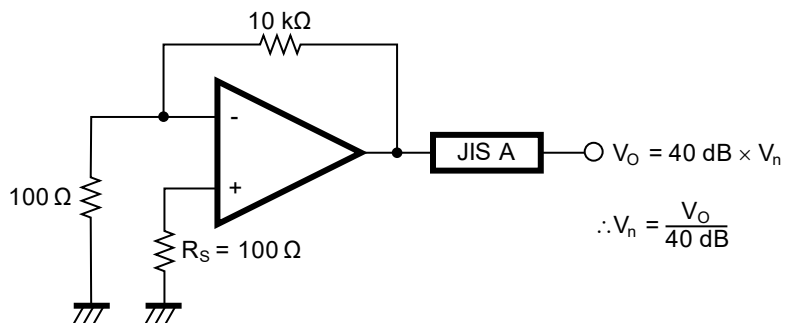
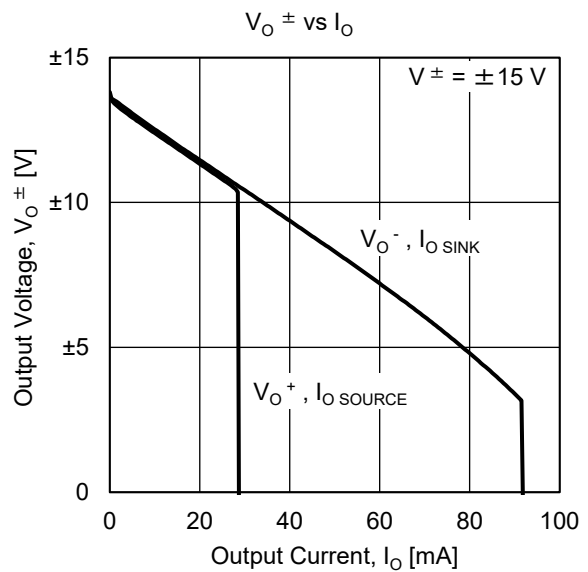
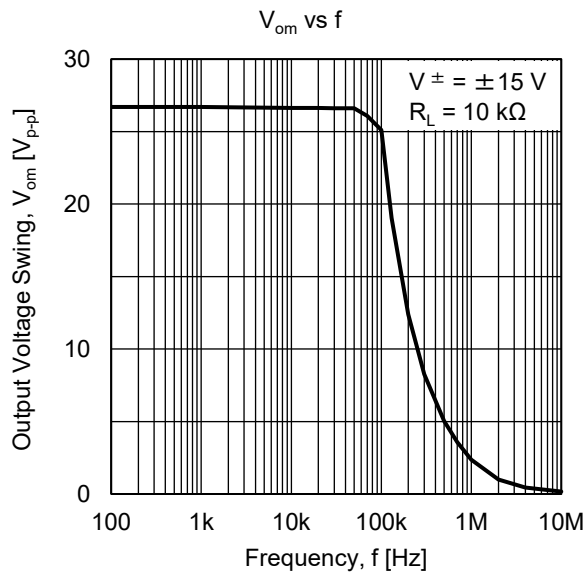
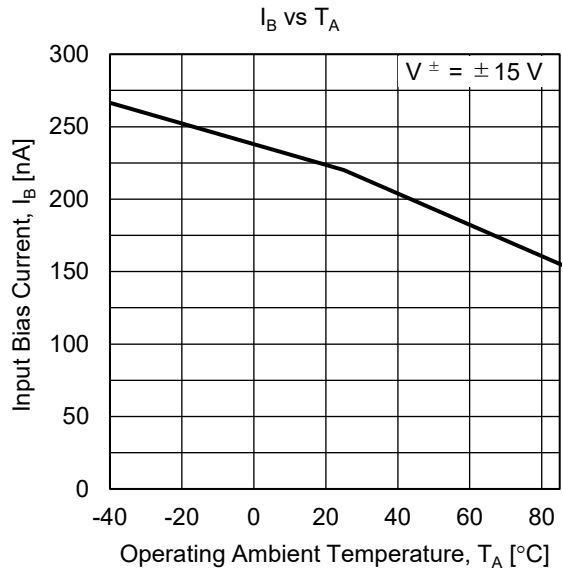
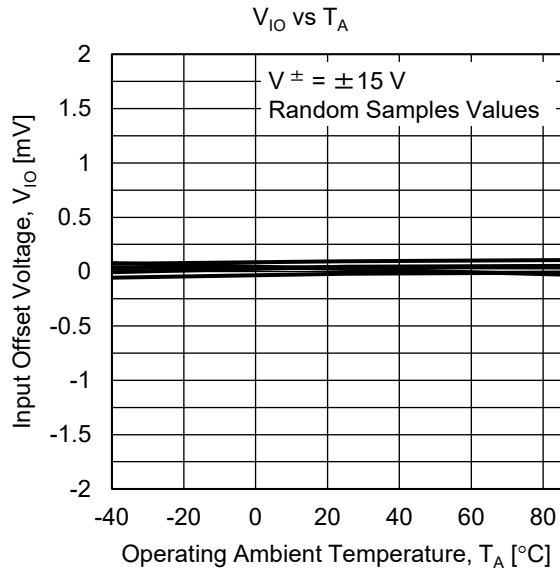
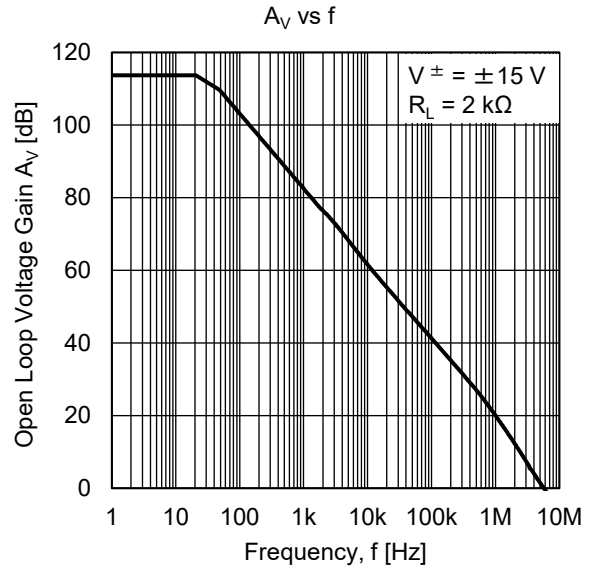
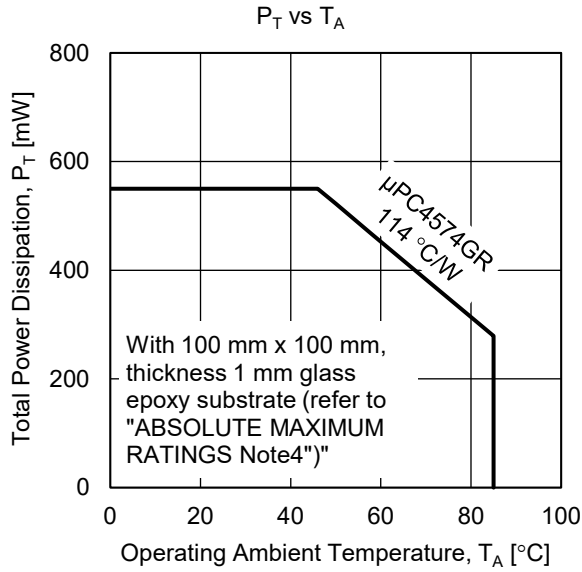
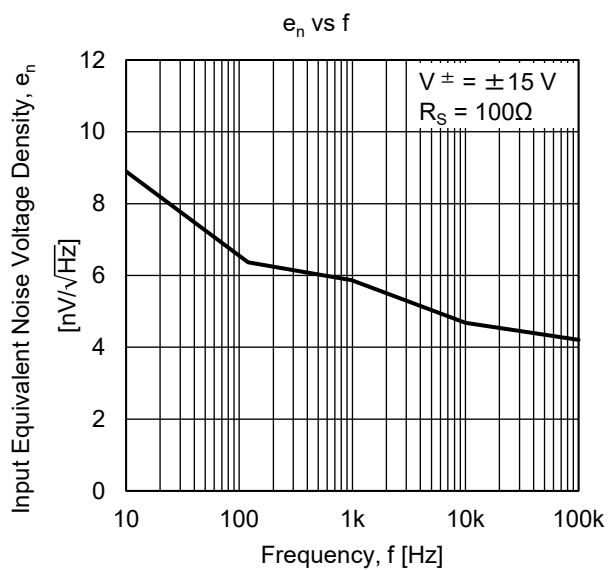
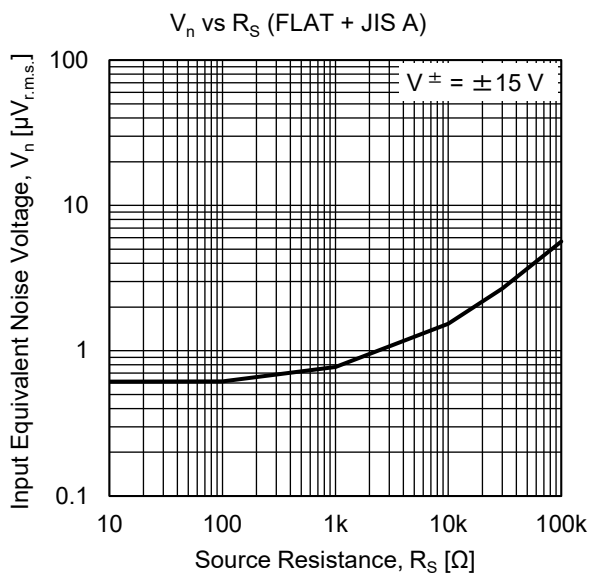
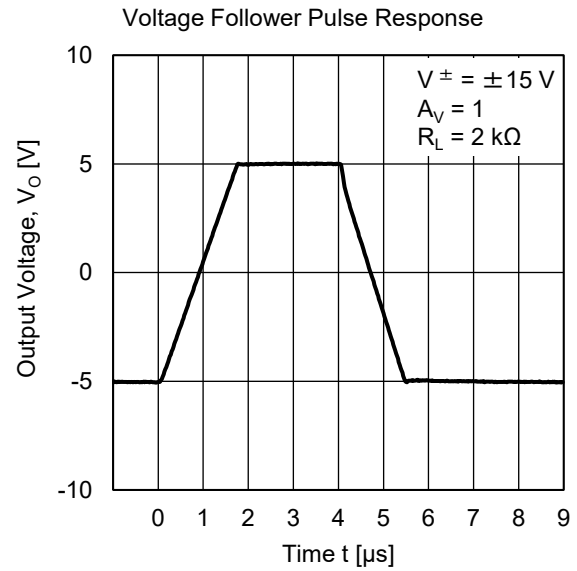
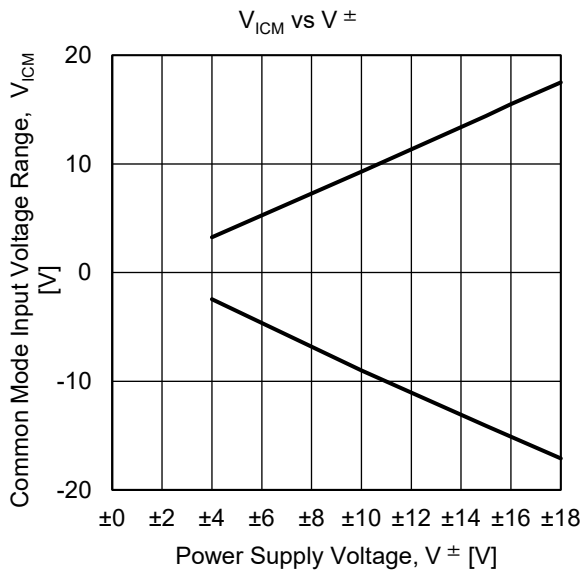
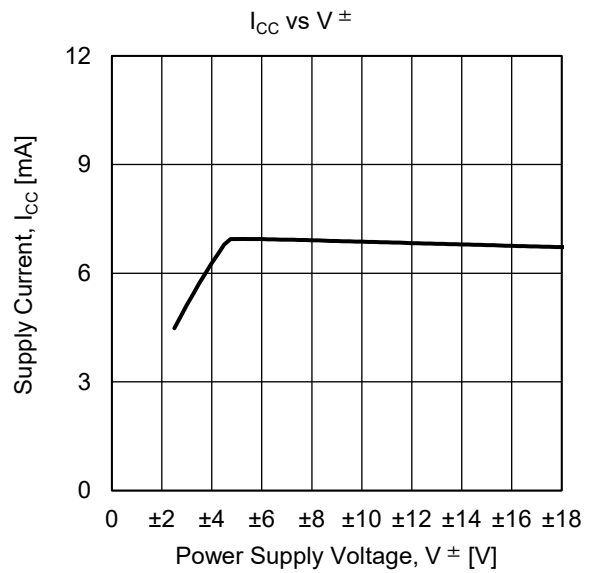
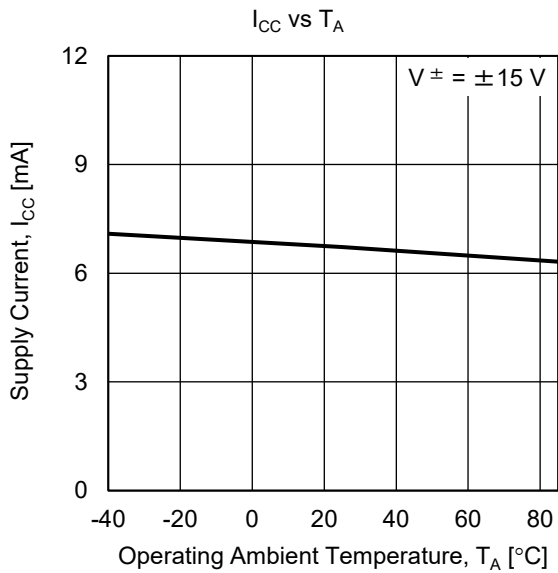


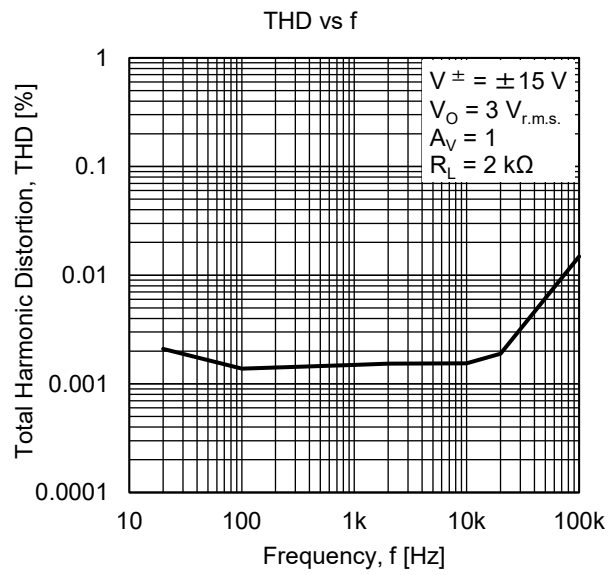
Figure 3: Noise Measurement Circuit (FLAT+JIS A)



**CHARACTERISTICS CURVE (T<sub>A</sub> = 25 °C, TYP.) (REFERENCE VALUE)**





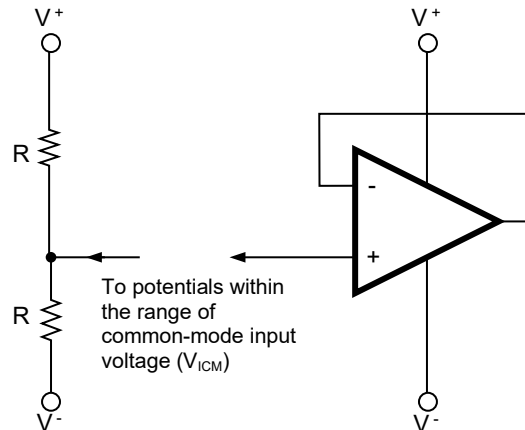


## USE WITH PRECAUTIONS

- **Managing unused circuits**

If there is an unused circuit, the following connection is recommended.

Example of unused circuit process



Remark: In this example, an intermediate potential between  $V^+$  and  $V^-$  is applied.

- **Power Supply (Dual Power Supply / Single Power Supply)**

The op-amp operates as long as a predetermined voltage is applied between  $V^+$  and  $V^-$ . Therefore, it can operate with a single power supply ( $V^- = \text{GND}$ ), but it cannot operate the input and output near GND. Common-mode input voltage please pay attention to the range and maximum output voltage.

- **Ratings of input/output pin voltage**

When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than  $V^-$ , or the output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- **Range of common-mode input voltage**

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

$$V_{ICM} (\text{TYP.}): V^- + 1 \sim V^+ - 1 \text{ [V]} (T_A = 25^\circ\text{C}).$$

During designing, do include some tolerance by considering temperature characteristics etc.

- **Maximum output voltage**

The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

$$V_{om^+} (\text{TYP.}): V^- - 1.6 \text{ [V]} (T_A = 25^\circ\text{C}), \quad V_{om^-} (\text{TYP.}): V^- + 1.6 \text{ [V]} (T_A = 25^\circ\text{C})$$

During designing, do include some tolerance by considering characteristics variation, temperature characteristics and so on. In addition, also note that the output voltage range ( $V_{om^+} - V_{om^-}$ ) will become narrow when the output current increases.

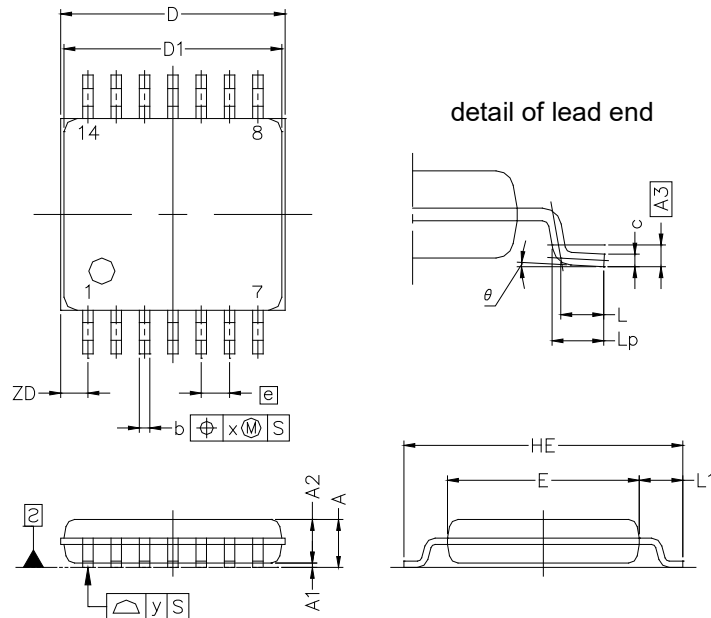
- **Handling of ICs**

When stress is added to ICs due to warpage or bending of a board, the characteristic may fluctuates due to piezoelectric (piezo) effect. Therefore, pay attention to warpage or bending of a board.

## PACKAGE DRAWINGS

## 14-PIN PLASTIC TSSOP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.) [g]
P-TSSOP14-0225-0.65	PTSP0014JB-A	P14GR-65-9LG-1	—



Unit : mm

**NOTE**

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

ITEM	MILLIMETERS
D	5.15 ±0.15
D1	5.00 ±0.10
E	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 <sup>+0.06</sup> <sub>-0.05</sub>
c	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	3° <sup>+5°</sup> <sub>-3°</sub>
e	0.65
x	0.10
y	0.10
ZD	0.625

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TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

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