

# UPC4572

Low Supply Voltage, Ultra Low-Noise, High Speed,  
Wide Band, Low  $I_B$  Dual Operational Amplifier

## DESCRIPTION

UPC4572 is a dual wide band, ultra low noise operational amplifier designed for low supply voltage operation of +4 V to +14 V single supply and  $\pm 2$  V to  $\pm 7$  V dual supplies. Using high  $h_{FE}$  PNP transistors for the input circuit, Input bias current and input equivalent noise are better than conventional wide band operational amplifier.

UPC4572 is an excellent choice for preamplifiers and active filters in audio, instrumentation, and communication circuit.

In addition, special arrangement products with sorted DC items are available.

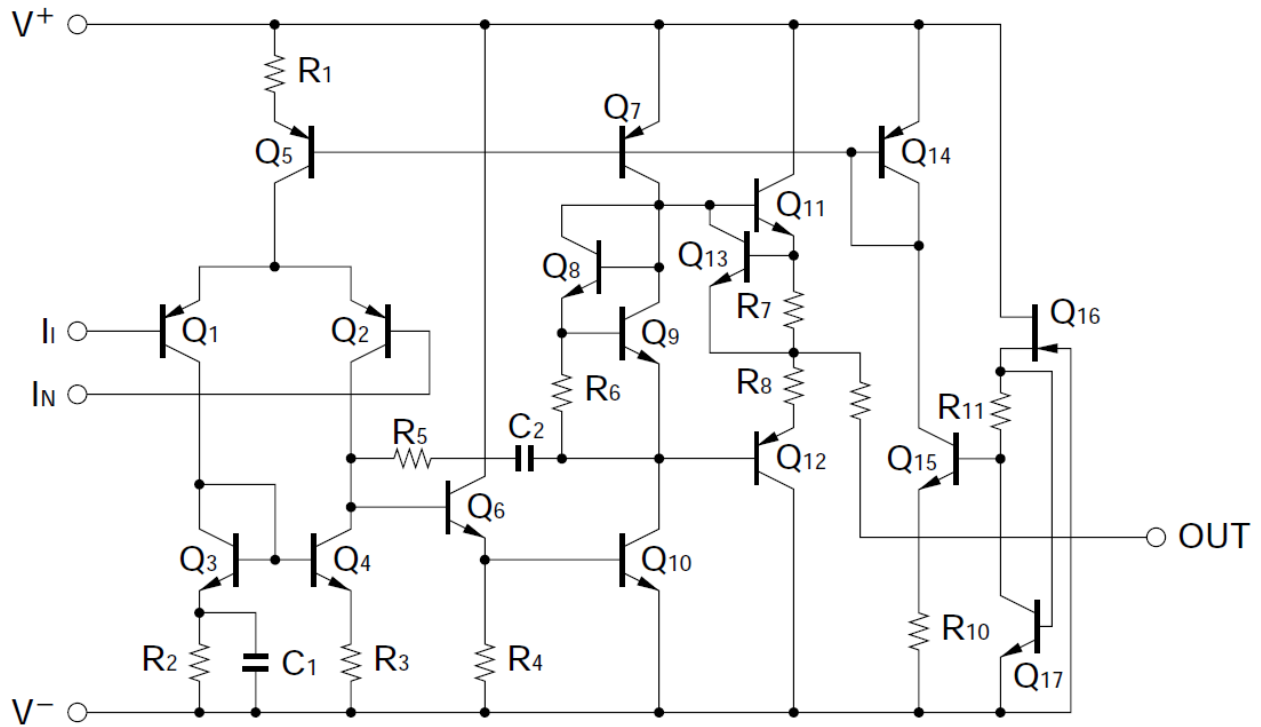
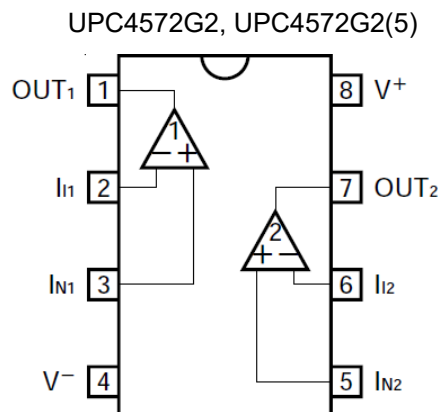
## FEATURES

- Input Equivalent Noise Voltage Density ( $f = 1$  kHz)     $4 \text{ nV}/\sqrt{\text{Hz}}$  (TYP.)
- Input Equivalent Noise Voltage (RIAA features)     $0.8 \text{ } \mu\text{V}_{\text{r.m.s.}}$  (TYP.)
- Total Harmonic Distortion    0.002 % (TYP.)
- Slew Rate     $6 \text{ V}/\mu\text{s}$  (TYP.)
- Gain Bandwidth Product GBW ( $f = 100$  kHz)    16 MHz (TYP.)
- Low Input Bias Current    100 nA (TYP.)
- Input Offset Voltage     $\pm 0.3 \text{ mV}$  (TYP.)
- Low Supply Voltage     $\pm 2 \text{ V} \sim \pm 7 \text{ V}$  (Dual)  
                                          $+4 \text{ V} \sim +14 \text{ V}$  (Single,  $V^- = \text{GND}$ )
- Internal Frequency Compensation
- Standard Dual Op-Amp terminal connection (pin compatible)

## ORDERING INFORMATION

| Order Name <sup>(1)</sup> | Selected Grade         | Package                               |
|---------------------------|------------------------|---------------------------------------|
| UPC4572G2-AP              | Standard               | 8-pin plastic SOP ( 5.72 mm ( 225 ) ) |
| UPC4572G2(5)-AP           | DC item sorted product | 8-pin plastic SOP ( 5.72 mm ( 225 ) ) |

- (1) Order names containing E1 or E2 indicate that the packaging format is embossed taping.  
Pin 1 of E1 is on draw-out side, and pin 1 of E2 is at take-up side.

**EQUIVALENT CIRCUIT (1/2 Circuit)****PIN CONFIGURATION (Marking Side)**

**ABSOLUTE MAXIMUM RATINGS( $T_A = 25\text{ }^{\circ}\text{C}$ )**

| Parameter                                       | Symbol      | UPC4572G2, UPC4572G2(5)    | Unit               |
|-------------------------------------------------|-------------|----------------------------|--------------------|
| Power Supply Voltage <sup>Note 1</sup>          | $V^+ - V^-$ | -0.3 ~ +15                 | V                  |
| Differential Input Voltage                      | $V_{ID}$    | $\pm 10$                   | V                  |
| Input Voltage <sup>Note 2</sup>                 | $V_I$       | $V^- - 0.3 \sim V^+ + 0.3$ | V                  |
| Output Applied Voltage <sup>Note 3</sup>        | $V_O$       | $V^- - 0.3 \sim V^+ + 0.3$ | V                  |
| Total Power Dissipation <sup>Note 4</sup>       | $P_T$       | 440                        | mW                 |
| Output Short Circuit Duration <sup>Note 5</sup> | $t_s$       | 10                         | s                  |
| Operating Ambient Temperature                   | $T_A$       | -20 ~ +80                  | $^{\circ}\text{C}$ |
| Storage Temperature                             | $T_{stg}$   | -55 ~ +125                 | $^{\circ}\text{C}$ |

**【Note】** 1. Reverse connection of supply voltage can cause destruction.

2. The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

3. This specification is the voltage, which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics

4. Thermal derating factor is -4.4 mW/ $^{\circ}\text{C}$  when ambient temperature is higher than 25  $^{\circ}\text{C}$ .

5. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings and Note 4.

**RECOMMENDED OPERATING CONDITIONS**

| Parameter                                   | Symbol    | MIN.    | TYP.     | MAX.     | Unit |
|---------------------------------------------|-----------|---------|----------|----------|------|
| Power Supply Voltage (Dual)                 | $V^{\pm}$ | $\pm 2$ | $\pm 5$  | $\pm 7$  | V    |
| Power Supply Voltage ( $V^- = \text{GND}$ ) | $V^+$     | +4      | +5 / +12 | +14      | V    |
| Output Current                              | $I_O$     |         |          | $\pm 10$ | mA   |
| Capacitive Load ( $A_V = +1$ )              | $C_L$     |         |          | 100      | pF   |

## ELECTRICAL CHARACTERISTICS

UPC4572G2 ( $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V^+ = \pm 5\text{ V}$ )

| Parameter                              | Symbol                   | MIN.      | TYP.      | MAX.      | Unit                           | Test Condition                                                                     |
|----------------------------------------|--------------------------|-----------|-----------|-----------|--------------------------------|------------------------------------------------------------------------------------|
| Input Offset Voltage                   | $V_{IO}$                 |           | $\pm 0.3$ | $\pm 5$   | mV                             | $R_S \leq 50\text{ }\Omega$                                                        |
| Input Offset Current                   | $I_{IO}$                 |           | $\pm 10$  | $\pm 100$ | nA                             |                                                                                    |
| Input Bias Current <sup>Note 6</sup>   | $I_B$                    |           | 100       | 400       | nA                             |                                                                                    |
| Large Signal Voltage Gain              | $A_v$                    | 10000     | 100000    |           |                                | $R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 2\text{ V}$                               |
| Circuit Current <sup>Note 7</sup>      | $I_{CC}$                 |           | 4.5       | 7         | mA                             | $I_O = 0\text{ A}$                                                                 |
| Common Mode Rejection Ratio            | CMR                      | 70        | 90        |           | dB                             |                                                                                    |
| Supply Voltage Rejection Ratio         | SVR                      | 70        | 85        |           | dB                             |                                                                                    |
| Output Voltage Swing                   | $V_{om}$                 | $\pm 3.3$ | $\pm 3.7$ |           | V                              | $R_L \geq 10\text{ k}\Omega$                                                       |
| Output Voltage Swing                   | $V_{om}$                 | $\pm 3.0$ | $\pm 3.5$ |           | V                              | $R_L \geq 2\text{ k}\Omega$                                                        |
| Common Mode Input Voltage Range        | $V_{ICM}$                | $\pm 3.5$ | $\pm 4$   |           | V                              |                                                                                    |
| Output Short Circuit Current           | $I_O$                    | $\pm 15$  | $\pm 20$  |           | mA                             | $R_L = 0\text{ }\Omega$                                                            |
| Slew Rate                              | SR                       | 3.5       | 6         |           | V/ $\mu$ s                     | $R_L \geq 2\text{ k}\Omega$                                                        |
| Gain Bandwidth Product                 | GBW                      | 10        | 16        |           | MHz                            | $f_O = 100\text{ kHz}$                                                             |
| Unity Gain Frequency                   | $f_{unity}$              |           | 9         |           | MHz                            | open loop                                                                          |
| Phase Margin                           | $\Phi_{unity}$           |           | 60        |           | Deg                            | open loop                                                                          |
| Total Harmonic Distortion              | THD                      |           | 0.002     |           | %                              | $V_O = 1\text{ V}_{r.m.s.}$ ,<br>$f = 20\text{ Hz} \sim 20\text{ kHz}$ (Figure 1 ) |
| Equivalent Noise Input Voltage         | $V_n$                    |           | 0.8       |           | $\mu\text{V}_{r.m.s.}$         | RIAA (Figure 2 )                                                                   |
| Equivalent Noise Input Voltage         | $V_n$                    |           | 0.5       | 0.65      | $\mu\text{V}_{r.m.s.}$         | FLAT + JIS A,<br>$R_S = 100\text{ }\Omega$ (Figure 3 )                             |
| Equivalent Noise Input Voltage Density | $e_n$                    |           | 4.5       |           | $\text{nV}/\sqrt{\text{Hz}}$   | $f_O = 10\text{ Hz}$                                                               |
| Equivalent Noise Input Voltage Density | $e_n$                    |           | 4.0       |           | $\text{nV}/\sqrt{\text{Hz}}$   | $f_O = 1\text{ kHz}$                                                               |
| Equivalent Noise Input Current Density | $i_n$                    |           | 0.7       |           | $\text{pA}/\sqrt{\text{Hz}}$   | $f_O = 1\text{ kHz}$                                                               |
| Channel Separation                     |                          |           | 120       |           | dB                             | $f = 20\text{ Hz} \sim 20\text{ kHz}$                                              |
| Average $V_{IO}$ Temperature Drift     | $\Delta V_{IO}/\Delta T$ |           | $\pm 2$   |           | $\mu\text{V}/^{\circ}\text{C}$ |                                                                                    |

UPC4572G2 ( $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V^+ = +5\text{ V}$ ,  $V^- = \text{GND}$ )

| Parameter                            | Symbol    | MIN. | TYP.      | MAX.      | Unit       | Test Condition                                            |
|--------------------------------------|-----------|------|-----------|-----------|------------|-----------------------------------------------------------|
| Input Offset Voltage                 | $V_{IO}$  |      | $\pm 0.3$ | $\pm 5$   | mV         | $R_S \leq 50\text{ }\Omega$                               |
| Input Offset Current                 | $I_{IO}$  |      | $\pm 10$  | $\pm 100$ | nA         |                                                           |
| Input Bias Current <sup>Note 6</sup> | $I_B$     |      | 100       | 400       | nA         |                                                           |
| Large Signal Voltage Gain            | $A_v$     | 8000 | 80000     |           |            | $R_L \geq 2\text{ k}\Omega$                               |
| Supply Current <sup>Note 7</sup>     | $I_{CC}$  |      | 4         | 6         | mA         | $I_O = 0\text{ A}$                                        |
| Common Mode Rejection Ratio          | CMR       | 60   | 75        |           | dB         |                                                           |
| Supply Voltage Rejection Ratio       | SVR       | 60   | 70        |           | dB         |                                                           |
| Output Voltage (High)                | $V_{OH}$  | 3.2  | 3.5       |           | V          | $R_L \geq 2\text{ k}\Omega$ ( $R_L$ to $1/2\text{ V}^+$ ) |
| Output Voltage (Low)                 | $V_{OL}$  |      | 1.3       | 1.6       | V          | $R_L \geq 2\text{ k}\Omega$ ( $R_L$ to $1/2\text{ V}^+$ ) |
| Common Mode Input Voltage Range      | $V_{ICM}$ | 1.5  |           | 3.5       | V          |                                                           |
| Slew Rate                            | SR        |      | 4         |           | V/ $\mu$ s |                                                           |
| Gain Band Width Product              | GBW       |      | 12        |           | MHz        |                                                           |

**【Note】 6.** Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage.

7. This current flows irrespective of the existence of use.

## ELECTRICAL CHARACTERISTICS

UPC4572G2(5) ( $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V^+ = \pm 5\text{ V}$ )

| Parameter                              | Symbol                   | MIN.                | TYP.      | MAX.      | Unit                           | Test Condition                                                                     |
|----------------------------------------|--------------------------|---------------------|-----------|-----------|--------------------------------|------------------------------------------------------------------------------------|
| Input Offset Voltage                   | $V_{IO}$                 |                     | $\pm 0.3$ | $\pm 1.5$ | mV                             | $R_S \leq 50\text{ }\Omega$                                                        |
| Input Offset Current <sup>Note 6</sup> | $I_{IO}$                 |                     | $\pm 10$  | $\pm 50$  | nA                             |                                                                                    |
| Input Bias Current <sup>Note 6</sup>   | $I_B$                    |                     | 100       | 200       | nA                             |                                                                                    |
| Large Signal Voltage Gain              | $A_V$                    | 30000               | 100000    |           |                                | $R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 2\text{ V}$                               |
| Circuit Current <sup>Note 7</sup>      | $I_{CC}$                 |                     | 4.5       | 5.5       | mA                             | $I_O = 0\text{ A}$                                                                 |
| Common Mode Rejection Ratio            | CMR                      | 75                  | 90        |           | dB                             |                                                                                    |
| Supply Voltage Rejection Ratio         | SVR                      | 70                  | 85        |           | dB                             |                                                                                    |
| Output Voltage Swing                   | $V_{om}$                 | $\pm 3.45$          | $\pm 3.7$ |           | V                              | $R_L \geq 10\text{ k}\Omega$                                                       |
| Output Voltage Swing                   | $V_{om}$                 | $\pm 3.3$           | $\pm 3.5$ |           | V                              | $R_L \geq 2\text{ k}\Omega$                                                        |
| Common Mode Input Voltage Range        | $V_{ICM}$                | $\pm 3.8$<br>$-3.7$ | $\pm 4$   |           | V                              |                                                                                    |
| Output Short Circuit Current           | $I_O$                    | $\pm 15$            | $\pm 20$  |           | mA                             | $R_L = 0\text{ }\Omega$                                                            |
| Slew Rate                              | SR                       | 3.5                 | 6         |           | V/ $\mu$ s                     | $R_L \geq 2\text{ k}\Omega$                                                        |
| Gain Bandwidth Product                 | GBW                      | 10                  | 16        |           | MHz                            | $f_O = 100\text{ kHz}$                                                             |
| Unity Gain Frequency                   | $f_{unity}$              |                     | 9         |           | MHz                            | open loop                                                                          |
| Phase Margin                           | $\phi_{unity}$           |                     | 60        |           | Deg                            | open loop                                                                          |
| Total Harmonic Distortion              | THD                      |                     | 0.002     |           | %                              | $V_O = 1\text{ V}_{r.m.s.}$ ,<br>$f = 20\text{ Hz} \sim 20\text{ kHz}$ (Figure 1 ) |
| Equivalent Noise Input Voltage         | $V_n$                    |                     | 0.8       |           | $\mu\text{V}_{r.m.s.}$         | RIAA (Figure 2 )                                                                   |
| Equivalent Noise Input Voltage         | $V_n$                    |                     | 0.5       | 0.65      | $\mu\text{V}_{r.m.s.}$         | FLAT + JIS A,<br>$R_S = 100\text{ }\Omega$ (Figure 3 )                             |
| Equivalent Noise Input Voltage Density | $e_n$                    |                     | 4.5       |           | $\text{nV}/\sqrt{\text{Hz}}$   | $f_O = 10\text{ Hz}$                                                               |
| Equivalent Noise Input Voltage Density | $e_n$                    |                     | 4.0       |           | $\text{nV}/\sqrt{\text{Hz}}$   | $f_O = 1\text{ kHz}$                                                               |
| Equivalent Noise Input Current Density | $i_n$                    |                     | 0.7       |           | $\text{pA}/\sqrt{\text{Hz}}$   | $f_O = 1\text{ kHz}$                                                               |
| Channel Separation                     |                          |                     | 120       |           | dB                             | $f = 20\text{ Hz} \sim 20\text{ kHz}$                                              |
| Average $V_{IO}$ Temperature Drift     | $\Delta V_{IO}/\Delta T$ |                     | $\pm 2$   |           | $\mu\text{V}/^{\circ}\text{C}$ |                                                                                    |

UPC4572G2(5) ( $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V^+ = +5\text{ V}$ ,  $V^- = \text{GND}$ )

| Parameter                              | Symbol    | MIN.  | TYP.      | MAX.      | Unit       | Test Condition                                            |
|----------------------------------------|-----------|-------|-----------|-----------|------------|-----------------------------------------------------------|
| Input Offset Voltage                   | $V_{IO}$  |       | $\pm 0.3$ | $\pm 1.5$ | mV         | $R_S \leq 50\text{ }\Omega$                               |
| Input Offset Current <sup>Note 6</sup> | $I_{IO}$  |       | $\pm 10$  | $\pm 50$  | nA         |                                                           |
| Input Bias Current <sup>Note 6</sup>   | $I_B$     |       | 100       | 200       | nA         |                                                           |
| Large Signal Voltage Gain              | $A_V$     | 40000 | 80000     |           |            | $R_L \geq 2\text{ k}\Omega$                               |
| Supply Current <sup>Note 7</sup>       | $I_{CC}$  |       | 4         | 5         | mA         | $I_O = 0\text{ A}$                                        |
| Common Mode Rejection Ratio            | CMR       | 65    | 75        |           | dB         |                                                           |
| Supply Voltage Rejection Ratio         | SVR       | 60    | 70        |           | dB         |                                                           |
| Output Voltage (High)                  | $V_{OH}$  | 3.4   | 3.5       |           | V          | $R_L \geq 2\text{ k}\Omega$ ( $R_L$ to $1/2\text{ V}^+$ ) |
| Output Voltage (Low)                   | $V_{OL}$  |       | 1.3       | 1.45      | V          | $R_L \geq 2\text{ k}\Omega$ ( $R_L$ to $1/2\text{ V}^+$ ) |
| Common Mode Input Voltage Range        | $V_{ICM}$ | 1.2   |           | 3.8       | V          |                                                           |
| Slew Rate                              | SR        |       | 4         |           | V/ $\mu$ s |                                                           |
| Gain Band Width Product                | GBW       |       | 12        |           | MHz        |                                                           |

**【Note】 6.** Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage.

7. This current flows irrespective of the existence of use.

## MEASUREMENT CIRCUIT

Figure 1: Total Harmonic Distortion Measurement Circuit

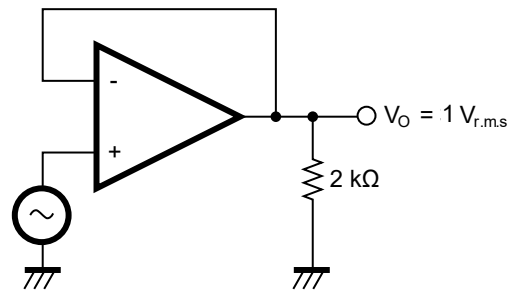


Figure 2: Noise Measurement Circuit (RIAA)

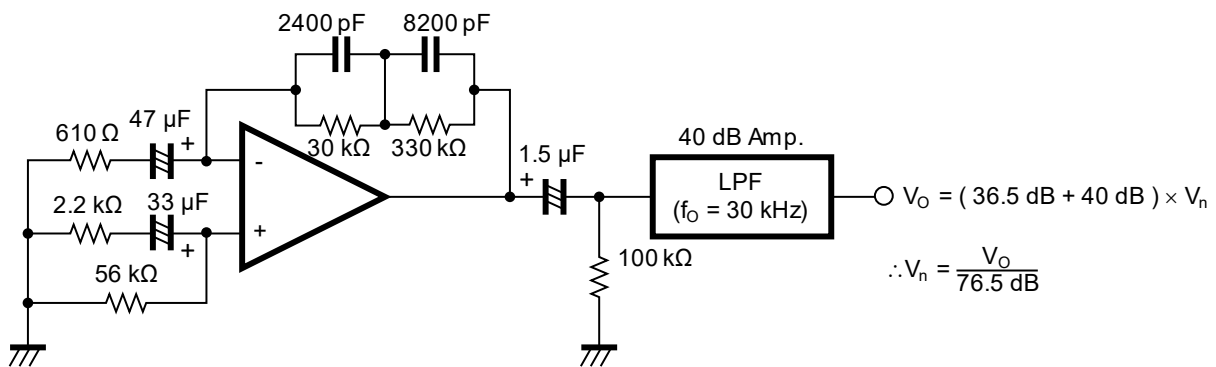
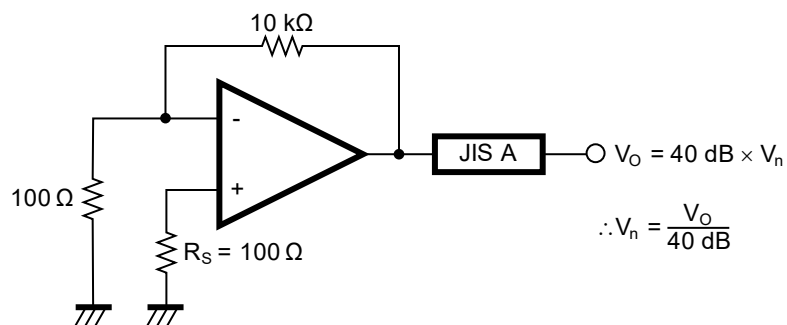
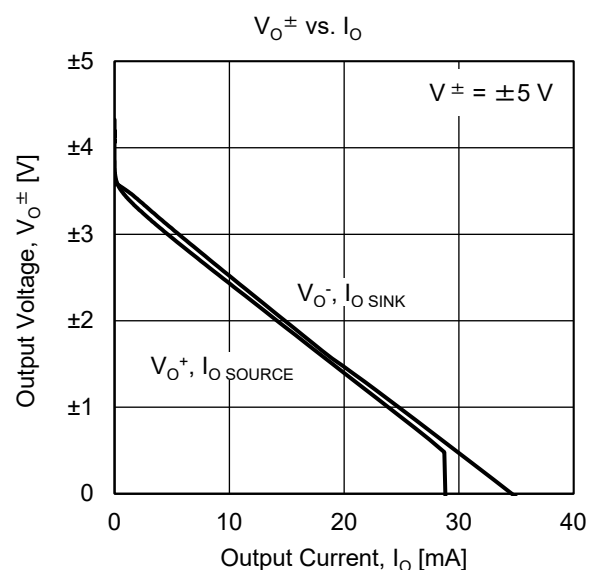
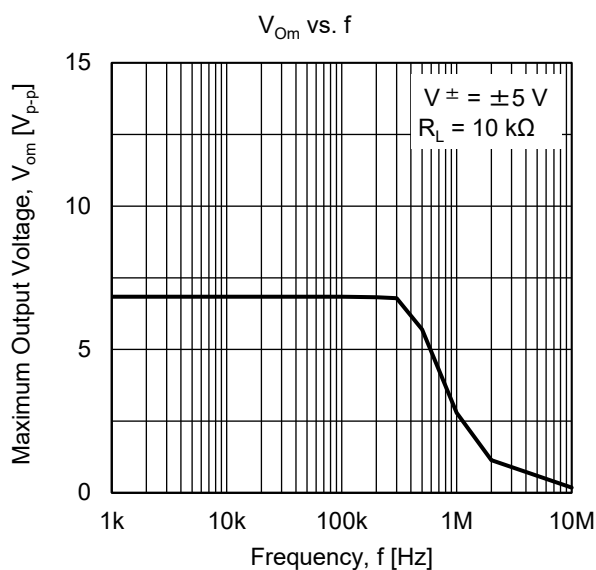
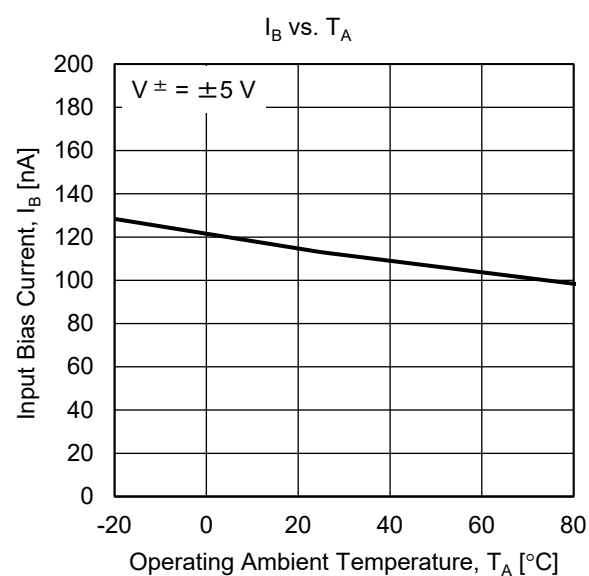
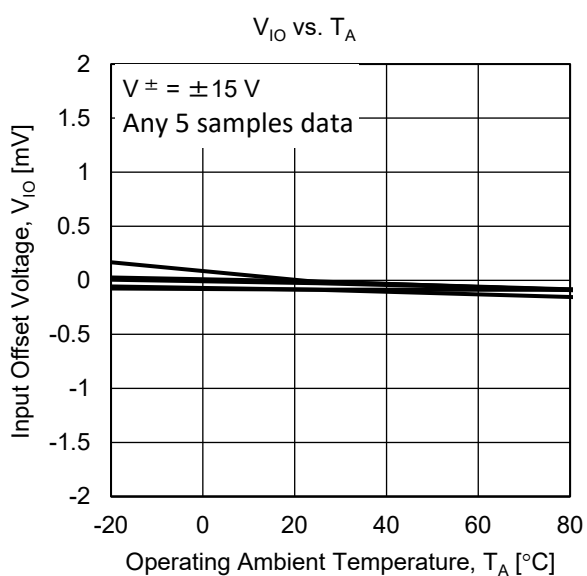
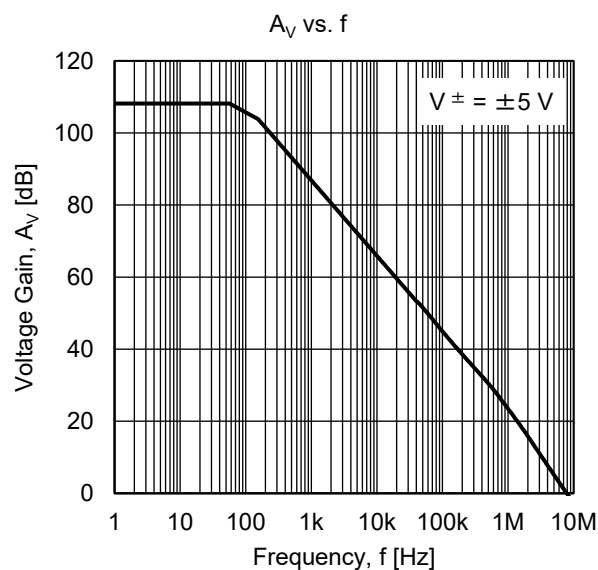
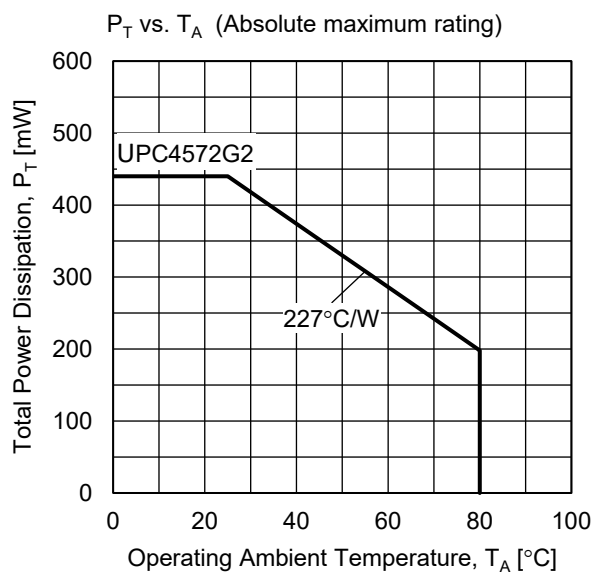
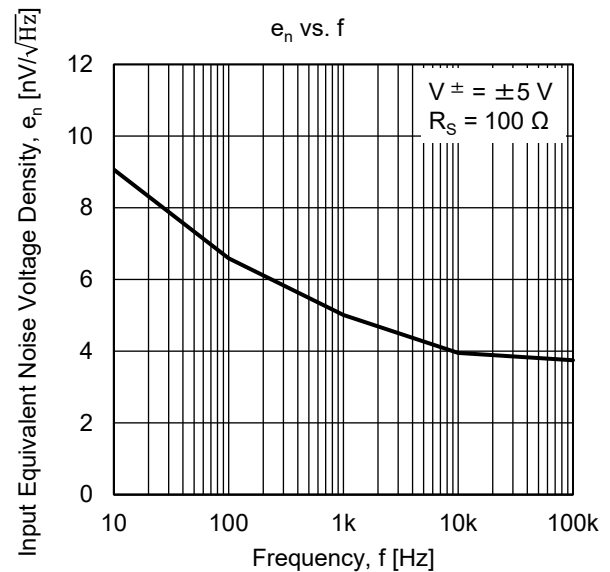
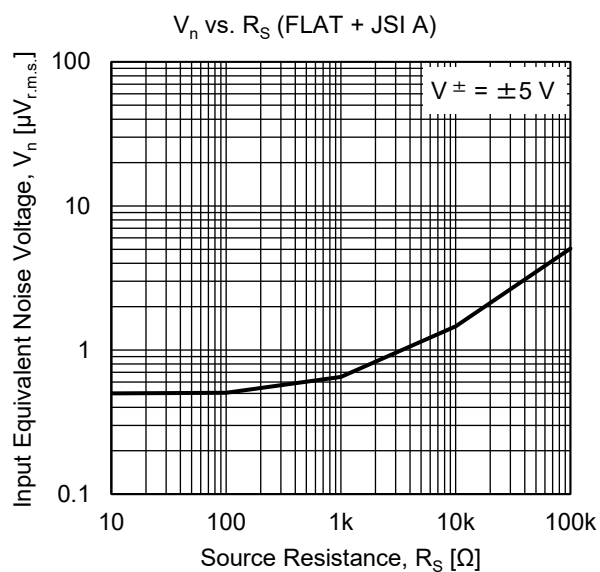
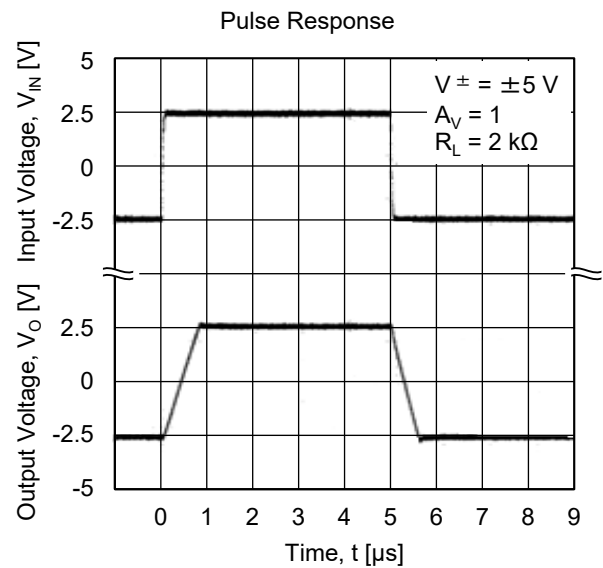
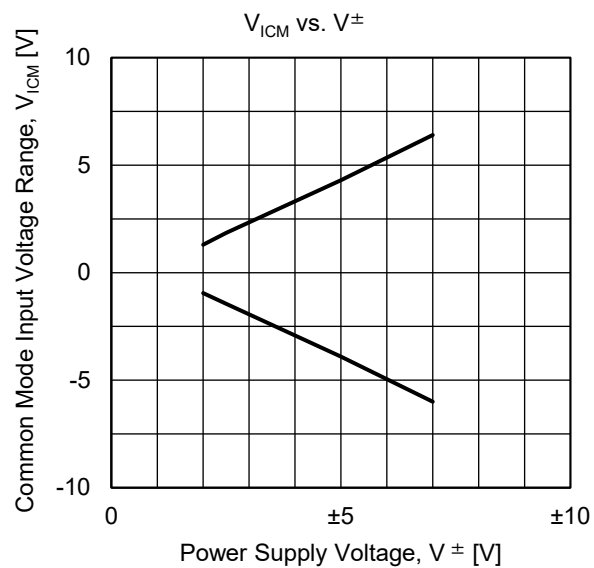
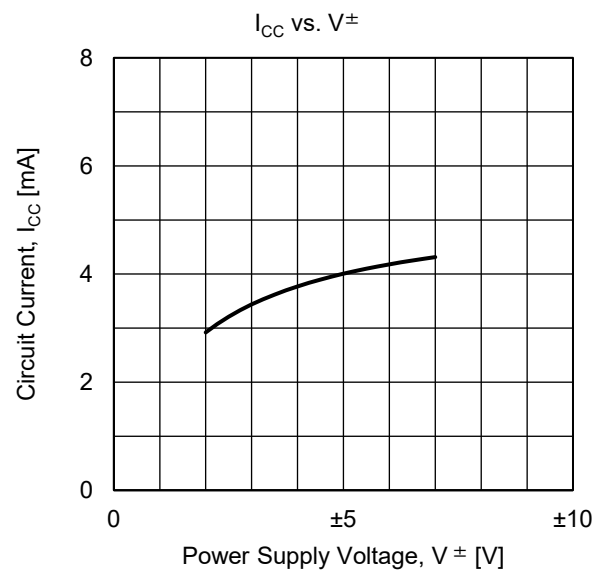
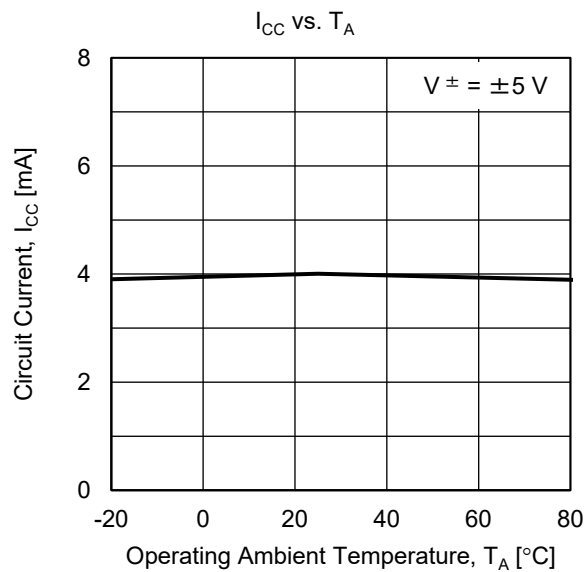


Figure 3: Noise Measurement Circuit (FLAT+JIS A)

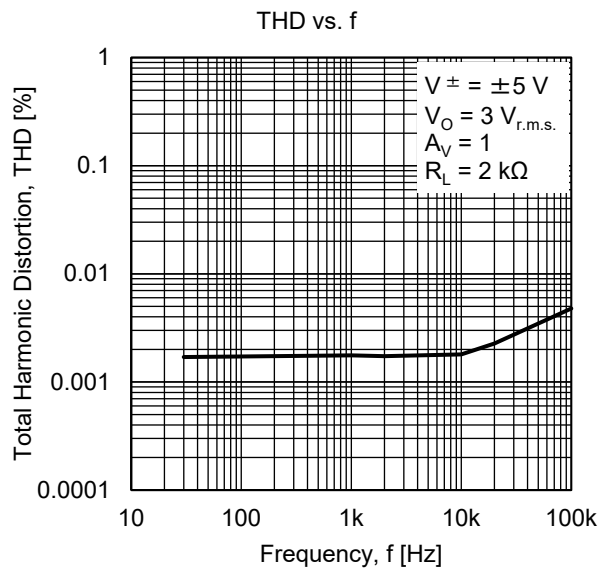


# CHARACTERISTICS CURVE ( $T_A = 25\text{ }^{\circ}\text{C}$ , TYP.) (REFERENCE VALUE)







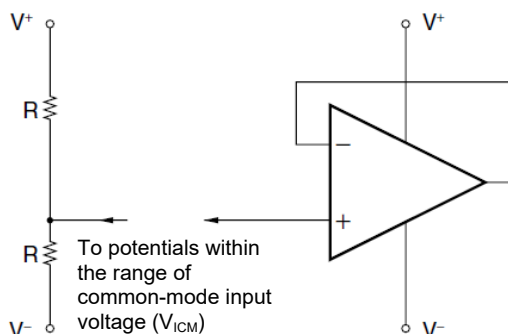


## USE WITH PRECAUTIONS

### • Managing unused circuits

If there is an unused circuit, the following connection is recommended.

Example of unused circuit process



Remark: In this example, an intermediate potential between  $V^+$  and  $V^-$  is applied.

### • Power Supply (Dual Power Supply / Single Power Supply)

The op-amp operates as long as a predetermined voltage is applied between  $V^+$  and  $V^-$ . Therefore, it can operate with a single power supply ( $V^- = \text{GND}$ ), but it cannot operate the input and output near GND. Common-mode input voltage Please pay attention to the range and maximum output voltage.

### • Ratings of input/output pin voltage

When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than  $V^-$ , or the output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

### • Range of common-mode input voltage

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

$V_{\text{ICM}} (\text{TYP.}): V^- + 1 \sim V^+ - 1 [\text{V}] (T_A = 25^\circ\text{C}).$

During designing, do include some tolerance by considering temperature characteristics etc.

### • Maximum output voltage

The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

$V_{\text{om}}^+ (\text{TYP.}): V^+ - 1.3 [\text{V}] (T_A = 25^\circ\text{C}), V_{\text{om}}^- (\text{TYP.}): V^- + 1.3 [\text{V}] (T_A = 25^\circ\text{C})$

During designing, do include some tolerance by considering characteristics variation, temperature characteristics and so on. In addition, also note that the output voltage range ( $V_{\text{om}}^+ - V_{\text{om}}^-$ ) will become narrow when the output current increases.

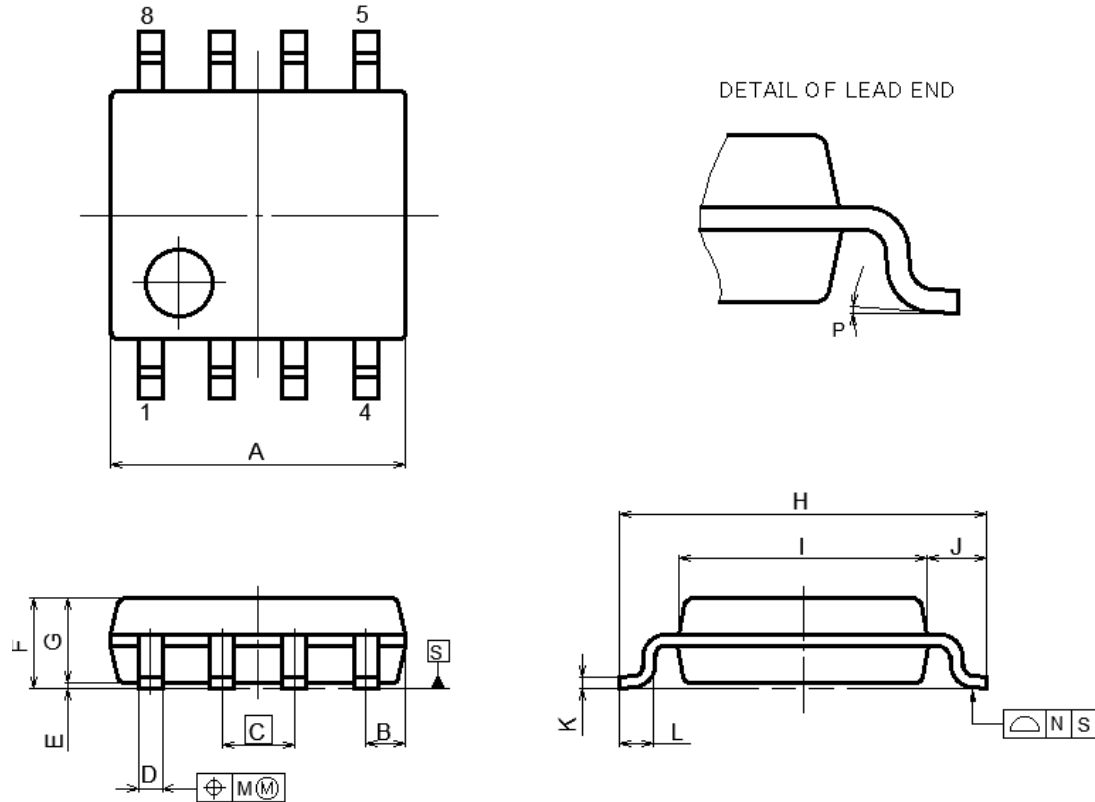
### • Handling of ICs

When stress is added to ICs due to warpage or bending of a board, the characteristic may fluctuates due to piezoelectric (piezo) effect. Therefore, pay attention to warpage or bending of a board.

## PACKAGE DRAWINGS

### 8-PIN PLASTIC SOP

| JEITA Package code   | RENESAS code | MASS (TYP.) [g] |
|----------------------|--------------|-----------------|
| P-LSOP8-4.4×5.2-1.27 | PLSP0008DE-A | 0.09[g]         |



#### NOTE

EACH LEAD CENTERLINE IS LOCATED WITHIN 0.12 MM OF ITS TRUE POSITION(T.P.) AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)

| ITEM | DIMENSIONS |
|------|------------|
| A    | 5.2±0.17   |
| B    | 0.78MAX    |
| C    | 1.27(T.P)  |
| D    | 0.40±0.05  |
| E    | 0.1±0.1    |
| F    | 1.59±0.21  |
| G    | 1.49       |
| H    | 6.5±0.3    |
| I    | 4.4±0.1    |
| J    | 1.05±0.15  |
| K    | 0.2±0.07   |
| L    | 0.6±0.20   |
| M    | 0.1MAX     |
| N    | 0.1MAX     |
| P    | 4°±4°      |

## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
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