μPC4570MF-DAA

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Rev.1.00
Jul 25, 2012

Ultra Low-Noise, High Speed, Wideband, Dual Operational Amplifier
e_n = 4.5 nV/√Hz, SR = 7 V/μs, GBW = 15 MHz, V_{IO} = ±0.3 mV

Description

The μPC4570MF-DAA is an ultra low-noise, wideband high slew-rate, dual operational amplifier. Input equivalent noise is three times better than the conventional μPC4558 type op-amps. The gain bandwidth products and the slew-rate are seven times better than μPC4558. In spite of fast AC performance, the μPC4570MF-DAA is extremely stable under voltage-follower circuit conditions. Supply current is also improved compared with conventional wideband op-amps.

The μPC4570MF-DAA is an excellent choice for pre-amplifiers and active filters in audio, instrumentation, and communication circuits.

Features

- Ultra low-noise (f = 1 kHz): 4.5 nV/√Hz (TYP.)
- Total harmonic distortion (f = 20 Hz to 20 kHz): 0.002% (TYP.)
- High slew rate : 7 V/μs (TYP.)
- High gain bandwidth product (f = 100 kHz) : 15 MHz (TYP.)
- Input offset voltage : ±0.3 mV (TYP.)
- Operating ambient temperature : −40 to +85°C
- Internal frequency compensation

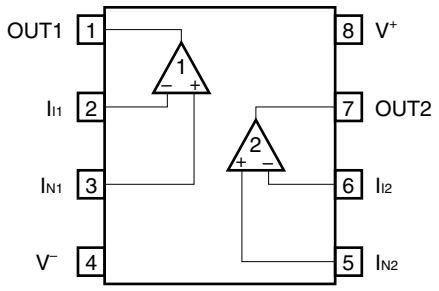
Ordering Information

Part Number	Package	Package Code (Previous Package Code)	Package Abbreviation	Supplying Form
μPC4570MF-DAA-E1-AT *1	8-pin plastic SOP (3.9 × 4.9)	PRSP0008DM-A (–)	MF	• 12 mm wide embossed taping • Pin 1 on draw-out side • 2500 p/reel

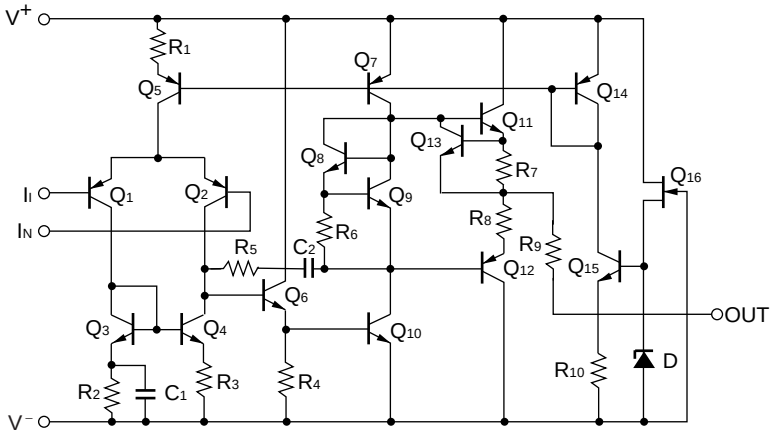
Note: *1. Pb-free (This product does not contain Pb in the external electrode and other parts.)

Caution Do not use the products in applications such as the transportation equipment (a car, a train, a ship, etc.) where “Special quality grade” is required, because the products are placed in a quality grade “standard” to be required at general devices.

Pin Configuration (Top View)



Equivalent Circuit (for Each Circuit)



Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Ratings	Unit
Voltage between V^+ and V^- *1	$V^+ - V^-$	−0.3 to +36	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage *2	V_I	V^- − 0.3 to V^+ + 0.3	V
Output Applied Voltage *3	V_O	V^- − 0.3 to V^+ + 0.3	V
Total Power Dissipation *4	P_T	440	mW
Output Short Circuit Duration (vs. GND) *5	t_S	10	s
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Notes: *1. Note that reverse connections of the power supply may damage ICs.

*2. The input voltage is allowed to input without damage or destruction independent of the magnitude of V^+. Either input signal is not allowed to go negative by more than 0.3 V. In addition, the input voltage that operates normally as an operational amplifier is within the Common Mode Input Voltage range of an electrical characteristic.

*3. A range where input voltage can be applied to an output pin externally with no deterioration or damage to the feature (characteristic). The input voltage can be applied regardless of the electric supply voltage. This specification which includes the transition state such as electric power ON/OFF must be kept.

*4. This is the value in $T_A \leq 56°C$ of when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted. Derate at −6.4 mW/°C when $T_A > 56°C$. In the condition same as the above, Junction − ambient thermal resistance $R_{th(J-A)}$ =156°C/W.

*5. Only as for $V^+ \leq 15$ V and any 1 channel. Please use the product within the derating condition or Total Power Dissipation, which are showed in Note 4.

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (Split)	$V^{\pm}$	±4		±16	V
Output Current	I_O			±10	mA
Source Resistance	R_S			50	kΩ
Capacitive Load (A_V = +1)	C_L			100	pF

Electrical Characteristics (T_A = 25°C, $V^{\pm}$ = ±15 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Conditions
Input Offset Voltage	V_{IO}		±0.3	±5	mV	R_S ≤ 50 Ω
Input Offset Current	I_{IO}		±10	±100	nA	
Input Bias Current *1	I_B		100	400	nA	
Large Signal Voltage Gain	A_V	30000	300000			R_L ≥ 2 kΩ, V_O = ±10 V
Supply Current *2	I_{CC}		5	8	mA	I_O = 0 A
Common Mode Rejection Ratio	CMR	80	100		dB	
Supply Voltage Rejection Ratio	SVR	80	100		dB	
Output Voltage Swing	V_{om}	±12	±13.4		V	R_L ≥ 10 kΩ
		±10	±12.8		V	R_L ≥ 2 kΩ
Common Model Input Voltage Range	V_{ICM}	±12	±14		V	
Slew Rate	SR	5	7		V/μs	A_V = +1, R_L ≥ 2 kΩ
Gain Bandwidth Product	GBW	10	15		MHz	f_O = 100 kHz
Unity Gain Frequency	f_{unity}		7		MHz	open loop
Phase Margin	ϕ_{unity}		50		degree	open loop
Total Harmonic Distortion	THD		0.002		%	V_O = 3 $V_{r.m.s.}$, f = 20 Hz to 20 kHz (Figure1)
Input Equivalent Noise Voltage	V_n		0.9		$\mu V_{r.m.s.}$	RIAA (Figure2)
			0.53	0.65	$\mu V_{r.m.s.}$	FLAT+JIS A, R_S = 100 Ω (Figure3)
Input Equivalent Noise Voltage Dencity	e_n		5.5		nV/√Hz	f_O = 10 Hz, R_S = 100 Ω
			4.5		nV/√Hz	f_O = 1 kHz, R_S = 100 Ω
Input Equivalent Noise Current Density	i_n		0.7		pA/√Hz	f_O = 1 kHz
Channel Separation			120		dB	f = 20 Hz to 20 kHz

Notes: *1. Input bias currents flow out from IC. Because each current is base current of PNP-transistor on input stage.

*2. This is a current that flows in the internal circuit. This current flows irrespective of the existence of use.

MEASUREMENT CIRCUIT

Figure1 Total Harmonic Distortion Measurement Circuit

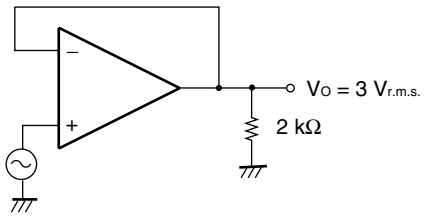


Figure2 Noise Measurement Circuit (RIAA)

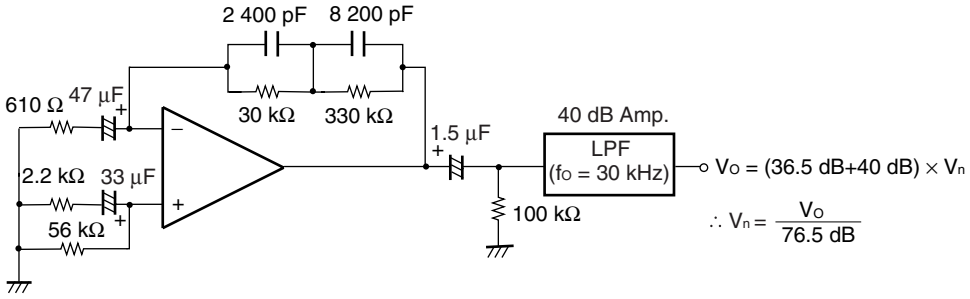
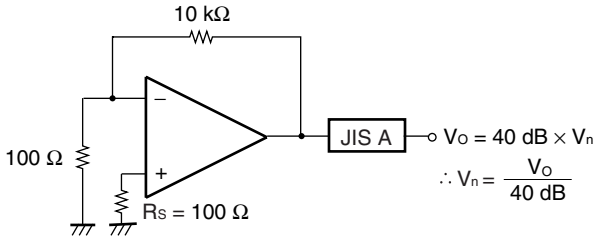
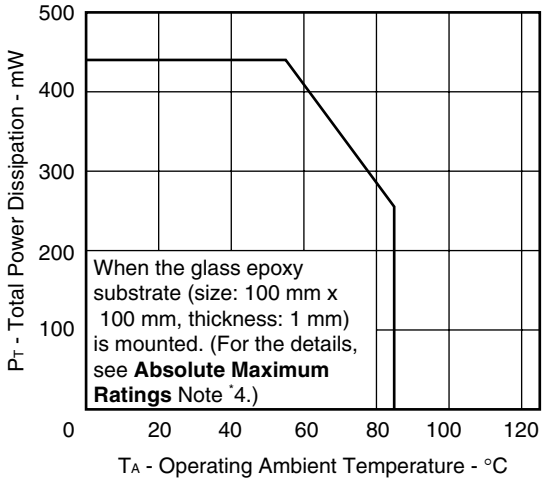


Figure3 Noise Measurement Circuit (FLAT+JIS A)

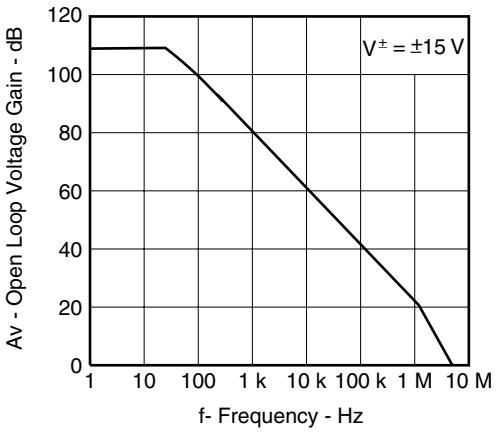


Typical Characteristics (T_A = 25°C, TYP.)

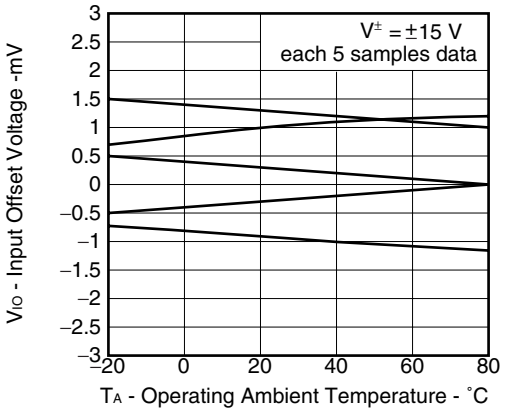
P_T vs. T_A



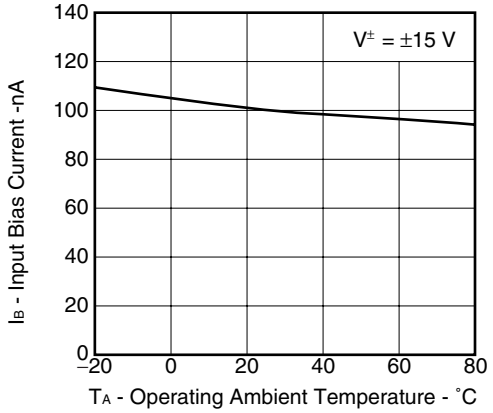
OPEN LOOP FREQUENCY RESPONSE



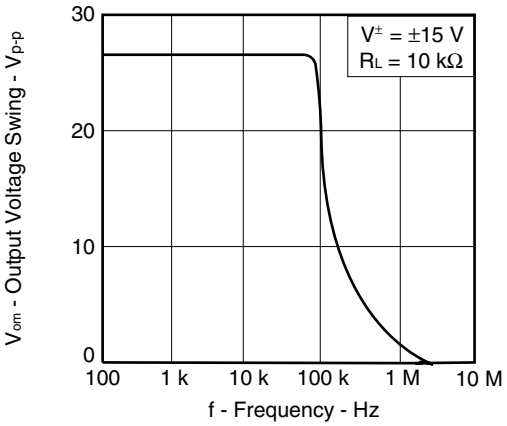
INPUT OFFSET VOLTAGE



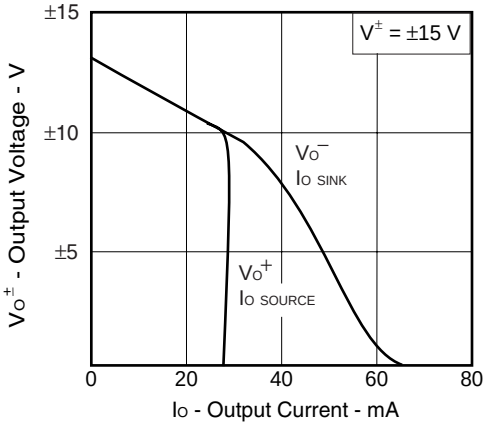
INPUT BIAS CURRENT



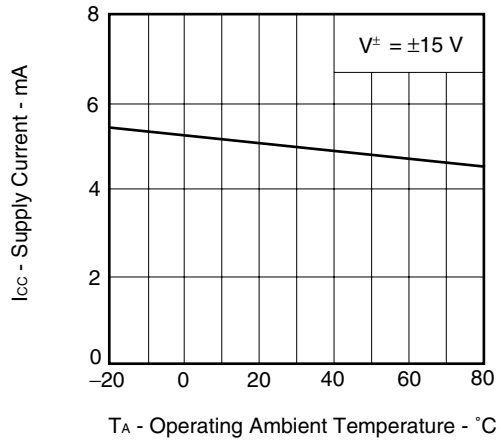
LARGE SIGNAL FREQUENCY RESPONSE



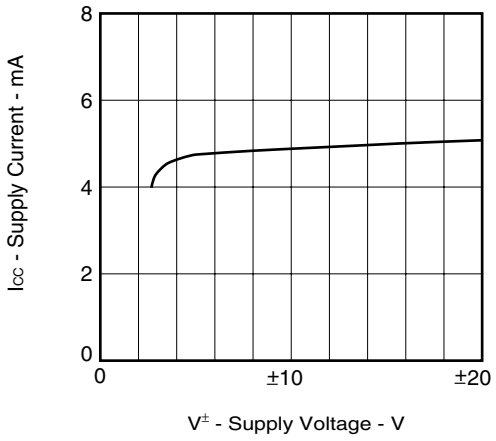
OUTPUT CURRENT LIMIT



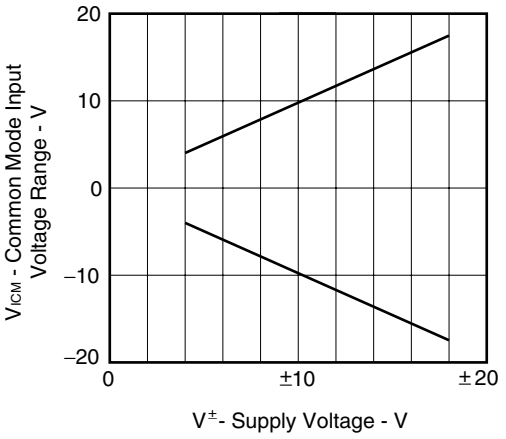
SUPPLY CURRENT vs. TEMPERATURE



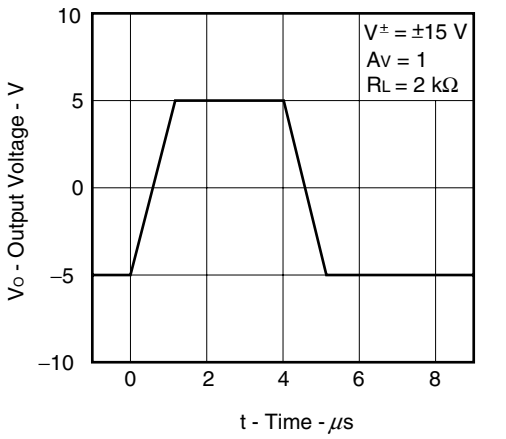
SUPPLY CURRENT vs. SUPPLY VOLTAGE



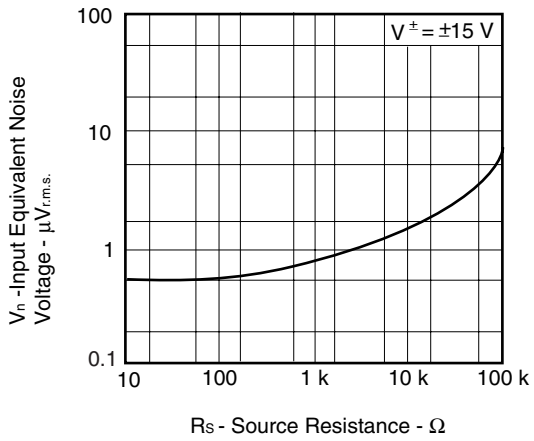
COMMON MODE INPUT VOLTAGE RANGE



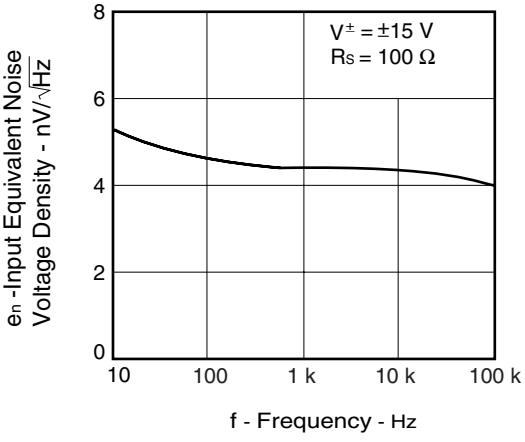
VOLTAGE FOLLOWER PULSE RESPONSE



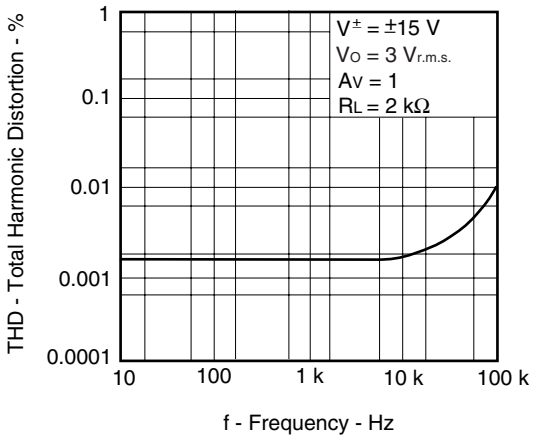
INPUT EQUIVALENT NOISE VOLTAGE (FLAT+JIS A)



INPUT EQUIVALENT NOISE VOLTAGE DENSITY



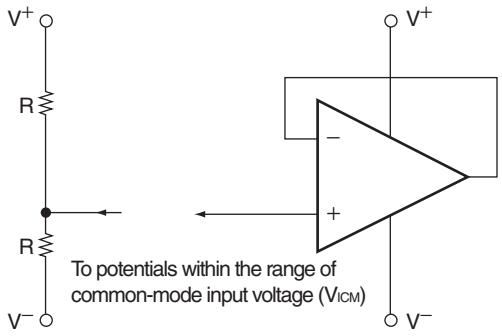
TOTAL HARMONIC DISTORTION



PRECAUTIONS FOR USE

- **The process of unused circuits**
  If there is an unused circuit, the following connection is recommended.

Process example of unused circuits



Remark A midpoint potential of V^+ and V^- is applied to this example.

- **Power supply used (Split/Single)**
  The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

- **Ratings of input/output pin voltage**
  When the voltage of input/output pin exceeds the absolute maximum rating, it may cause degradation of characteristics or damages, by a conduction of a parasitic diode within an IC. In addition, when the input pin may be lower than V^-, or the output pin may exceed the power supply voltage, it is recommended to make a clump circuit by a diode whose forward voltage is low (e.g.: Schottky diode) for protection.

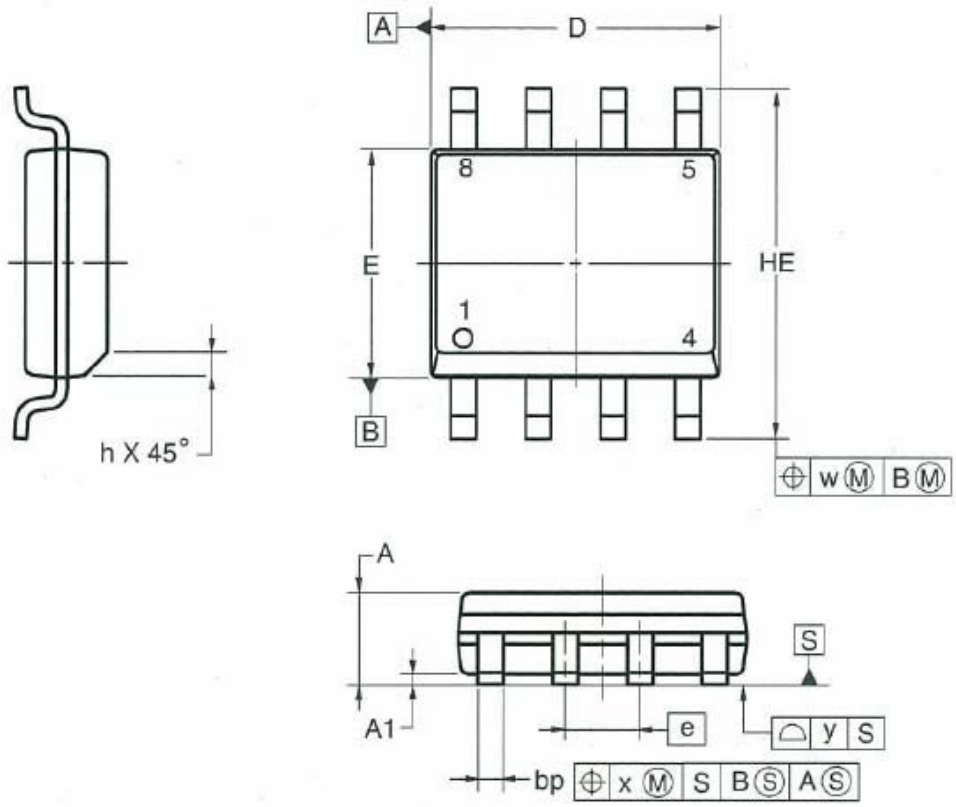
- **Range of common-mode input voltage**
  When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.
  V_{ICM} (TYP.): V^- + 1 (V) to V^+ −1 (V) (T_A = 25°C)
  During designing, temperature characteristics for use with allowance.

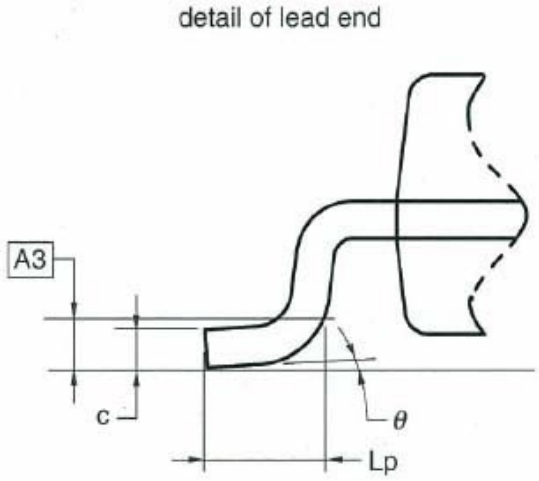
- **The maximum output voltage**
  The range of the TYP. value of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:
  V_{om}^+ (TYP.): V^+ −1.6 (V) (T_A = 25°C), V_{om}^- (TYP.): V^- + 1.6 (V) (T_A = 25°C)
  During designing, consider variations in characteristics and temperature characteristics for use with allowance.
  In addition, also note that the output voltage range (V_{om}^+ − V_{om}^-) becomes narrow when an output current increases.

- **Handling of ICs**
  When stress is added to ICs due to warpage or bending of a board, the characteristic fluctuates due to piezoelectric effect. Therefore, pay attention to warpage or bending of a board.

Package Drawings

8-pin Plastic SOP (3.9 × 4.9)





(UNIT:mm)

ITEM	DIMENSIONS
D	4.80 to 5.00
E	3.80 to 4.00
HE	5.80 to 6.20
e	1.27
bp	0.35 to 0.49
A	1.35 to 1.75
A1	0.10 to 0.25
A3	0.25
c	0.19 to 0.25
Lp	0.40 to 1.25
h	0.25 to 0.50
w	0.25
x	0.25
y	0.10
θ	0° to 7°

Revision History	μPC4570MF-DAA Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Jul 25, 2012	–	First Edition Issued

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