

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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Not recommended  
for new design

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BIPOLAR ANALOG INTEGRATED CIRCUIT  
**μPC3226TB**

**5 V, SILICON GERMANIUM MMIC  
 MEDIUM OUTPUT POWER AMPLIFIER**

**DESCRIPTION**

The μPC3226TB is a silicon germanium (SiGe) monolithic integrated circuit designed as IF amplifier for DBS tuners. This IC is manufactured using our 50 GHz  $f_{max}$  UHS2 (Ultra High Speed Process) SiGe bipolar process.

**FEATURES**

- Low current :  $I_{CC} = 15.5$  mA TYP. @  $V_{CC} = 5.0$  V
- Medium output power :  $P_{O(sat)} = +13.0$  dBm TYP. @  $f = 1.0$  GHz  
 :  $P_{O(sat)} = +9.0$  dBm TYP. @  $f = 2.2$  GHz
- High linearity :  $P_{O(1dB)} = +7.5$  dBm TYP. @  $f = 1.0$  GHz  
 :  $P_{O(1dB)} = +5.7$  dBm TYP. @  $f = 2.2$  GHz
- Power gain :  $G_P = 25.0$  dB TYP. @  $f = 1.0$  GHz  
 :  $G_P = 26.0$  dB TYP. @  $f = 2.2$  GHz
- Noise Figure :  $NF = 5.3$  dB TYP. @  $f = 1.0$  GHz  
 :  $NF = 4.9$  dB TYP. @  $f = 2.2$  GHz
- Supply voltage :  $V_{CC} = 4.5$  to  $5.5$  V
- Port impedance : input/output  $50 \Omega$

**APPLICATIONS**

- IF amplifiers in LNB for DBS converters etc.

**ORDERING INFORMATION**

Part Number	Order Number	Package	Marking	Supplying Form
μPC3226TB-E3	μPC3226TB-E3-A	6-pin super minimold (Pb-Free) <sup>Note</sup>	C3N	Embossed tape 8 mm wide. 1, 2, 3 pins face the perforation side of the tape. Qty 3 kpcs/reel.

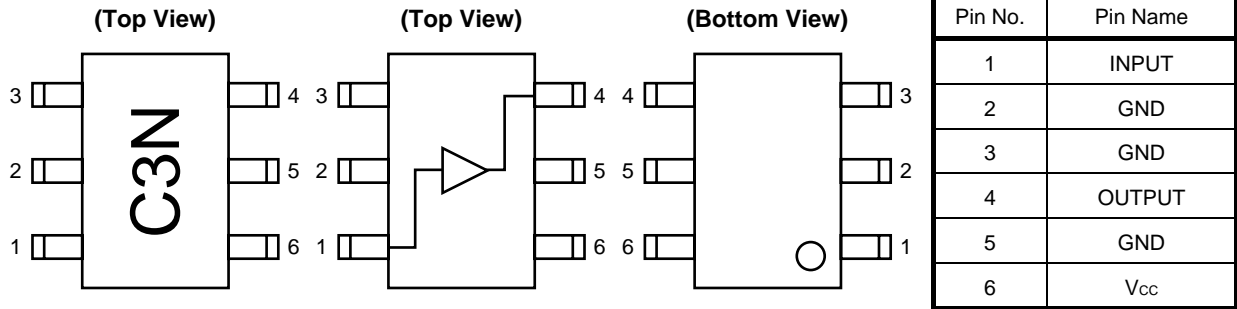
**Note** With regards to terminal solder (the solder contains lead) plated products (conventionally plated), contact your nearby sales office.

**Remark** To order evaluation samples, please contact your nearby sales office  
 Part number for sample order: μPC3226TB

**Caution** Observe precautions when handling because these devices are sensitive to electrostatic discharge.

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 Not all devices/types available in every country. Please check with local NEC Compound Semiconductor Devices representative for availability and additional information.

PIN CONNECTIONS



PRODUCT LINE-UP OF 5 V-BIAS SILICON MMIC MEDIUM OUTPUT POWER AMPLIFIER  
(T<sub>A</sub> = +25°C, f = 1 GHz, V<sub>CC</sub> = V<sub>out</sub> = 5.0 V, Z<sub>s</sub> = Z<sub>L</sub> = 50 Ω)

Part No.	f <sub>u</sub> (GHz)	P <sub>O (sat)</sub> (dBm)	G <sub>P</sub> (dB)	NF (dB)	I <sub>cc</sub> (mA)	Package	Marking
$\mu$ PC2708TB	2.9	+10.0	15	6.5	26	6-pin super minimold	C1D
$\mu$ PC2709TB	2.3	+11.5	23	5.0	25		C1E
$\mu$ PC2710TB	1.0	+13.5	33	3.5	22		C1F
$\mu$ PC2776TB	2.7	+8.5	23	6.0	25		C2L
$\mu$ PC3223TB	3.2	+12.0	23	4.5	19		C3J
$\mu$ PC3225TB	2.8	+15.5 <sup>Note</sup>	32.5 <sup>Note</sup>	3.7 <sup>Note</sup>	24.5		C3M
$\mu$ PC3226TB	3.2	+13.0	25	5.3	15.5		C3N

**Note**  $\mu$ PC3225TB is f = 0.95 GHz

**Remark** Typical performance. Please refer to **ELECTRICAL CHARACTERISTICS** in detail.

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V <sub>CC</sub>	T <sub>A</sub> = +25°C	6.0	V
Total Circuit Current	I <sub>CC</sub>	T <sub>A</sub> = +25°C	40	mA
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> = +85°C <b>Note</b>	270	mW
Operating Ambient Temperature	T <sub>A</sub>		-40 to +85	°C
Storage Temperature	T <sub>stg</sub>		-55 to +150	°C
Input Power	P <sub>in</sub>	T <sub>A</sub> = +25°C	+10	dBm

**Note** Mounted on double-sided copper-clad 50 × 50 × 1.6 mm epoxy glass PWB

**RECOMMENDED OPERATING RANGE**

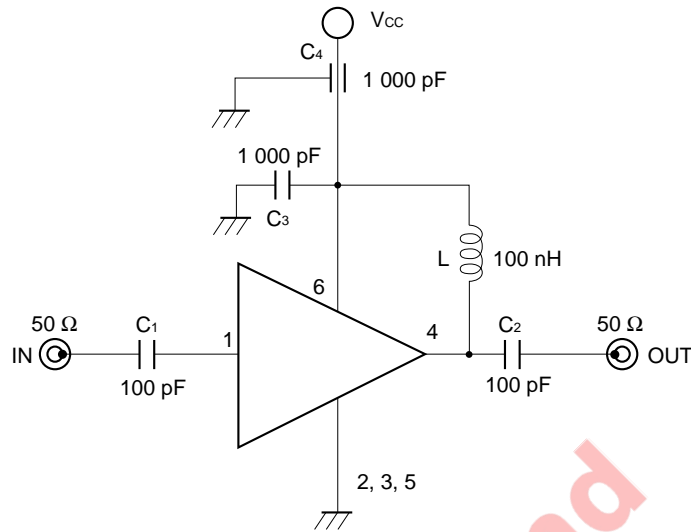
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply Voltage	V <sub>CC</sub>		4.5	5.0	5.5	V
Operating Ambient Temperature	T <sub>A</sub>		-40	+25	+85	°C

Not recommended for new design

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = +25°C, V<sub>CC</sub> = V<sub>out</sub> = 5.0 V, Z<sub>s</sub> = Z<sub>L</sub> = 50 Ω)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I <sub>CC</sub>	No input signal	12.5	15.5	19.5	mA
Power Gain 1	G <sub>P1</sub>	f = 0.1 GHz, P <sub>in</sub> = -30 dBm	22.0	24.0	26.0	dB
Power Gain 2	G <sub>P2</sub>	f = 1.0 GHz, P <sub>in</sub> = -30 dBm	23.0	25.0	27.5	
Power Gain 3	G <sub>P3</sub>	f = 1.8 GHz, P <sub>in</sub> = -30 dBm	23.0	26.0	29.0	
Power Gain 4	G <sub>P4</sub>	f = 2.2 GHz, P <sub>in</sub> = -30 dBm	23.0	26.0	29.0	
Power Gain 5	G <sub>P5</sub>	f = 2.6 GHz, P <sub>in</sub> = -30 dBm	22.5	25.5	29.0	
Power Gain 6	G <sub>P6</sub>	f = 3.0 GHz, P <sub>in</sub> = -30 dBm	22.0	25.0	28.5	
Saturated Output Power 1	P <sub>O(sat)1</sub>	f = 1.0 GHz, P <sub>in</sub> = -2 dBm	+10.0	+13.0	-	dBm
Saturated Output Power 2	P <sub>O(sat)2</sub>	f = 2.2 GHz, P <sub>in</sub> = -8 dBm	+6.0	+9.0	-	
Gain 1 dB Compression Output Power 1	P <sub>O(1dB)1</sub>	f = 1.0 GHz	+5.0	+7.5	-	dBm
Gain 1 dB Compression Output Power 2	P <sub>O(1dB)2</sub>	f = 2.2 GHz	+3.0	+5.7	-	
Noise Figure 1	NF1	f = 1.0 GHz	-	5.3	6.0	dB
Noise Figure 2	NF2	f = 2.2 GHz	-	4.9	6.0	
Isolation 1	ISL1	f = 1.0 GHz, P <sub>in</sub> = -30 dBm	31	34	-	dB
Isolation 2	ISL2	f = 2.2 GHz, P <sub>in</sub> = -30 dBm	33	36	-	
Input Return Loss 1	RL <sub>in1</sub>	f = 1.0 GHz, P <sub>in</sub> = -30 dBm	10.0	14.0	-	dB
Input Return Loss 2	RL <sub>in2</sub>	f = 2.2 GHz, P <sub>in</sub> = -30 dBm	9.0	13.0	-	
Output Return Loss 1	RL <sub>out1</sub>	f = 1.0 GHz, P <sub>in</sub> = -30 dBm	10.0	13.0	-	dB
Output Return Loss 2	RL <sub>out2</sub>	f = 2.2 GHz, P <sub>in</sub> = -30 dBm	10.0	13.0	-	
Input 3rd Order Distortion Intercept Point 1	IIP <sub>31</sub>	f <sub>1</sub> = 1 000 MHz, f <sub>2</sub> = 1 001 MHz, P <sub>in</sub> = -30 dBm	-	-5.0	-	dBm
Input 3rd Order Distortion Intercept Point 2	IIP <sub>32</sub>	f <sub>1</sub> = 2 200 MHz, f <sub>2</sub> = 2 201 MHz, P <sub>in</sub> = -30 dBm	-	-11.0	-	
Output 3rd Order Distortion Intercept Point 1	OIP <sub>31</sub>	f <sub>1</sub> = 1 000 MHz, f <sub>2</sub> = 1 001 MHz, P <sub>in</sub> = -30 dBm	-	+20.0	-	dBm
Output 3rd Order Distortion Intercept Point 2	OIP <sub>32</sub>	f <sub>1</sub> = 2 200 MHz, f <sub>2</sub> = 2 201 MHz, P <sub>in</sub> = -30 dBm	-	+15.0	-	
2nd Order Intermodulation Distortion	IM <sub>2</sub>	f <sub>1</sub> = 1 000 MHz, f <sub>2</sub> = 1 001 MHz, P <sub>in</sub> = -30 dBm	-	43.0	-	dBc
K factor 1	K1	f = 1.0 GHz	-	1.4	-	-
K factor 2	K2	f = 2.2 GHz	-	1.6	-	-

TEST CIRCUIT



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

COMPONENTS OF TEST CIRCUIT FOR MEASURING ELECTRICAL CHARACTERISTICS

	Type	Value
C1, C2	Chip Capacitor	100 pF
C3	Chip Capacitor	1 000 pF
C4	Feed-through Capacitor	1 000 pF
L	Chip Inductor	100 nH

INDUCTOR FOR THE OUTPUT PIN

The internal output transistor of this IC, to output medium power. To supply current for output transistor, connect an inductor between the Vcc pin (pin 6) and output pin (pin 4). Select inductance, as the value listed above.

The inductor has both DC and AC effects. In terms of DC, the inductor biases the output transistor with minimum voltage drop to output enable high level. In terms of AC, the inductor makes output-port impedance higher to get enough gain. In this case, large inductance and Q is suitable.

CAPACITORS FOR THE Vcc, INPUT AND OUTPUT PINS

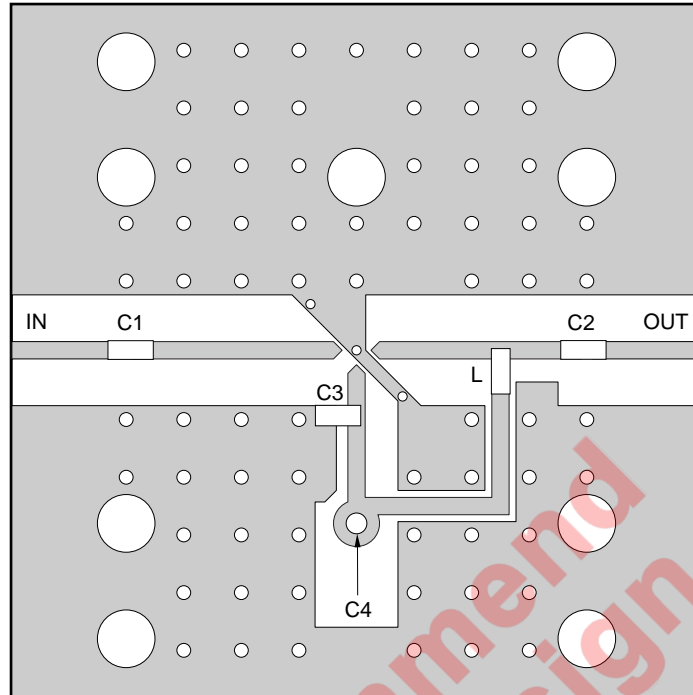
Capacitors of 1 000 pF are recommendable as the bypass capacitor for the Vcc pin and the coupling capacitors for the input and output pins.

The bypass capacitor connected to the Vcc pin is used to minimize ground impedance of Vcc pin. So, stable bias can be supplied against Vcc fluctuation.

The coupling capacitors, connected to the input and output pins, are used to cut the DC and minimize RF serial impedance. Their capacitances are therefore selected as lower impedance against a 50 Ω load. The capacitors thus perform as high pass filters, suppressing low frequencies to DC.

To obtain a flat gain from 100 MHz upwards, 1 000 pF capacitors are used in the test circuit. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 10 000 pF. Because the coupling capacitors are determined by equation,  $C = 1/(2 \pi Rf_c)$ .

ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

	Value
C1, C2	100 pF
C3, C4	1 000 pF
L1	100 nH

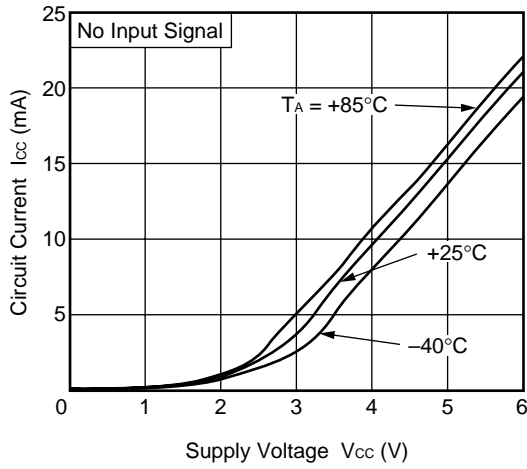
Notes

1. 30 × 30 × 0.4 mm double sided copper clad polyimide board.
2. Back side: GND pattern
3. Solder plated on pattern
4. ○: Through holes

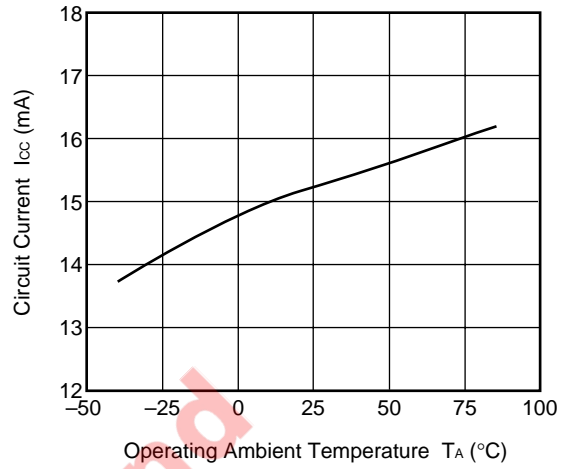


TYPICAL CHARACTERISTICS ( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{out} = 5.0\text{ V}$ ,  $Z_s = Z_L = 50\ \Omega$ , unless otherwise specified)

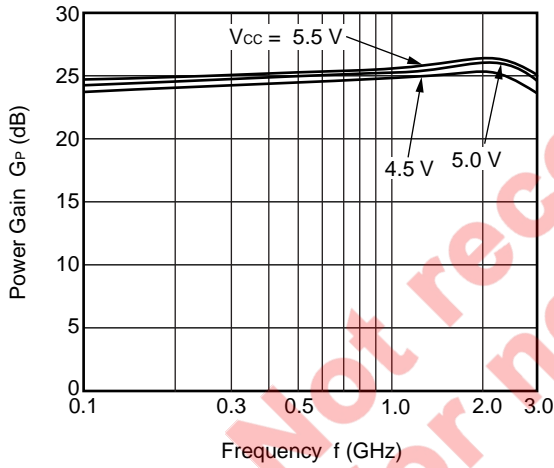
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



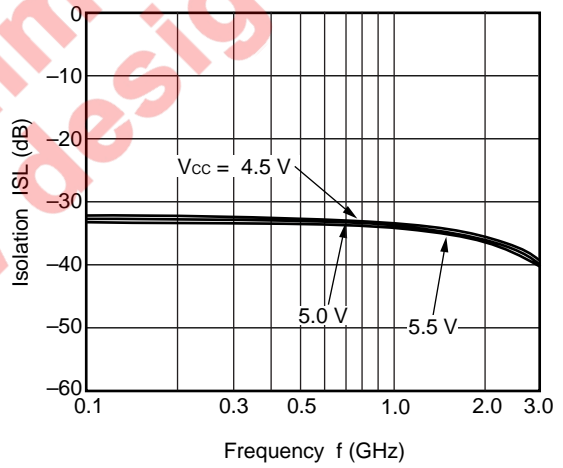
CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE



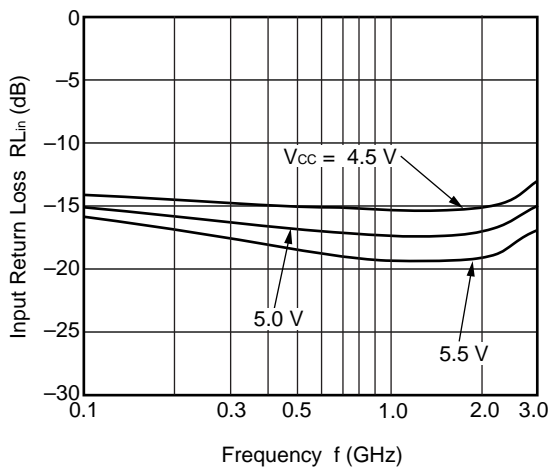
POWER GAIN vs. FREQUENCY



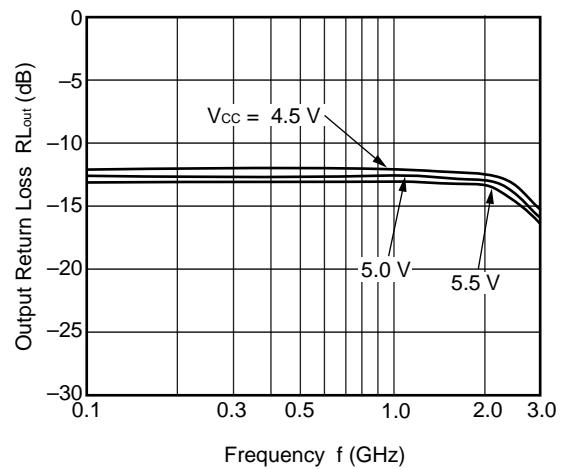
ISOLATION vs. FREQUENCY



INPUT RETURN LOSS vs. FREQUENCY

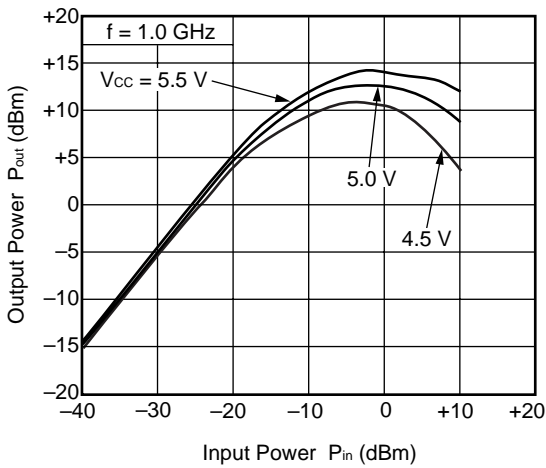


OUTPUT RETURN LOSS vs. FREQUENCY

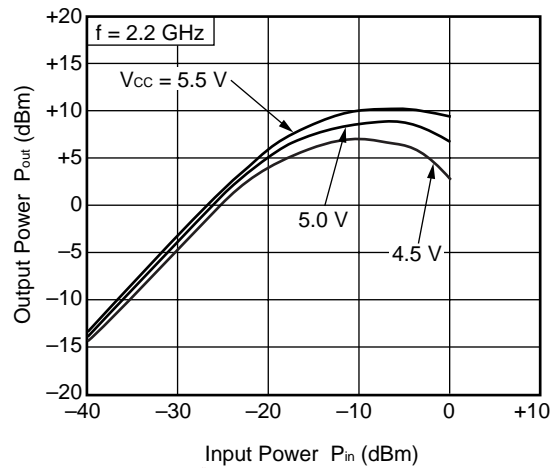


**Remark** The graphs indicate nominal characteristics.

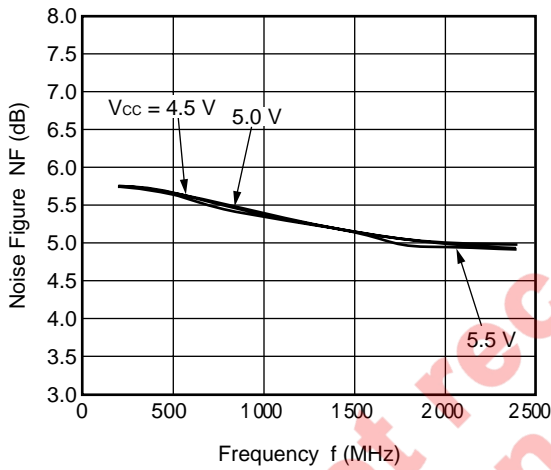
OUTPUT POWER vs. INPUT POWER



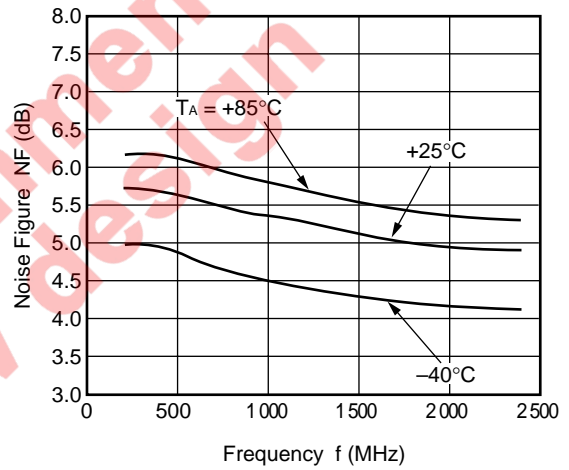
OUTPUT POWER vs. INPUT POWER



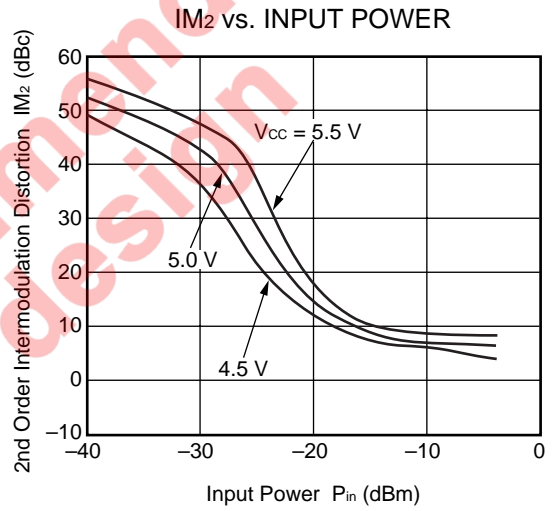
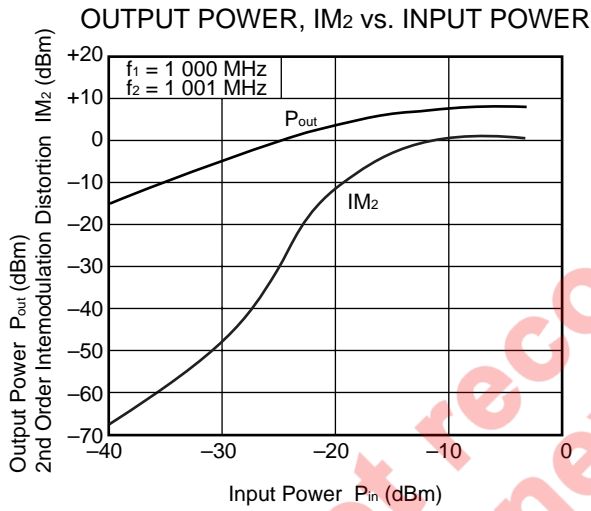
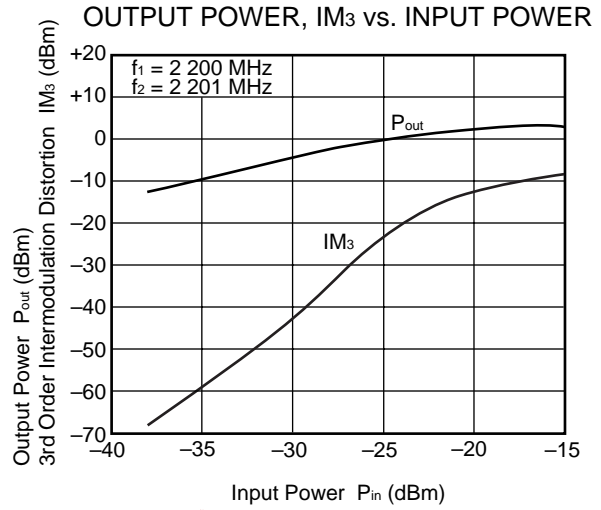
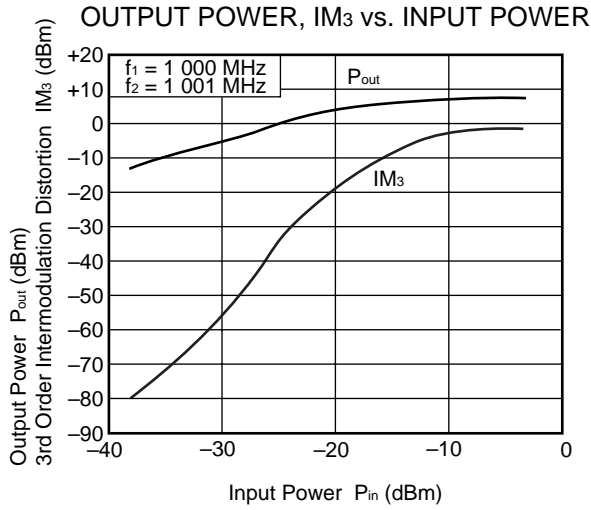
NOISE FIGURE vs. FREQUENCY



NOISE FIGURE vs. FREQUENCY



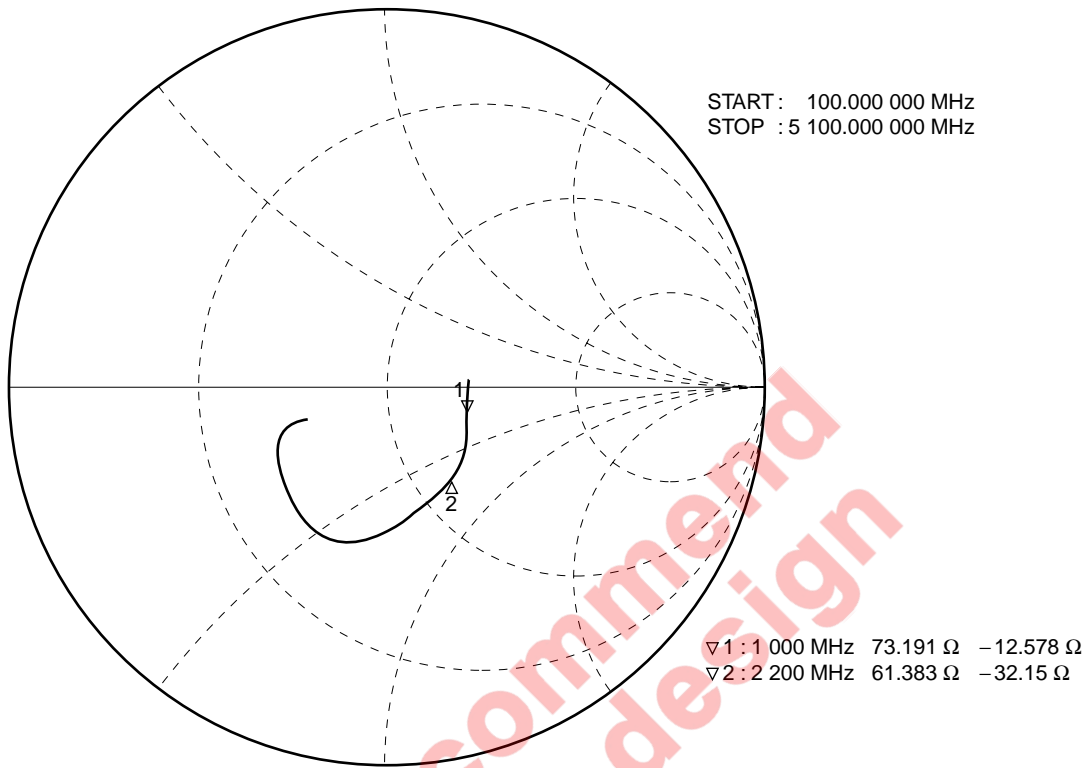
**Remark** The graphs indicate nominal characteristics.



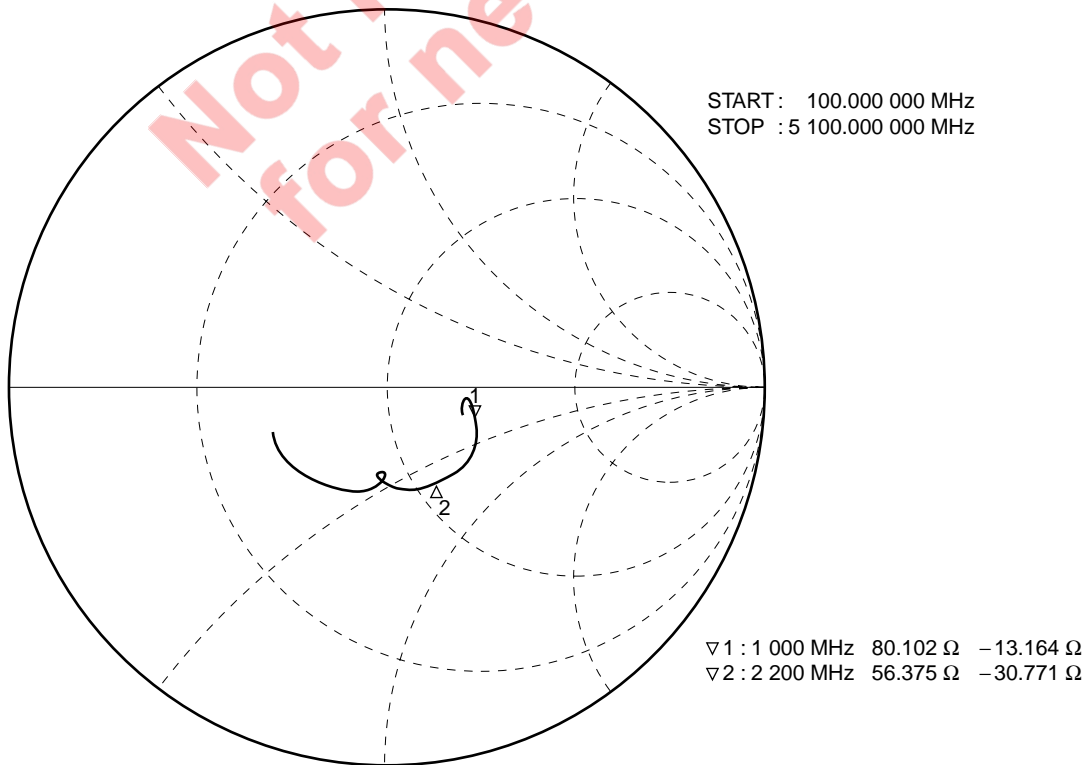
**Remark** The graphs indicate nominal characteristics.

S-PARAMETERS ( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{out} = 5.0\text{ V}$ ,  $P_{in} = -30\text{ dBm}$ )

S<sub>11</sub>-FREQUENCY

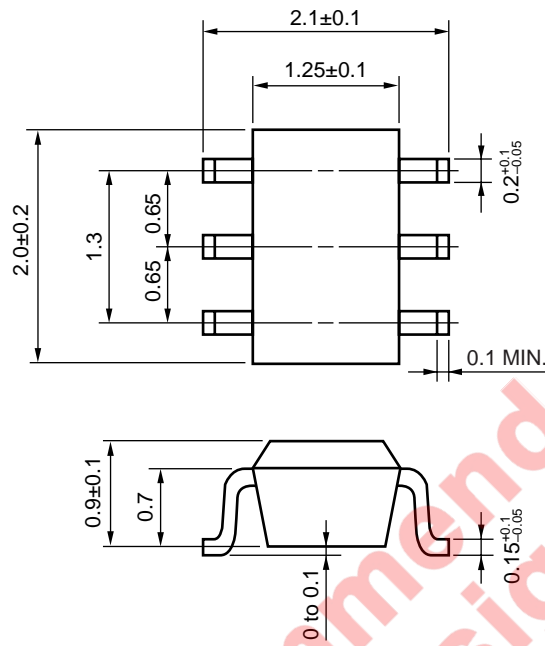


S<sub>22</sub>-FREQUENCY



PACKAGE DIMENSIONS

6-PIN SUPER MINIMOLD (UNIT: mm)



Not recommend  
for new design

**NOTES ON CORRECT USE**

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation).  
All the ground terminals must be connected together with wide ground pattern to decrease impedance difference.
- (3) The bypass capacitor should be attached to the V<sub>CC</sub> line.
- (4) The inductor (L) must be attached between V<sub>CC</sub> and output pins. The inductance value should be determined in accordance with desired frequency.
- (5) The DC cut capacitor must be attached to input and output pin.

**RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions	Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) : 260°C or below Time at peak temperature : 10 seconds or less Time at temperature of 220°C or higher : 60 seconds or less Preheating time at 120 to 180°C : 120±30 seconds Maximum number of reflow processes : 3 times Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	IR260
Wave Soldering	Peak temperature (molten solder temperature) : 260°C or below Time at peak temperature : 10 seconds or less Preheating temperature (package surface temperature) : 120°C or below Maximum number of flow processes : 1 time Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	WS260
Partial Heating	Peak temperature (terminal temperature) : 350°C or below Soldering time (per side of device) : 3 seconds or less Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	HS350

**Caution Do not use different soldering methods together (except for partial heating).**

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 "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots  
 "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)  
 "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

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(Note)

- (1) "NEC" as used in this statement means NEC Corporation, NEC Compound Semiconductor Devices, Ltd. and also includes its majority-owned subsidiaries.
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