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April 1st, 20<mark>10</mark> Renesas Electronics Corporation

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DATA SHEET



BIPOLAR ANALOG INTEGRATED CIRCUIT μPC1228

LOW NOISE DUAL PREAMPLIFIER

DESCRIPTION

The μ PC1228, a silicon monolithic integrated circuit, is a low noise dual preamplifier designed for car stereo applications. The device consists of two separate amplification channels, and its major features are low noise, low distortion, high gain, large dynamic range and wide supply voltage range.

FEATURES

• High open loop gain

 $A_{VO} = 100 \text{ dB TYP}.$

Low noise

: $V_{nin} = 1.1 \, \mu V \, TYP$.

• Low distortion

: THD = 0.05 % TYP.

• Large dynamic range

: $V_{OM} = 2.0 \text{ V TYP}$.

Wide supply voltage range

 $: V_{CC} = 6 \text{ to } 16 \text{ V}$

High output current

: I_{ODC} = 1 mA MAX.

Low impedance load driving capability

: $R_L = 1 k\Omega MIN$.

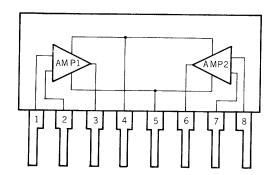
Small feedback capacitance capability

ORDERING INFORMATION

| PART NUMBER | PACKAGE | QUALITY GRADE |
|-------------|------------------------|---------------|
| μPC1228HA | 8 PIN PLASTIC SLIM SIP | Standard |

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

CONNECTION DIAGRAM



| Pin No. | Electrical connection |
|---------|-----------------------|
| 1 | Input 1 |
| 2 | Negative feed back 1 |
| 3 | Output 1 |
| 4 | Power supply: +Vcc |
| 5 | Ground |
| 6 | Output 2 |
| 7 | Negative feed back 2 |
| 8 | Input 2 |

ABSOLUTE MAXIMUM RATINGS (Ta = 25 $^{\circ}$ C)

| Supply Voltage | V _{CC} | 18 | V |
|-----------------------|-----------------|-------------------------|----|
| Package Dissipation | P_{D} | 270* | mW |
| Operating Temperature | T_{opt} | −30 to +75 | °C |
| Storage Temperature | T_{stg} | -40 to +125 | °c |
| | | * T _a =75 °C | |

RECOMMENDED OPERATING CONDITIONS ($T_a = 25$ °C)

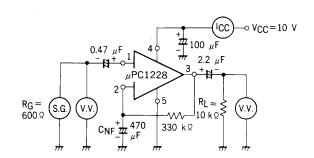
| Operating Supply Voltage | Vcc | 13.2 | V |
|-------------------------------|-----------------|------------|------------|
| Supply Voltage Range | V _{CC} | 6 to 16 | V |
| Operating Ambient Tamperature | Ta | −30 to +75 | °C |
| Load impedance | RL | 10 | k Ω |

ELECTRICAL CHARACTERISTICS ($T_a = 25$ °C, $V_{CC} = 10$ V, f = 1 kHz, $R_L = 10$ k Ω)

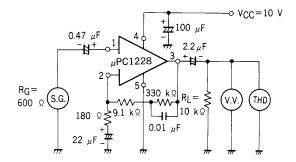
| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CIRCUIT | TEST CONDITIONS |
|--------------------------------|------------------|------|------|------|------|--------------|---|
| Quiescent Current | Icc | 2.5 | 3.3 | 4.8 | mA | (1) | V _{in} = 0 |
| Open Loop Voltage Gain | A _{vo} | 90 | 100 | | dB | (1) | V _O = 0.3 V, f = 100 Hz |
| Voltage Gain | A _V | | 40 | | dB | (2) | V _O = 0.3 V, NAB |
| Maximum Output Voltage | V _{OM} | 1.0 | 2.0 | | V | (2) | THD = 1 %, NAB |
| Total Harmonic Distortion | THD | | 0.05 | 0.3 | % | (2) | V _O = 0.3 V, NAB |
| Input Impedance | ri | 50 | 100 | | kΩ | (2) | |
| Equivalent Input Noise Voltage | V _{nin} | | 1.1 | 1.7 | μV | (3) | R _G = 2.2 kΩ, NAB |
| Cross Talk | СТ | -50 | -65 | | dB | (4) | $V_O = 1 \text{ V}$, (The other channel $V_{in} = 0$, $R_G = 2.2 \text{ k}\Omega$) |
| Channel Balance | Ch. B | -0.3 | 0 | +0.3 | dB | (4) | V _O = 0.3 V |

TEST CIRCUITS

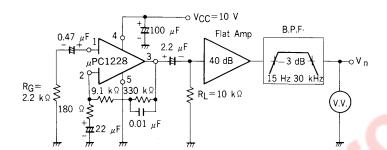
(1) I_{CC}, A_{vo} test circuit



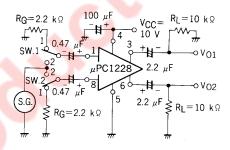
(2) A_{ν} , V_{OM} , THD, Z_{in} test circuit (for Ch. 1)



(3) V_{nin} test circuit (for Ch. 1)



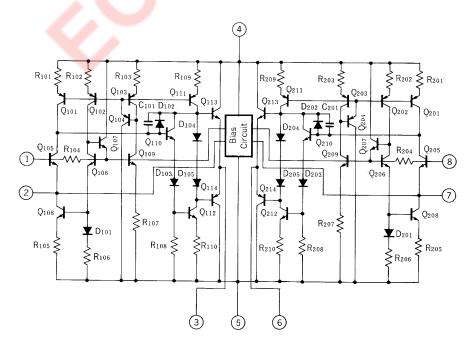
(4) Cross talk, Channel balance test circuit



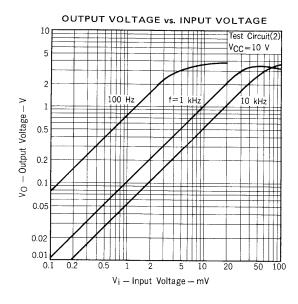
NOTE: V_{nin} is calculated by V_n and amp. gain $(A_V + 40 \text{ dB})$.

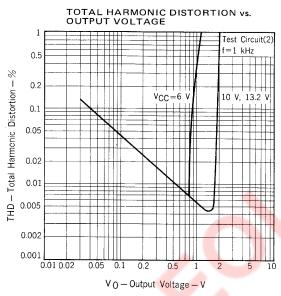
- NOTE 1: External components of the IC are the same as the test circuit (2).
 - 2: Cross talk procedure Switch position SW.1 \rightarrow 2, SW.2 \rightarrow 1, 20 log V_{02}/V_{01} Switch position SW.1 \rightarrow 1, SW.2 \rightarrow 2, 20log V_{01}/V_{02}
 - 3: Channel balance Switch position SW.1 \rightarrow 2, SW.2 \rightarrow 2, 20 log V₀₁/V₀₂

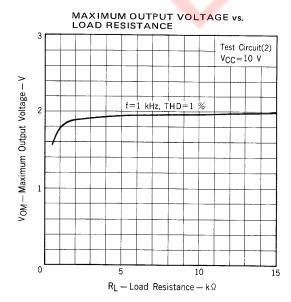
EQUIVALENT CIRCUIT

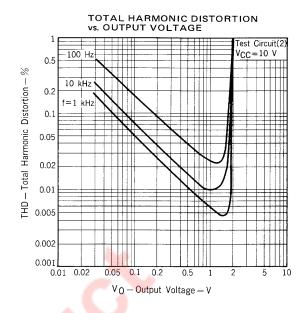


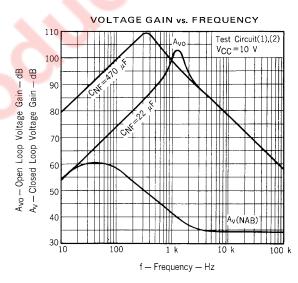
TYPICAL CHARACTERISTICS (Ta = 25 °C)

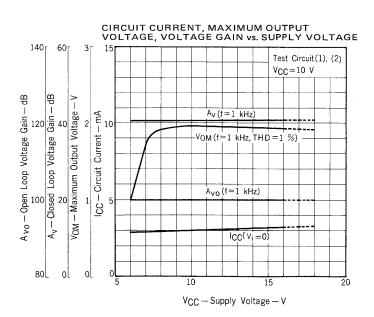


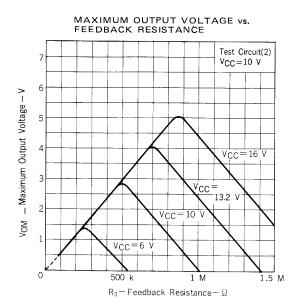


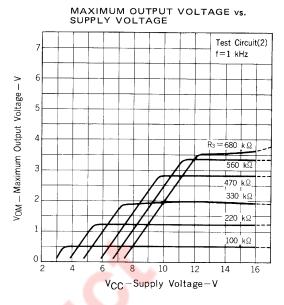


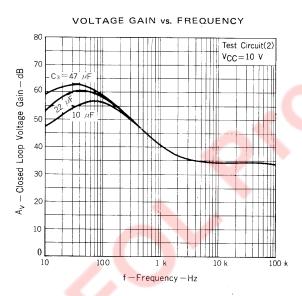


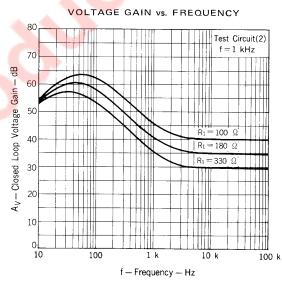


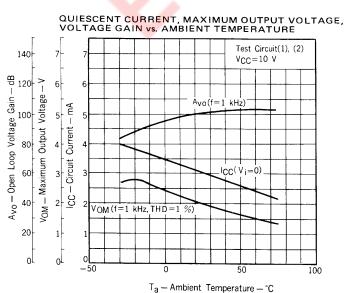


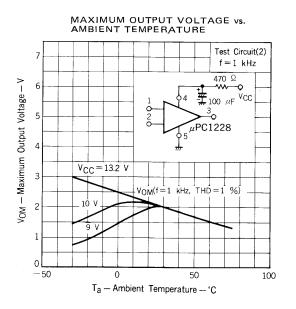




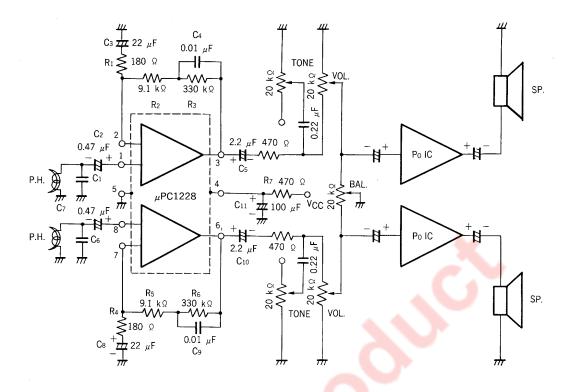




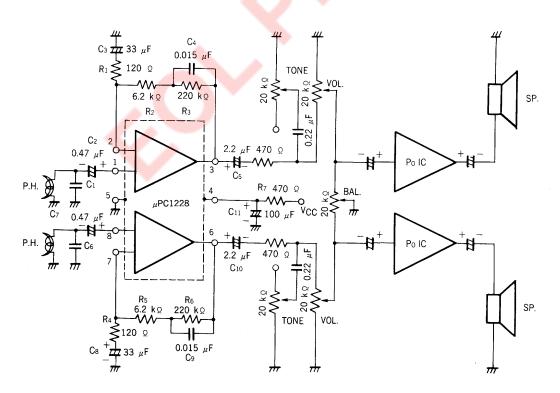




APPLICATION 1 (NAB EQ, $V_{CC} = 8$ to 17 V, $V_{OM} = 2$ V)

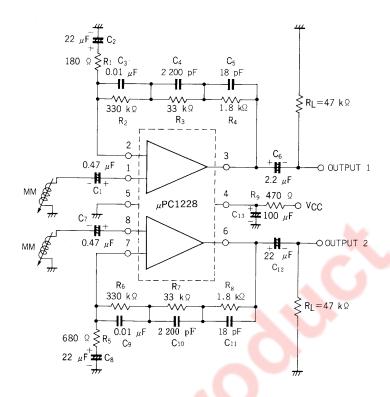


APPLICATION 2 (NAB EQ, $V_{CC} = 6$ to 17 V, $V_{OM} = 1.2$ V)



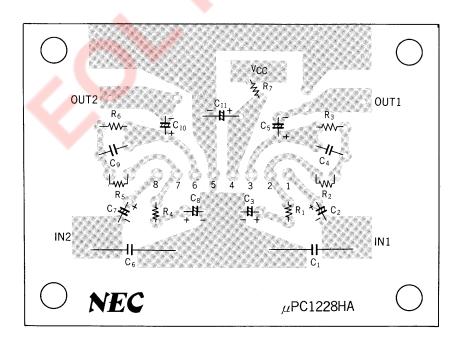
^{*} When supply voltage of pin 4 is down to 6 V, please use TYPICAL APPLICATION 2.

APPLICATION 3 (NAB EQ, V_{CC} = 8 to 18 V, V_{OM} = 2 V)

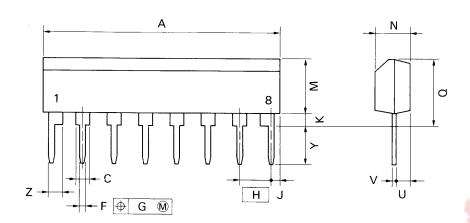


TYPICAL PRINTED CIRCUIT BOARD PATTERN

Copper foil side



8 PIN PLASTIC SLIM SIP



NOTE

Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

| P8H | ۸ ٦ | EAD |
|-----|-----|------|
| гоп | M-2 | .040 |

| ITEM | MILLIMETERS | INCHES |
|------|----------------------|-------------------------|
| Α | 20.32 MAX. | 0.8 MAX. |
| С | 1.1 MIN. | 0.043 MIN. |
| F | 0.5 ^{± 0.1} | 0.02 0.004 |
| G | 0.25 | 0.01 |
| Н | 2.54 | 0.1 |
| J | 1.27 MAX. | 0.05 MAX. |
| К | 0.51 MIN. | 0.02 MIN. |
| М | 5.08 MAX. | 0.2 MAX. |
| N | 2.8 · 0.2 | 0.11 0.009 |
| Q | 5.75 MAX. | 0.227 MAX. |
| U | 1.5 MAX. | 0.059 MAX. |
| V | 0.25 - 0.05 | 0.01 10.004 |
| Υ | 3.2 * 0.5 | 0.126 ^{± 0.02} |
| Z | 1.1 MIN. | 0.043 MIN. |

[MEMO]

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