

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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BIPOLAR DIGITAL INTEGRATED CIRCUITS

μ PB1502GR, 1502GR(1)

1.7 GHz/ 2.0 GHz LOW-POWER TWO-MODULUS PRESCALER DIVIDED-BY-64/65, 128/129

FEATURES

- High toggle frequency – 2.0 GHz: μ PB1502GR(1), 1.7 GHz: μ PB1502GR
- Low power consumption – 6.7 mA TYP. at 3 V
- Operating supply voltage – 2.7 V to 3.3 V
- High input sensitivity – 130 to 220 mV_{P-P}: μ PB1502GR(1), 100 to 320 mV_{P-P}: μ PB1502GR (@50 Ω)
- Equipped with power-save function: 5 μ A (standard) on power-save mode.
- Packaged in 8 pins plastic SOP suitable for surface mounting.

DESCRIPTION

μ PB1502GR and μ PB1502GR(1) are two-modulus prescaler divided by 64/65 or 128/129. This device is designed for mobile communication applications for example 0.8-1.9 GHz cellular and cordless telephones. The ICs operate on low power and therefore are suitable for hand-held, battery-operated systems.

These products are manufactured using NEC's 20 GHz fr NESAT™ III silicon bipolar process. This process uses silicon nitride passivation film and gold metallization wirings. These materials can protect the chips from external pollution and prevent corrosion and migration. Thus, these products have excellent performance, uniformity and reliability.

ORDER INFORMATION

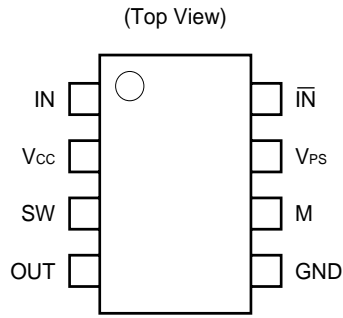
ORDER NUMBER	PACKAGE	SUPPLYING FORM	f _{in} MAX.
μ PB1502GR-E1	8 pin plastic SOP (225 mil)	Embossed tape 12 mm wide. QTY 2.5 k/reel Pin1 is in tape pull-out direction.	1.7 GHz
μ PB1502GR(1)-E1			2.0 GHz

Remarks To order evaluation samples, please contact your local NEC sales office. (Order number: μ PB1502GR, μ PB1502GR(1))

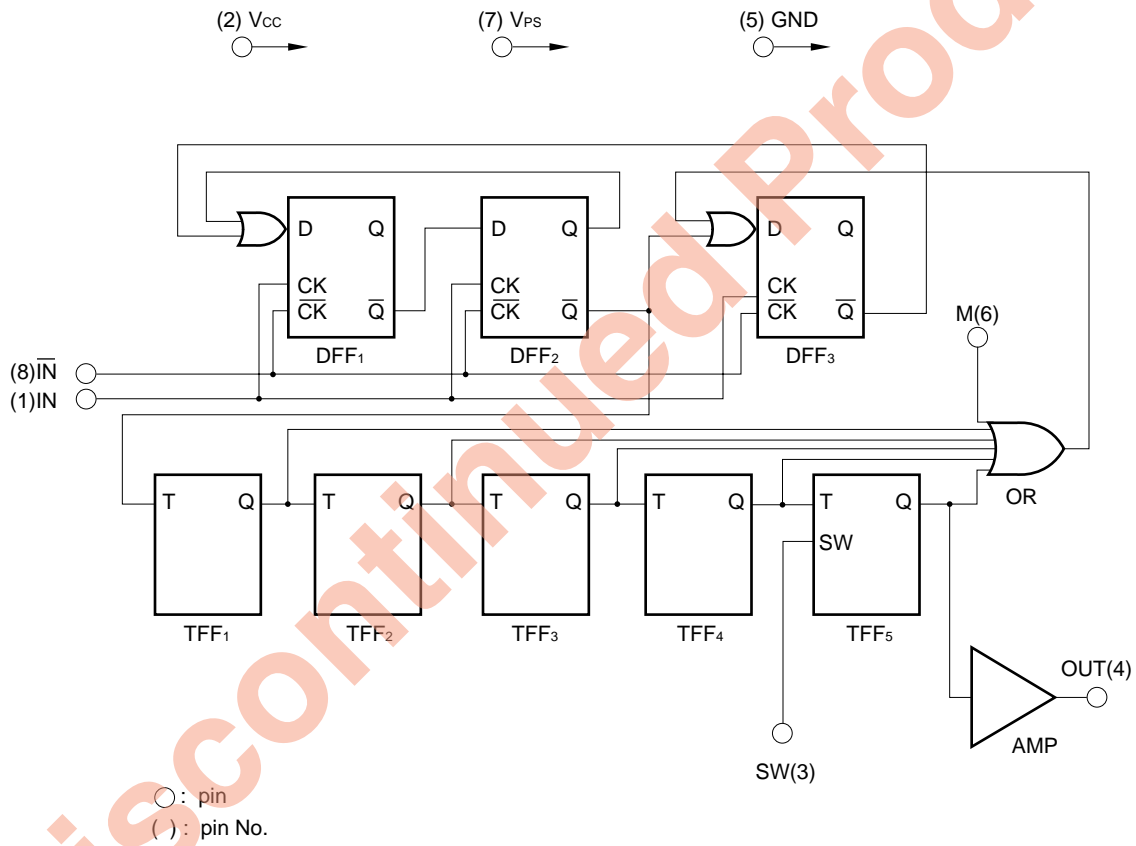
Caution electro-static sensitive devices

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

PIN ASSIGNMENT



INTERNAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT	CONDITION
Supply voltage	V _{CC}	-0.5 to +6	V	T _A = +25 °C
Input voltage	V _{IN}	-0.5 to V _{CC} +0.5	V	T _A = +25 °C
Total power dissipation	P _D	250	mW	Mounted on double sided copper clad 50 × 50 × 1.6 mm epoxy glass PWB (T _A = +85 °C)
Operating temperature	T _{opt}	-40 to +85	°C	
Storage temperature	T _{stg}	-65 to +150	°C	

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	2.7	3.0	3.3	V
Operating temperature	T _{opt}	-40	+25	+85	°C

ELECTRICAL CHARACTERISTICS (T_A = -40 to +85 °C, V_{CC} = 2.7 to 3.3 V)

PARAMETER	SYMBOL	μPB1502GR			μPB1502GR(1)			UNIT	CONDITION
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Response frequency	f _{in}	0.5		1.7	0.5		2.0	GHz	P _{in} = -10 dBm
Circuit current	I _{CC}	3.2	6.7	11.0	3.2	6.7	11.0	mA	V _{PSH} level, No input signal
Input power sensitivity 1	P _{in1}	-11	—	0	-11	—	0	dBm	f _{in} = 0.5 to 0.8 GHz
Input power sensitivity 2	P _{in2}	-15	—	0	-15	—	0	dBm	f _{in} = 0.8 to 1.5 GHz
Input power sensitivity 3	P _{in3}	-15	—	-6	-15	—	-1	dBm	f _{in} = 1.5 to 1.7 GHz
Input power sensitivity 4	P _{in4}	—	—	—	-14	—	-9	dBm	f _{in} = 1.7 to 2.0 GHz
Modulus control input high (M)	V _{IH1}	2.5	—	—	2.5	—	—	V	
Modulus control input low (M)	V _{IL1}	—	—	0.8	—	—	0.8	V	
Divide ratio control input high (SW)	V _{IH2}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V	
Divide ratio control input low (SW)	V _{IL2}	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	V	
Output voltage swing	V _{OUT}	0.8	—	—	0.8	—	—	V _{P-P}	C _L = 8 pF
Modulus set up time	t _{set}	—	11	—	—	11	—	ns	f _{in} MAX.
Power-save input high	V _{PSH}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V	
Power-save input low	V _{inL}	—	—	0.8	—	—	0.8	V	*
Circuit current on power-save mode	I _{PS}	—	5	20	—	5	20	μA	V _{PSL} level *

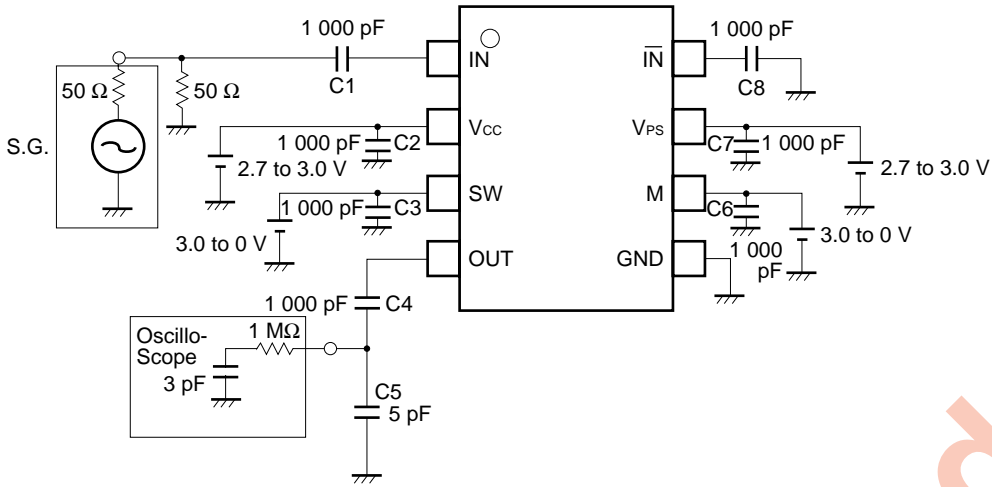
* Standard reference value on power-save mode.

PIN DESCRIPTIONS

Pin No.	Symbol	Assignment	Functions and Explanation															
1	IN	Frequency input pin	Input frequency from an external VCO output. Must be coupled with capacitor (e.g. 1 000 pF) for DC cut.															
2	Vcc	Power supply pin	Supply voltage 3.0 ± 0.3 V for operation. Must be connected bypass capacitor (e.g. 1 000 pF) to minimize ground impedance.															
3	SW	Divided ratio control input pin	Divided ratio and modulus control can be governed by following input data to these pins.															
6	M	Modulus control input pin																
			<table border="1"> <thead> <tr> <th colspan="2"></th> <th colspan="2">M</th> </tr> <tr> <th colspan="2"></th> <th>H</th> <th>L</th> </tr> </thead> <tbody> <tr> <th rowspan="2">SW</th> <th>H</th> <td>1/64</td> <td>1/65</td> </tr> <tr> <th>L</th> <td>1/128</td> <td>1/129</td> </tr> </tbody> </table>			M				H	L	SW	H	1/64	1/65	L	1/128	1/129
		M																
		H	L															
SW	H	1/64	1/65															
	L	1/128	1/129															
4	OUT	Divided frequency output pin	This frequency output can be interfaced to CMOS PLL. Must be coupled with capacitor (e.g. 1 000 pF) for DC cut.															
5	GND	Ground pin	Must be connected to the system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. (Track length should be kept as short as possible).															
7	Vps	Power-save function pin	ON/OFF-operation control can be governed by following input data to this pin.															
			<table border="1"> <thead> <tr> <th colspan="2"></th> <th>Operation</th> </tr> </thead> <tbody> <tr> <th rowspan="2">Vps</th> <th>H</th> <td>ON</td> </tr> <tr> <th>L</th> <td>OFF</td> </tr> </tbody> </table>			Operation	Vps	H	ON	L	OFF							
		Operation																
Vps	H	ON																
	L	OFF																
8	$\overline{\text{IN}}$	Frequency-input bypass pin	Must be connected bypass capacitor (e.g. 1 000 pF) to minimize ground impedance.															

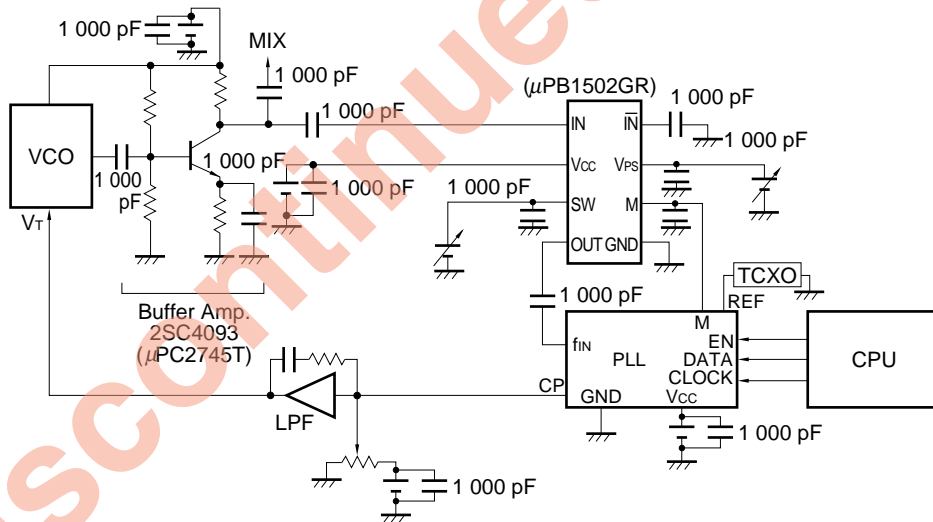
Discontinued Product

TEST CIRCUIT



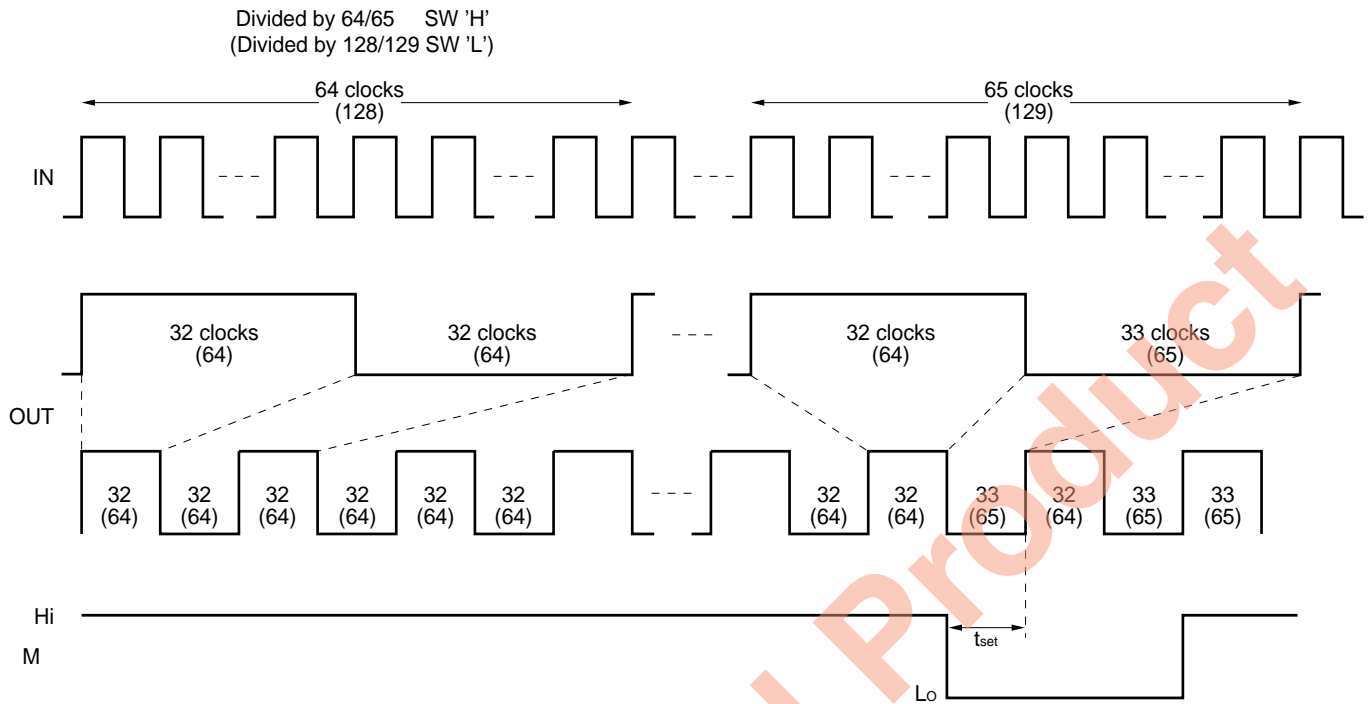
		M	
		H	L
SW	H	1/64	1/65
	L	1/128	1/129

APPLICATION CIRCUIT FOR REFERENCE



The application circuits and their parameters are for references only and are not intended for use in actual design-in's. To know the real application circuits, please refer to PLL synthesizer LSI's documentations (e.g. μ PD3160GS).

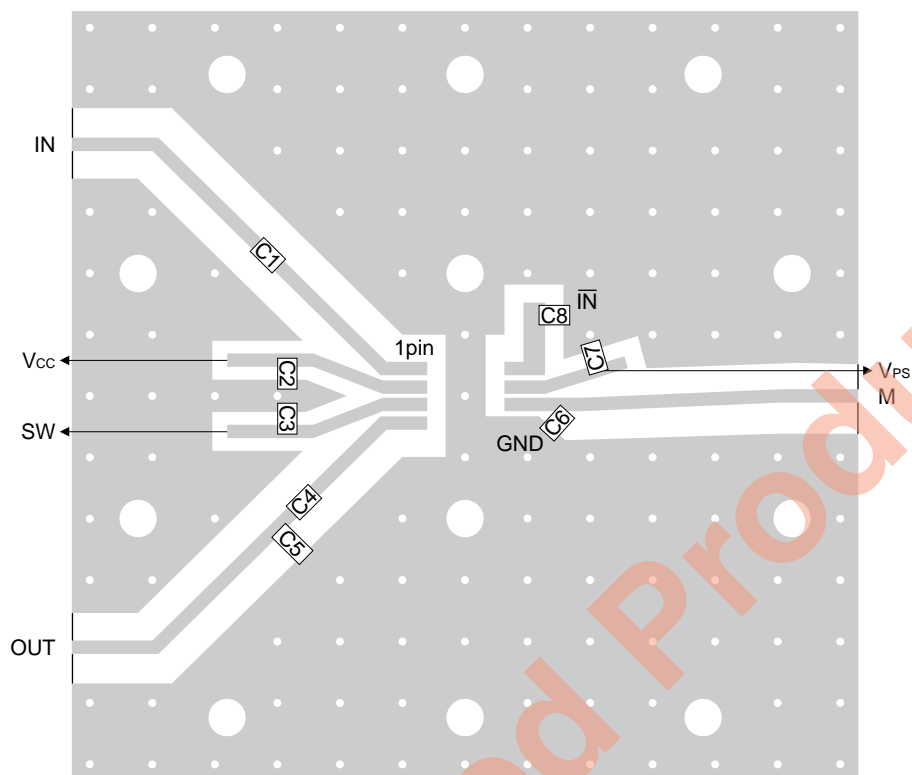
TIMING DIAGRAM



t_{set} = The minimum time required between 'Modulus Control' going low and next output rising edge, in order to ensure a P+1 modulus change.

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ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



Component List

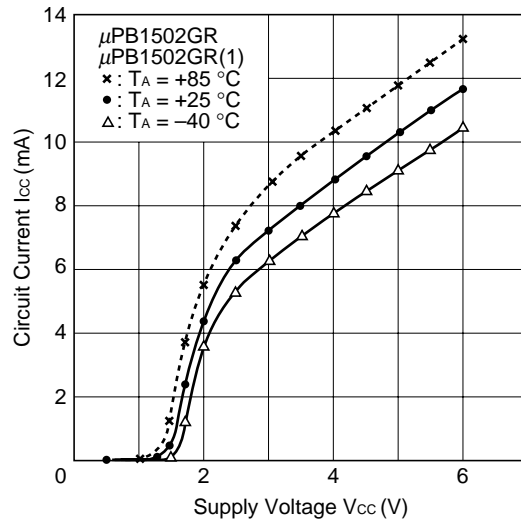
No.	Value
C _{1 to 4}	1 000 pF
C ₅	8 pF
C _{6 to 8}	1 000 pF

Note

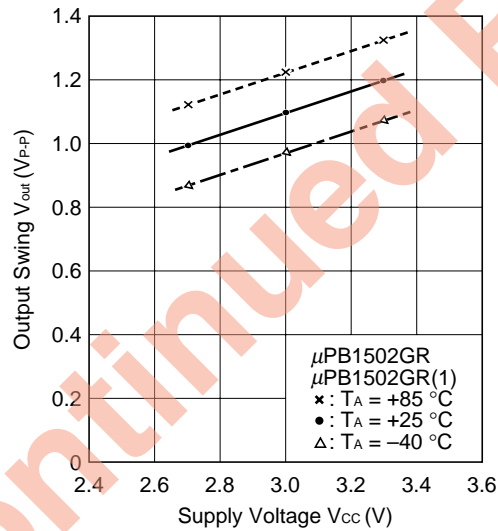
- (1) 50 × 50 × 0.4 mm double copper clad polyimide board.
- (2) Back side: GND pattern
- (3) Solder plated on pattern
- (4) ◦ ○: Through holes

TYPICAL CHARACTERISTICS ($T_A = +25\text{ }^\circ\text{C}$)

— μ PB1502GR, μ PB1502GR(1) in common —
CIRCUIT CURRENT vs. SUPPLY VOLTAGE

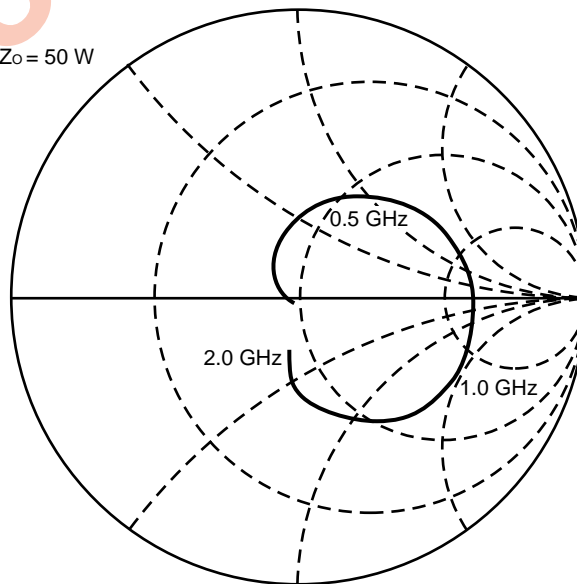


OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE



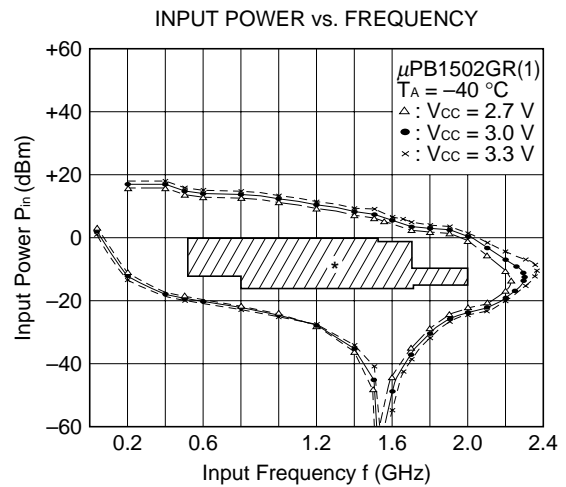
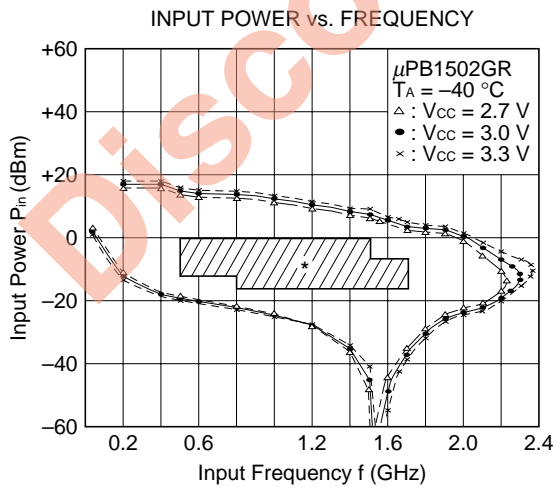
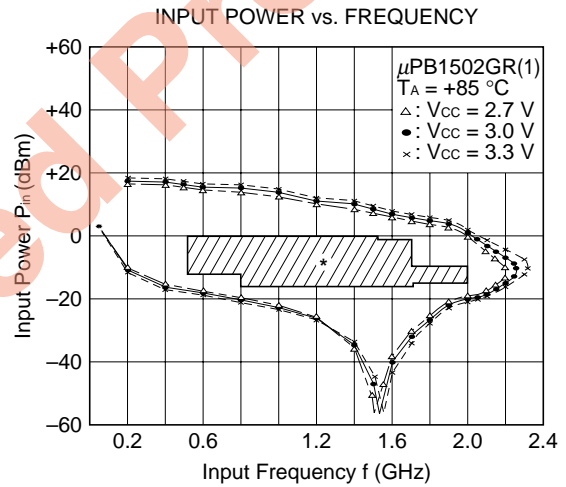
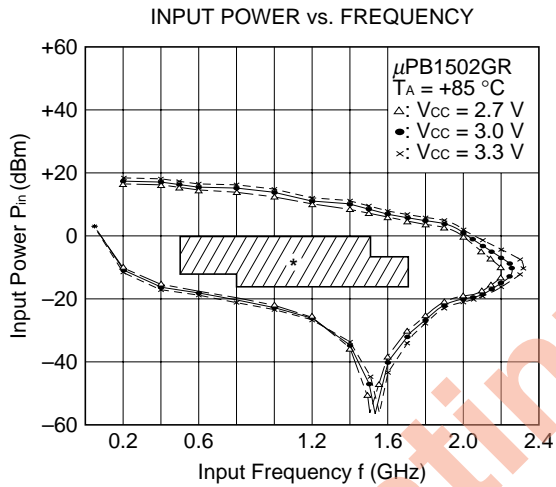
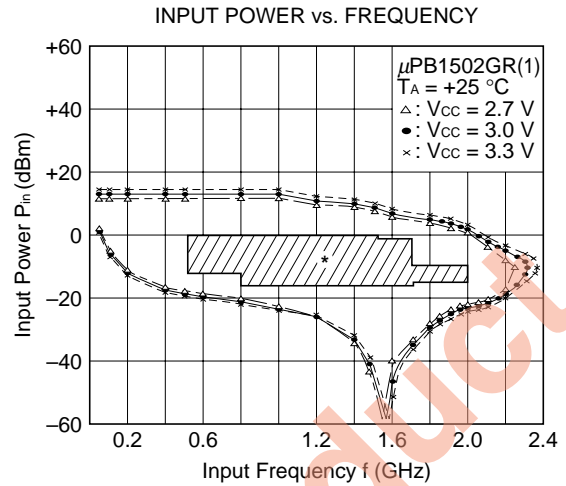
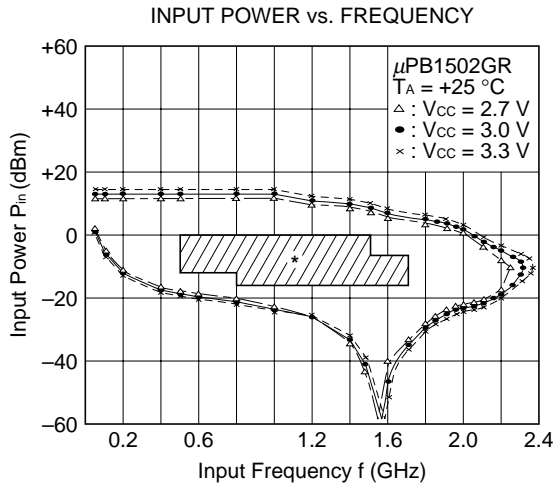
S_{11} vs. f

$V_{CC} = 3.0\text{ V}$, $I_{CC} = 6.7\text{ mA}$, $Z_o = 50\text{ } \Omega$



— μ PB1502GR — <Left line>

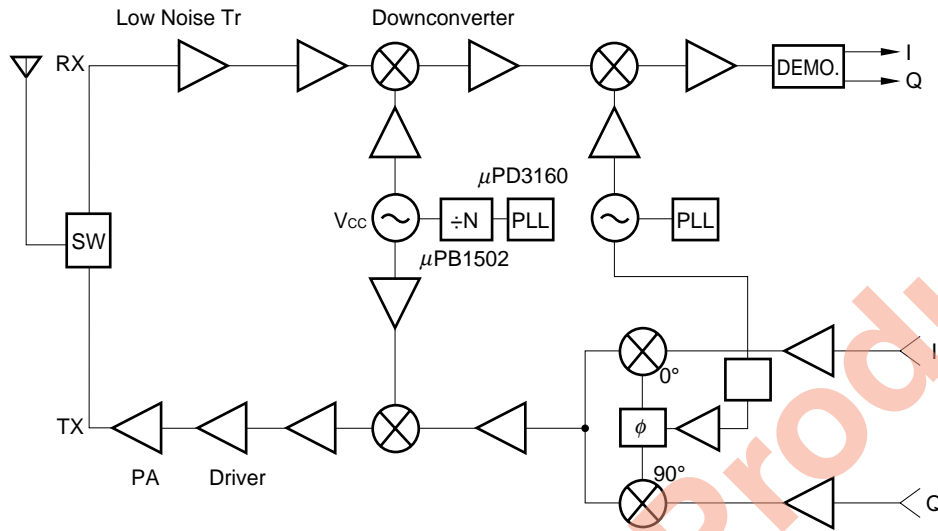
— μ PB1502GR(1) — <Right line>



* Guaranteed Operating Window

TYPICAL SYSTEM APPLICATION

Digital Cellular System Block Diagram



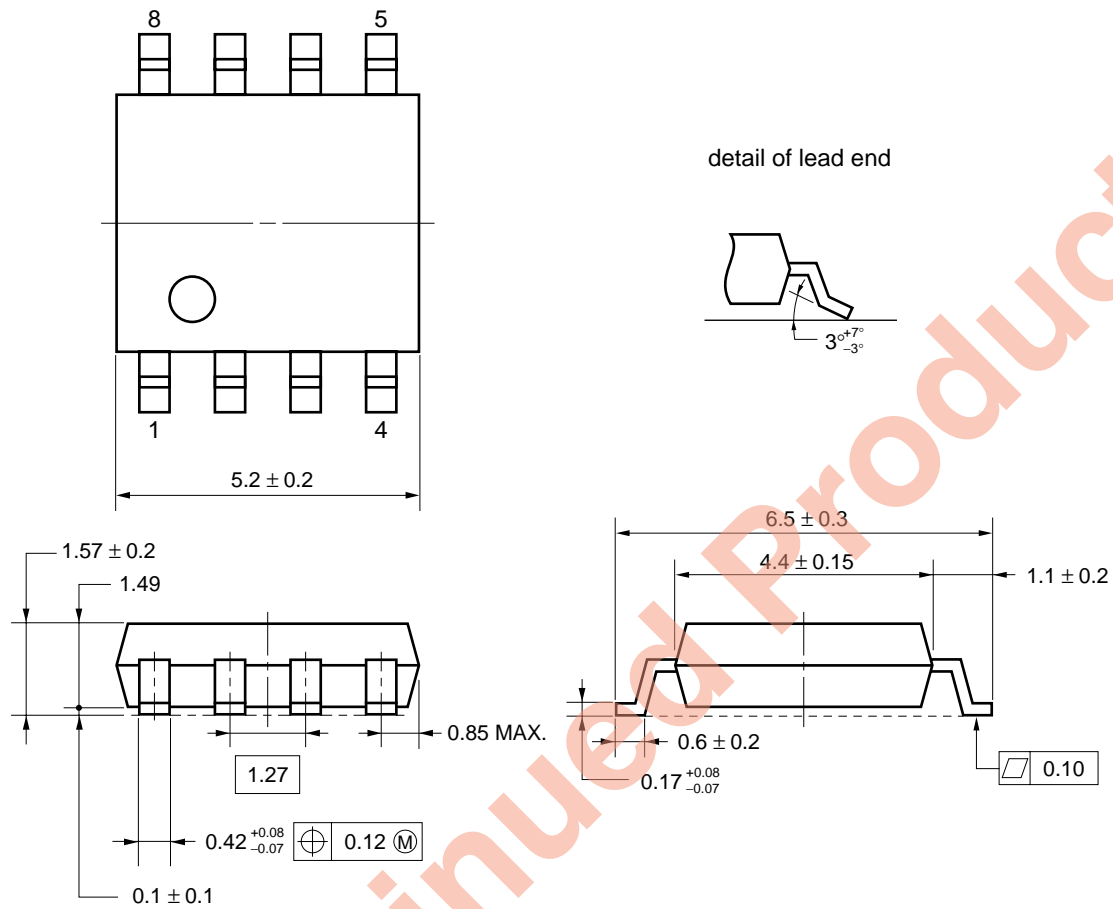
Other applicable systems

1.9 GHz digital cordless telephone, hand-held radio.

Discontinued Product

PACKAGE DIMENSIONS

★ 8 PIN PLASTIC SOP (225 mil) (UNIT: mm)



NOTE Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

NOTE ON CORRECT USE

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent abnormal operation).
- (3) Keep the wiring length of the ground pins as short as possible.
- (4) Connect a bypass capacitor (e.g. 1 000 pF) to the Vcc pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

μPB1502GR, 1502GR(1)

Soldering method	Soldering conditions	Recommended condition symbol
Infrared ray reflow	Package peak temperature: 235 °C, Hour: within 30 s. (more than 210 °C), Time: 3 times, Limited days: no.*	IR35-00-3
VPS	Package peak temperature: 215 °C, Hour: within 40 s. (more than 200 °C), Time: 3 times, Limited days: no.*	VP15-00-3
Wave soldering	Soldering tub temperature: less than 260 °C, Hour: within 10 s. Time: 1 time, Limited days: no.	WS60-00-1
Pin part heating	Pin area temperature: less than 300 °C, Hour: within 3 s./pin Limited days: no.*	

*: It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 % RH.

Note 1. The combined use of soldering method is to be avoided (However, except the pin area heating method).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

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ATTENTION

OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

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 - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
 - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.
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