To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

DATA SHEET

MOS FIELD EFFECT TRANSISTOR

μPA2790GR

SWITCHING
N- AND P-CHANNEL POWER MOS FET

DESCRIPTION

The μPA2790GR is N- and P-channel MOS Field Effect Transistors designed for Motor Drive application.

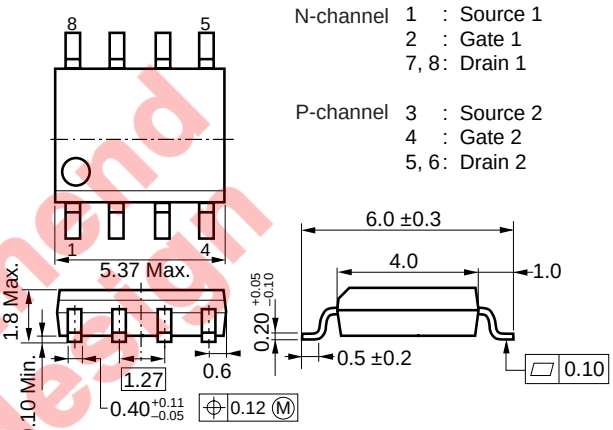
FEATURES

- Low on-state resistance
  - N-channel $R_{DS(on)1}$ = 28 mΩ MAX. (V_{GS} = 10 V, I_D = 3 A)
  - $R_{DS(on)2}$ = 40 mΩ MAX. (V_{GS} = 4.5 V, I_D = 3 A)
  - P-channel $R_{DS(on)1}$ = 60 mΩ MAX. (V_{GS} = –10 V, I_D = –3 A)
  - $R_{DS(on)2}$ = 80 mΩ MAX. (V_{GS} = –4.5 V, I_D = –3 A)
- Low input capacitance
  - N-channel C_{iss} = 500 pF TYP.
  - P-channel C_{iss} = 460 pF TYP.
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

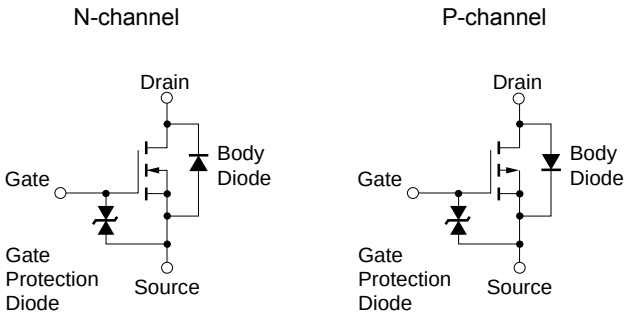
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2790GR	Power SOP8

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUITS



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Document No. G16954EJ3V0DS00 (3rd edition)
Date Published September 2006 NS CP(K)
Printed in Japan

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C. All terminals are connected.)

PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	−30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	∓20	V
Drain Current (DC)	$I_{D(DC)}$	±6	∓6	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±24	∓24	A
Total Power Dissipation (1 unit) Note2	P_T	1.7		W
Total Power Dissipation (2 units) Note2	P_T	2.0		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	−55 to +150		°C
Single Avalanche Current Note3	I_{AS}	6	−6	A
Single Avalanche Energy Note3	E_{AS}	3.6	3.6	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on ceramic substrate of 2000 mm^2 x 1.6 mm

3. Starting T_{ch} = 25°C, $V_{DD} = \frac{1}{2} \times V_{DSS}$, R_G = 25 Ω, L = 100 μH, $V_{GS} = V_{GSS} \rightarrow 0$ V

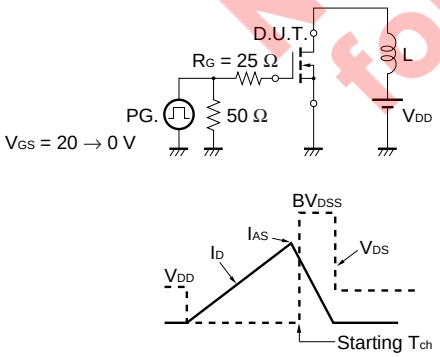
ELECTRICAL CHARACTERISTICS (T_A = 25°C. All terminals are connected.)

N-channel

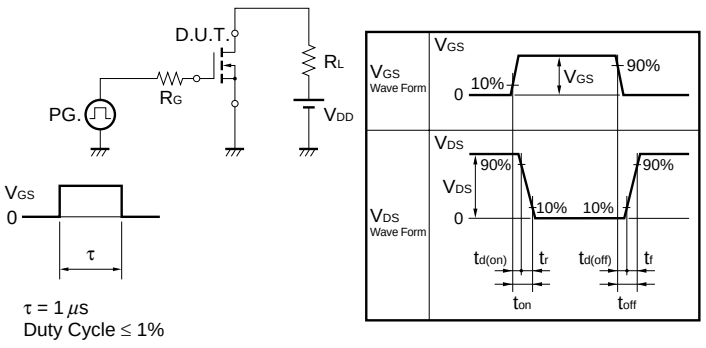
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5		2.5	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 3 A	2			S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 3 A		21	28	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 3 A		28	40	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.0 V, I_D = 3 A		34	53	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		500		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		135		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		77		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 3 A		9.2		ns
Rise Time	t_r	V_{GS} = 10 V		8.8		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		28		ns
Fall Time	t_f			7.4		ns
Total Gate Charge	Q_G	I_D = 6 A		12.6		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 24 V		1.7		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 10 V		3.8		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 6 A, V_{GS} = 0 V		0.85		V
Reverse Recovery Time	t_{rr}	I_F = 6 A, V_{GS} = 0 V		18		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		11		nC

Note Pulsed

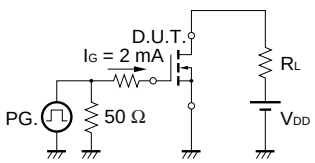
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

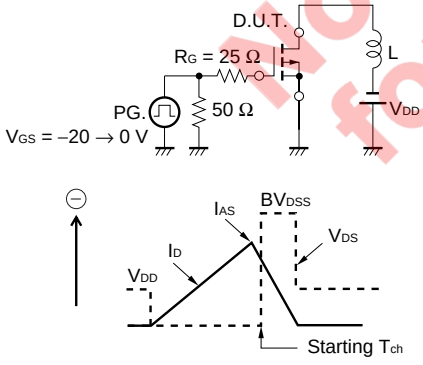


P-channel

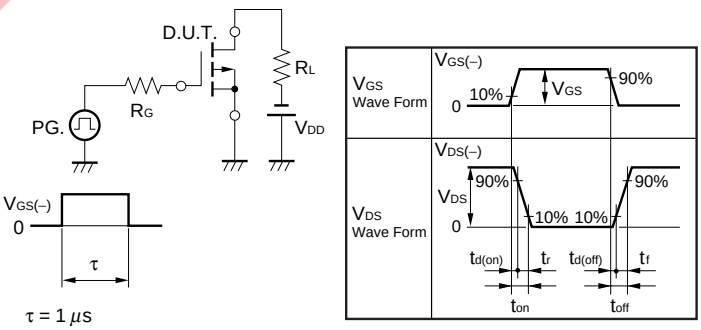
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓16 V, V_{DS} = 0 V			∓10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0		–2.5	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –3 A	2			S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –3 A		43	60	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.5 V, I_D = –3 A		58	80	mΩ
	$R_{DS(on)3}$	V_{GS} = –4.0 V, I_D = –3 A		65	110	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		460		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		130		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		77		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –15 V, I_D = –3 A		8.5		ns
Rise Time	t_r	V_{GS} = –10 V		4.8		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		42		ns
Fall Time	t_f			19		ns
Total Gate Charge	Q_G	I_D = –6 A		11		nC
Gate to Source Charge	Q_{GS}	V_{DD} = –24 V		1.7		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = –10 V		3.3		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 6 A, V_{GS} = 0 V		0.92		V
Reverse Recovery Time	t_{rr}	I_F = 6 A, V_{GS} = 0 V		21		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		12		nC

Note Pulsed

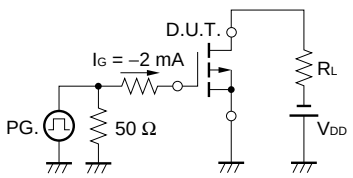
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



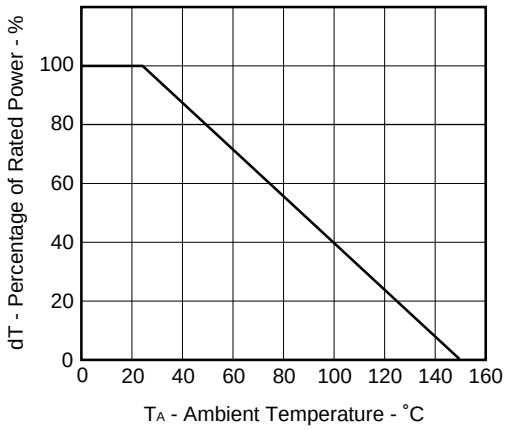
TEST CIRCUIT 3 GATE CHARGE



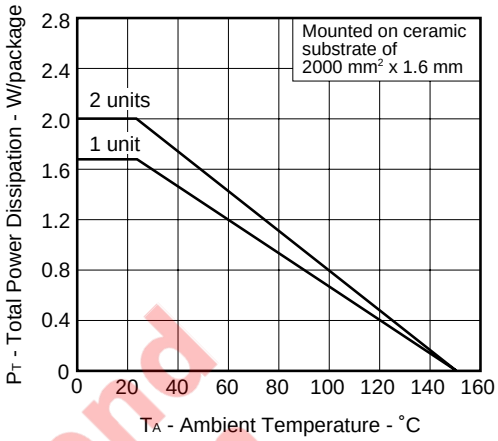
TYPICAL CHARACTERISTICS (T_A = 25°C)

(1) N-channel

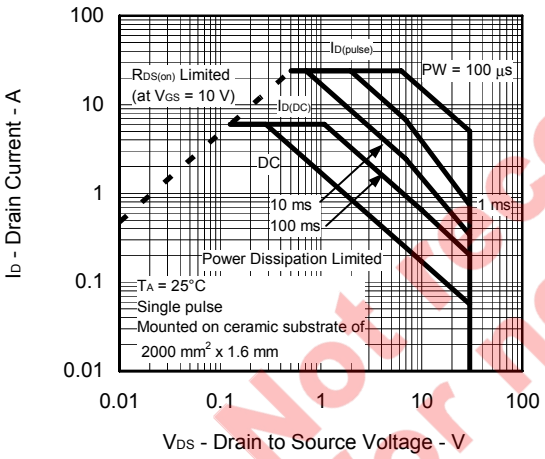
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



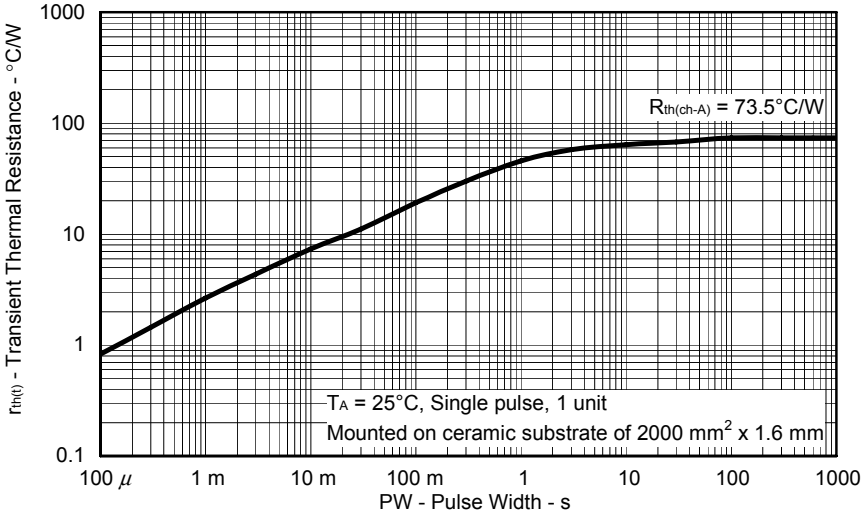
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



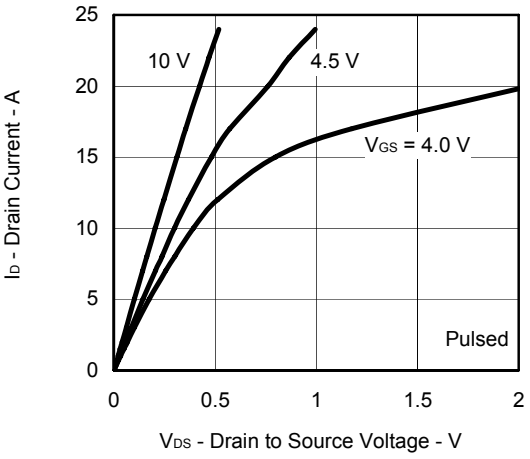
FORWARD BIAS SAFE OPERATING AREA



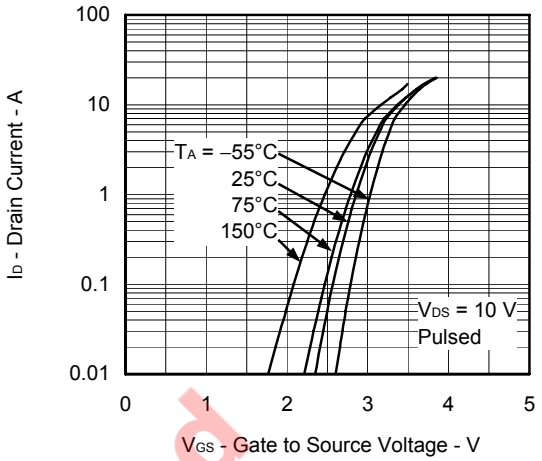
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



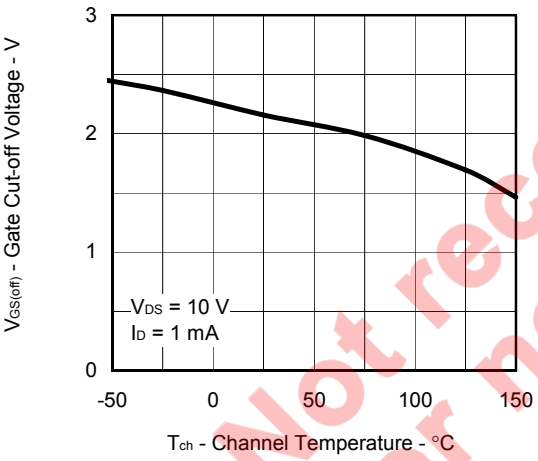
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



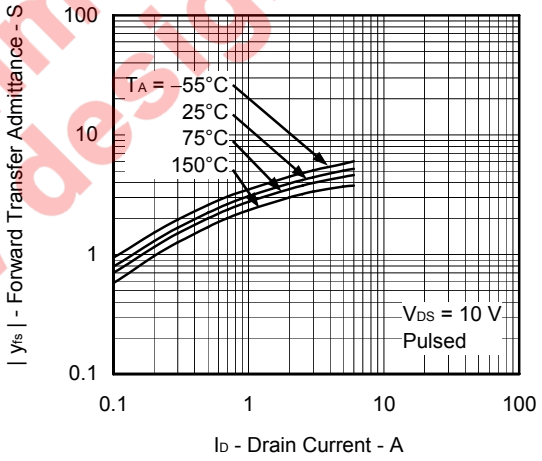
FORWARD TRANSFER CHARACTERISTICS



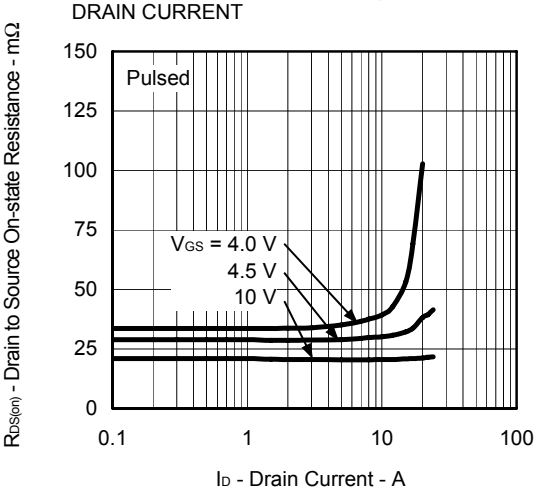
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



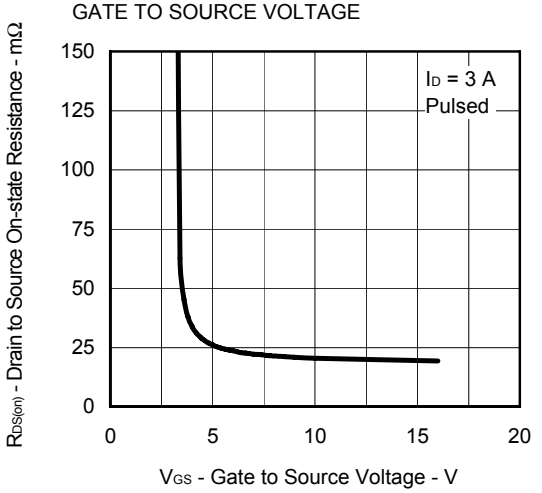
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



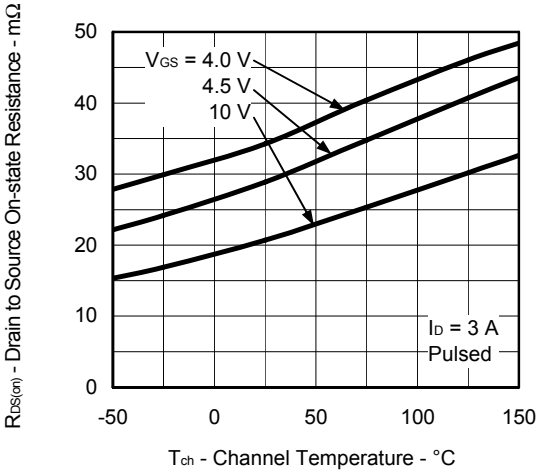
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



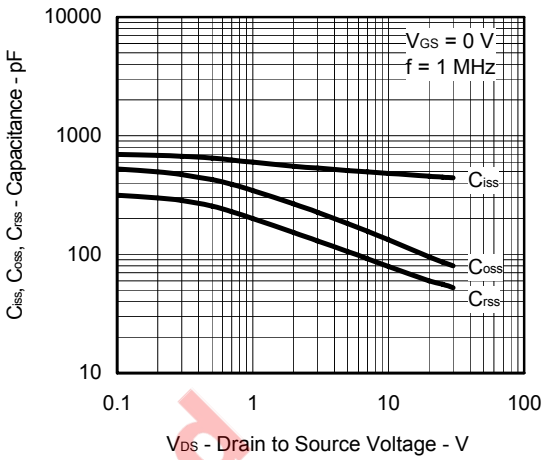
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



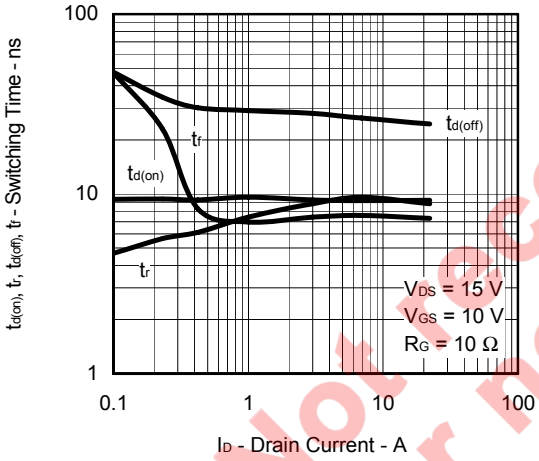
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



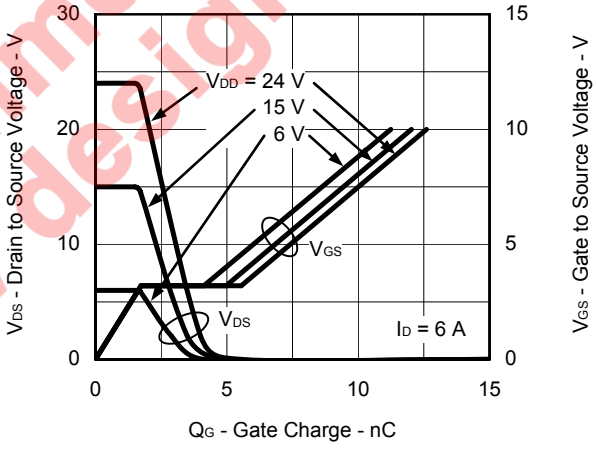
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



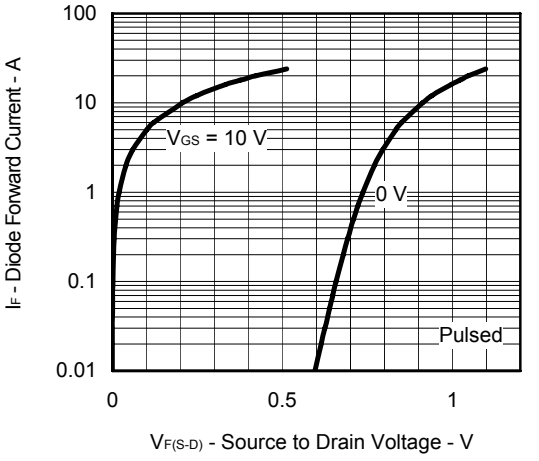
SWITCHING CHARACTERISTICS



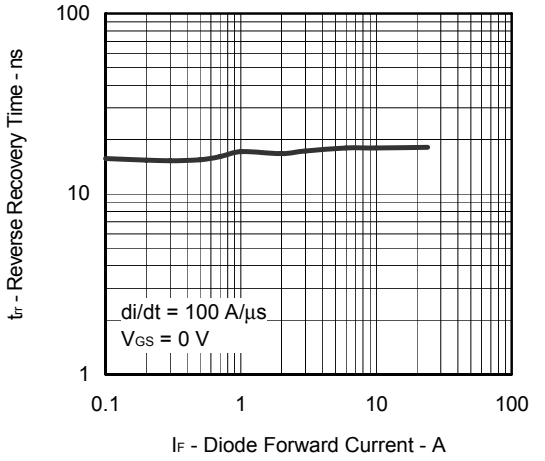
<R> DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

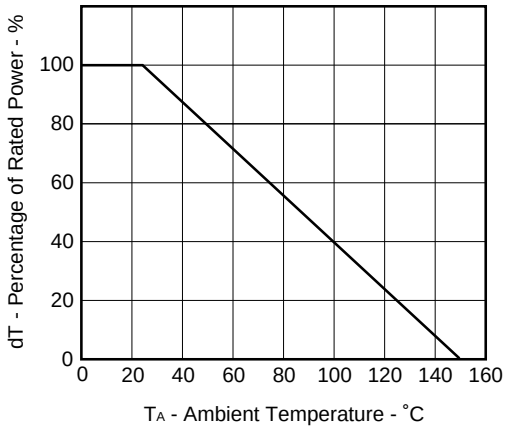


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

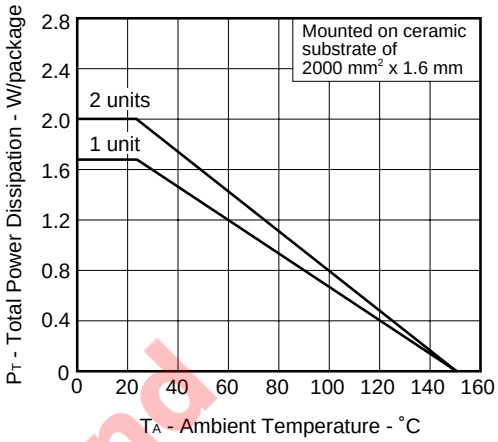


(2) P-channel

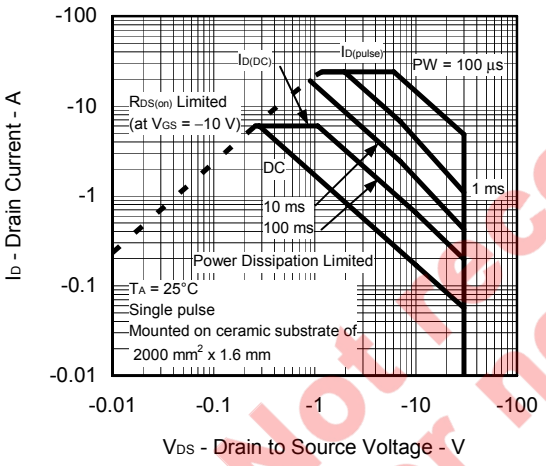
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



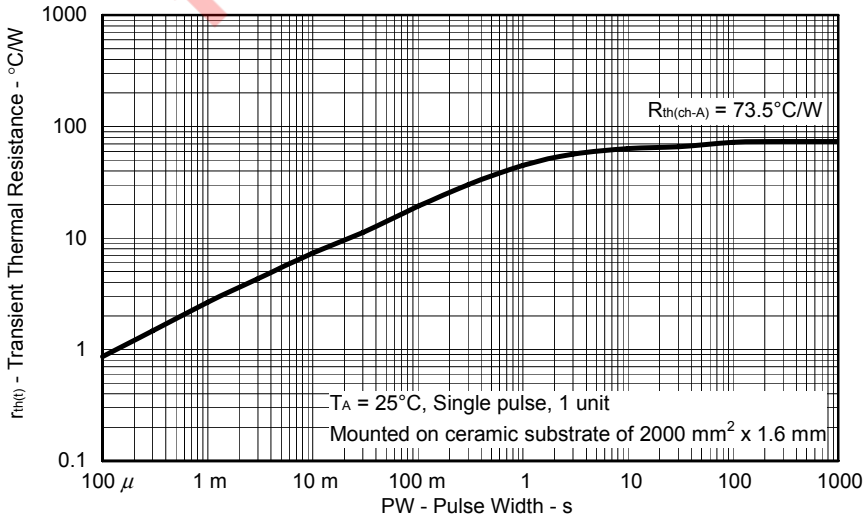
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



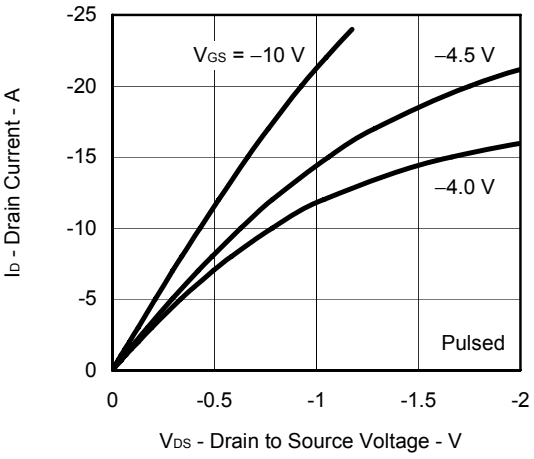
FORWARD BIAS SAFE OPERATING AREA



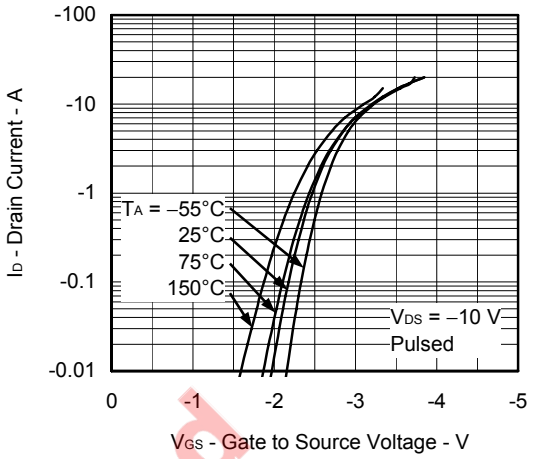
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



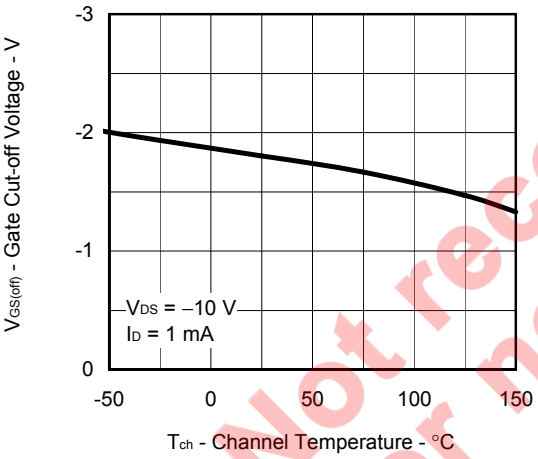
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



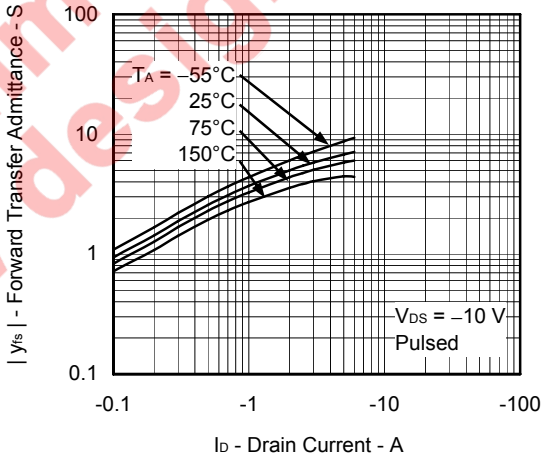
FORWARD TRANSFER CHARACTERISTICS



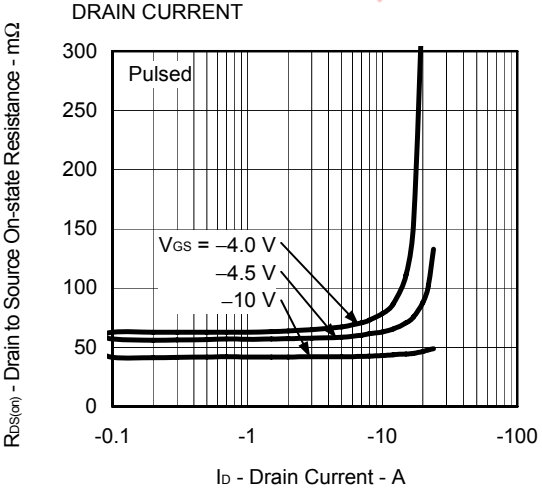
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



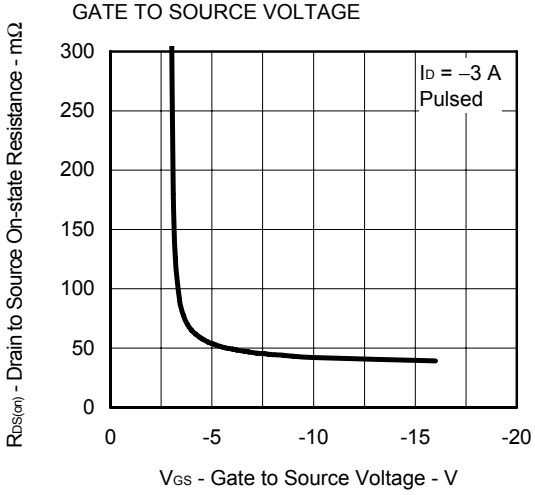
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



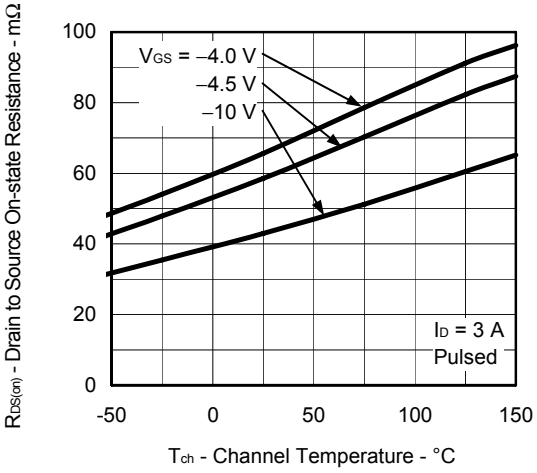
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



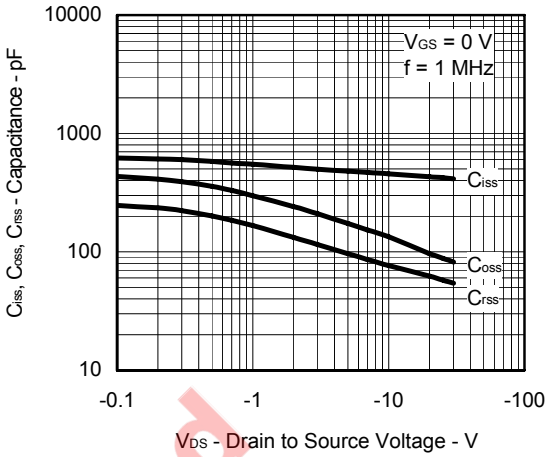
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



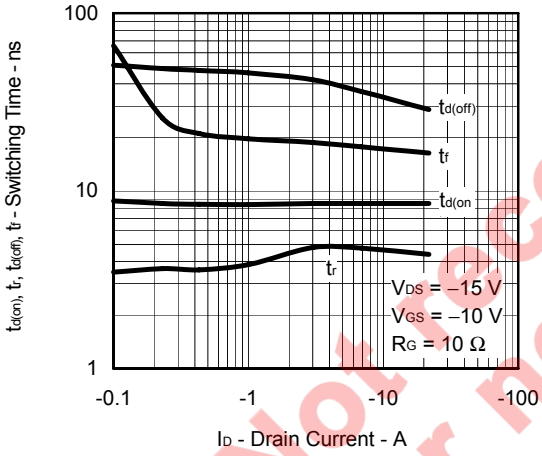
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



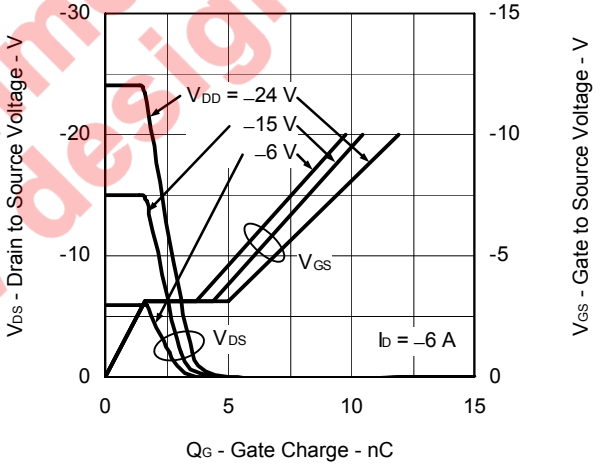
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



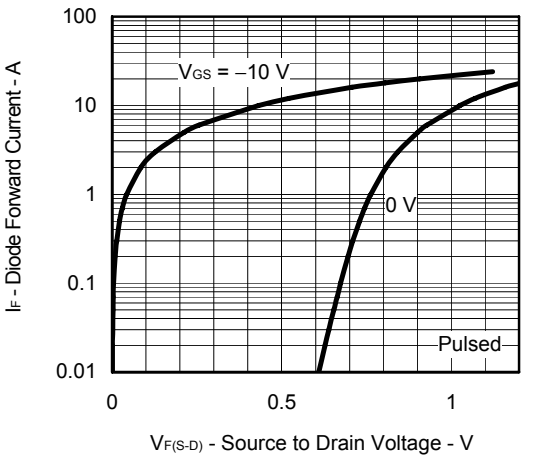
SWITCHING CHARACTERISTICS



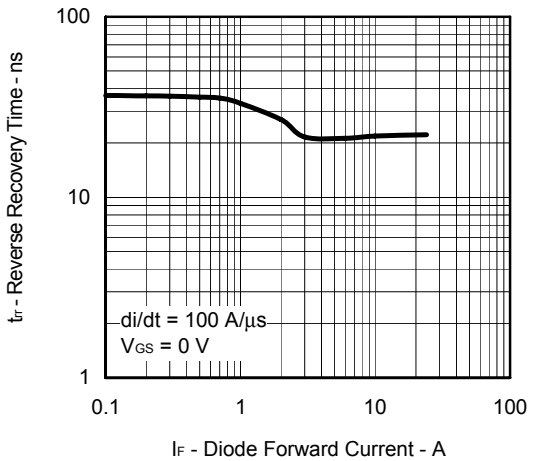
<R> DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



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