

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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**Phase-out/Discontinued**

**μPA1520B**

**N-CHANNEL POWER MOS FET ARRAY  
SWITCHING USE**

**DESCRIPTION**

The μPA1520B is N-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

**FEATURES**

- 4 V driving is possible
- Large Current and Low On-state Resistance  
 $I_{D(DC)} = \pm 2.0$  A  
 $R_{DS(on) 1} \leq 0.17 \Omega$  MAX. ( $V_{GS} = 10$  V,  $I_D = 1$  A)  
 $R_{DS(on) 1} \leq 0.25 \Omega$  MAX. ( $V_{GS} = 4$  V,  $I_D = 1$  A)
- Low Input Capacitance  $C_{iss} = 220$  pF TYP.

**ORDERING INFORMATION**

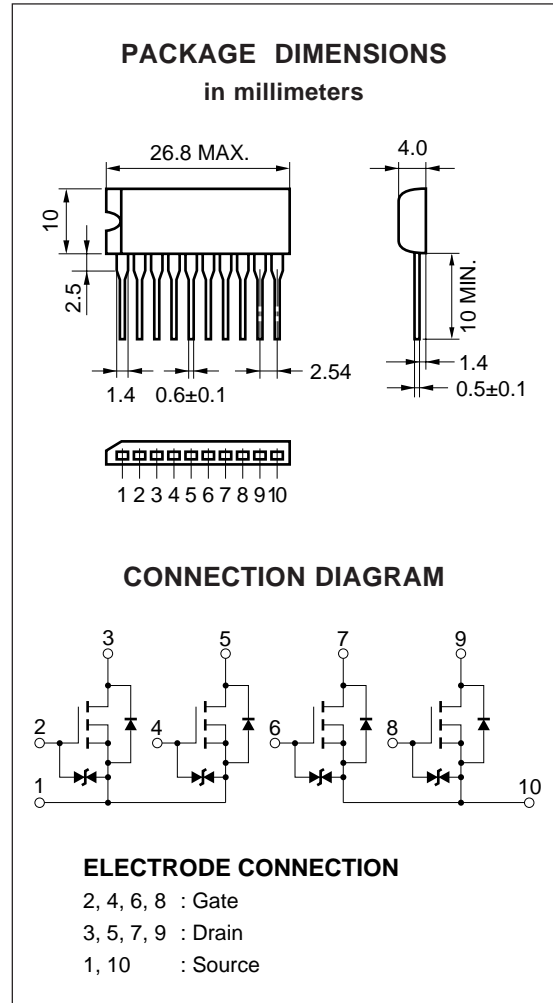
Type Number	Package
μPA1520BH	10 Pin SIP

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C)**

Drain to Source Voltage	$V_{DSS}$ <b>Note 1</b>	30	V
Gate to Source Voltage	$V_{GSS}$ <b>Note 2</b>	±20	V
Drain Current (DC)	$I_{D(DC)}$	±2.0	A/unit
Drain Current (pulse)	$I_{D(pulse)}$ <b>Note 3</b>	±8.0	A/unit
Total Power Dissipation	$P_{T1}$ <b>Note 4</b>	28	W
Total Power Dissipation	$P_{T2}$ <b>Note 5</b>	3.5	W
Channel Temperature	$T_{CH}$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C

- Notes**
- $V_{GS} = 0$
  - $V_{DS} = 0$
  - $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1 \%$
  - 4 circuits,  $T_C = 25 \text{ °C}$
  - 4 circuits,  $T_A = 25 \text{ °C}$

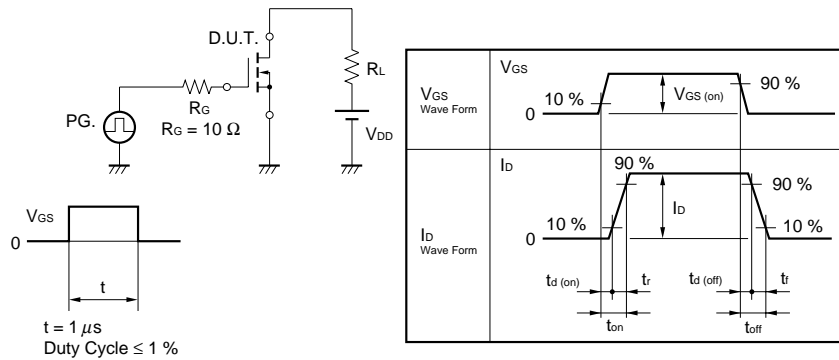
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.



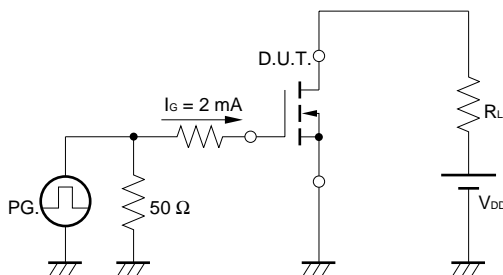
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0			±10	μA
Gate Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.0 mA	1.0		2.0	V
Forward Transfer Admittance	Y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.0 A	1.0			S
Drain to Source On-State Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.0 A		0.10	0.17	Ω
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 1.0 A		0.13	0.25	Ω
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0, f = 1.0 MHz		220		pF
Output Capacitance	C <sub>oss</sub>			220		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			90		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 1.0 A, V <sub>GS</sub> = 10 V, V <sub>DD</sub> ≅ 15 V, R <sub>L</sub> = 15 Ω		27		ns
Rise Time	t <sub>r</sub>			125		ns
Turn-off Delay Time	t <sub>d(off)</sub>			590		ns
Fall Time	t <sub>f</sub>			500		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.0 A, V <sub>DD</sub> = 24 V		14		nC
Gate to Source Charge	Q <sub>GS</sub>			2		nC
Gate to Drain Charge	Q <sub>GD</sub>			5.5		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 2.0 A, V <sub>GS</sub> = 0		1.0		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.0 A, V <sub>GS</sub> = 0, di/dt = 50 A/μs		640		ns
Reverse Recovery Charge	Q <sub>rr</sub>			3.4		μC

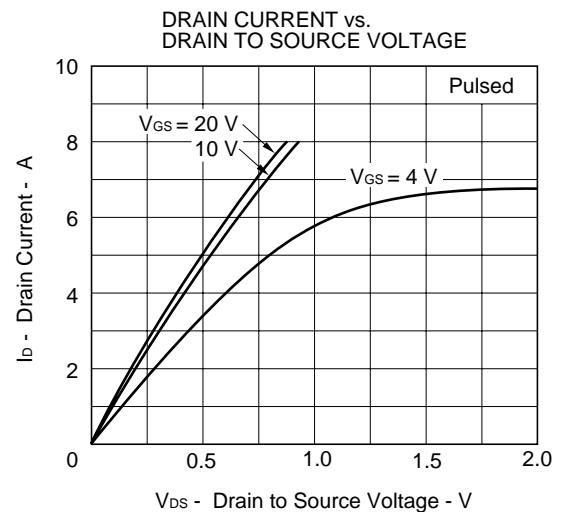
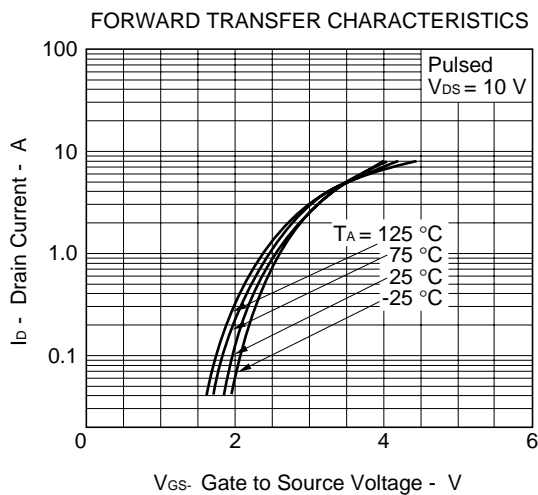
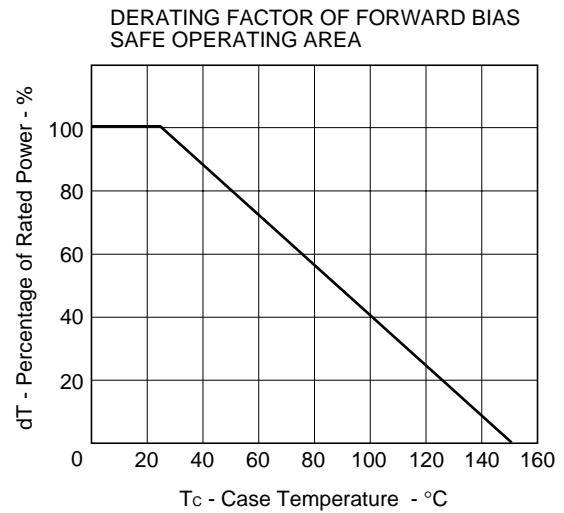
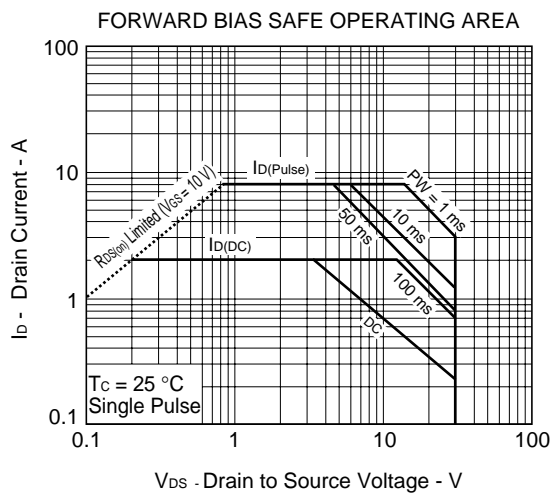
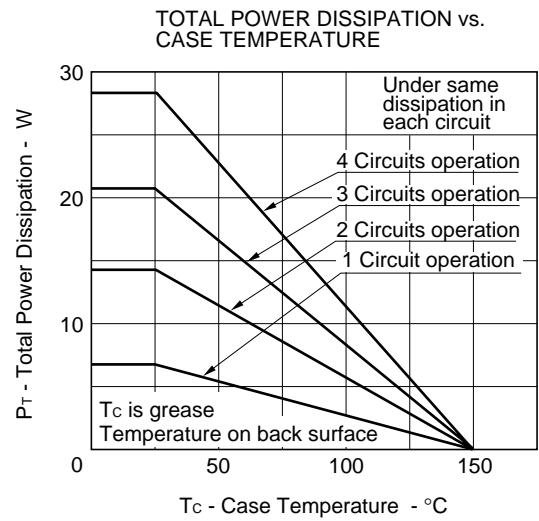
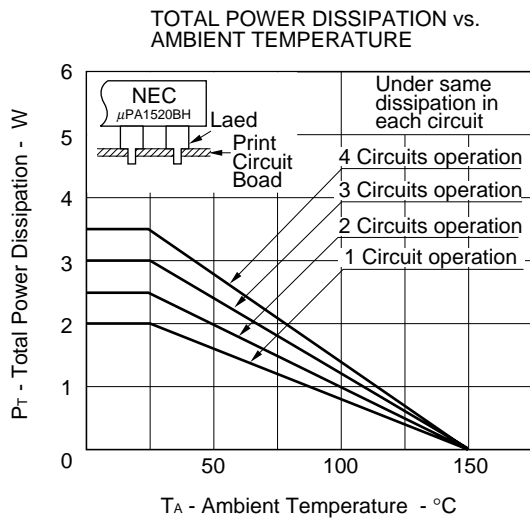
**Test Circuit 1 Switching Time**



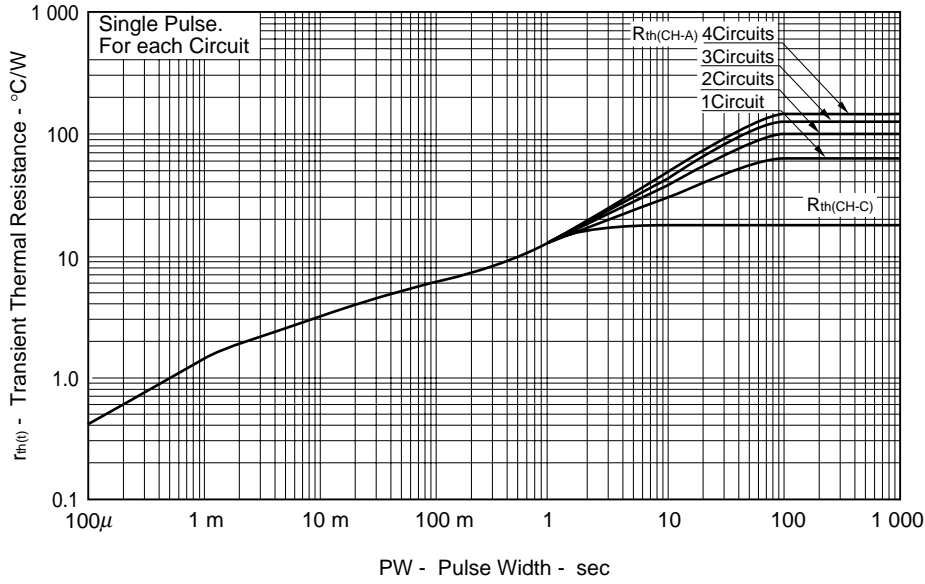
**Test Circuit 2 Gate Charge**



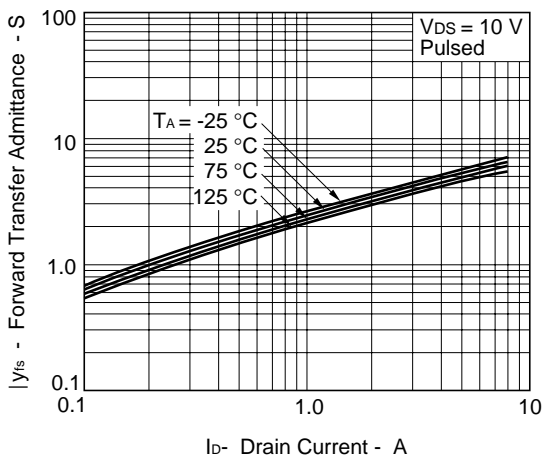
CHARACTERISTICS ( $T_A = 25\text{ }^\circ\text{C}$ )



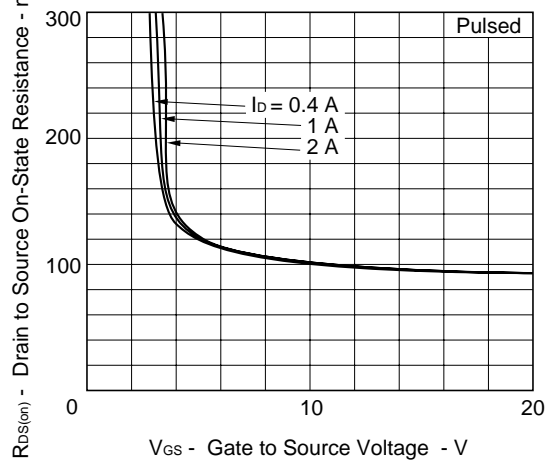
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



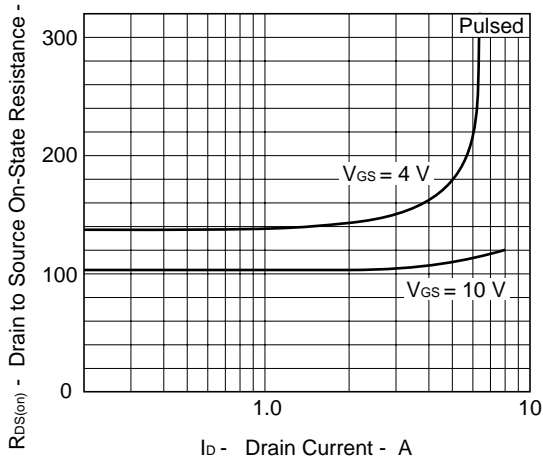
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



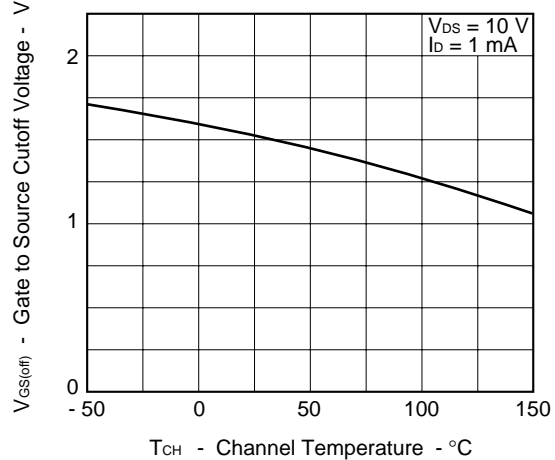
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

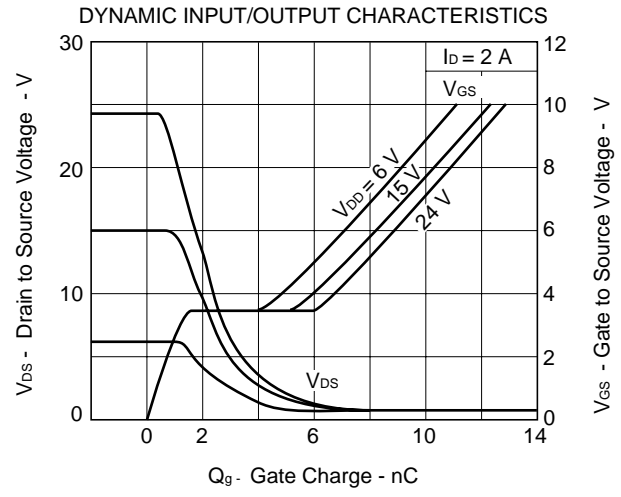
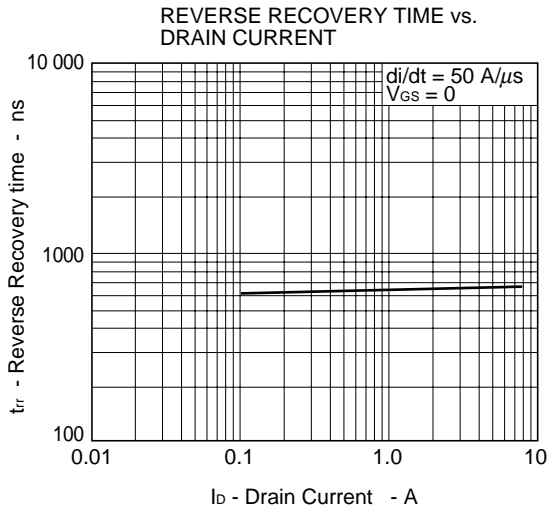
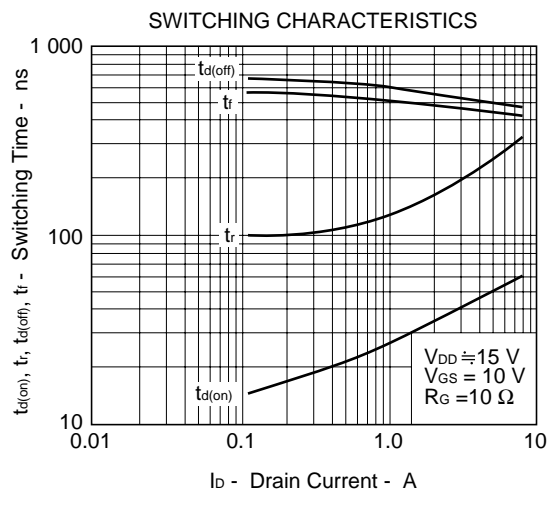
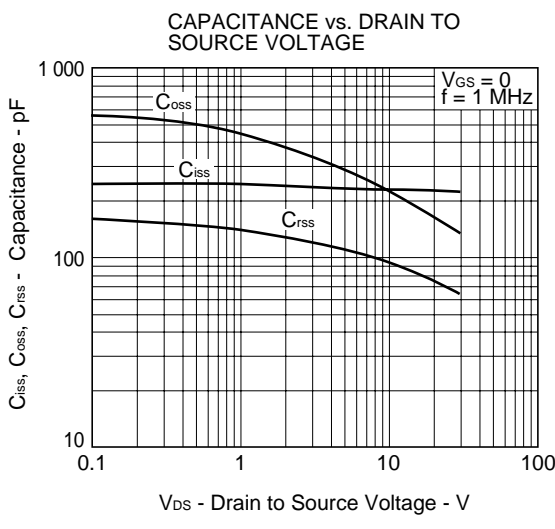
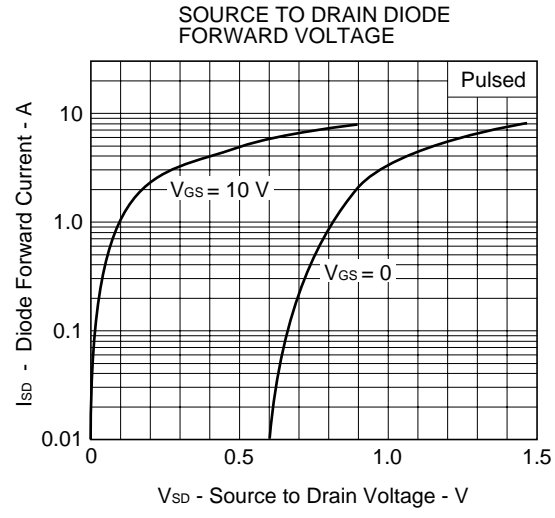
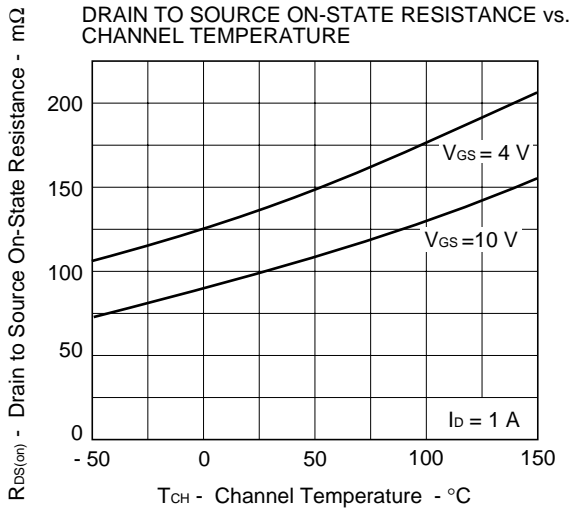


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





**REFERENCE**

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	IEI-1207
Semiconductor device package manual	IEI-1213
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	MF-1134
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037



[MEMO]

[MEMO]

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