To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

COMPOUND FIELD EFFECT POWER TRANSISTOR

Phase-out/Discontinued

μPA1500B

N-CHANNEL POWER MOS FET ARRAY SWITCHING USE

DESCRIPTION

The μPA1500B is N-channel Power MOS FET Array that built in 4 circuits and surge absorber designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Large Current and Low On-state Resistance
  $I_{D(DC)}$ = ±3 A
  $R_{DS(on)1} \leq 0.18\ \Omega$ MAX. (V_{GS} = 10 V, I_D = 2 A)
  $R_{DS(on)2} \leq 0.24\ \Omega$ MAX. (V_{GS} = 4 V, I_D = 2 A)
- Low Input Capacitance Ciss = 200 pF TYP.
- Surge Absorber, built in

ORDERING INFORMATION

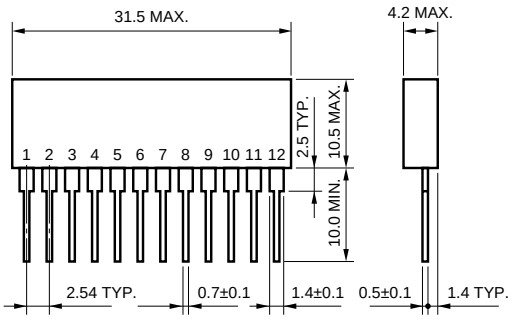
Type Number	Package
μPA1500BH	12 Pin SIP

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage	V_{DSS} Note 1	60	V
Gate to Source Voltage	V_{GSS} Note 2	±20	V
Drain Current (DC)	$I_{D(DC)}$	±3.0	A/unit
Drain Current (pulse)	$I_{D(pulse)}$ Note 3	±12	A/unit
Repetitive peak Reverse Voltage	V_{RRM} Note 4	65	V
Diode Forward Current	$I_{F(av)}$ Note 4	3.0	A/unit
Total Power Dissipation	P_{T1} Note 5	28	W
Total Power Dissipation	P_{T2} Note 6	4.0	W
Channel Temperature	T_{CH}	150	°C
Storage Temperature	T_{stg}	–55 to 150	°C
Single Avalanche Current	I_{AS} Note 7	3.0	A
Single Avalanche Energy	E_{AS} Note 7	0.9	mJ

Notes 1. V_{GS} = 0
2. V_{DS} = 0
3. PW ≤ 10 μs, Duty Cycle ≤ 1 %
4. Rating of Surge Absorber
5. 4 Circuits, T_C = 25 °C
6. 4 Circuits, T_A = 25 °C
7. Starting T_{CH} = 25 °C, V_{DD} = 30 V, V_{GS} = 20 V → 0, R_G = 25 Ω, L = 100 μH

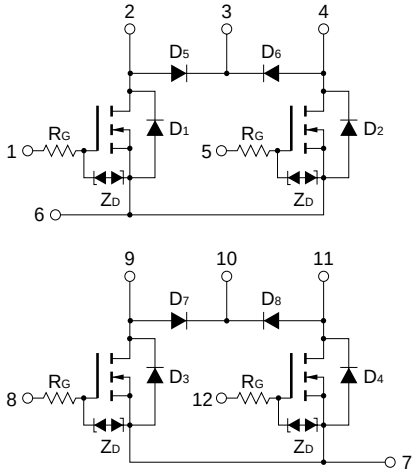
PACKAGE DIMENSIONS
(in millimeters)



ELECTRODE CONNECTION

1, 5, 8, 12	GATE
2, 4, 9, 11	DRAIN, ANODE
6, 7	SOURCE
3, 10	CATHODE

CONNECTION DIAGRAM



D_1 to D_4 : Body Diode
D_5 to D_8 : Surge Absorber
Z_D : Gate to Source Protection Diode
R_G : Gate Input Resistance 330 Ω TYP.

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Document No. G10597EJ2V0DS00 (2nd edition)
Date Published December 1995 P
Printed in Japan

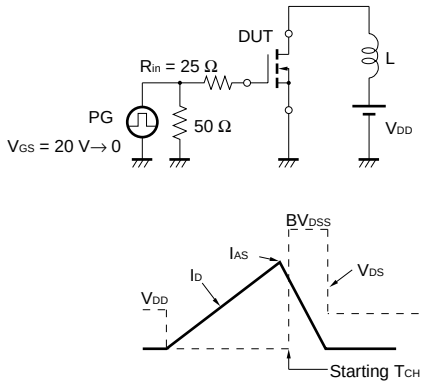
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0			±10	μA
Gate Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1.0 mA	1.0		2.0	V
Forward Transfer Admittance	$\|Y_{fs}\|$	V_{GS} = 10 V, I_D = 2.0 A	2.0			S
Drain to Source On-State Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 2.0 A		0.10	0.18	Ω
	$R_{DS(on)2}$	V_{GS} = 4.0 V, I_D = 2.0 A		0.14	0.24	Ω
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz		200		pF
Output Capacitance	C_{oss}			150		pF
Reverse Transfer Capacitance	C_{rss}			55		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 2.0 A, V_{GS} = 10 V, V_{DD} ≒ 30 V, R_L = 15 Ω		20		ns
Rise Time	t_r			100		ns
Turn-off Delay Time	$t_{d(off)}$			735		ns
Fall Time	t_f			350		ns
Total Gate Charge	Q_G	V_{GS} = 10 V, I_D = 3.0 A, V_{DD} = 48 V		13		nC
Gate to Source Charge	Q_{GS}			2		nC
Gate to Drain Charge	Q_{GD}			4.7		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 3 A, V_{GS} = 0		1.0		V

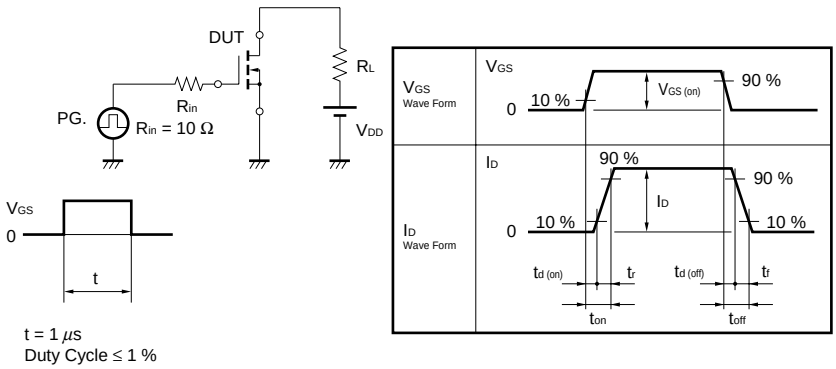
SURGE ABSORBER (Diode, builtin) 1 Unit

Repetitive peak Reverse Current	I_{RRM}	V_R = 65 V			10	μA
Diode Forward Voltage	V_F	I_F = 3.0 A			1.5	V

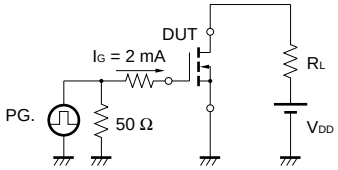
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time

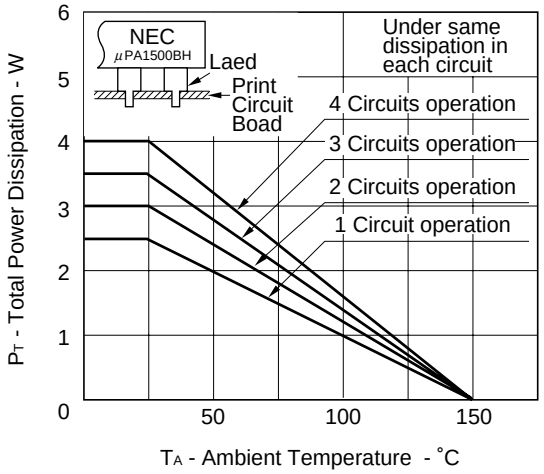


Test Circuit 3 Gate Charge

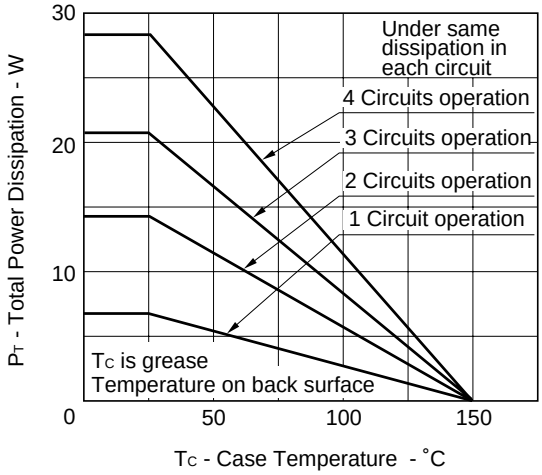


TYPICAL CHARACTERISTICS (T_A = 25 ˚C)

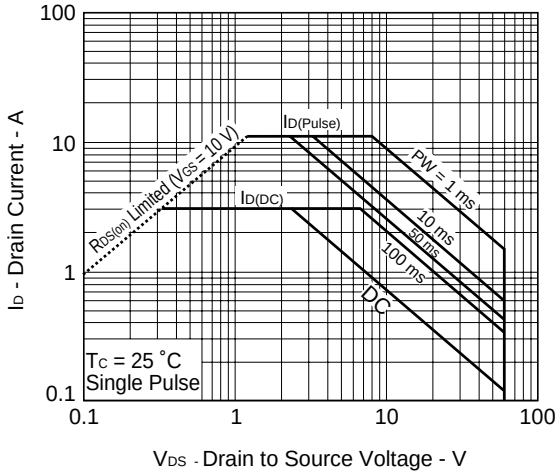
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



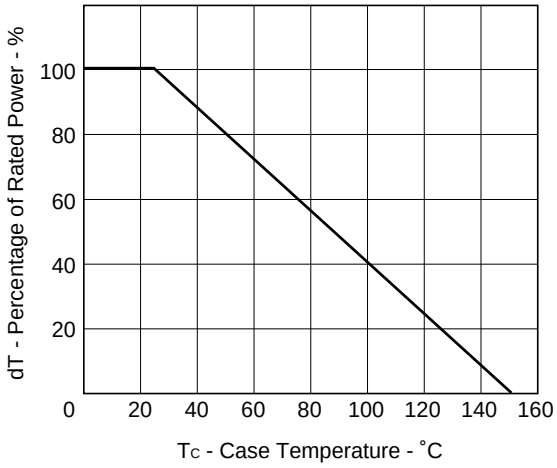
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



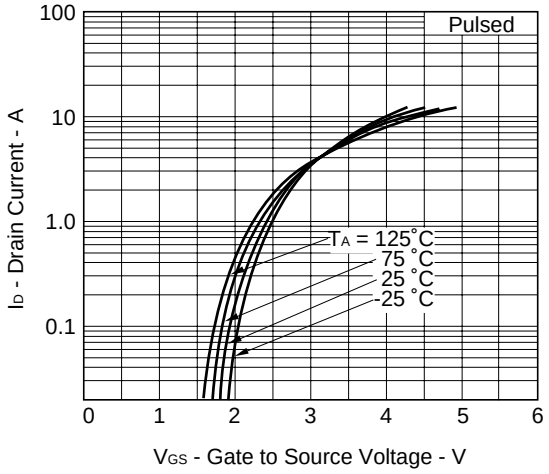
FORWARD BIAS SAFE OPERATING AREA



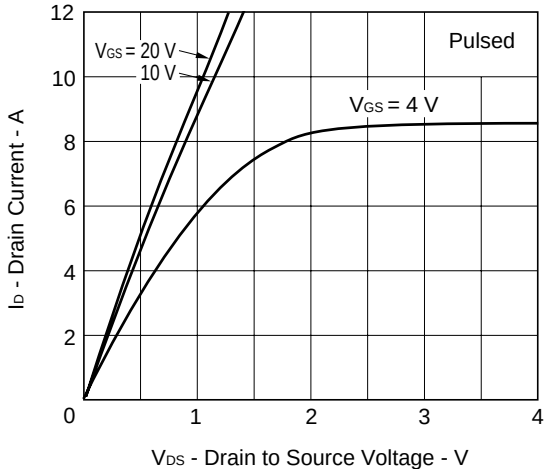
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



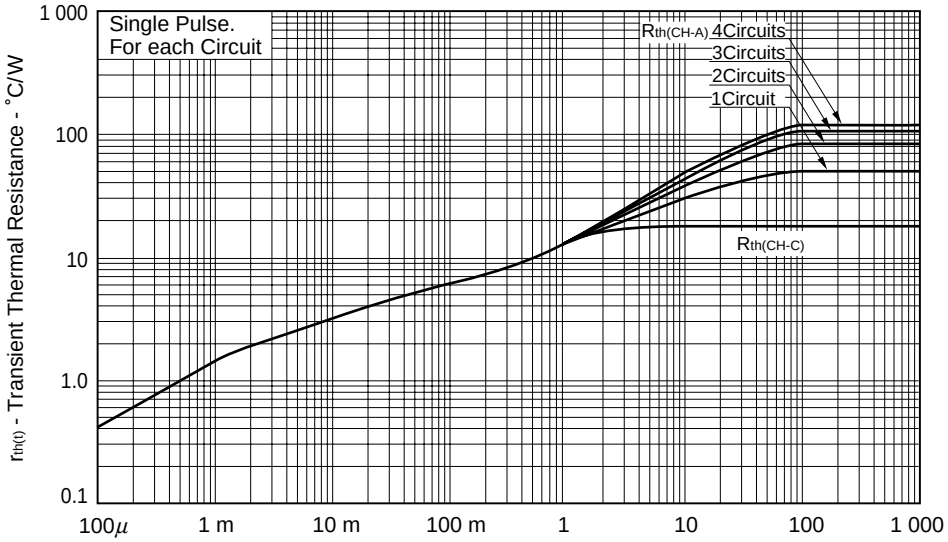
FORWARD TRANSFER CHARACTERISTICS



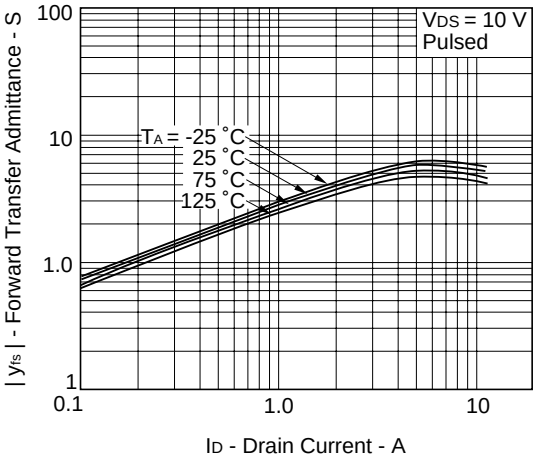
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



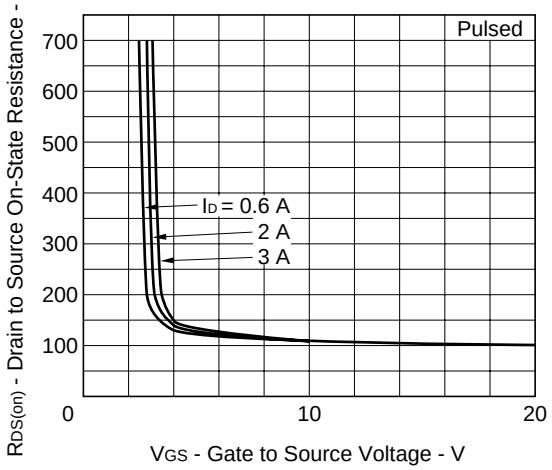
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



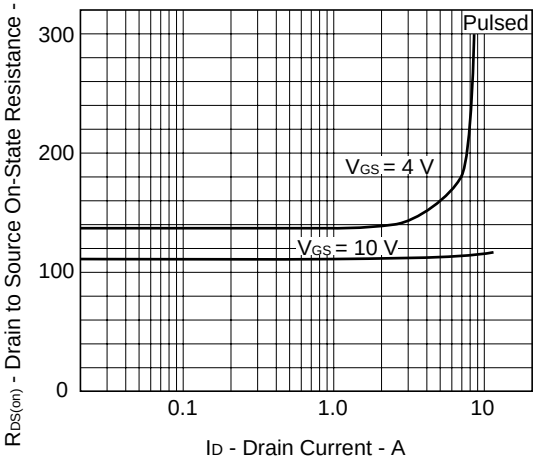
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



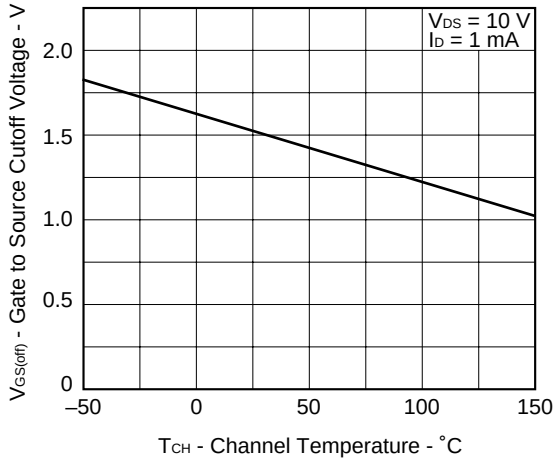
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



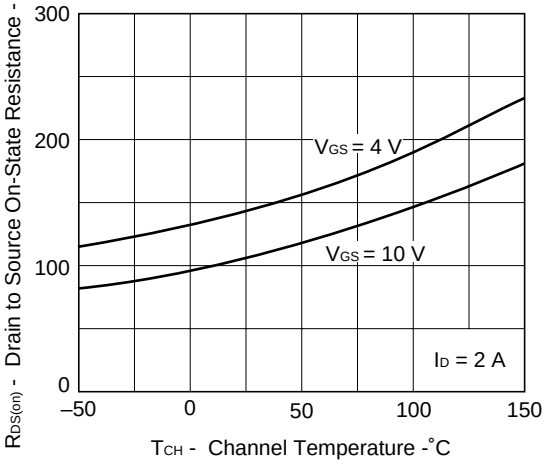
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



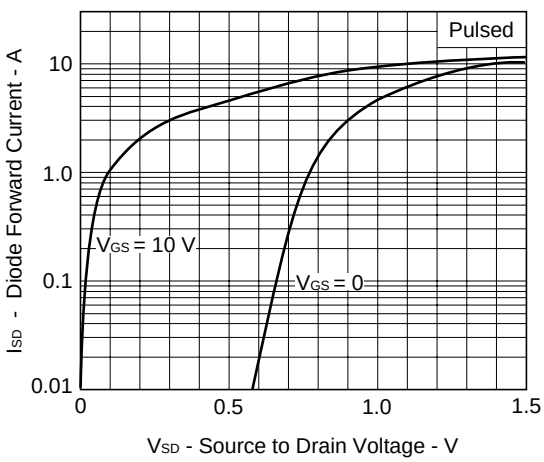
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



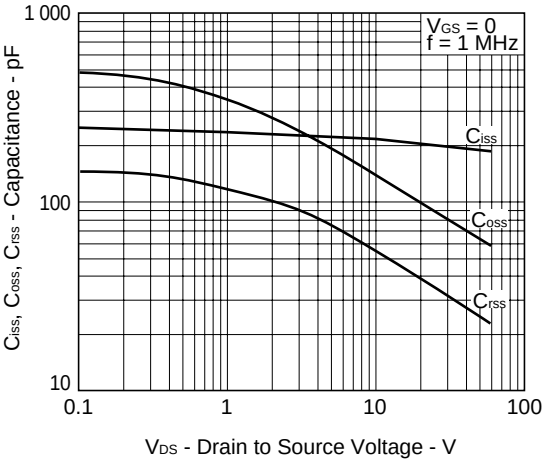
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



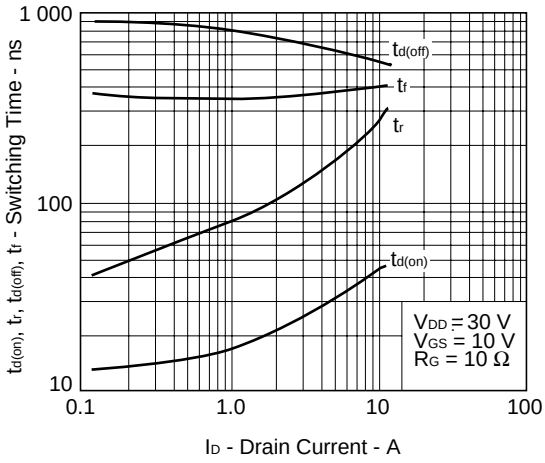
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



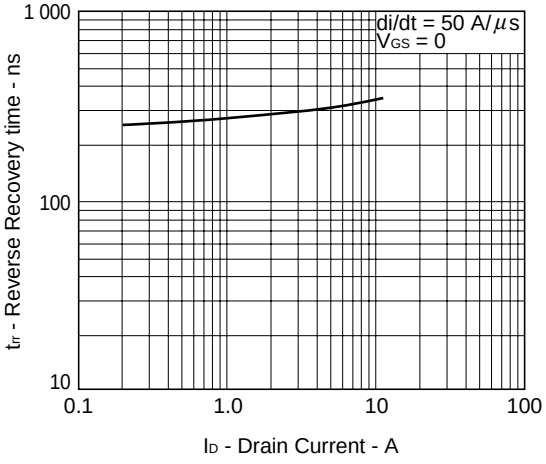
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



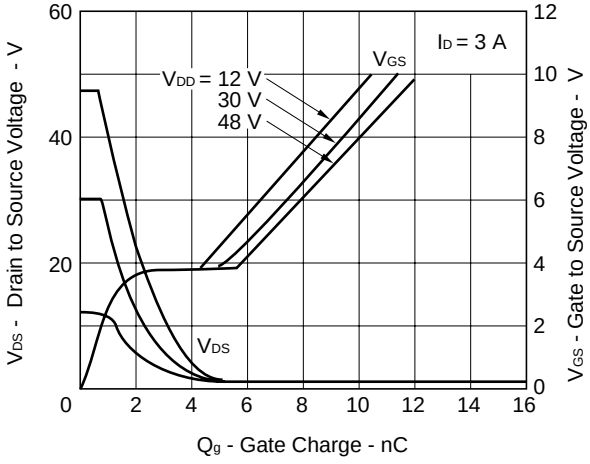
SWITCHING CHARACTERISTICS



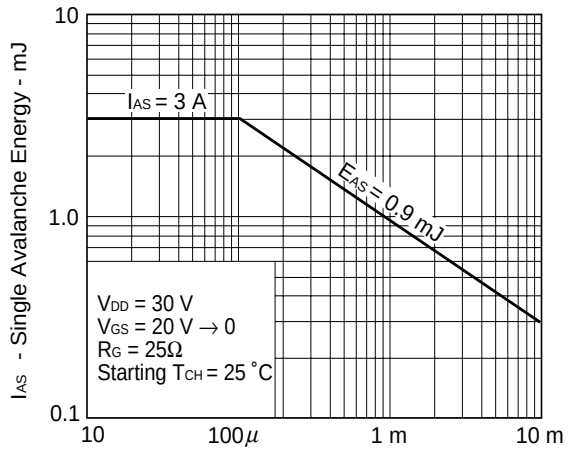
REVERSE RECOVERY TIME vs. DRAIN CURRENT



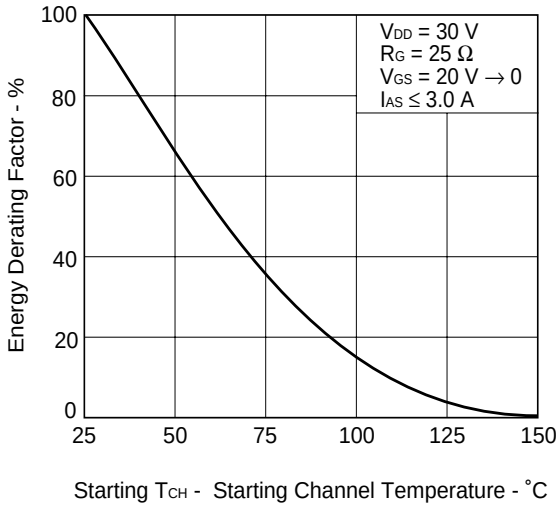
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE ENERGY vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY
DERATING FACTOR



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	IEI-1207
Semiconductor device package manual	IEI-1213
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	MF-1134
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

[MEMO]

M4 94.11