Traffic Manager Co-processor Data Sheet

89TTM553

Preliminary Information*

Description

The 89TTM553 is a flow-based traffic management co-processor that can be used in conjunction with the 89TTM552.

It has two major functional parts: the queue manager (QM) and the FLQ scheduler. The QM is responsible for all the non-bandwidth functions, which include managing up to 1 Million queuing structures, handling cell and packet arrivals and departures from these queues, and maintaining a database of congestion management and statistics parameters for each flow queue (FLQ). The FLQ scheduler is responsible for managing the FLQ bandwidth functions.

The 89TTM553 FLQ scheduler supports traffic scheduling on up to 1M discrete flows. In addition to the scheduling levels provided by the 89TTM552, the 89TTM553 provides one or two levels of additional scheduling hierarchy. It also provides guaranteed minimum rate, maximum rate capping, excess rate distribution using weighted fair queuing (WFQ), byte rate shaping, and dynamic configuration adjustments.

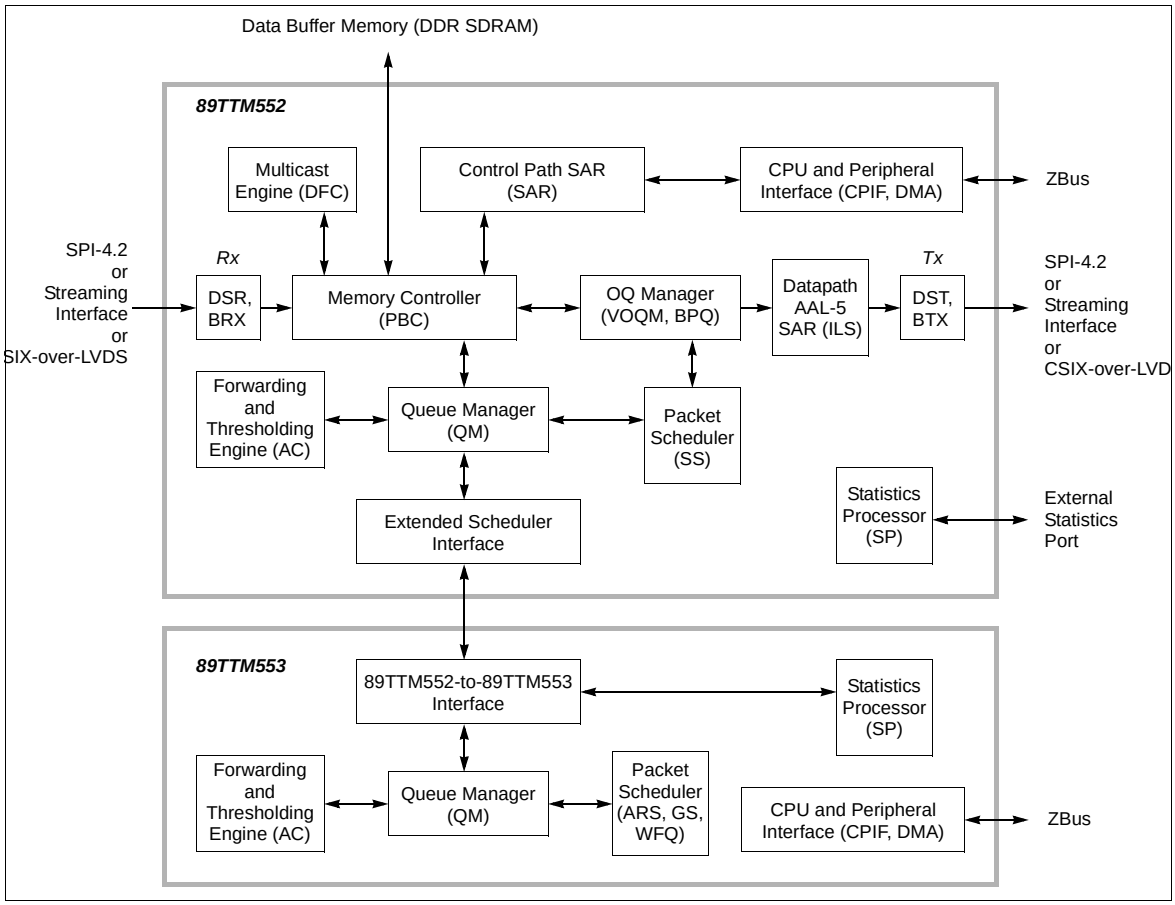
The 89TTM553 stores all the flow-based parameters (and state information) that are made available to the 89TTM552 for flow-based processing. When the 89TTM553 is used with the 89TTM552, congestion and bandwidth management features are enabled at the flow level as well as at the aggregate-flow level.

89TTM55x Features

- **Deterministic performance at 10 Gbps wire-speed (35 Mcps) regardless of the number of flows, traffic size, and patterns.**
- **Up to 256 megabytes of external memory buffer space (equivalent to a 210 ms buffer at 10 Gbps).**
- **Support (Rx and Tx) for industry-standard SPI-4 phase 2, NPF Streaming Interface, and CSIX over LVDS.**
- **Hierarchical queuing and precise scheduling:**
  - *Traffic management flexibility.*
  - *Support for up to 4K aggregate flow queues (AFQs), 1K port queues (PQs), 2K arrival reassembly queues (ARQs), and 1K output queues/channels (OQs) with no external memory required. Configurable AFQ-to-port assignments.*
  - *Support for up to 1M discrete flows (FLQs), with queuing for each flow, using external memory. Configurable mapping of FLQs into aggregate flow queues.*
  - *Two-level FLQ scheduling mode that supports up to 128K or 256K virtual pipe or subscriber queues with up to 8 or 4 CoS priority queues each.*
  - *Accurate byte-rate shaping at the FLQ, AFQ and port levels.*
- **Multiple levels of buffer congestion management.**
  - *Hierarchical queue structure and thresholding.*
  - *Congestion indication.*
  - *Dynamic adjustment of thresholds during periods of congestion.*
  - *Packet discard (PD).*
  - *Weighted random early discard (WRED).*
  - *Local congestion indication (CI).*

- **Configurable forwarding based on classification index.**
- **Two ports for obtaining event-based statistics.**
- **Configurable on-chip diagnostic statistics.**
- **Bandwidth management rate guarantee and shaping mechanisms for each flow, each aggregate flow and each port queue.**
  - *Priority and weighted bandwidth distribution mechanisms across groups of flows and aggregate flows.*
  - *Schedules rates as low as 2 kbps for each flow.*
  - *One- and two-level byte-rate FLQ scheduling: maximum and minimum rates, and strict priority and weighted fair queuing (WFQ) for each FLQ. Per-flow byte-rate shaping.*
  - *AFQ scheduling with byte-rate shaping: minimum and maximum rates with VBR MBS and PCR enforcement. Excess distribution using weighted fair queuing (WFQ) and PRR.*
  - *Port queues: maximum rates with byte-rate scheduling.*
- **Wire-speed logical multicasting.**
  - *Four classes of service.*
  - *Programmable service rate (minimum and excess bandwidth distribution).*
  - *Programmable thresholds.*
  - *Branch connections can be added and deleted during live traffic.*
  - *Traffic management features on all multicast roots and branches.*
- **Multicast label generation for spatial multicast support.**
- **Integrated wire-speed AAL-5 segmentation and reassembly (AAL-5 CPCS SAR) in the datapath.**
- **32-bit processor interface running at up to 66 MHz with integrated AAL-5 SAR and DMA engine for data insertion and extraction.**
  - *Four classes of service.*
  - *Integrated AAL-5-compliant and packet-based SAR.*
  - *Programmable service rate.*
  - *Programmable queue thresholds.*
  - *Use of descriptors and DMA support for maximum performance.*
  - *16-bit data bus transfer at up to 66 MHz.*
- **Algorithms implemented in hardware; software intervention required for initialization and configuration only.**
- **Error protection on all external RAM and BIST on all internal RAM.**
- **Inter-operable with the IDT ZTM200 traffic manager.**

89TTM55x Functional Block Diagram



89TTM553 Pin Description

Note: Information in this section is subject to change. Contact your IDT FAE before making design decisions.

In this data sheet, direction is indicated as follows: I for In, O for Out, B for Bi-directional, and P for power.

Signal Name	I/O Type	Dir.	Freq.	Remarks
BLL_CLK_CP, BLL_CLK_CN	1.5V HSTL Class 1	I	175 MHz	BLL QDR SRAM input clock: This clock pair registers data inputs on the rising edge of C and C#. All synchronous inputs must meet setup and hold times around the clock rising edges.
BLL_CLK_KP, BLL_CLK_KN	1.5V HSTL Class 1	O	175 MHz	BLL QDR SRAM output clock: This clock pair times the control outputs to the rising edge of K, and times the address and data outputs to the rising edge of K and K#.
BLL_ADDR[21:0]	1.5V HSTL Class 1	O	175 MHz	BLL QDR SRAM address outputs.
BLL_RD_N	1.5V HSTL Class 1	O	175 MHz	BLL QDR SRAM synchronous read output (active low): When asserted, a read cycle is initiated to the external QDR SRAM devices.
BLL_DIN[17:0]	1.5V HSTL Class 1	I	175 MHz	BLL QDR SRAM data inputs: Input data must meet setup and hold times around the rising edges of C and C# during read operations
BLL_WR_N	1.5V HSTL Class 1	O	175 MHz	BLL QDR SRAM synchronous write output (active low): When asserted, a write cycle is initiated to the external QDR SRAM devices.
BLL_DOUT[17:0]	1.5V HSTL Class 1	O	175 MHz	BLL QDR SRAM write data outputs: Output data is synchronized to the K and K# during write operations
BLL_VREF	0.75V	—	—	HSTL reference. Nominally V_{DDQ} / 2, so connect to 0.75 V

Table 1 Buffer Linked List QDR SRAM

Signal Name	I/O Type	Dir.	Freq.	Remarks
BXT_CLK_CP, BXT_CLK_CN	1.5V HSTL Class 1	I	175 MHz	BXT QDR SRAM input clock: This clock pair registers data inputs on the rising edge of C and C#. All synchronous inputs must meet setup and hold times around the clock rising edges.
BXT_CLK_KP, BXT_CLK_KN	1.5V HSTL Class 1	O	175 MHz	BXT QDR SRAM output clock: This clock pair times the control outputs to the rising edge of K, and times the address and data outputs to the rising edge of K and K#.
BXT_ADDR[21:0]	1.5V HSTL Class 1	O	175 MHz	BXT QDR SRAM address outputs.
BXT_RD_N	1.5V HSTL Class 1	O	175 MHz	BXT QDR SRAM synchronous read output (active low): When asserted, a read cycle is initiated to the external QDR SRAM devices.
BXT_DIN[3:0]	1.5V HSTL Class 1	I	175 MHz	BXT QDR SRAM data inputs: Input data must meet setup and hold times around the rising edges of C and C# during read operations

Table 2 Buffer Linked List Extension QDR SRAM (Part 1 of 2)

Signal Name	I/O Type	Dir.	Freq.	Remarks
BXT_WR_N	1.5V HSTL Class 1	O	175 MHz	BXT QDR SRAM synchronous write output (active low): When asserted, a write cycle is initiated to the external QDR SRAM devices.
BXT_DOUT[3:0]	1.5V HSTL Class 1	O	175 MHz	BXT QDR SRAM write data outputs: Output data is synchronized to the K and K# during write operations
BXT_LLT_VREF	0.75V	—	—	HSTL reference. Nominally V_{DDQ} / 2, so connect to 0.75 V

Table 2 Buffer Linked List Extension QDR SRAM (Part 2 of 2)

Signal Name	I/O Type	Dir.	Freq.	Remarks
FCT_CLK_CP, FCT_CLK_CN	1.5V HSTL Class 1	I	175 MHz	FCT QDR SRAM input clock: This clock pair registers data inputs on the rising edge of C and C#. All synchronous inputs must meet setup and hold times around the clock rising edges.
FCT_CLK_KP, FCT_CLK_KN	1.5V HSTL Class 1	O	175 MHz	FCT QDR SRAM output clock: This clock pair times the control outputs to the rising edge of K, and times the address and data outputs to the rising edge of K and K#.
FCT_ADDR[19:0]	1.5V HSTL Class 1	O	175 MHz	FCT QDR SRAM address outputs.
FCT_RD_N	1.5V HSTL Class 1	O	175 MHz	FCT QDR SRAM synchronous read output (active low): When asserted, a read cycle is initiated to the external QDR SRAM devices.
FCT_DIN[27:0]	1.5V HSTL Class 1	I	175 MHz	FCT QDR SRAM data inputs: Input data must meet setup and hold times around the rising edges of C and C# during read operations
FCT_WR_N	1.5V HSTL Class 1	O	175 MHz	FCT QDR SRAM synchronous write output (active low): When asserted, a write cycle is initiated to the external QDR SRAM devices.
FCT_DOUT[27:0]	1.5V HSTL Class 1	O	175 MHz	FCT QDR SRAM write data outputs: Output data is synchronized to the K and K# during write operations
FCT_VREF[1:0]	0.75	—	—	HSTL reference. Nominally V_{DDQ} / 2, so connect to 0.75 V

Table 3 Flow Control Table QDR SRAM

Signal Name	I/O Type	Dir.	Freq.	Remarks
FPT_CLK_CP, FPT_CLK_CN	1.5V HSTL Class 1	I	175 MHz	FPT QDR SRAM input clock: This clock pair registers data inputs on the rising edge of C and C#. All synchronous inputs must meet setup and hold times around the clock rising edges.
FPT_CLK_KP, FPT_CLK_KN	1.5V HSTL Class 1	O	175 MHz	FPT QDR SRAM output clock: This clock pair times the control outputs to the rising edge of K, and times the address and data outputs to the rising edge of K and K#.
FPT_ADDR[20:0]	1.5V HSTL Class 1	O	175 MHz	FPT QDR SRAM address outputs.
FPT_RD_N	1.5V HSTL Class 1	O	175 MHz	FPT QDR SRAM synchronous read output (active low): When asserted, a read cycle is initiated to the external QDR SRAM devices.

Table 4 Flow Parameters Table QDR SRAM (Part 1 of 2)

Signal Name	I/O Type	Dir.	Freq.	Remarks
FPT_DIN[35:0]	1.5V HSTL Class 1	I	175 MHz	FPT QDR SRAM data inputs: Input data must meet setup and hold times around the rising edges of C and C# during read operations
FPT_WR_N	1.5V HSTL Class 1	O	175 MHz	FPT QDR SRAM synchronous write output (active low): When asserted, a write cycle is initiated to the external QDR SRAM devices.
FPT_BW_N[3:0]	1.5V HSTL Class 1	O	175 MHz	FPT QDR SRAM synchronous write byte enables (active low)
FPT_DOUT[35:0]	1.5V HSTL Class 1	O	175 MHz	FPT QDR SRAM write data outputs: Output data is synchronized to the K and K# during write operations
FPT_VREF[1:0]	0.75V	—	—	HSTL reference. Nominally V_{DDQ} / 2, so connect to 0.75 V

Table 4 Flow Parameters Table QDR SRAM (Part 2 of 2)

Signal Name	I/O Type	Dir.	Freq.	Remarks
GPT_CLK_CP, GPT_CLK_CN	1.5V HSTL Class 1	I	175 MHz	GPT QDR SRAM input clock: This clock pair registers data inputs on the rising edge of C and C#. All synchronous inputs must meet setup and hold times around the clock rising edges.
GPT_CLK_KP, GPT_CLK_KN	1.5V HSTL Class 1	O	175 MHz	GPT QDR SRAM output clock: This clock pair times the control outputs to the rising edge of K, and times the address and data outputs to the rising edge of K and K#.
GPT_ADDR[20:0]	1.5V HSTL Class 1	O	175 MHz	GPT QDR SRAM address outputs.
GPT_RD_N	1.5V HSTL Class 1	O	175 MHz	GPT QDR SRAM synchronous read output (active low): When asserted, a read cycle is initiated to the external QDR SRAM devices.
GPT_DIN[17:0]	1.5V HSTL Class 1	I	175 MHz	GPT QDR SRAM data inputs: Input data must meet setup and hold times around the rising edges of C and C# during read operations.
GPT_WR_N	1.5V HSTL Class 1	O	175 MHz	GPT QDR SRAM synchronous write output (active low): When asserted, a write cycle is initiated to the external QDR SRAM devices.
GPT_BW_N[1:0]	1.5V HSTL Class 1	O	175 MHz	GPT QDR SRAM synchronous byte enables (active low).
GPT_DOUT[17:0]	1.5V HSTL Class 1	O	175 MHz	GPT QDR SRAM write data outputs: Output data is synchronized to the K and K# during write operations.
GPT_VREF	0.75V	—	—	HSTL reference. Nominally V_{DDQ} / 2, so connect to 0.75 V

Table 5 Group Parameters Table QDR SRAM

Signal Name	I/O Type	Dir.	Freq.	Remarks
HT_CLK_CP, HT_CLK_CN	1.5V HSTL Class 1	I	175 MHz	HT QDR SRAM input clock: This clock pair registers data inputs on the rising edge of C and C#. All synchronous inputs must meet setup and hold times around the clock rising edges.
HT_CLK_KP, HT_CLK_KN	1.5V HSTL Class 1	O	175 MHz	HT QDR SRAM output clock: This clock pair times the control outputs to the rising edge of K, and times the address and data outputs to the rising edge of K and K#.
HT_ADDR[19:0]	1.5V HSTL Class 1	O	175 MHz	HT QDR SRAM address outputs.
HT_RD_N	1.5V HSTL Class 1	O	175 MHz	HT QDR SRAM synchronous read output (active low): When asserted, a read cycle is initiated to the external QDR SRAM devices.
HT_DIN[35:0]	1.5V HSTL Class 1	I	175 MHz	HT QDR SRAM data inputs: Input data must meet setup and hold times around the rising edges of C and C# during read operations.
HT_WR_N	1.5V HSTL Class 1	O	175 MHz	HT QDR SRAM synchronous write output (active low): When asserted, a write cycle is initiated to the external QDR SRAM devices.
HT_DOUT[35:0]	1.5V HSTL Class 1	O	175 MHz	HT QDR SRAM write data outputs: Output data is synchronized to the K and K# during write operations.
HT_VREF[1:0]	0.75V	—	—	HSTL reference. Nominally V_{DDQ} / 2, so connect to 0.75 V

Table 6 Head Tail QDR SRAM

Signal Name	I/O Type	Dir.	Freq.	Remarks
LLT_CLK_CP, LLT_CLK_CN	1.5V HSTL Class 1	I	175 MHz	LLT QDR SRAM input clock: This clock pair registers data inputs on the rising edge of C and C#. All synchronous inputs must meet setup and hold times around the clock rising edges.
LLT_CLK_KP, LLT_CLK_KN	1.5V HSTL Class 1	O	175 MHz	LLT QDR SRAM output clock: This clock pair times the control outputs to the rising edge of K, and times the address and data outputs to the rising edge of K and K#.
LLT_ADDR[19:0]	1.5V HSTL Class 1	O	175 MHz	LLT QDR SRAM address outputs.
LLT_RD_N	1.5V HSTL Class 1	O	175 MHz	LLT QDR SRAM synchronous read output (active low): When asserted, a read cycle is initiated to the external QDR SRAM devices.
LLT_DIN[10:0]	1.5V HSTL Class 1	I	175 MHz	LLT QDR SRAM data inputs: Input data must meet setup and hold times around the rising edges of C and C# during read operations.
LLT_WR_N	1.5V HSTL Class 1	O	175 MHz	LLT QDR SRAM synchronous write output (active low): When asserted, a write cycle is initiated to the external QDR SRAM devices.
LLT_DOUT[10:0]	1.5V HSTL Class 1	O	175 MHz	LLT QDR SRAM write data outputs: Output data is synchronized to the K and K# during write operations.

Table 7 Linked List Table QDR SRAM

Signal Name	I/O Type	Dir.	Freq.	Remarks
FLQS_DIN[14:0] FLQS_DIN_PRTY	1.5V HSTL Class 1	I	175 MHz	Control serial interface to 89TTM552 (15 signal lines + 1 parity line)
FLQS_DOUT[19:0] FLQS_DOUT_PRTY	1.5V HSTL Class 1	O	175 MHz	Control serial interface to 89TTM552 (20 signal lines + 1 parity line)
FLQS_CLKIN	1.5V HSTL Class 1	I	175 MHz	Clock input from 89TTM552
FLQS_CLKOUT	1.5V HSTL Class 1	O	175 MHz	Clock output to 89TTM552
FLQS_TIC_IN	1.5V HSTL Class 1	I	175 MHz	Cell time tic input from 89TTM552
FLQS_TIC_OUT	1.5V HSTL Class 1	O	175 MHz	Cell time tic out to 89TTM552
FLQS_VREF	0.75V	—	—	HSTL reference. Nominally V_{DDQ} / 2, so connect to 0.75 V

Table 8 89TTM552/89TTM553 Interface

Signal Name	I/O Type	Dir.	Freq.	Remarks
ZBUS_AVALID_N	3.3V LVTTL, 12mA drive, internal pullup	B	33 or 66 MHz	ZBus address valid flag (active low)
ZBUS_CLK	3.3V, no internal pullup	I	33 or 66 MHz	ZBus clock input (up to 66 MHz)
ZBUS_AD[15:0]	3.3V LVTTL, 12mA drive, internal pullup	B	33 or 66 MHz	ZBus 16-bit multiplexed address/data bus
ZBUS_DEVID[4:0]	3.3V, internal pullup	I	33 or 66 MHz	Used for ZBus device identification
ZBUS_DVALID_N	3.3V LVTTL, 12mA drive, internal pullup	B	33 or 66 MHz	ZBus data valid flag (active low)
ZBUS_GNT_N	3.3V, internal pullup	I	33 or 66 MHz	ZBus grant (active low)
ZBUS_INT_N[2:0]	3.3V LVTTL, 12mA drive	O	33 or 66 MHz	ZBus device interrupt (active low)
ZBUS_PRTY	3.3V LVTTL, 12mA drive, internal pullup	B	33 or 66 MHz	ZBus parity over address/data; one parity bit for 16 bits
ZBUS_DIR	3.3V LVTTL, 12mA drive	O	33 or 66 MHz	ZBus write/read flag
ZBUS_REQ_N	3.3V LVTTL, 12mA drive	O	33 or 66 MHz	ZBus master cycle request (active low)

Table 9 Processor Interface (ZBus)

Signal Name	I/O Type	Dir.	Freq.	Remarks
IDDQ	3.3V, internal pulldown	I	N/A	IDDQ input (active high). *For IDT use only. Do not connect.*
RESERVE_1	3.3V LVTTL, 4 mA drive	O	N/A	*For IDT use only. Do not connect.*
SCAN_EN	3.3V	I	N/A	Scan enable (active high) *For IDT use only.* Attach to a 4.7K resistor to 0V
RESERVE_0	3.3V, internal pullup	I	N/A	Tristate enable (active low) *For IDT use only.* Attach to a 4.7K resistor to 3.3V
TCK	3.3V	I	—	JTAG (IEEE 1149.1) clock input.
TDI	3.3V, internal pullup	I	—	JTAG (IEEE 1149.1) test data input.
TDO	3.3V LVTTL, 12 mA drive	O	—	JTAG (IEEE 1149.1) test data output.
TMS	3.3V, internal pullup	I	—	JTAG (IEEE 1149.1) test mode select
TRST_N	3.3V, internal pullup	I	—	JTAG (IEEE 1149.1) test reset input.

Table 10 Test I/O

Signal Name	I/O Type	Dir.	Freq.	Remarks
PLL_2X_BPCLK	3.3V, internal pulldown	I	N/A	Bypass Clock Input *For IDT use only. Do not connect.*
PLL_BP_MODE	3.3V, internal pulldown	I	N/A	Bypass Clock Input *For IDT use only. Do not connect.*
PLL_MON	3.3V LVTTL, 12mA drive	O	N/A	PLL Monitor *For IDT use only. Do not connect.*
PLL_CFG_OVR	3.3V, internal pulldown	I	N/A	PLL Configuration Override
PLL_RST	3.3V	I	Async	PLL reset. A special initialization sequence is required.
PLL_VDDA	1.8V	—	—	PLL Analog VDD
PLL_VSSA	—	—	—	PLL Analog VSS
PLL_SYS_REFCLK	3.3V	I	100 MHz	Chip core PLL reference clock.
RESET_N	3.3V, internal pullup	I	Async	Chip reset input (active low).
VDD18	—	—	—	1.8V core power
VDD15	—	—	—	1.5V I/O power for HSTL-2 I/Os: Isolated output buffer supply set nominally to 1.5V

Table 11 PLL I/O (Part 1 of 2)

Signal Name	I/O Type	Dir.	Freq.	Remarks
VDD33	—	—	—	3.3V I/O power for LVTTL I/Os
N/C	—	—	N/A	*Do not connect.*
GND	—	I	N/A	Ground

Table 11 PLL I/O (Part 2 of 2)

89TTM553 Electrical Specifications

Some data are TBD and will be published as they become available. The specifications are subject to change without notice.

Absolute Maximum Ratings

The absolute maximum ratings are the maximum conditions that the device can withstand without sustaining permanent damage. Exceeding any of these conditions could result in permanent damage to the device. Normal operation should not be expected at these conditions. In addition, exposure to absolute maximum rated conditions (or near absolute maximum rated conditions) for extended periods may affect device reliability.

Operation of the device is not guaranteed at the absolute maximum ratings, but rather at the operating conditions outlined in “DC Characteristics” on page 11 and “AC Characteristics” on page 12.

Symbol	Parameter	Min	Max	Units	Conditions
T_{JMAX}	Junction temperature under bias	—	105	°C	
$T_{STORAGE}$	Storage temperature	—	150	°C	
	Storage temperature range	–40	85	°C	Long term storage
T_{SOLDER}	Soldering temperature	—	215	°C	
T_{REWORK}	Rework temperature	—	204	°C	

Table 12 Absolute Maximum Ratings

Operating Ranges

Symbol	Parameter	Min	Typical	Max	Units	Conditions
T_J	Operating junction temperature range	0	—	85	°C	
I_{V15}	Input current for 1.5V power supply	—	800	—	mA	
I_{V18}	Input current for 1.8V power supply	—	1.16	—	A	
I_{V33}	Input current for 3.3V power supply	—	60	—	mA	
VDD_{15}	1.5V HSTL supply	1.425	1.5	1.575	V	±5%
VDD_{18}	1.8V Core supply	1.71	1.8	1.89	V	±5%

Table 13 Operating Ranges (Part 1 of 2)

Symbol	Parameter	Min	Typical	Max	Units	Conditions
VDD_{33}	3.3V LVTTL supply	3.135	3.3	3.465	V	±5%
VRF_{HSTL} [1]	0.75V HSTL reference voltage	0.7125	0.75	0.7875	V	±5%
Power Dissipation		—	3.49	3.66	W	Max. values use the maximum voltages and current listed in this table and typical values use the typical voltages and current.

Table 13 Operating Ranges (Part 2 of 2)

1. This operating range applies to the following pins: BLL_VREF, BXT_LLT_VREF, FCT_VREF[1:0], FPT_VREF[1:0], GPT_VREF, HT_VREF[1:0], and FLQS_VREF.

DC Characteristics

Unless otherwise stated, the following parameters are provided given the conditions outlined in Table 13.

Symbol	Parameter	Min	Typical	Max	Units
V_{ILHSTL} (1.5v HSTL)	Input low voltage for 1.5V HSTL inputs (VREF = 0.75V)	—	VREF – 0.1	V	
V_{IHHSTL} (1.5v HSTL)	Input high voltage for 1.5V HSTL inputs (VREF = 0.75V, VDDQ = 1.5V)	VREF+ 0.1	VDDQ+0.3	V	
V_{IL33} (3.3v LVTTL)	Input low voltage for 3.3V LVTTL inputs	—	0.8	V	
V_{IH33} (3.3v LVTTL)	Input high voltage for 3.3V LVTTL inputs	2.0	—	V	
V_{OLHSTL}	Output low voltage for 1.5V HSTL outputs	—	0.4	V	1.5v HSTL classI w/8mA Drive)
V_{OHHSTL}	Output high voltage for 1.5V HSTL outputs (VDDQ = 1.5V)	VDDQ-0.4	-	V	1.5v HSTL classI w/ 8mA Drive)
V_{OL33}	Output low voltage for 3.3V CMOS outputs (12mA pads)	—	0.5	V	3.3v LVTTL w/ 12mA Drive
V_{OH33}	Output high voltage for 3.3V CMOS outputs (12mA pads)	2.4	—	V	3.3v LVTTL w/ 12mA Drive
I_{ILHSTL} (1.5v HSTL)	Input Leakage low current for 1.5V HSTL Inputs	-10	10	uA	
I_{IHHSTL} (1.5v HSTL)	Input Leakage high current for 1.5V HSTL Inputs	-10	10	uA	
I_{IL33} (3.3v pads w/o Pull Up/Down)	Input Leakage low current for 3.3V Inputs	-10	10	uA	
I_{IH33} (3.3v pads w/o Pull Up/Down)	Input Leakage high current for 3.3V Inputs	-10	10	uA	
I_{IL33PU} (3.3v pads w/ Pull Up)	Input Leakage low current for 3.3V with Pull-Up Inputs	-200	-10	uA	

Table 14 DC Parameters (Part 1 of 2)

Symbol	Parameter	Min	Typical	Max	Units
I_{IH33PU} (3.3v pads w/ Pull Up)	Input Leakage high current for 3.3V with Pull-Up Inputs	-10	+10	uA	
I_{IL33PD} (3.3v pads w/ Pull Down)	Input Leakage low current for 3.3V with Pull-Down Inputs	-10	+10	uA	
I_{IH33PD} (3.3v pads w/ Pull Down)	Input Leakage high current for 3.3V with Pull-Down Inputs	10	200	uA	

Table 14 DC Parameters (Part 2 of 2)

AC Characteristics

Unless otherwise stated, the following parameters are provided given the conditions outlined in Table 13.

Symbol	Parameter	Min	Typical	Max	Units
f_{SYS}	Frequency for system (core) clock reference	—	100	—	MHz
T_{JSYS}	Jitter requirements for system clock	—	—	80	ps
D_{SYS}	Percentage duty for system clock	45	50	55	%
f_{ZB}	Frequency for ZBus clock	33	33	66	MHz
D_{ZB}	Percentage duty for ZBus clock	45	50	55	%

Table 15 System Clock Timing

Symbol	Parameter	Min	Typical	Max	Units
T_{KQOV}	$K/\overline{K}$ rising edge to address/data output valid	—	—	1.6[1]	ns
T_{KQOX}	$K/\overline{K}$ rising edge to address/data output invalid	0.8[1]	—	—	ns
T_{CQIS}	$C/\overline{C}$ rising edge to data input setup	–0.2	—	—	ns
T_{CQIH}	$C/\overline{C}$ rising edge to data input hold	—	—	1.6	ns

Table 16 QDR SSRAM Interface Timing

1. The parameter is specified at 89TTM55x core clock frequency of 175 MHz.

Symbol	Parameter	Min	Typical	Max	Units
T_{KQV}	Zbus clock high to output valid	—	—	8.3	ns
T_{KQX}	Zbus clock high to output invalid	2.5	—	—	ns
T_{KQLZ}	Zbus clock high to output low-Z	1.0	—	6.0	ns
T_{KQHZ}	Zbus clock high to output high-Z	1.0	—	6.0	ns
T_S	Input setup time from system clock	3.0	—	—	ns
T_H	Input hold time from system clock	0	—	—	ns

Table 17 Zbus Interface Timing

AC Test Conditions

Input Rise/Fall Time	1 V / ns (20% / 80%)
Output timing measurement reference level (V_{REF}) for 3.3V interfaces	(VDDQ/2) V
Output load	As shown in Figure 1

Table 18 AC Test Conditions

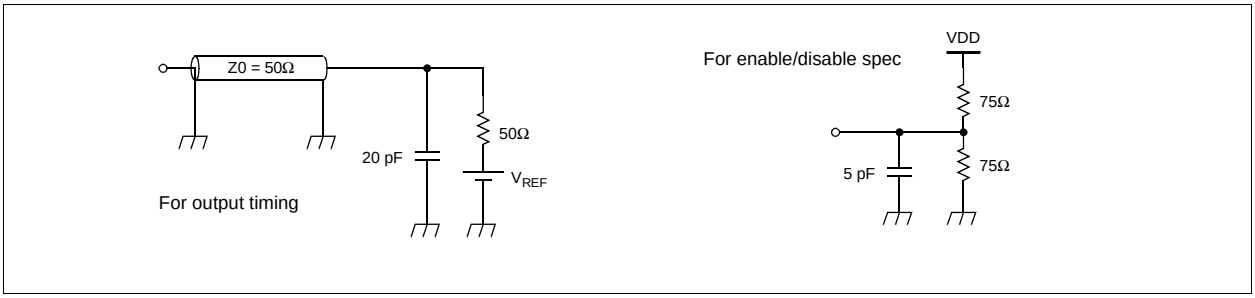


Figure 1 AC Test Load

89TTM553 Thermal Considerations

This section describes the temperature and heat sink calculations for flip-chip BGA devices.

Symbol	Parameter	Value	Units	Conditions
$Ø_{JA}$	Thermal resistance, junction to ambient (no heat sink)	9.8	°C / W	Max: still air.
		7.8	°C / W	Typical: 200 FPM.
$Ø_{JB}$	Estimated thermal resistance, junction to board	3.1	°C / W	
$Ø_{JC}$	Thermal resistance, junction to case	0.7	°C / W	

Table 19 89TTM553 Thermal Characteristics

The thermal circuit is as shown below.

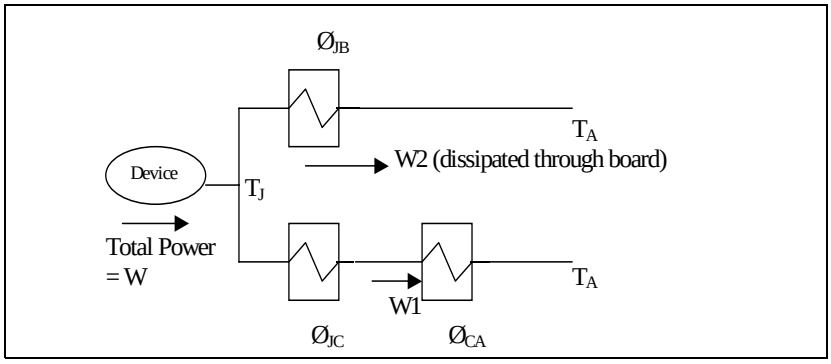


Figure 2 89TTM553 Thermal Circuit

For flip-chip BGA devices, there are two paths for heat dissipation: one through the package balls to the board and other through the package case to air. The device specifications provide $Ø_{JB}$ and $Ø_{JC}$ numbers. The $Ø_{CA}$ number comes from the heat sink manufacturer and depends on type of heat sink (area, height, fin type, etc.) and the airflow across the heat sink. The device specifications also provide the maximum operating junction temperature (T_J) that will not degrade the device reliability. The system designer should ensure that the device maximum junction temperature is not exceeded under any operating condition. One method of accomplishing this is to calculate the maximum ambient temperature (T_A) that can be tolerated based on the above device parameters. The formula is shown below.

$$T_A = T_J - W \times \frac{Ø_{JB} \times (Ø_{JC} + Ø_{CA})}{Ø_{JB} + Ø_{JC} + Ø_{CA}}$$

The following graph depicts the ambient temperature (T_A) versus $Ø_{CA}$.

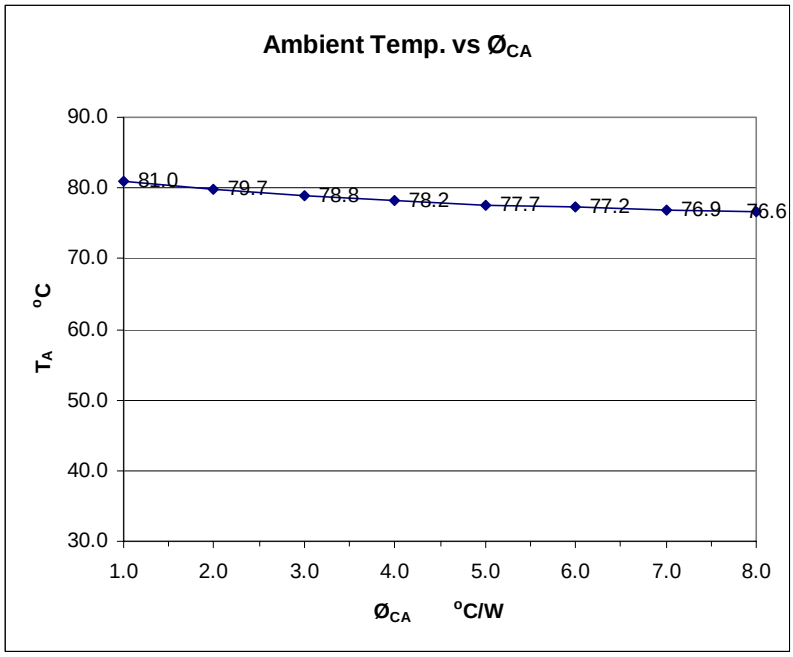


Figure 3 89TTM553 Ambient Temperature Curve

For system designers, specification of the maximum device junction temperature (operating) is critical, since it allows them to select a heat sink that meets the maximum ambient temperature requirements of their system.

The other parameter that is device package-specific is $Ø_{JA}$, without a heat sink, and is specified for various air-flow conditions. This is the intrinsic thermal resistance of the package (junction to case + case to ambient) and is mainly specified as a reference parameter. (This is when a heat sink is not present and the top surface of the package is essentially acting as the heat sink). However, in devices that have high power dissipation, heat sink usage is highly desirable. Consequently, system designers may have limited use for this parameter.

89TTM553 Reset Sequence

A PLL reset sequence must be followed when resetting the 89TTM553 to ensure that clocks are stable when the chip comes out of reset. This section describes the reset sequence for the 89TTM553 device.

The 89TTM553 uses data presented on the ZBus data and parity pins to determine the clock frequencies when the chip is in reset. The PLL_CFG_OVR pin controls this feature. When left high, the PLL will determine its clock frequency by sampling these values on the ZBus pins. The feature is not necessary if the default clock frequencies are desired. (The default frequency for the core clock is 133 MHz when a 100 MHz clock reference is used.) When default frequencies are desired, the PLL_CFG_OVR should be held low and it is not necessary to drive the ZBus data and parity lines during the reset.

Core PLL Frequency Setting

Following is the summary of the reset sequence:

1. Assert chip reset.
2. Drive LOR (latch on reset) values on ZBus (described below) and enable configuration override on all PLLs. (Configuration override remains ON forever).
3. Reset PLLs.
4. Release reset on PLLs.
5. Release chip reset.
6. Release LOR value on ZBus.

The following values must be driven on ZBUS_AD[ ] and ZBUS_PRTY before the reset sequences in order to set the chip operation frequency properly. Note that the setting is based on a *100MHz* reference input clock (PLL_SYS_REFCLK pin).

ZB_PRTY[1:0] = 0x3, must be driven “LOW” for the entire reset sequence cycles

ZB_AD[31:16], and ZB_AD[15:0] = bits are set as:

	Core/system clock frequency
0x154F =	187.50MHz
0x1527 =	175.00MHz
0x153a =	166.67MHz
0x1526 =	150.00MHz
0x1538 =	133.33MHz
0x1525 =	125.00MHz

Reset Sequence Timing Diagram

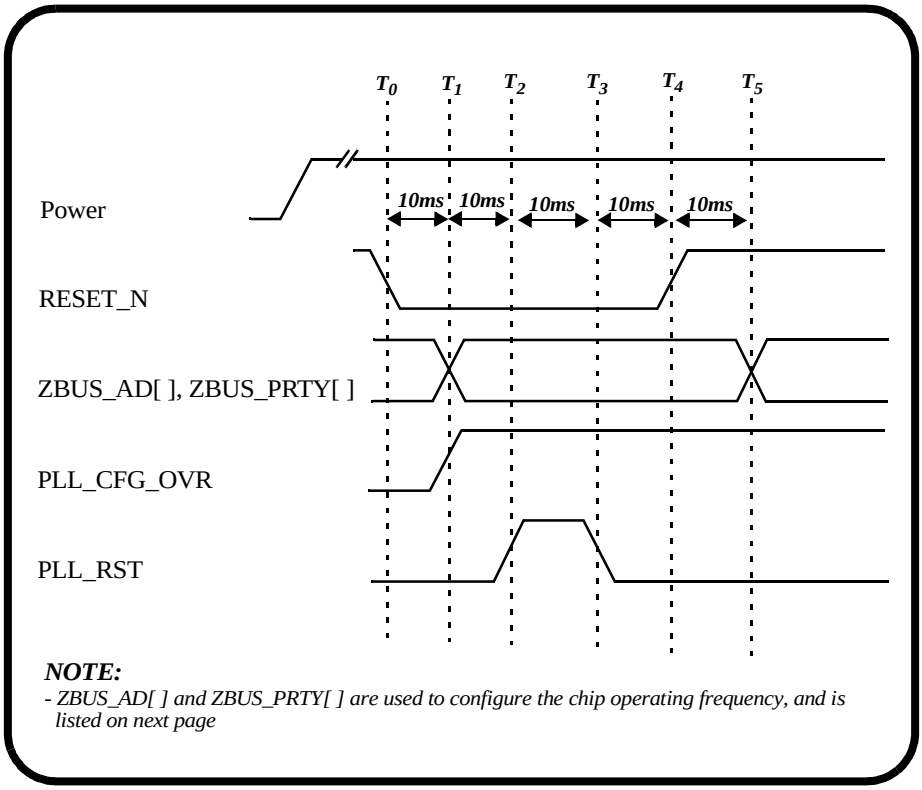


Figure 4 89TTM553 Reset Sequence Timing Diagram

Pin List I/O Description

The 89TTM553 Pin List on page 17 uses the following I/O notations:

I	Input
O	Output
B	Bidirectional
P	Power

89TTM553 Pin List

Pin	Signal	Type
A2	GND	P
A3	VDD15	P
A4	HT_CLK_CN	I
A5	HT_CLK_CP	I
A6	HT_DIN_19	I
A7	HT_DIN_20	I
A8	VDD15	P
A9	GND	P
A10	HT_DIN_34	I
A11	HT_DIN_35	I
A12	HT_DOUT_14	O
A13	HT_DOUT_15	O
A14	VDD15	P
A15	GND	P
A16	HT_DOUT_16	O
A17	HT_DOUT_31	O
A18	HT_DOUT_35	O
A19	HT_ADDR_14	O
A20	GND	P
A21	VDD15	P
A22	HT_ADDR_16	O
A23	HT_ADDR_17	O
A24	FCT_ADDR_12	O
A25	FCT_ADDR_13	O
A26	GND	P
A27	VDD15	P
A28	FCT_DOUT_02	O
A29	FCT_DOUT_03	O
A30	FCT_DOUT_04	O
A31	FCT_DOUT_05	O
A32	VDD15	P
A33	GND	P
B1	GND	P
B2	GND	P
B3	VDD15	P
B4	HT_DIN_13	I
B5	HT_DIN_14	I
B6	HT_DIN_15	I
B7	HT_DIN_16	I
B8	VDD15	P
B9	GND	P
B10	HT_DIN_33	I
B11	HT_DIN_32	I
B12	HT_DOUT_13	O
B13	HT_DOUT_12	O
B14	VDD15	P
B15	GND	P
B16	HT_DOUT_17	O
B17	HT_CLK_KP	O
B18	HT_DOUT_34	O
B19	HT_ADDR_15	O
B20	GND	P
B21	VDD15	P
B22	HT_ADDR_18	O
B23	HT_ADDR_19	O
B24	FCT_ADDR_17	O
B25	FCT_ADDR_16	O
B26	GND	P
B27	VDD15	P
B28	FCT_DOUT_09	O
B29	FCT_DOUT_08	O
B30	FCT_DOUT_10	O
B31	FCT_DOUT_11	O
B32	VDD15	P
B33	GND	P
B34	GND	P
C1	VDD15	P
C2	VDD15	P
C3	HT_DIN_03	I
C4	HT_DIN_08	I
C5	HT_DIN_09	I
C6	HT_DIN_12	I
C7	HT_DIN_11	I
C8	VDD15	P
C9	GND	P
C10	HT_DIN_28	I
C11	HT_DIN_29	I
C12	HT_DOUT_08	O
C13	HT_DOUT_09	O
C14	VDD15	P
C15	GND	P
C16	HT_DOUT_21	O
C17	HT_CLK_KN	O
C18	HT_ADDR_00	O
C19	HT_ADDR_11	O

Pin	Signal	Type
C20	GND	P
C21	VDD15	P
C22	FCT_ADDR_01	O
C23	FCT_ADDR_00	O
C24	FCT_ADDR_18	O
C25	FCT_ADDR_19	O
C26	GND	P
C27	VDD15	P
C28	FCT_DOUT_12	O
C29	FCT_DOUT_13	O
C30	FCT_DOUT_17	O
C31	FCT_DOUT_16	O
C32	FCT_DOUT_22	O
C33	VDD15	P
C34	VDD15	P
D1	BLL_DIN_03	I
D2	BLL_CLK_CP	I
D3	BLL_DIN_11	I
D4	HT_DIN_02	I
D5	HT_DIN_04	I
D6	HT_DIN_06	I
D7	HT_DIN_07	I
D8	VDD15	P
D9	GND	P
D10	HT_DIN_26	I
D11	HT_DIN_27	I
D12	HT_DOUT_06	O
D13	HT_DOUT_07	O
D14	VDD15	P
D15	GND	P
D16	HT_DOUT_20	O
D17	HT_DOUT_30	O
D18	HT_ADDR_01	O
D19	HT_ADDR_10	O
D20	GND	P
D21	VDD15	P
D22	FCT_ADDR_02	O
D23	FCT_ADDR_03	O
D24	FCT_CLK_KN	O
D25	FCT_CLK_KP	O
D26	GND	P
D27	VDD15	P
D28	FCT_DOUT_18	O

Pin	Signal	Type
D29	FCT_DOUT_19	O
D30	FCT_DOUT_20	O
D31	FCT_DOUT_23	O
D32	FCT_DIN_05	I
D33	FCT_DIN_10	I
D34	FCT_CLK_CP	I
E1	BLL_DIN_04	I
E2	BLL_CLK_CN	I
E3	BLL_DIN_10	I
E4	BLL_DIN_15	I
E5	BLL_DIN_14	I
E6	HT_DIN_05	I
E7	HT_DIN_10	I
E8	VDD15	P
E9	GND	P
E10	HT_VREF_01	P
E11	HT_DIN_25	I
E12	HT_DOUT_05	O
E13	HT_DOUT_04	O
E14	VDD15	P
E15	GND	P
E16	HT_DOUT_22	O
E17	HT_DOUT_28	O
E18	HT_ADDR_02	O
E19	HT_ADDR_09	O
E20	GND	P
E21	VDD15	P
E22	FCT_ADDR_04	O
E23	FCT_ADDR_05	O
E24	FCT_DOUT_01	O
E25	FCT_DOUT_00	O
E26	GND	P
E27	VDD15	P
E28	FCT_DIN_08	I
E29	FCT_DOUT_21	O
E30	FCT_DIN_01	I
E31	FCT_DIN_00	I
E32	FCT_DIN_04	I
E33	FCT_DIN_09	I
E34	FCT_CLK_CN	I
F1	BLL_DIN_00	I
F2	BLL_DIN_06	I
F3	BLL_DIN_08	I

Pin	Signal	Type
F4	BLL_DIN_12	I
F5	BLL_DIN_16	I
F6	HT_DIN_00	I
F7	HT_VREF_00	P
F8	VDD15	P
F9	GND	P
F10	HT_DIN_21	I
F11	HT_DIN_22	I
F12	HT_DOUT_00	O
F13	HT_DOUT_01	O
F14	VDD15	P
F15	GND	P
F16	HT_DOUT_23	O
F17	HT_DOUT_29	O
F18	HT_ADDR_03	O
F19	HT_ADDR_08	O
F20	GND	P
F21	VDD15	P
F22	FCT_ADDR_09	O
F23	FCT_ADDR_08	O
F24	FCT_ADDR_15	O
F25	FCT_ADDR_14	O
F26	GND	P
F27	VDD15	P
F28	FCT_VREF_00	P
F29	FCT_DOUT_25	O
F30	FCT_DOUT_27	O
F31	FCT_DIN_02	I
F32	FCT_DIN_06	I
F33	FCT_DIN_11	I
F34	FCT_DIN_16	I
G1	BLL_DOUT_17	O
G2	BLL_DIN_05	I
G3	BLL_DIN_09	I
G4	BLL_DIN_13	I
G5	BLL_DIN_17	I
G6	HT_DIN_01	I
G7	VDD15	P
G8	VDD15	P
G9	GND	P
G10	HT_DIN_31	I
G11	HT_DIN_30	I
G12	HT_DOUT_19	O

Pin	Signal	Type
G13	HT_DOUT_18	O
G14	VDD15	P
G15	GND	P
G16	HT_DOUT_24	O
G17	HT_DOUT_25	O
G18	HT_ADDR_07	O
G19	HT_ADDR_06	O
G20	GND	P
G21	VDD15	P
G22	FCT_ADDR_10	O
G23	FCT_ADDR_11	O
G24	FCT_WR_N	O
G25	FCT_RD_N	O
G26	GND	P
G27	VDD15	P
G28	VDD15	P
G29	FCT_DOUT_24	O
G30	FCT_DOUT_26	O
G31	FCT_DIN_03	I
G32	FCT_DIN_07	I
G33	FCT_DIN_12	I
G34	FCT_DIN_15	I
H1	VDD15	P
H2	VDD15	P
H3	VDD15	P
H4	VDD15	P
H5	VDD15	P
H6	VDD15	P
H7	VDD15	P
H8	GND	P
H9	BLL_DIN_07	I
H10	HT_DIN_24	I
H11	HT_DIN_23	I
H12	HT_DOUT_11	O
H13	HT_DOUT_10	O
H14	VDD15	P
H15	GND	P
H16	HT_DOUT_33	O
H17	HT_DOUT_32	O
H18	HT_ADDR_04	O
H19	HT_ADDR_13	O
H20	GND	P
H21	VDD15	P

Pin	Signal	Type
H22	HT_WR_N	O
H23	HT_RD_N	O
H24	FCT_DOUT_07	O
H25	FCT_DOUT_06	O
H26	GND	P
H27	GND	P
H28	VDD15	P
H29	VDD15	P
H30	VDD15	P
H31	VDD15	P
H32	VDD15	P
H33	VDD15	P
H34	VDD15	P
J1	GND	P
J2	GND	P
J3	GND	P
J4	GND	P
J5	GND	P
J6	GND	P
J7	GND	P
J8	GND	P
J9	BLL_VREF	P
J10	HT_DIN_18	I
J11	HT_DIN_17	I
J12	HT_DOUT_03	O
J13	HT_DOUT_02	O
J14	VDD15	P
J15	GND	P
J16	HT_DOUT_27	O
J17	HT_DOUT_26	O
J18	HT_ADDR_05	O
J19	HT_ADDR_12	O
J20	GND	P
J21	VDD15	P
J22	FCT_ADDR_07	O
J23	FCT_ADDR_06	O
J24	FCT_DOUT_15	O
J25	FCT_DOUT_14	O
J26	FCT_DIN_14	I
J27	FCT_DIN_13	I
J28	GND	P
J29	GND	P
J30	GND	P

Pin	Signal	Type
J31	GND	P
J32	GND	P
J33	GND	P
J34	GND	P
K1	BLL_DOUT_02	O
K2	BLL_DOUT_05	O
K3	BLL_DOUT_08	O
K4	BLL_DOUT_10	O
K5	BLL_DOUT_13	O
K6	BLL_DOUT_16	O
K7	BLL_DOUT_03	O
K8	BLL_DOUT_11	O
K9	BLL_DIN_01	I
K26	FCT_DIN_21	I
K27	FLQS_DOUT_PRTY	O
K28	FCT_DIN_17	I
K29	FCT_DIN_19	I
K30	FCT_VREF_01	P
K31	FCT_DIN_24	I
K32	FCT_DIN_26	I
K33	FLQS_DOUT_01	O
K34	FLQS_DOUT_02	O
L1	BLL_DOUT_01	O
L2	BLL_DOUT_06	O
L3	BLL_DOUT_07	O
L4	BLL_DOUT_09	O
L5	BLL_DOUT_14	O
L6	BLL_DOUT_15	O
L7	BLL_DOUT_04	O
L8	BLL_DOUT_12	O
L9	BLL_DIN_02	I
L26	FCT_DIN_22	I
L27	FLQS_TIC_OUT	O
L28	FCT_DIN_18	I
L29	FCT_DIN_20	I
L30	FCT_DIN_23	I
L31	FCT_DIN_25	I
L32	FCT_DIN_27	I
L33	FLQS_DOUT_00	O
L34	FLQS_DOUT_03	O
M1	BLL_ADDR_13	O
M2	BLL_ADDR_15	O
M3	BLL_ADDR_18	O

Pin	Signal	Type
M4	BLL_CLK_KP	O
M5	BLL_ADDR_21	O
M6	BLL_ADDR_02	O
M7	BLL_DOUT_00	O
M8	BLL_ADDR_01	O
M9	BLL_ADDR_00	O
M26	FLQS_DOUT_06	O
M27	FLQS_DOUT_13	O
M28	FLQS_TIC_IN	I
M29	FLQS_DOUT_04	O
M30	FLQS_DOUT_09	O
M31	FLQS_CLKOUT	O
M32	FLQS_DOUT_11	O
M33	FLQS_DOUT_16	O
M34	FLQS_DOUT_17	O
N1	BLL_ADDR_12	O
N2	BLL_ADDR_14	O
N3	BLL_ADDR_19	O
N4	BLL_CLK_KN	O
N5	BLL_ADDR_20	O
N6	BLL_RD_N	O
N7	BLL_WR_N	O
N8	BLL_ADDR_17	O
N9	BLL_ADDR_16	O
N26	FLQS_DOUT_07	O
N27	FLQS_DOUT_14	O
N28	FLQS_DIN_14	I
N29	FLQS_DOUT_05	O
N30	FLQS_DOUT_08	O
N31	FLQS_DOUT_10	O
N32	FLQS_DOUT_12	O
N33	FLQS_DOUT_15	O
N34	FLQS_DOUT_18	O
P1	VDD15	P
P2	VDD15	P
P3	VDD15	P
P4	VDD15	P
P5	VDD15	P
P6	VDD15	P
P7	VDD15	P
P8	VDD15	P
P9	VDD15	P
P14	GND	P

Pin	Signal	Type
P15	VDD18	P
P16	GND	P
P17	VDD18	P
P18	GND	P
P19	VDD18	P
P20	GND	P
P21	VDD18	P
P26	VDD15	P
P27	VDD15	P
P28	VDD15	P
P29	VDD15	P
P30	VDD15	P
P31	VDD15	P
P32	VDD15	P
P33	VDD15	P
P34	VDD15	P
R1	GND	P
R2	GND	P
R3	GND	P
R4	GND	P
R5	GND	P
R6	GND	P
R7	GND	P
R8	GND	P
R9	GND	P
R14	VDD18	P
R15	GND	P
R16	VDD18	P
R17	GND	P
R18	VDD18	P
R19	GND	P
R20	VDD18	P
R21	GND	P
R26	GND	P
R27	GND	P
R28	GND	P
R29	GND	P
R30	GND	P
R31	GND	P
R32	GND	P
R33	GND	P
R34	GND	P
T1	BLL_ADDR_10	O

Pin	Signal	Type
T2	BLL_ADDR_11	O
T3	BLL_ADDR_07	O
T4	BLL_ADDR_06	O
T5	BLL_ADDR_05	O
T6	BLL_ADDR_04	O
T7	BXT_WR_N	O
T8	BLL_ADDR_09	O
T9	BLL_ADDR_08	O
T14	GND	P
T15	VDD18	P
T16	GND	P
T17	VDD18	P
T18	GND	P
T19	VDD18	P
T20	GND	P
T21	VDD18	P
T26	FLQS_VREF	P
T27	FLQS_DIN_01	I
T28	FLQS_DIN_09	I
T29	FLQS_DIN_10	I
T30	FLQS_DIN_11	I
T31	FLQS_DIN_13	I
T32	FLQS_DIN_12	I
T33	FLQS_DIN_PRTY	I
T34	FLQS_DOUT_19	O
U1	BXT_ADDR_19	O
U2	BXT_ADDR_18	O
U3	BXT_ADDR_20	O
U4	BXT_ADDR_21	O
U5	BXT_ADDR_00	O
U6	BXT_ADDR_01	O
U7	BLL_ADDR_03	O
U8	BXT_RD_N	O
U9	BXT_ADDR_02	O
U14	VDD18	P
U15	GND	P
U16	VDD18	P
U17	GND	P
U18	VDD18	P
U19	GND	P
U20	VDD18	P
U21	GND	P
U26	FLQS_DIN_07	I

Pin	Signal	Type
U27	FLQS_DIN_00	I
U28	FLQS_DIN_08	I
U29	FLQS_DIN_06	I
U30	FLQS_CLKIN	I
U31	FLQS_DIN_05	I
U32	FLQS_DIN_04	I
U33	FLQS_DIN_03	I
U34	FLQS_DIN_02	I
V1	BXT_ADDR_15	O
V2	BXT_CLK_KP	O
V3	BXT_CLK_KN	O
V4	BXT_ADDR_14	O
V5	BXT_ADDR_12	O
V6	BXT_ADDR_13	O
V7	BXT_ADDR_09	O
V8	BXT_ADDR_17	O
V9	BXT_ADDR_11	O
V14	GND	P
V15	VDD18	P
V16	GND	P
V17	VDD18	P
V18	GND	P
V19	VDD18	P
V20	GND	P
V21	VDD18	P
V26	TDO	O
V27	TMS	I
V28	PLL_2X_BPCLK	I
V29	TDI	I
V30	TCK	I
V31	RESERVE_0	I
V32	SCAN_EN	I
V33	IDDQ	I
V34	RESERVE_1	I
W1	BXT_DOUT_01	O
W2	BXT_DOUT_02	O
W3	BXT_ADDR_05	O
W4	BXT_ADDR_04	O
W5	BXT_ADDR_06	O
W6	BXT_ADDR_07	O
W7	BXT_ADDR_08	O
W8	BXT_ADDR_16	O
W9	BXT_ADDR_10	O

Pin	Signal	Type
W14	VDD18	P
W15	GND	P
W16	VDD18	P
W17	GND	P
W18	VDD18	P
W19	GND	P
W20	VDD18	P
W21	GND	P
W26	RESET_N	I
W27	PLL_SYS_REFCLK	I
W28	TRST_N	I
W29	PLL_BP_MODE	I
W30	PLL_MON	O
W31	PLL_CFG_OVR	I
W32	PLL_RST	I
W33	NC	
W34	PLL_VSSA	I
Y1	GND	P
Y2	GND	P
Y3	GND	P
Y4	GND	P
Y5	GND	P
Y6	GND	P
Y7	GND	P
Y8	GND	P
Y9	GND	P
Y14	GND	P
Y15	VDD18	P
Y16	GND	P
Y17	VDD18	P
Y18	GND	P
Y19	VDD18	P
Y20	GND	P
Y21	VDD18	P
Y26	GND	P
Y27	GND	P
Y28	GND	P
Y29	GND	P
Y30	GND	P
Y31	GND	P
Y32	GND	P
Y33	GND	P
Y34	GND	P

Pin	Signal	Type
AA1	VDD15	P
AA2	VDD15	P
AA3	VDD15	P
AA4	VDD15	P
AA5	VDD15	P
AA6	VDD15	P
AA7	VDD15	P
AA8	VDD15	P
AA9	VDD15	P
AA14	VDD18	P
AA15	GND	P
AA16	VDD18	P
AA17	GND	P
AA18	VDD18	P
AA19	GND	P
AA20	VDD18	P
AA21	GND	P
AA26	VDD33	P
AA27	VDD33	P
AA28	VDD33	P
AA29	VDD33	P
AA30	VDD33	P
AA31	VDD33	P
AA32	VDD33	P
AA33	VDD33	P
AA34	VDD33	P
AB1	BXT_DOUT_00	O
AB2	BXT_CLK_CP	I
AB3	BXT_DIN_00	I
AB4	LLT_DIN_09	I
AB5	LLT_DIN_06	I
AB6	LLT_DIN_04	I
AB7	BXT_ADDR_03	O
AB8	BXT_DIN_02	I
AB9	BXT_LLT_VREF	P
AB26	ZBUS_AD_00	B
AB27	ZBUS_AD_01	B
AB28	ZBUS_AD_12	B
AB29	ZBUS_AD_11	B
AB30	ZBUS_AD_06	B
AB31	ZBUS_AD_04	B
AB32	ZBUS_AD_03	B
AB33	ZBUS_AVALID_N	B

Pin	Signal	Type
AB34	PLL_VDDA	I
AC1	BXT_DIN_03	I
AC2	BXT_CLK_CN	I
AC3	LLT_DIN_10	I
AC4	LLT_DIN_08	I
AC5	LLT_DIN_07	I
AC6	LLT_DIN_03	I
AC7	BXT_DOUT_03	O
AC8	BXT_DIN_01	I
AC9	LLT_DIN_05	I
AC26	ZBUS_AD_08	B
AC27	ZBUS_AD_09	B
AC28	ZBUS_AD_13	B
AC29	ZBUS_AD_10	B
AC30	ZBUS_AD_07	B
AC31	ZBUS_AD_05	B
AC32	ZBUS_AD_02	B
AC33	ZBUS_CLK	I
AC34	NC	
AD1	LLT_CLK_CP	I
AD2	LLT_DIN_01	I
AD3	LLT_DOUT_09	O
AD4	LLT_DOUT_07	O
AD5	LLT_DOUT_04	O
AD6	LLT_DOUT_01	O
AD7	LLT_WR_N	O
AD8	LLT_DIN_00	I
AD9	LLT_DOUT_03	O
AD26	GPT_DIN_02	I
AD27	ZBUS_INT_N_01	O
AD28	ZBUS_DEVID_01	I
AD29	ZBUS_PRTY	B
AD30	VDD33	P
AD31	ZBUS_DVALID_N	B
AD32	VDD33	P
AD33	ZBUS_DEVID_03	I
AD34	ZBUS_AD_14	B
AE1	LLT_CLK_CN	I
AE2	LLT_DIN_02	I
AE3	LLT_DOUT_08	O
AE4	LLT_DOUT_06	O
AE5	LLT_DOUT_05	O
AE6	LLT_DOUT_00	O

Pin	Signal	Type
AE7	LLT_RD_N	O
AE8	LLT_DOUT_10	O
AE9	LLT_DOUT_02	O
AE26	GPT_DIN_01	I
AE27	ZBUS_INT_N_00	O
AE28	ZBUS_DEVID_00	I
AE29	ZBUS_DIR	O
AE30	ZBUS_INT_N_02	O
AE31	ZBUS_GNT_N	I
AE32	ZBUS_DEVID_04	I
AE33	ZBUS_DEVID_02	I
AE34	ZBUS_AD_15	B
AF1	GND	P
AF2	GND	P
AF3	GND	P
AF4	GND	P
AF5	GND	P
AF6	GND	P
AF7	GND	P
AF8	LLT_ADDR_16	O
AF9	LLT_ADDR_17	O
AF10	FPT_DIN_25	I
AF11	FPT_DIN_26	I
AF12	FPT_BW_N_01	O
AF13	FPT_BW_N_02	O
AF14	VDD15	P
AF15	GND	P
AF16	FPT_ADDR_07	O
AF17	FPT_ADDR_00	O
AF18	FPT_DOUT_21	O
AF19	FPT_DOUT_22	O
AF20	GND	P
AF21	VDD15	P
AF22	GPT_BW_N_00	O
AF23	GPT_BW_N_01	O
AF24	GPT_ADDR_00	O
AF25	GPT_ADDR_01	O
AF26	GPT_VREF	P
AF27	GND	P
AF28	GND	P
AF29	GND	P
AF30	GND	P
AF31	GND	P

Pin	Signal	Type
AF32	GND	P
AF33	GND	P
AF34	GND	P
AG1	VDD15	P
AG2	VDD15	P
AG3	VDD15	P
AG4	VDD15	P
AG5	VDD15	P
AG6	VDD15	P
AG7	VDD15	P
AG8	GND	P
AG9	GND	P
AG10	FPT_DIN_17	I
AG11	FPT_DIN_18	I
AG12	FPT_ADDR_15	O
AG13	FPT_ADDR_16	O
AG14	VDD15	P
AG15	GND	P
AG16	FPT_ADDR_08	O
AG17	FPT_DOUT_35	O
AG18	FPT_DOUT_29	O
AG19	FPT_DOUT_30	O
AG20	GND	P
AG21	VDD15	P
AG22	FPT_DOUT_05	O
AG23	FPT_DOUT_06	O
AG24	GPT_ADDR_08	O
AG25	GPT_ADDR_09	O
AG26	GPT_DIN_07	I
AG27	GND	P
AG28	VDD15	P
AG29	VDD15	P
AG30	VDD15	P
AG31	VDD15	P
AG32	VDD15	P
AG33	VDD15	P
AG34	VDD15	P
AH1	LLT_ADDR_18	O
AH2	LLT_ADDR_13	O
AH3	LLT_ADDR_07	O
AH4	LLT_CLK_KP	O
AH5	LLT_ADDR_00	O
AH6	FPT_DIN_34	I

Pin	Signal	Type
AH7	VDD15	P
AH8	VDD15	P
AH9	GND	P
AH10	FPT_DIN_11	I
AH11	FPT_DIN_12	I
AH12	FPT_DIN_01	I
AH13	FPT_DIN_00	I
AH14	VDD15	P
AH15	GND	P
AH16	FPT_ADDR_01	O
AH17	FPT_ADDR_02	O
AH18	FPT_DOUT_20	O
AH19	FPT_DOUT_19	O
AH20	GND	P
AH21	VDD15	P
AH22	FPT_DOUT_13	O
AH23	FPT_DOUT_14	O
AH24	GPT_ADDR_14	O
AH25	GPT_ADDR_15	O
AH26	GND	P
AH27	VDD15	P
AH28	VDD15	P
AH29	GPT_DOUT_01	O
AH30	GPT_DIN_17	I
AH31	GPT_DIN_13	I
AH32	GPT_DIN_09	I
AH33	GPT_DIN_05	I
AH34	ZBUS_REQ_N	O
AJ1	LLT_ADDR_19	O
AJ2	LLT_ADDR_12	O
AJ3	LLT_ADDR_06	O
AJ4	LLT_CLK_KN	O
AJ5	LLT_ADDR_01	O
AJ6	FPT_DIN_35	I
AJ7	LLT_ADDR_09	O
AJ8	VDD15	P
AJ9	GND	P
AJ10	FPT_DIN_04	I
AJ11	FPT_DIN_05	I
AJ12	FPT_BW_N_03	O
AJ13	FPT_WR_N	O
AJ14	VDD15	P
AJ15	GND	P

Pin	Signal	Type
AJ16	FPT_ADDR_03	O
AJ17	FPT_DOUT_34	O
AJ18	FPT_DOUT_24	O
AJ19	FPT_DOUT_18	O
AJ20	GND	P
AJ21	VDD15	P
AJ22	GPT_RD_N	O
AJ23	GPT_ADDR_20	O
AJ24	GPT_ADDR_07	O
AJ25	GPT_ADDR_06	O
AJ26	GND	P
AJ27	VDD15	P
AJ28	GPT_DOUT_10	O
AJ29	GPT_DOUT_00	O
AJ30	GPT_DIN_16	I
AJ31	GPT_DIN_12	I
AJ32	GPT_DIN_08	I
AJ33	GPT_DIN_06	I
AJ34	GPT_DIN_00	I
AK1	LLT_ADDR_15	O
AK2	LLT_ADDR_10	O
AK3	LLT_ADDR_04	O
AK4	LLT_ADDR_02	O
AK5	LLT_ADDR_03	O
AK6	FPT_DIN_31	I
AK7	LLT_ADDR_08	O
AK8	VDD15	P
AK9	GND	P
AK10	FPT_DIN_13	I
AK11	FPT_DIN_14	I
AK12	FPT_BW_N_00	O
AK13	FPT_RD_N	O
AK14	VDD15	P
AK15	GND	P
AK16	FPT_ADDR_04	O
AK17	FPT_DOUT_33	O
AK18	FPT_DOUT_23	O
AK19	FPT_DOUT_17	O
AK20	GND	P
AK21	VDD15	P
AK22	GPT_WR_N	O
AK23	FPT_DOUT_00	O
AK24	GPT_ADDR_10	O

Pin	Signal	Type
AK25	GPT_ADDR_11	O
AK26	GND	P
AK27	VDD15	P
AK28	GPT_DOUT_11	O
AK29	GPT_DOUT_05	O
AK30	GPT_DIN_14	I
AK31	GPT_DIN_15	I
AK32	GPT_DIN_10	I
AK33	GPT_CLK_CN	I
AK34	GPT_DIN_04	I
AL1	LLT_ADDR_14	O
AL2	LLT_ADDR_11	O
AL3	LLT_ADDR_05	O
AL4	FPT_DIN_33	I
AL5	FPT_DIN_30	I
AL6	FPT_DIN_29	I
AL7	FPT_VREF_01	P
AL8	VDD15	P
AL9	GND	P
AL10	FPT_VREF_00	P
AL11	FPT_DIN_10	I
AL12	FPT_ADDR_20	O
AL13	FPT_ADDR_19	O
AL14	VDD15	P
AL15	GND	P
AL16	FPT_ADDR_05	O
AL17	FPT_DOUT_32	O
AL18	FPT_DOUT_25	O
AL19	FPT_DOUT_15	O
AL20	GND	P
AL21	VDD15	P
AL22	FPT_DOUT_02	O
AL23	FPT_DOUT_01	O
AL24	GPT_CLK_KP	O
AL25	GPT_CLK_KN	O
AL26	GND	P
AL27	VDD15	P
AL28	GPT_DOUT_07	O
AL29	GPT_DOUT_06	O
AL30	GPT_DOUT_04	O
AL31	GPT_DOUT_02	O
AL32	GPT_DIN_11	I
AL33	GPT_CLK_CP	I

Pin	Signal	Type
AL34	GPT_DIN_03	I
AM1	VDD15	P
AM2	VDD15	P
AM3	FPT_DIN_32	I
AM4	FPT_DIN_27	I
AM5	FPT_DIN_28	I
AM6	FPT_DIN_24	I
AM7	FPT_DIN_23	I
AM8	VDD15	P
AM9	GND	P
AM10	FPT_DIN_09	I
AM11	FPT_DIN_08	I
AM12	FPT_ADDR_17	O
AM13	FPT_ADDR_18	O
AM14	VDD15	P
AM15	GND	P
AM16	FPT_ADDR_06	O
AM17	FPT_DOUT_31	O
AM18	FPT_DOUT_26	O
AM19	FPT_DOUT_16	O
AM20	GND	P
AM21	VDD15	P
AM22	FPT_DOUT_04	O
AM23	FPT_DOUT_03	O
AM24	GPT_ADDR_13	O
AM25	GPT_ADDR_12	O
AM26	GND	P
AM27	VDD15	P
AM28	GPT_DOUT_12	O
AM29	GPT_DOUT_13	O
AM30	GPT_DOUT_09	O
AM31	GPT_DOUT_08	O
AM32	GPT_DOUT_03	O
AM33	VDD15	P
AM34	VDD15	P
AN1	GND	P
AN2	GND	P
AN3	VDD15	P
AN4	FPT_DIN_22	I
AN5	FPT_DIN_21	I
AN6	FPT_DIN_19	I
AN7	FPT_DIN_20	I
AN8	VDD15	P

Pin	Signal	Type
AN9	GND	P
AN10	FPT_DIN_06	I
AN11	FPT_DIN_07	I
AN12	FPT_ADDR_14	O
AN13	FPT_ADDR_13	O
AN14	VDD15	P
AN15	GND	P
AN16	FPT_ADDR_10	O
AN17	FPT_CLK_KP	O
AN18	FPT_DOUT_27	O
AN19	FPT_DOUT_12	O
AN20	GND	P
AN21	VDD15	P
AN22	FPT_DOUT_07	O
AN23	FPT_DOUT_08	O
AN24	GPT_ADDR_16	O
AN25	GPT_ADDR_17	O
AN26	GND	P
AN27	VDD15	P
AN28	GPT_DOUT_17	O
AN29	GPT_DOUT_16	O
AN30	GPT_DOUT_15	O
AN31	GPT_DOUT_14	O
AN32	VDD15	P
AN33	GND	P
AN34	GND	P
AP2	GND	P
AP3	VDD15	P
AP4	FPT_CLK_CN	I
AP5	FPT_CLK_CP	I
AP6	FPT_DIN_16	I
AP7	FPT_DIN_15	I
AP8	VDD15	P
AP9	GND	P
AP10	FPT_DIN_03	I
AP11	FPT_DIN_02	I
AP12	FPT_ADDR_12	O
AP13	FPT_ADDR_11	O
AP14	VDD15	P
AP15	GND	P
AP16	FPT_ADDR_09	O
AP17	FPT_CLK_KN	O
AP18	FPT_DOUT_28	O

Pin	Signal	Type
AP19	FPT_DOUT_11	O
AP20	GND	P
AP21	VDD15	P
AP22	FPT_DOUT_10	O
AP23	FPT_DOUT_09	O
AP24	GPT_ADDR_19	O
AP25	GPT_ADDR_18	O
AP26	GND	P
AP27	VDD15	P
AP28	GPT_ADDR_05	O
AP29	GPT_ADDR_04	O
AP30	GPT_ADDR_02	O
AP31	GPT_ADDR_03	O
AP32	VDD15	P
AP33	GND	P

89TTM553 Package

The package is an LSI Logic FPBGA-HP, having 960 pins, with 1 mm pitch; a 34 ×34 pin array; and a 35 × 35 mm enclosure. Figure 5 shows the package geometry.

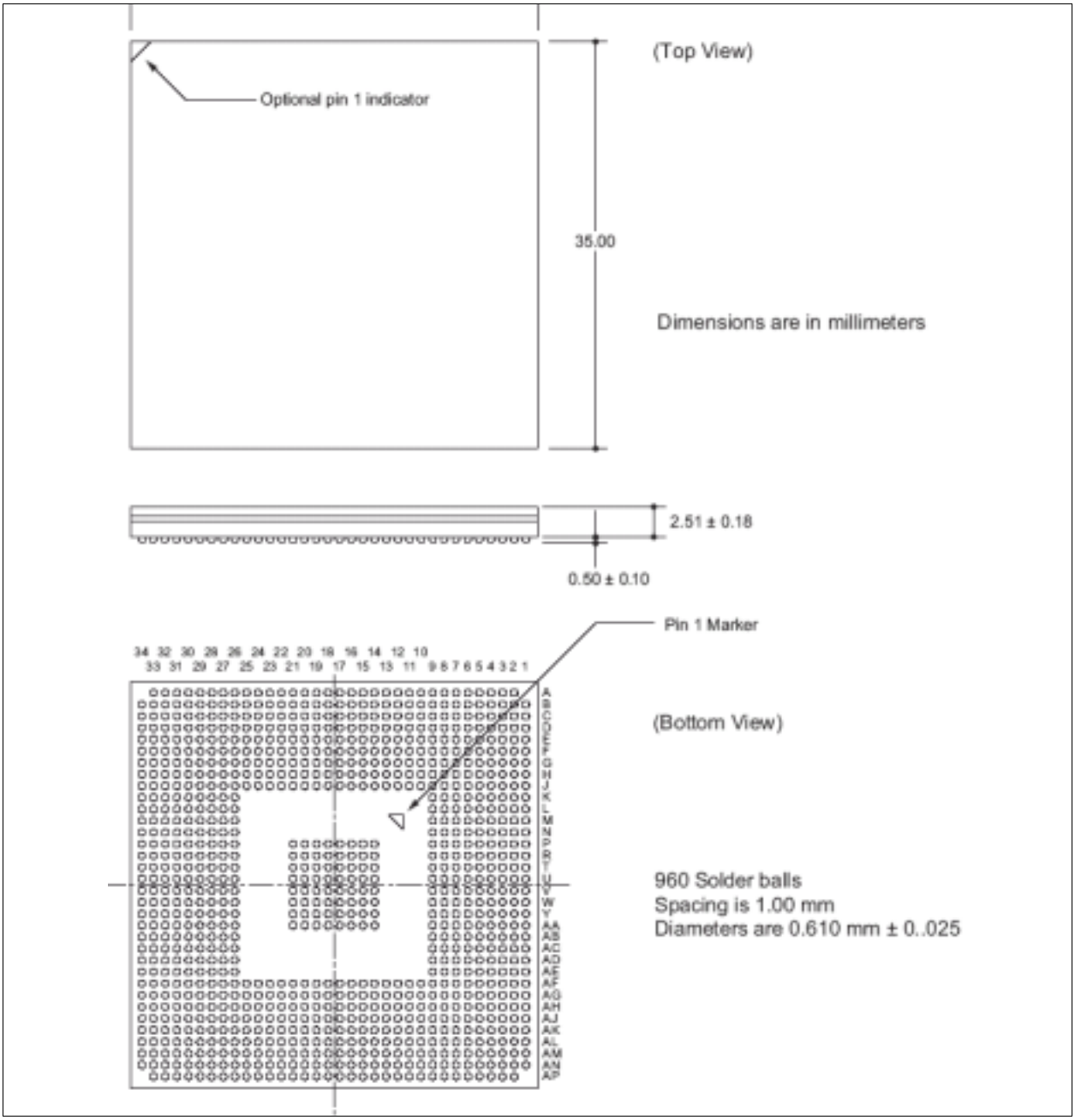
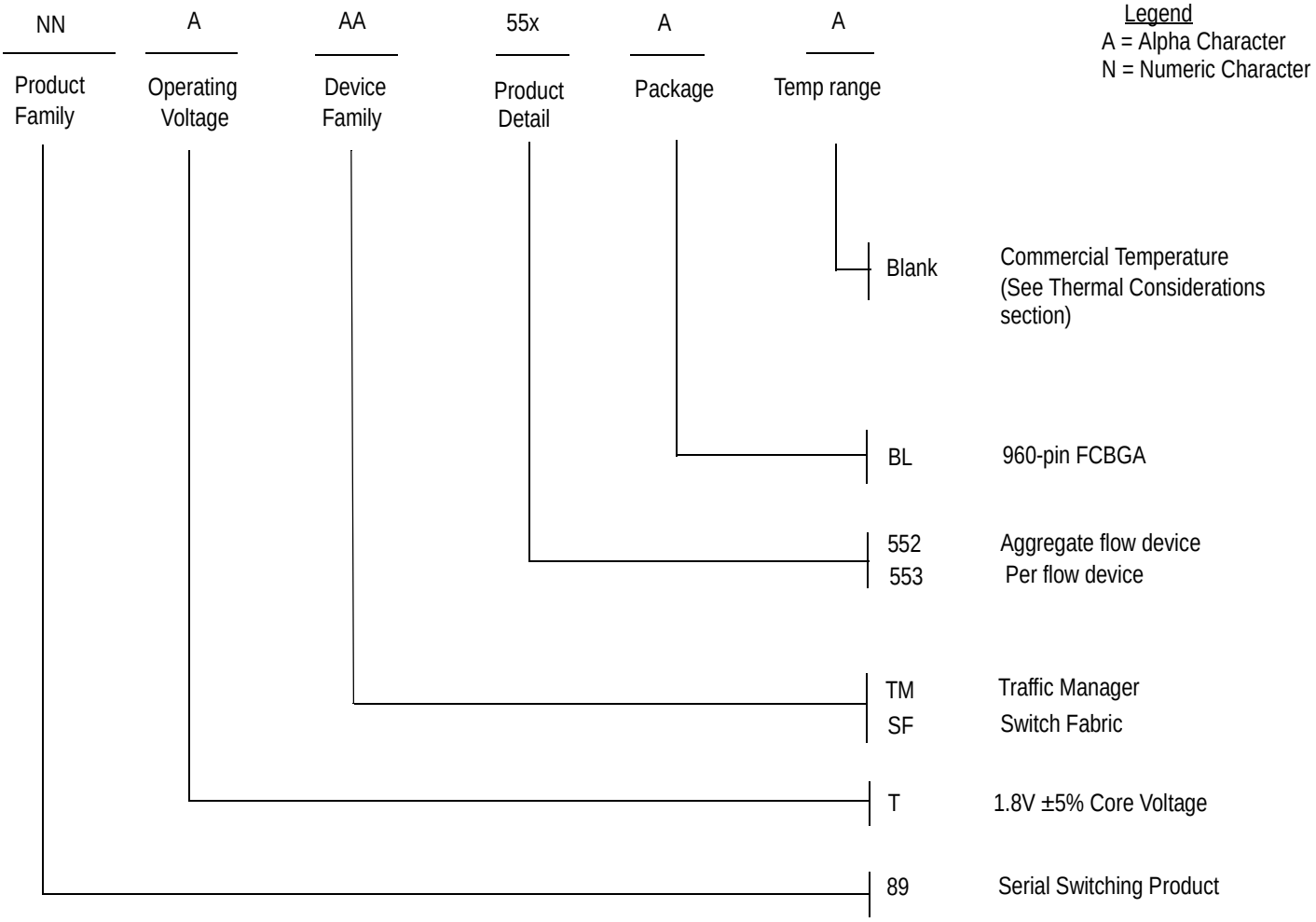


Figure 5 89TTM553 Package Diagram

Ordering Information



Valid Combinations

89TTM553BL	960-pin FCBGA package, Commercial Temperature

Revision History

November 23, 2004: Initial publication by IDT.

January 12, 2005: On page 14, deleted reference to LVDS in the Core PLL Frequency Setting heading.

March 3, 2005: In Table 11, changed frequency for PLL_SYS_REFCLK from 125 to 100 MHz.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

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