# TP70H240G4PZS

700V SuperGaN® GaN FET with Slew-Rate Limiter in DPAK Package (source tab)

## Description

The TP70H240G4PZS 700V, 240mΩ Gallium Nitride (GaN) FET is a normally-off switch that uses Renesas' Gen IV plus platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior performance, standard drive, ease of adoption and reliability.

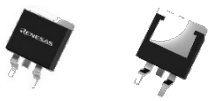
The Gen IV plus SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

This product is specifically designed for flyback applications and features an integrated slew-rate limiter for improved EMI performance.

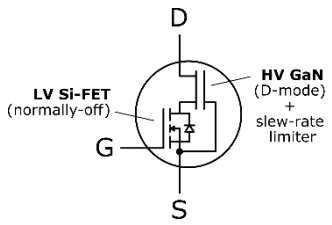
## Benefits

- Superior normally off architecture with D-mode GaN HEMT
- Compatible with standard silicon drivers
- Enhanced noise immunity with high threshold voltage and no negative gate drive requirement
- No external slew rate control circuit needed
- Enables high-efficiency, high power density, and reliable power conversion in hard- and soft-switching circuits
- Low standby power consumption
- Facilitates cost-effective GaN adoption, reducing system size, weight, and costs

## Product Diagrams



**TP70H240G4PZS DPAK**




**Cascode Device Structure**

## Features

- Ultra-fast switching Gen IV plus GaN
- JEDEC-qualified GaN technology
- Robust design, defined by:
  - Transient over-voltage capability
  - Operation with E-mode gate drivers without need for Zener protection
  - Integrated turn-on slew-rate limiter (< 4V/ns)
- Extremely low crossover loss
- Negligible Qrr
- RoHS compliant and Halogen-free packaging
- Low reverse conduction drop $V_{SD}$
- 2kV ESD HBM rating

## Applications

- Power adapters
- Flyback Converters
- Auxiliary power supplies

## Specifications

| | |
|---|---|
| $V_{DS}$ (V) | 700 |
| $V_{DSS(TR)}$(V) maximum | 800 |
| $R_{DS(on)}$ (mΩ) | 240 |
| $Q_{OSS}$ (nC) typical | 16.3 |
| $Q_G$ (nC) typical | 5.4 |

# Contents



## Figures

# 1. Symbol Pin Information

## 1.1 Pin Assignments

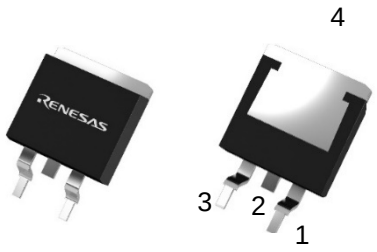



**Figure 1. Pin Assignments**

## 1.2 Pin Descriptions

| Pin Number | Primary Pin Name | Primary Electrical Type | Description |
|---|---|---|---|
| 1 | G | Input | Gate. |
| 2 | S | - | Source. |
| 3 | D | Power | Drain. |
| 4 | S | Power | Source. |

# 2. Specifications

## 2.1 Absolute Maximum Ratings

$T_c$ = 25°C unless otherwise stated.

***Caution***: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

| Symbol | Parameter | Minimum | Maximum | Test Condition | Unit |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage | - | 700 | $V_{GS}$ = 0V,Test as per JEP-198 | V |
| $V_{DSS(TR)}$ | Transient Drain to Source Voltage | - | 900 | $V_{GS}$ = 0V, ≤ 10µs, ≤ 1% Duty Cycle, cumulative 60s (60 million pulses) | |
| $V_{DSS, pulsed}$ | Drain to Source Voltage, Pulsed | - | 750 | $V_{GS}$ = 0V, ≤ 1µs ,≤ 1% Duty Cycle, cumulative 10h (36 billion pulses) | |
| $V_{GSS}$ | Gate to Source Voltage | -20 | +20 | - | |
| $P_D$ | Maximum Power Dissipation | - | 30.2 | $T_C$ = 25°C | W |
| $I_D$ | Continuous Drain Current at $T_C$ = 25°C | - | 7.8 | $V_{GS}$ = 6V, forward and reverse conduction | A |
| | Continuous Drain Current at $T_C$ = 100°C | - | 4.9 | | |
| $I_{D(PULSE)}$ | Pulsed Drain Current at $T_C$ = 25°C | - | 26 | $V_{GS}$ = 6V, pulse width = 10µs | |
| | Pulsed Drain Current at $T_C$ = 100°C | - | 18 | | |
| $I_{SD(PULSE)}$ | Pulsed Reverse Drain Current at $T_C$ = 25°C | - | 26 | $V_{GS}$ = 0V, pulse width = 10µs | A |
| | Pulsed Reverse Drain Current at $T_C$ = 100°C | - | 18 | | |
| $T_J$ | Operating Temperature Junction | -55 | +150 | - | °C |
| $T_S$ | Storage Temperature | -55 | +150 | Max shelf life depends on storage conditions | °C |
| $T_{SOLD}$ | Reflow Soldering Temperature [1] | - | 260 | - | °C |

1. Reflow MSL3.

## 2.2 Thermal Specifications

| Symbol | Parameter | Typical Value | Test Condition | Unit |
|---|---|---|---|---|
| $R_{\Theta JC}$ | Junction-to-case | 4.1 | - | °C/W |
| $R_{\Theta JA}$ | Junction-to-ambient | 50 | Device on 40 × 40 mm × 1.5mm epoxy PCB FR4 with 6 cm² (one layer, 70µm thickness) copper area for tab (source) connection and cooling. PCB is vertical without air stream cooling. | |

## 2.3 Electrical Specifications – Forward Characteristics

$T_J$ = 25°C unless otherwise stated.

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{DSS(BL)}$ | Maximum Drain-Source Voltage | $V_{GS}$ = 0V | 700 | - | - | V |
| $V_{GS(th)}$ | Gate Threshold | $V_{DS}$ = $V_{GS}$, $I_D$ = 0.5mA | 1.5 | 2 | 2.5 | V |
| $\Delta V_{GS(th)}/T_J$ | Gate Threshold Voltage Temperature Coefficient | | - | -7.6 | - | mV/°C |
| $R_{DS(on)eff}$ | Drain-Source on-Resistance | $V_{GS}$ = 6V, $I_D$ = 3A, $T_J$ = 25°C | - | 240 | 320 | mΩ |
| | | $V_{GS}$ = 6V, $I_D$ = 3A, $T_J$ = 150°C | - | 492 | - | |
| $I_{DSS}$ | Drain-to-Source Leakage Current | $V_{DS}$ = 700V, $V_{GS}$ = 0V, $T_J$ = 25°C | - | 1 | 10 | µA |
| | | $V_{DS}$ = 700V, $V_{GS}$ = 0V, $T_J$ = 150°C | - | 3 | - | |
| $I_{GSS}$ | Gate-to-Source Forward Leakage Current [1] | $V_{GS}$ = 20V | - | - | 10 | µA |
| | Gate-to-Source Reverse Leakage Current [1] | $V_{GS}$ = -20V | - | - | -10 | |
| $I_{GSS}$ | Gate-to-Source Forward Leakage Current [1] | $V_{GS}$ = 6V | - | - | 0.1 | µA |
| | Gate-to-Source Reverse Leakage Current [1] | $V_{GS}$ = -6V | - | - | -0.1 | |
| $C_{ISS}$ | Input Capacitance | $V_{GS}$ = 0V, $V_{DS}$ = 400V, *f* = 1MHz | - | 455 | - | pF |
| $C_{OSS}$ | Output Capacitance | | - | 15.1 | - | |
| $C_{RSS}$ | Reverse Transfer Capacitance | | - | 1 | - | |
| $C_{O(er)}$ | Output Capacitance, Energy Related [2] | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 400V | - | 22.2 | - | pF |
| $C_{O(tr)}$ | Output Capacitance, Time Related [3] | | - | 40.2 | - | |
| $Q_G$ | Total Gate Charge | $V_{DS}$ = 400V, $V_{GS}$ = 0V to 6V, $I_D$ = 3A | - | 5.4 | - | nC |
| $Q_{GS}$ | Gate-source Charge | | - | 1.4 | - | |
| $Q_{GD}$ | Gate-drain Charge | | - | 2.1 | - | |
| $Q_{OSS}$ | Output Charge | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 400V | - | 16.3 | - | nC |
| $t_{D(on)}$ | Turn-on Delay | $V_{DS}$ = 400V, $V_{GS}$ = 0 to 6V, $R_{G\_on}$ = 100Ω, $R_{G\_off}$ = 0Ω, $I_D$ = 3A (see Figure 15) | - | 72 | - | ns |
| $t_R$ | Rise Time | | - | 85.6 | - | |
| $t_{D(off)}$ | Turn-off Delay | | - | 15.6 | - | |
| $t_F$ | Fall Time | | - | 9.6 | - | |

1. MOSFET has integrated ESD Protection Circuit
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

## 2.4 Electrical Specifications – Reverse Device

$T_J$ = 25°C unless otherwise stated.

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{SD}$ | Reverse voltage | $V_{GS}$ = 0V, $I_S$ = 3A | - | 1.6 | - | V |
| | | $V_{GS}$ = 0V, $I_S$ = 1.5A | - | 1.2 | - | |

*Note*: Reverse recovery charge is negligible enabled by the LV Si FET technology.

# 3. Typical Performance Graphs

$T_C$ = 25°C unless otherwise stated.

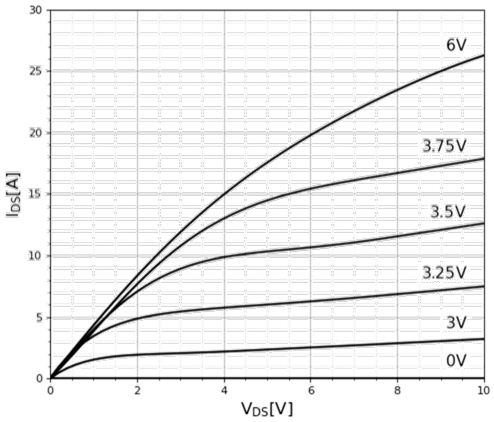



**Figure 2. Typical Output Characteristics, $T_J$ = 25°C**

Parameter: $V_{GS}$

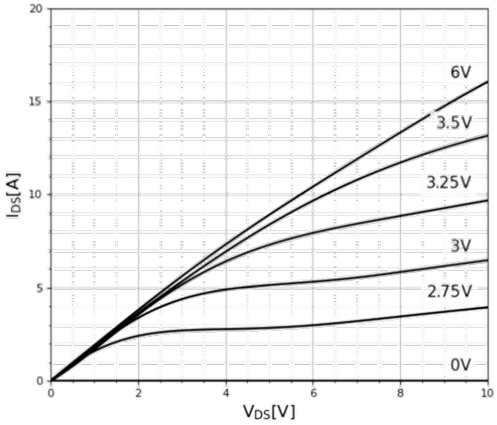



**Figure 3. Typical Output Characteristics, $T_J$ = 150°C**

Parameter: $V_{GS}$

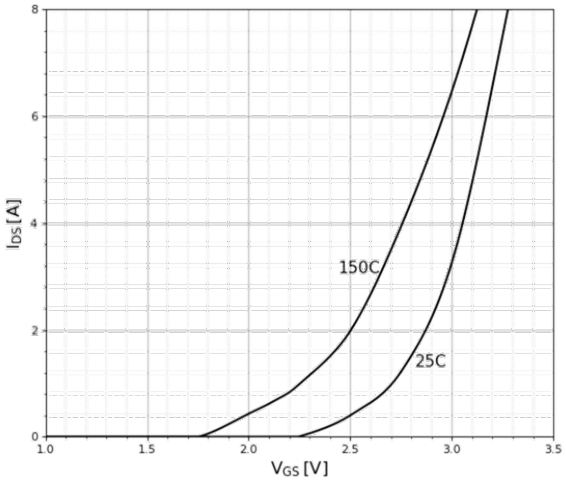



**Figure 4. Typical Transfer Characteristics,**

$V_{DS}$ = 10V, Parameter: $T_J$

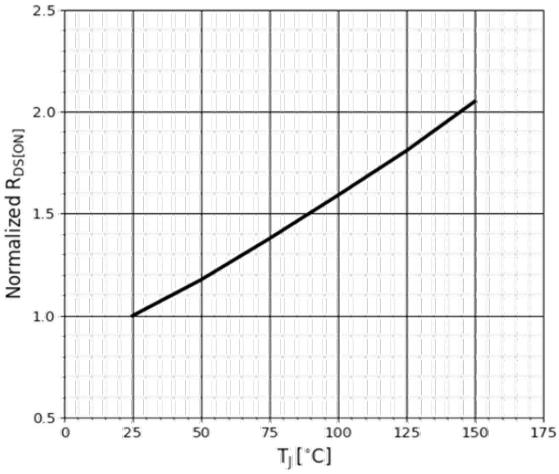



**Figure 5. Normalized On-Resistance,**

$I_D$ = 3A, $V_{GS}$ = 6V

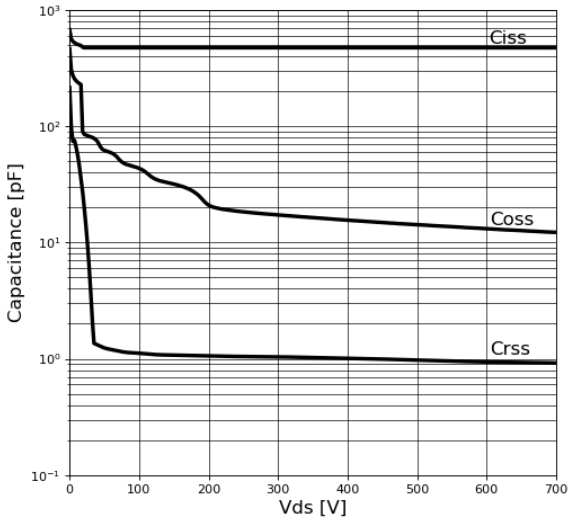



**Figure 6. Typical Capacitance,**
$V_{GS}$ = 0V, f = 100kHz

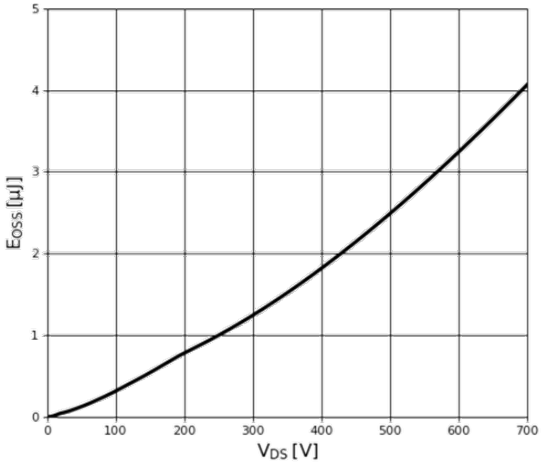



**Figure 7. Typical $C_{OSS}$ Stored Energy**

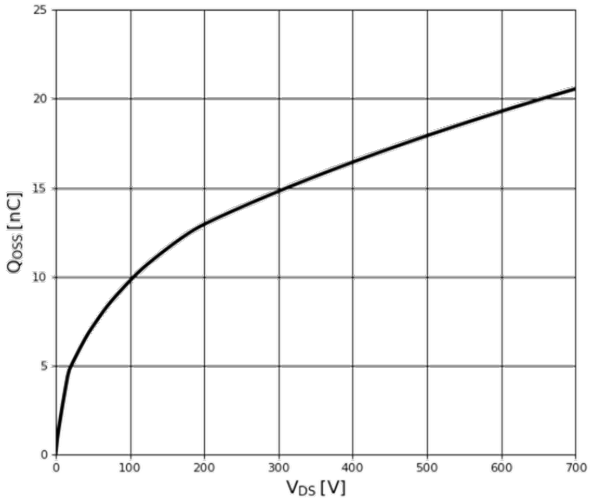



**Figure 8. Typical $Q_{OSS}$**

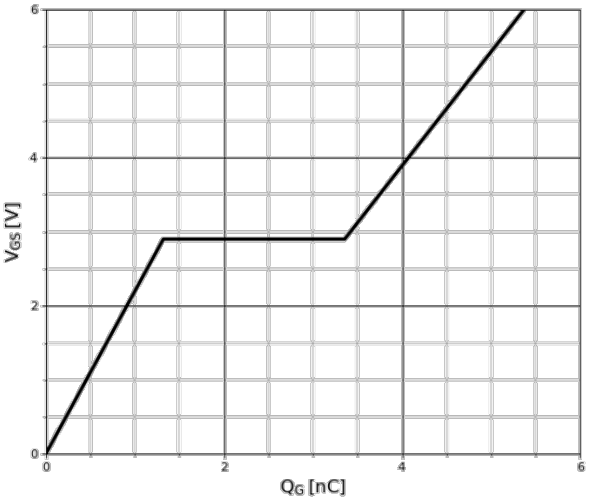



**Figure 9. Typical Gate Charge,**
$I_{DS}$ = 3A, $V_{DS}$ = 400V

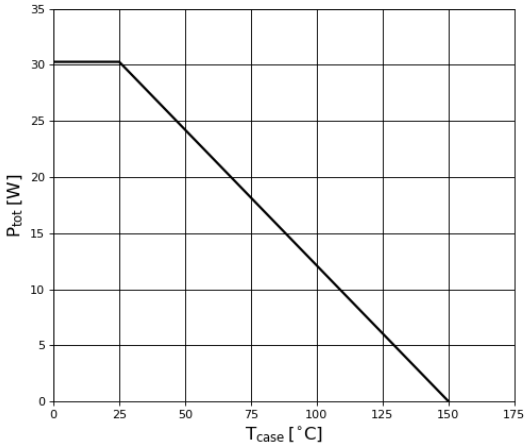



**Figure 10. Power Dissipation**

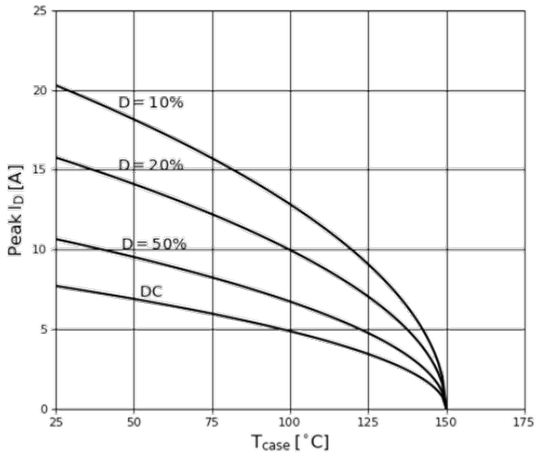



**Figure 11. Current Derating,**

Pulse width ≤ 10µs, $V_{GS}$ ≥ 6V

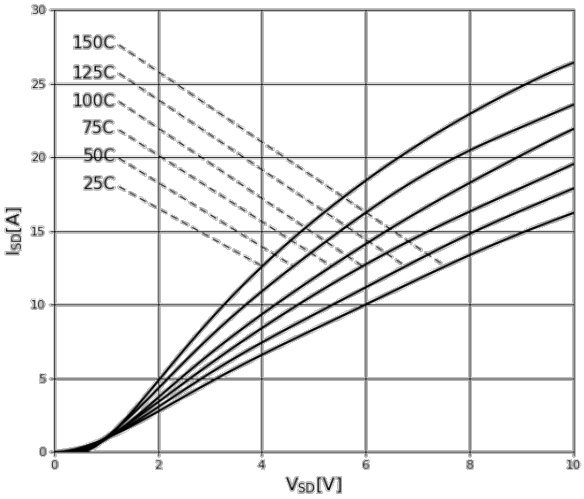



**Figure 12. Forward Characteristics of Rev. Diode**

$I_S = f(V_{SD})$, Parameter: $T_J$

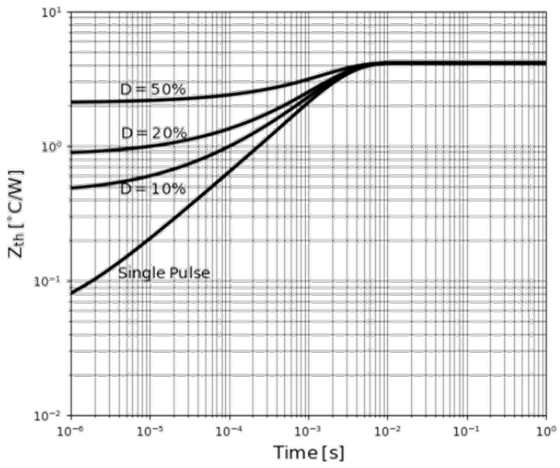



**Figure 13. Transient Thermal Resistance**

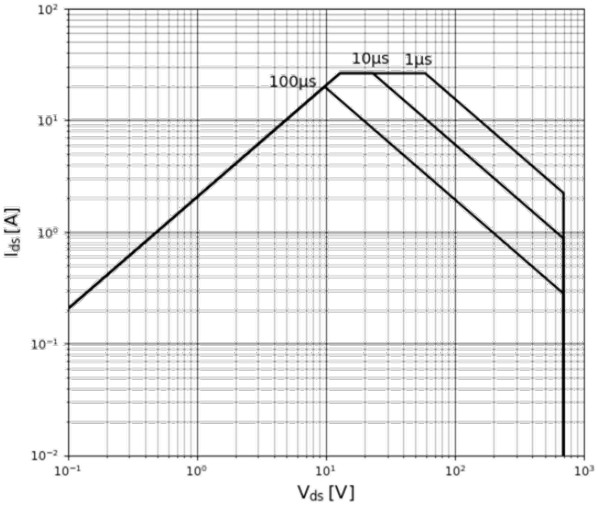



**Figure 14. Safe Operating Area $T_C$ = 25°C**

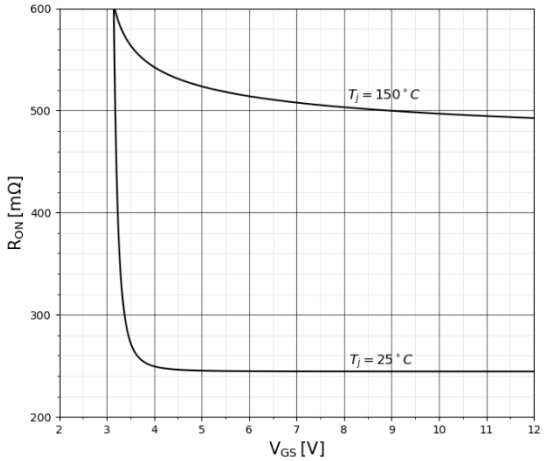



**Figure 15. $R_{ds(on)}$ = *f*($V_{gs}$);$I_D$ = 3A**

# 4. Test Circuits and Waveforms

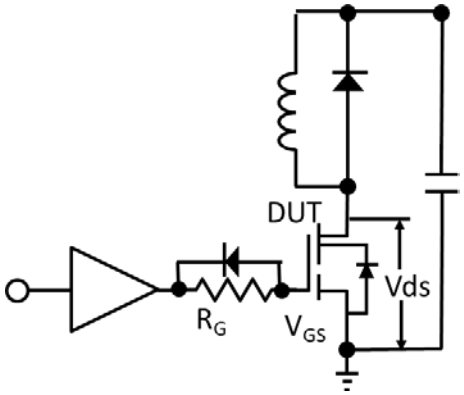



**Figure 16. Switching Time Test Circuit**

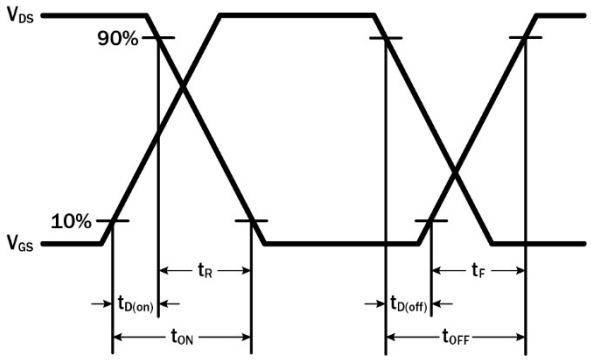
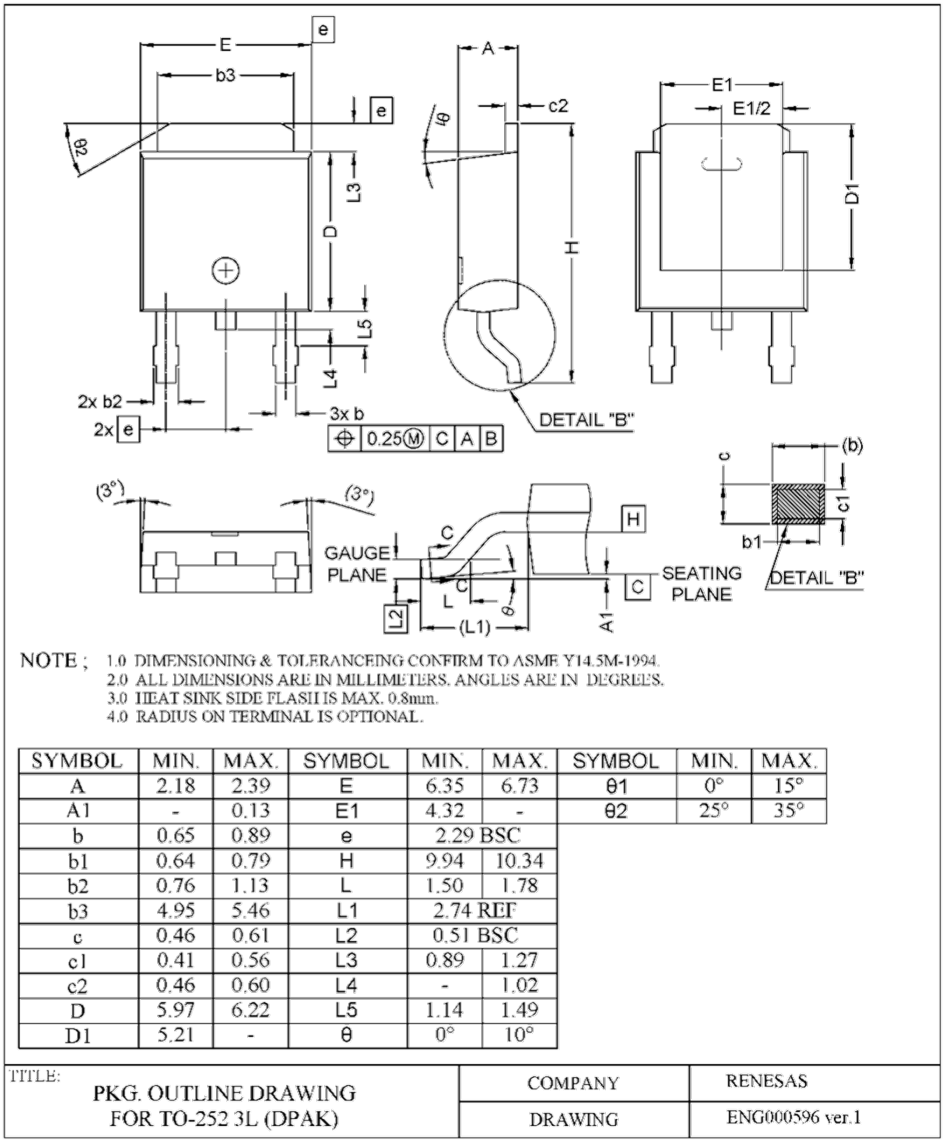



**Figure 17. Switching Time Waveform**

# 5. Package Outline Drawings




NOTE ; 1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3.0 HEAT SINK SIDE FLASH IS MAX. 0.8mm.
4.0 RADIUS ON TERMINAL IS OPTIONAL.

| SYMBOL | MIN. | MAX. | SYMBOL | MIN. | MAX. | SYMBOL | MIN. | MAX. |
|---|---|---|---|---|---|---|---|---|
| A | 2.18 | 2.39 | E | 6.35 | 6.73 | θ1 | 0° | 15° |
| A1 | - | 0.13 | E1 | 4.32 | - | θ2 | 25° | 35° |
| b | 0.65 | 0.89 | e | 2.29 BSC | | | | |
| b1 | 0.64 | 0.79 | H | 9.94 | 10.34 | | | |
| b2 | 0.76 | 1.13 | L | 1.50 | 1.78 | | | |
| b3 | 4.95 | 5.46 | L1 | 2.74 REF | | | | |
| c | 0.46 | 0.61 | L2 | 0.51 BSC | | | | |
| c1 | 0.41 | 0.56 | L3 | 0.89 | 1.27 | | | |
| c2 | 0.46 | 0.60 | L4 | - | 1.02 | | | |
| D | 5.97 | 6.22 | L5 | 1.14 | 1.49 | | | |
| D1 | 5.21 | - | θ | 0° | 10° | | | |

| TITLE: | COMPANY | RENESAS |
|---|---|---|
| PKG. OUTLINE DRAWING FOR TO-252 3L (DPAK) | DRAWING | ENG000596 ver.1 |

**Figure 18. Package Outline Drawing – DPAK**

# 6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the GaN Power Solutions page.

# 7. Ordering Information

| Orderable Part Number | Number of Pins | Package Type | Package Code/POD Number |
|---|---|---|---|
| TP70H240G4PZS-TR [1] | 3 | DPAK | ENG000596 |

1. "-TR" suffix refers to tape and reel.

# 8. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.01 | Aug 7, 2026 | Minor edits and reformatting. |
| 1.00 | Jul 6, 2026 | Initial release. |

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