

TP70H130G4PPS

700V SuperGaN® GaN FET in TO-220 Package (source tab)

Description

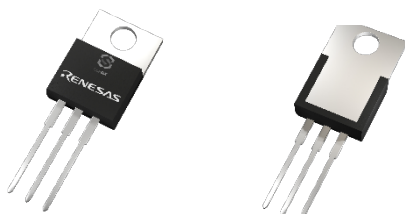
The TP70H130G4PPS 700V, 130mΩ Gallium Nitride (GaN) FET is a normally-off switch that uses Renesas' Gen IV plus platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior performance, standard drive, ease of adoption and reliability.

The Gen IV plus SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

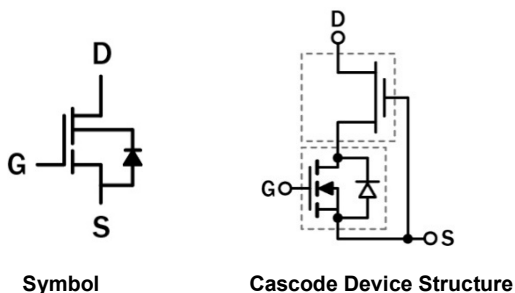
Benefits

- Superior normally off architecture with D-mode GaN HEMT
- Compatible with standard silicon drivers
- Enhanced noise immunity with high threshold voltage and no negative gate drive requirement
- Enables high-efficiency, high power density, and reliable power conversion in hard- and soft-switching circuits.
- Facilitates cost-effective GaN adoption, reducing system size, weight, and costs

Product Diagrams



TP70H130G4PPS TO-220



Features

- Ultra-fast switching Gen IV plus GaN
- JEDEC-qualified GaN technology
- Robust design, defined by
 - Transient over-voltage capability
 - Operation with E-mode gate drivers without need for Zener protection.
- Extremely low crossover loss
- Negligible Qrr
- RoHS compliant and Halogen-free packaging
- Low reverse conduction drop V_{SD}

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting



Specifications

V_{DS} (V)	700
$V_{DSS(TR)}$ (V) maximum	800
$R_{DS(on)}$ (mΩ) maximum	163
Q_{OSS} (nC) typical	29.2
Q_G (nC) typical	10.7

Contents

1. Pin Information	3
1.1 Pin Assignments	3
1.2 Pin Descriptions	3
2. Specifications	4
2.1 Absolute Maximum Ratings	4
2.2 Thermal Specifications	4
2.3 Electrical Specifications – Forward Device	5
2.4 Electrical Specifications – Reverse Device	5
3. Typical Performance Graphs	6
4. Test Circuits and Waveforms	9
5. Package Outline Drawings	10
6. Related Information	10
7. Ordering Information	11
8. Revision History	11

Figures

Figure 1. Pin Assignments	3
Figure 2. Typical Output Characteristics, $T_J = 25^\circ\text{C}$ Parameter: V_{GS}	6
Figure 3. Typical Output Characteristics, $T_J = 150^\circ\text{C}$ Parameter: V_{GS}	6
Figure 4. Typical Transfer Characteristics, $V_{DS} = 10\text{V}$, Parameter: T_J	6
Figure 5. Normalized On-Resistance, $I_D = 4\text{A}$, $V_{GS} = 9\text{V}$	6
Figure 6. Typical Capacitance, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	7
Figure 7. Typical C_{OSS} Stored Energy	7
Figure 8. Typical Q_{OSS}	7
Figure 9. Typical Gate Charge, $I_{DS} = 4\text{A}$, $V_{DS} = 400\text{V}$	7
Figure 10. Power Dissipation	8
Figure 11. Current Derating, Pulse width $\leq 10\mu\text{s}$, $V_{GS} \geq 9\text{V}$	8
Figure 12. Forward Characteristics of Rev. Diode, $I_S = f(V_{SD})$, Parameter: T_J	8
Figure 13. Transient Thermal Resistance	8
Figure 14. Safe Operating Area $T_C = 25^\circ\text{C}$	8
Figure 15. Switching Time Test Circuit	9
Figure 16. Switching Time Waveform	9
Figure 17. Package Outline Drawing – TO-220 3L	10

1. Pin Information

1.1 Pin Assignments

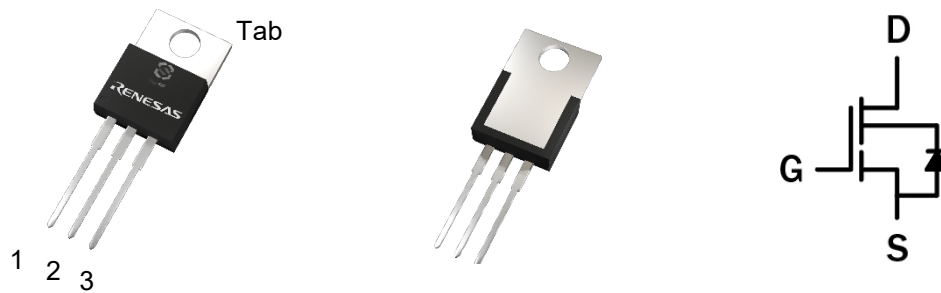


Figure 1. Pin Assignments

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1	G	Gate.
2	S	Source.
3	D	Drain.
Tab	S	Source.

2. Specifications

2.1 Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$ unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Test Condition	Unit
V_{DSS}	Drain to source voltage	-	700	$V_{GS} = 0V$, Test as per JEDEC	V
$V_{DSS(TR), non-repetitive}$	Transient drain to source voltage, non-repetitive	-	800	$V_{GS} = 0V$, spike duration $< 30\mu\text{s}$	
$V_{DSS(TR), pulsed}$	Drain to source voltage, pulsed	-	750	$V_{GS} = 0V$, spike duration $< 5\mu\text{s}$	
V_{GSS}	Gate to source voltage	-20	+20	-	
P_D	Maximum power dissipation	-	69.4	$T_c = 25^\circ\text{C}$	W
I_D	Continuous drain current at $T_c = 25^\circ\text{C}$	-	16	$V_{GS} = 9V$, V_{DS} can be positive and negative	A
	Continuous drain current at $T_c = 100^\circ\text{C}$	-	10		
$I_{D(PULSE)}$	Pulsed drain current at $T_c = 25^\circ\text{C}$	-	54	$V_{GS} = 9V$, pulse width = $10\mu\text{s}$ V_{DS} can be positive and negative	A
	Pulsed drain current at $T_c = 100^\circ\text{C}$	-	47		
$I_{SD(PULSE)}$	Pulsed reverse drain current at $T_c = 25^\circ\text{C}$	-	54	$V_{GS} = 0V$, pulse width = $10\mu\text{s}$, $V_{DS} < 0$	A
	Pulsed reverse drain current at $T_c = 100^\circ\text{C}$	-	47		
T_J	Operating temperature junction	-55	+150	-	$^\circ\text{C}$
T_S	Storage temperature	-55	+150	Max shelf life depends on storage conditions	$^\circ\text{C}$
T_{SOLD}	Reflow soldering temperature ^[1]	-	260	-	$^\circ\text{C}$

1. Reflow MSL3.

2.2 Thermal Specifications

Symbol	Parameter	Typical Value	Test Condition	Unit
$R_{\theta JC}$	Junction-to-case	1.8	-	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-ambient	52	Device on $40 \times 40 \text{ mm} \times 1.5\text{mm}$ epoxy PCB FR4 with 6cm^2 (one layer, $70\mu\text{m}$ thickness) copper area for tab (source) connection and cooling. PCB is vertical without air stream cooling.	

2.3 Electrical Specifications – Forward Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V _{DSS(BL)}	Maximum drain-source voltage	V _{GS} = 0V	700	-	-	V
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 0.5 mA	3.2	4	4.8	V
ΔV _{GS(th)/T_J}	Gate threshold voltage temperature coefficient		-	-7.6	-	mV/°C
R _{DS(on)eff}	Drain-source on-resistance	V _{GS} = 9V, I _D = 4A, T _J = 25°C	-	130	163	mΩ
		V _{GS} = 9V, I _D = 4A, T _J = 150°C	-	267	-	
I _{DSS}	Drain-to-source leakage current	V _{DS} = 700V, V _{GS} = 0V, T _J = 25°C	-	0.7	10	μA
		V _{DS} = 700V, V _{GS} = 0V, T _J = 150°C	-	5	-	
I _{GSS}	Gate-to-source forward leakage current ^[1]	V _{GS} = 20V	-	-	10	μA
	Gate-to-source reverse leakage current ^[1]	V _{GS} = -20V	-	-	-10	
C _{ISS}	Input capacitance	V _{GS} = 0V, V _{DS} = 400V, f = 1MHz	-	567	-	pF
C _{OSS}	Output capacitance		-	28	-	
C _{RSS}	Reverse transfer capacitance		-	3.9	-	
C _{O(er)}	Output capacitance, energy related ^[2]	V _{GS} = 0V, V _{DS} = 0V to 400V	-	40.2	-	pF
C _{O(tr)}	Output capacitance, time related ^[3]		-	73	-	
Q _G	Total gate charge	V _{DS} = 400V, V _{GS} = 0V to 9V, I _D = 4A	-	10.7	-	nC
Q _{GS}	Gate-source charge		-	3.2	-	
Q _{GD}	Gate-drain charge		-	4.6	-	
Q _{OSS}	Output charge	V _{GS} = 0V, V _{DS} = 0V to 400V	-	29.2	-	nC
t _{D(on)}	Turn-on delay	V _{DS} = 400V, V _{GS} = 0 to 9V, R _G = 30Ω, I _D = 4A, at 100MHz (see Figure 15)	-	41.7	-	ns
t _R	Rise time		-	6	-	
t _{D(off)}	Turn-off delay		-	42.2	-	
t _F	Fall time		-	14.7	-	

1. MOSFET has integrated ESD Protection Circuit.
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

2.4 Electrical Specifications – Reverse Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V _{SD}	Reverse voltage ^[1]	V _{GS} = 0V, I _S = 4A	-	1.3	-	V
		V _{GS} = 0V, I _S = 2A	-	1.1	-	

1. Reverse recovery charge is negligible enabled by the LV Si FET technology.

3. Typical Performance Graphs

$T_c = 25^\circ\text{C}$ unless otherwise stated.

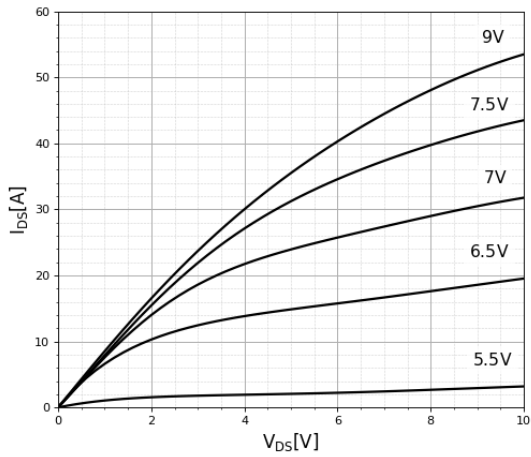


Figure 2. Typical Output Characteristics, $T_J = 25^\circ\text{C}$
Parameter: V_{GS}

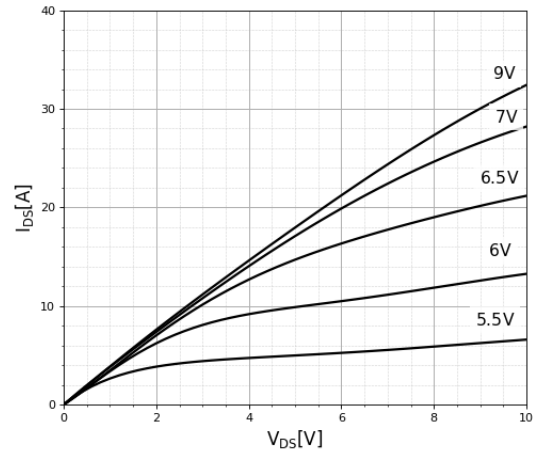


Figure 3. Typical Output Characteristics, $T_J = 150^\circ\text{C}$
Parameter: V_{GS}

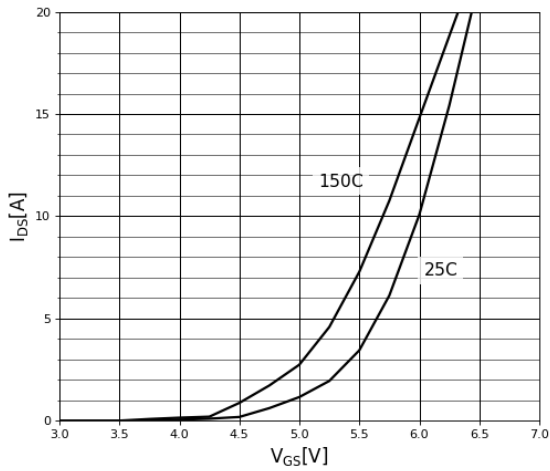


Figure 4. Typical Transfer Characteristics,
 $V_{DS} = 10\text{V}$, Parameter: T_J

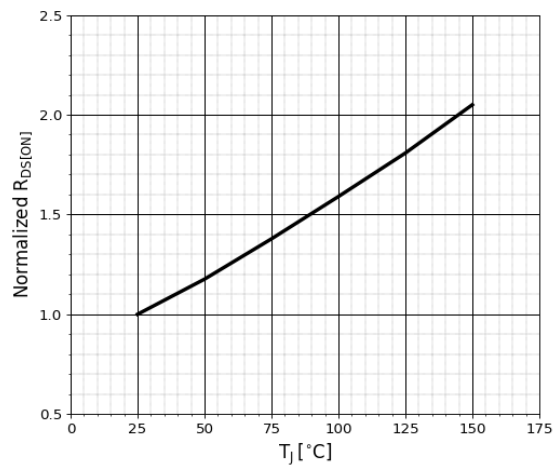


Figure 5. Normalized On-Resistance,
 $I_D = 4\text{A}$, $V_{GS} = 9\text{V}$

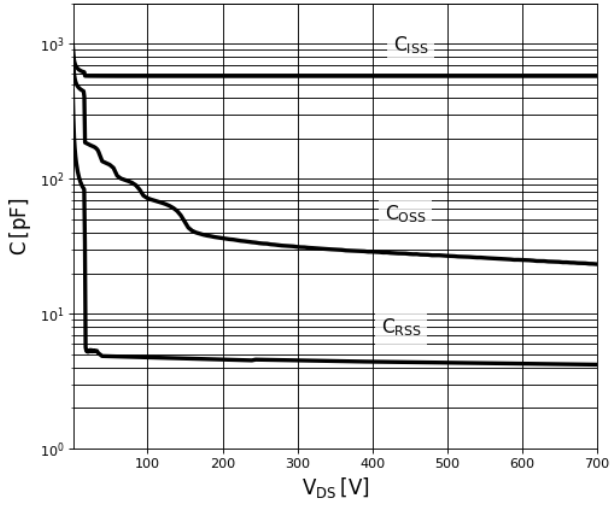


Figure 6. Typical Capacitance,
V_{GS} = 0V, f = 1MHz

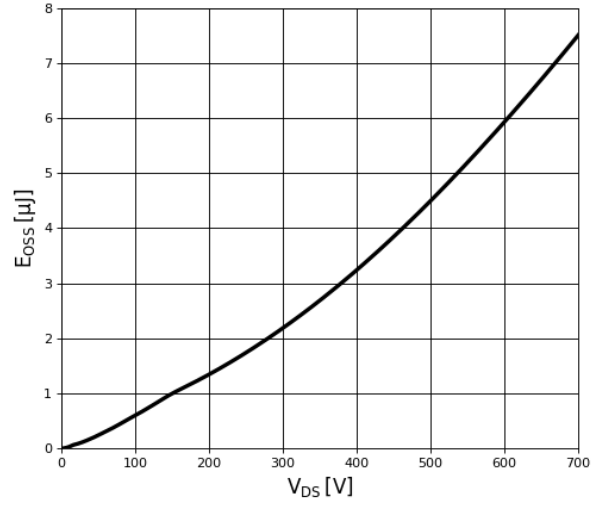


Figure 7. Typical C_{oss} Stored Energy

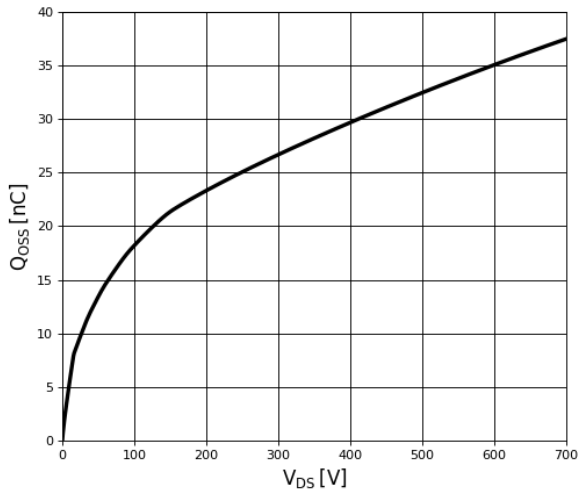


Figure 8. Typical Q_{oss}

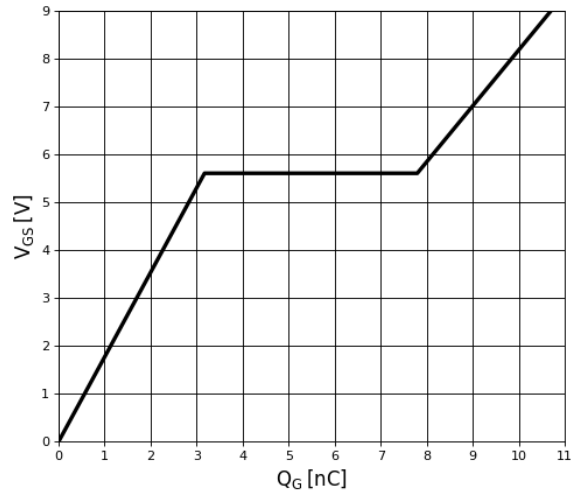


Figure 9. Typical Gate Charge,
I_{DS} = 4A, V_{DS} = 400V

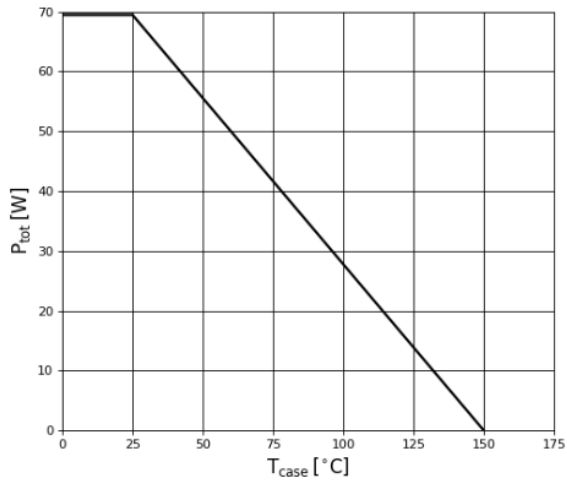


Figure 10. Power Dissipation

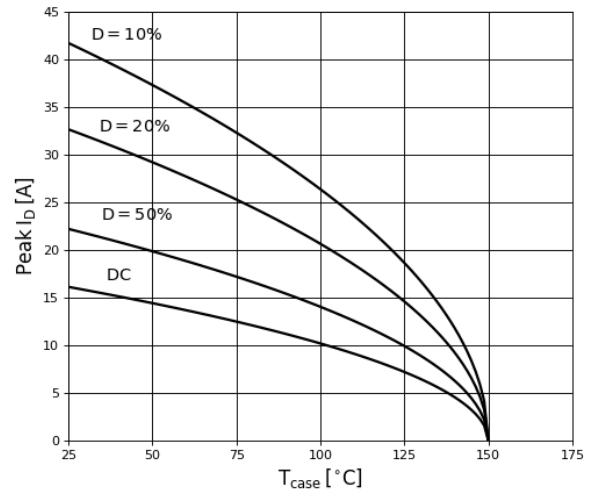


Figure 11. Current Derating,
Pulse width ≤ 10μs, V_{GS} ≥ 9V

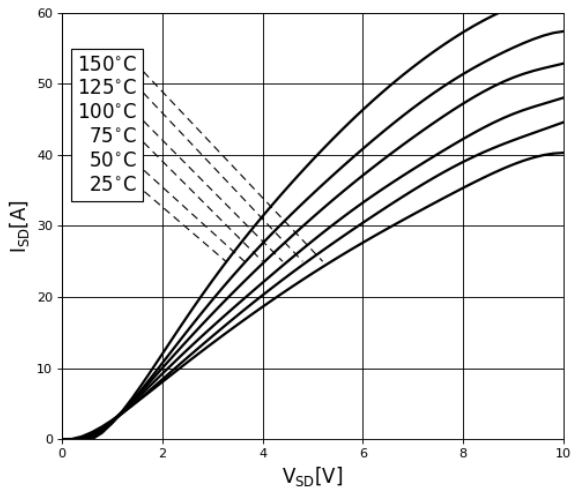


Figure 12. Forward Characteristics of Rev. Diode,
I_S = f(V_{SD}), Parameter: T_J

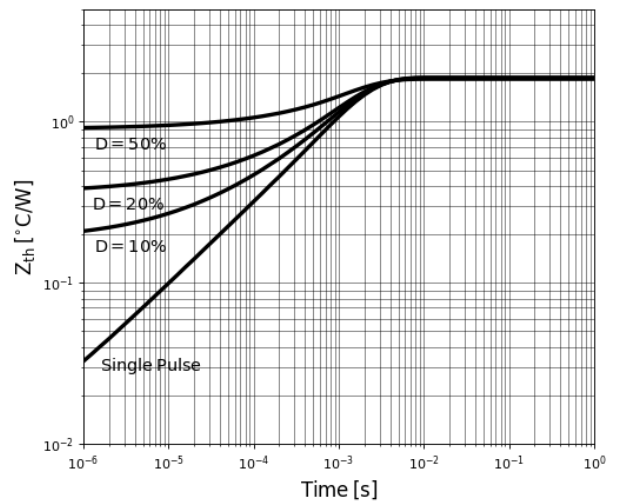


Figure 13. Transient Thermal Resistance

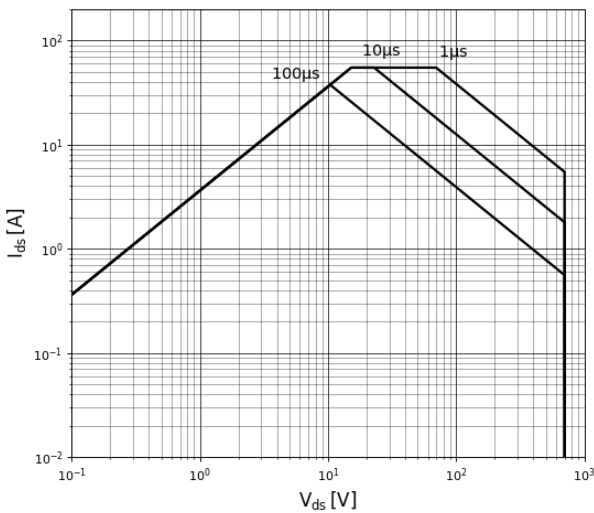


Figure 14. Safe Operating Area T_C = 25°C

4. Test Circuits and Waveforms

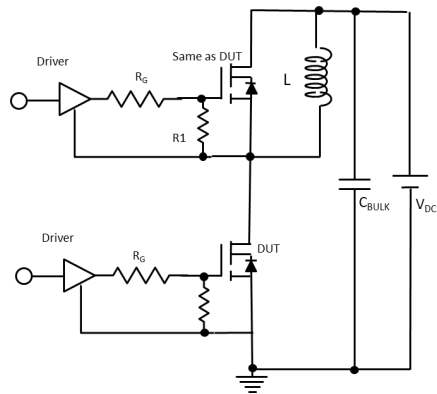


Figure 15. Switching Time Test Circuit

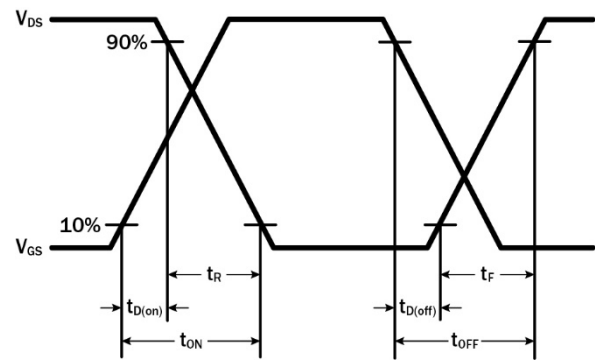


Figure 16. Switching Time Waveform

5. Package Outline Drawings

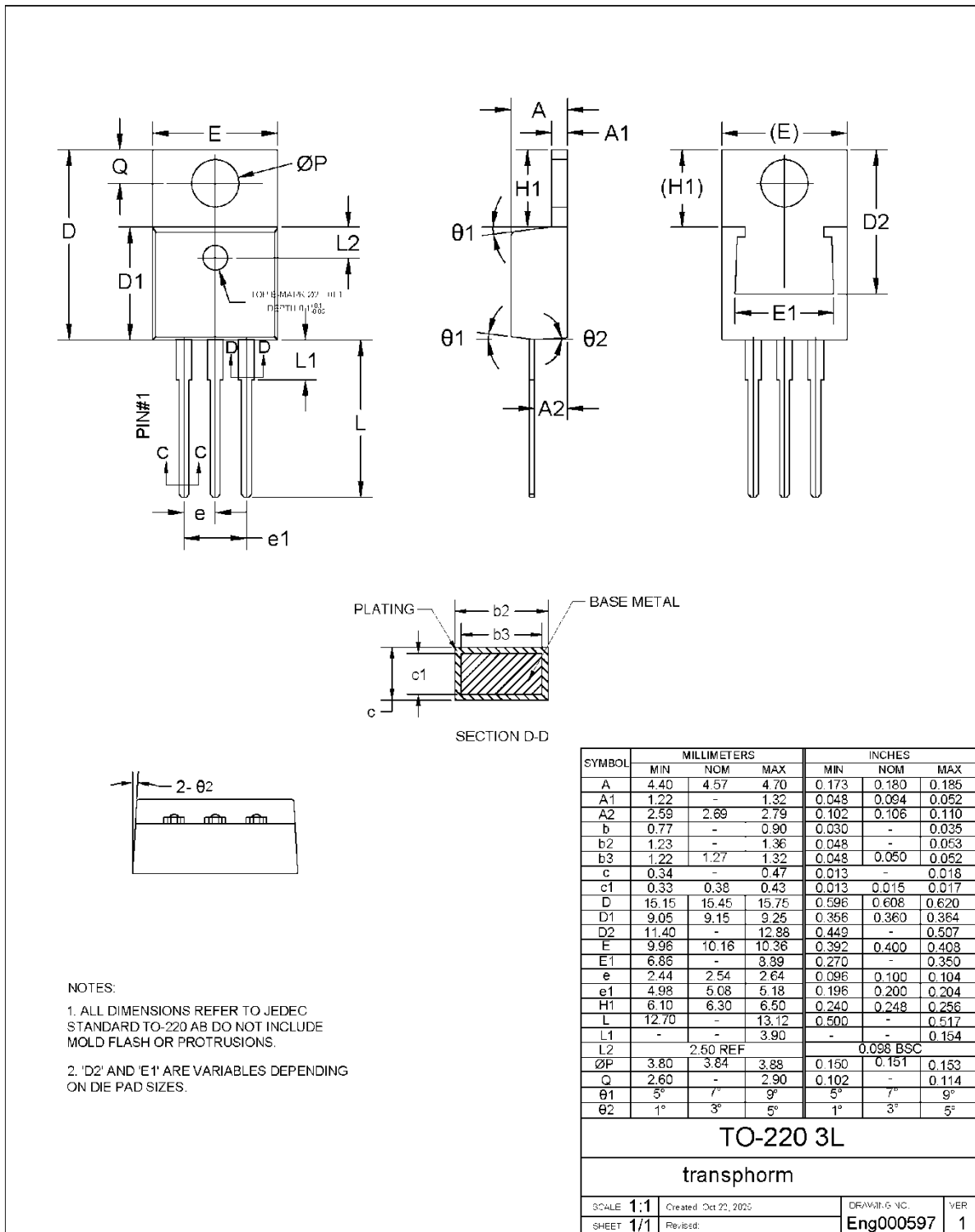


Figure 17. Package Outline Drawing – TO-220 3L

6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the [GaN Power Solutions](#) page.

7. Ordering Information

Part Number	Package Description	Package Configuration
TP70H130G4PPS	TO-220 3L	Source tab

8. Revision History

Revision	Date	Description
1.01	Mar 25, 2026	Updated Ordering Information
1.00	Feb 20, 2026	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.