

650V SuperGaN® GaN FET in PQFN (source tab)

* Dynamic $R_{DS(on)}$: see Figures 18 and 19

Absolute Maximum Ratings ($T_c=25^{\circ}\text{C}$ unless otherwise stated.)

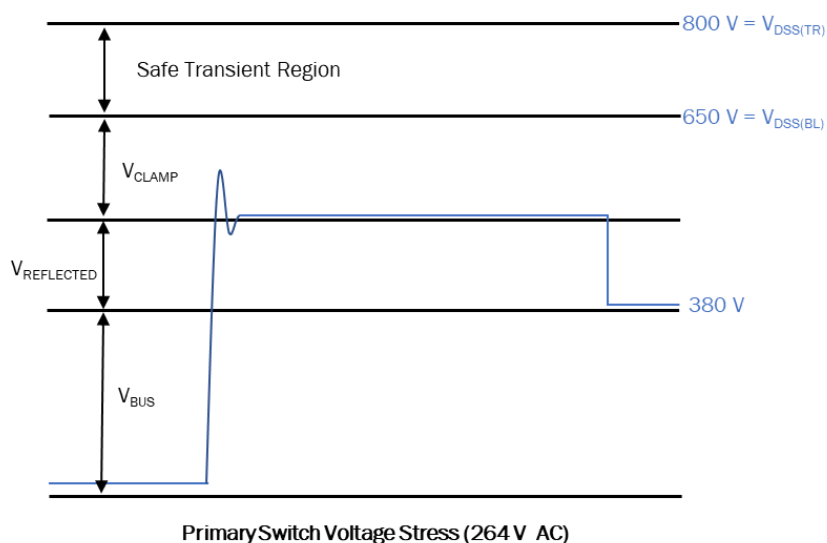
Symbol	Parameter		Limit Value	Unit
V _{DSS}	Drain to source voltage (T _J = -55 °C to 150 °C)		650	V
V _{DSS(TR)}	Transient drain to source voltage ^a		800	
V _{GSS}	Gate to source voltage		±10	
P _D	Maximum power dissipation @T _C =25 °C		21	W
I _D	Continuous drain current @T _C =25 °C ^b		6.5	A
	Continuous drain current @T _C =100 °C ^b		4.1	A
I _{DM}	Pulsed drain current (pulse width: 10μs)		30	A
T _C	Operating temperature	Case	-55 to +150	°C
T _J		Junction	-55 to +150	°C
T _S	Storage temperature		-55 to +150	°C
T _{SOLD}	Reflow soldering temperature ^c		260	°C

Notes:

a. In off-state, spike duration < 30 μs , Non-repetitive

b. For increased stability at high current operation, see Circuit Implementation on page 3

c. Reflow MSL3

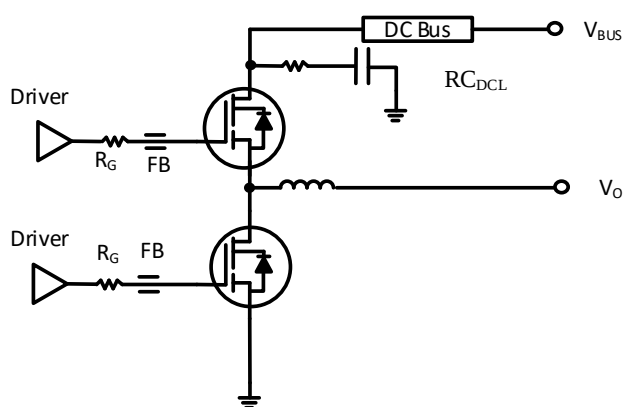
**Thermal Resistance**

Symbol	Parameter	Typical	Unit
$R_{\theta\text{JC}}$	Junction-to-case	5.5	$^{\circ}\text{C/W}$
$R_{\theta\text{JA}}$	Junction-to-ambient ^d	50	$^{\circ}\text{C/W}$

Notes:

d. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper area and 70 μm thickness)

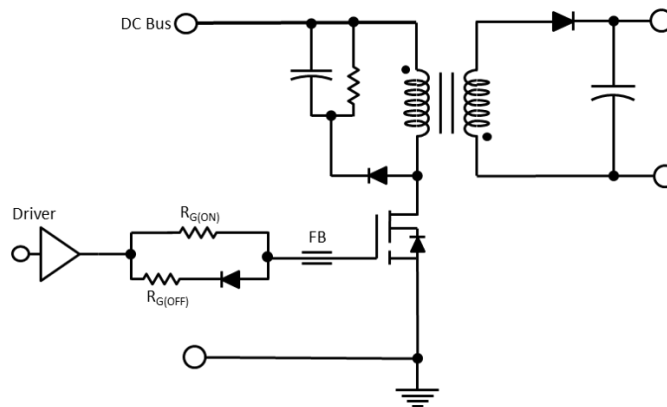
Circuit Implementation



Simplified Half-bridge Schematic

Recommended gate drive: (0V, 6V) with $R_{G(tot)} = 45 - 50 \Omega^a$

For additional driver configurations/options please see application note AN0009.



Simplified Single Ended Schematic

Recommended gate drive:

Gate drive: (0V, 6V): $R_{G(ON)} = 50$ to 150Ω ; $R_{G(OFF)} = 0$ to 10Ω

Gate drive*: (-6V, 6V): $R_{G(ON)} = 50$ to 100Ω ; $R_{G(OFF)} = 0$ to 20Ω

*Drop-in with discrete e-mode gate drive that level shifts any standard silicon MOSFET controller with integrated driver (i.e. NCP1342)

Gate Ferrite Bead (FB)	Required DC Link RC Snubber (RC_{DCL}) ^b
240 Ω @ 100MHz	4.7–10nF + 3.3 Ω

Notes:

- For bridge topologies only. R_G could be much smaller in single ended topologies.
- RC_{DCL} should be placed as close as possible to the drain pin.

Electrical Parameters ($T_J=25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{DSS(BL)}$	Maximum drain-source voltage	650	—	—	V	$V_{GS}=0V$
$V_{GS(th)}$	Gate threshold voltage	2	2.4	2.8	V	$V_{DS}=V_{GS}, I_D=0.5mA$
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	—	-5.8	—	mV/ $^\circ\text{C}$	
$R_{DS(on)eff}$	Drain-source on-resistance ^a	—	240	312	m Ω	$V_{GS}=6V, I_D=6.5A, T_J=25^\circ\text{C}$
		—	492	—		$V_{GS}=6V, I_D=6.5A, T_J=150^\circ\text{C}$
I_{DSS}	Drain-to-source leakage current	—	1.2	12	μA	$V_{DS}=650V, V_{GS}=0V, T_J=25^\circ\text{C}$
		—	8	—		$V_{DS}=650V, V_{GS}=0V, T_J=150^\circ\text{C}$
I_{GSS}	Gate-to-source forward leakage current	—	—	100	nA	$V_{GS}=12V$
	Gate-to-source reverse leakage current	—	—	-100		$V_{GS}=-12V$
C_{ISS}	Input capacitance	—	414	—	pF	$V_{GS}=0V, V_{DS}=400V, f=1MHz$
C_{OSS}	Output capacitance	—	16	—		
C_{RSS}	Reverse transfer capacitance	—	1	—		
$C_{O(er)}$	Output capacitance, energy related ^b	—	24	—	pF	$V_{GS}=0V, V_{DS}=0V$ to 400V
$C_{O(tr)}$	Output capacitance, time related ^c	—	47	—		
Q_G	Total gate charge	—	4.5	—	nC	$V_{DS}=400V, V_{GS}=0V$ to 10V, $I_D=6.5A$
Q_{GS}	Gate-source charge	—	1.5	—		
Q_{GD}	Gate-drain charge	—	0.6	—		
Q_{OSS}	Output charge	—	19	—	nC	$V_{GS}=0V, V_{DS}=0V$ to 400V
$t_{D(on)}$	Turn-on delay	—	33.6	—	ns	$V_{DS}=400V, V_{GS}=0V$ to 6V, $I_D=6.5A, R_G=65\Omega, Z_{FB}=330\Omega$ at 100MHz (See Figure 14)
t_R	Rise time	—	4.4	—		
$t_{D(off)}$	Turn-off delay	—	20	—		
t_F	Fall time	—	3.6	—		

Notes:

a. Dynamic $R_{DS(on)}$ value; see Figures 18 and 19 for conditions

b. Equivalent capacitance to give same stored energy from 0V to 400V

c. Equivalent capacitance to give same charging time from 0V to 400V

Electrical Parameters ($T_J=25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	3.7	A	$V_{GS}=0V$, $T_C=100^\circ\text{C}$, $\leq 20\%$ duty cycle
V_{SD}	Reverse voltage ^a	—	1.7	—	V	$V_{GS}=0V$, $I_S=8.5A$
		—	1.2	—		$V_{GS}=0V$, $I_S=4.5A$
t_{RR}	Reverse recovery time	—	16	—	ns	$I_S=10A$, $V_{DD}=400V$, $di/dt=1000A/ms$
Q_{RR}	Reverse recovery charge	—	23	—	nC	

Notes:

a. Includes dynamic $R_{DS(on)}$ effect

Typical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise stated)

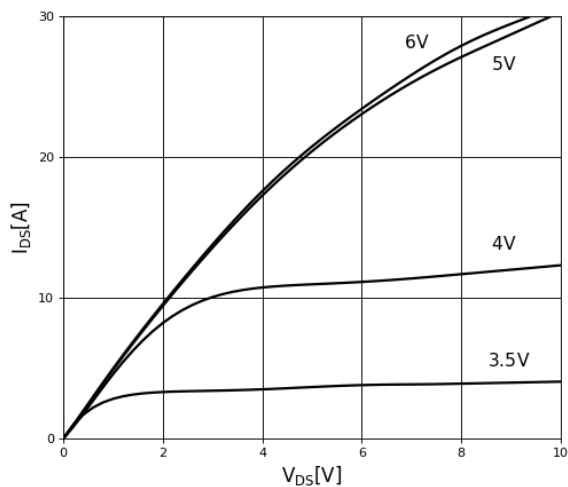


Figure 1. Typical Output Characteristics $T_J=25^\circ\text{C}$
Parameter: V_{GS}

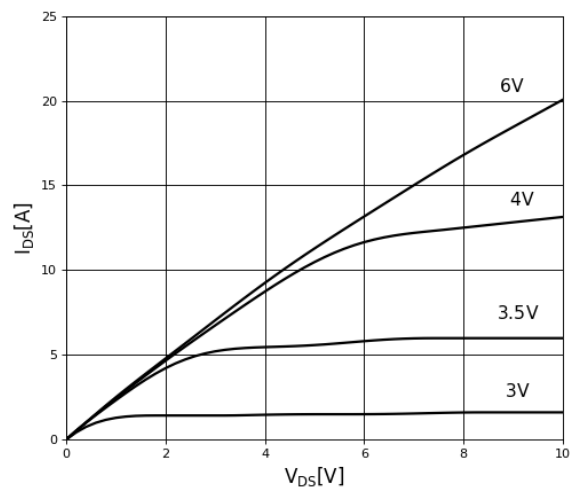


Figure 2. Typical Output Characteristics $T_J=150^\circ\text{C}$
Parameter: V_{GS}

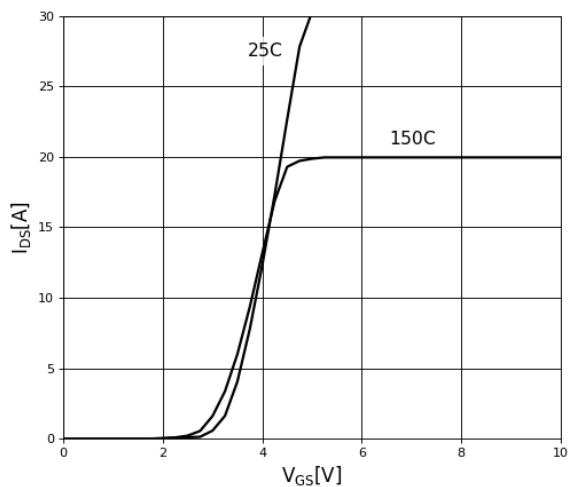


Figure 3. Typical Transfer Characteristics
 $V_{DS}=10\text{V}$, parameter: T_J

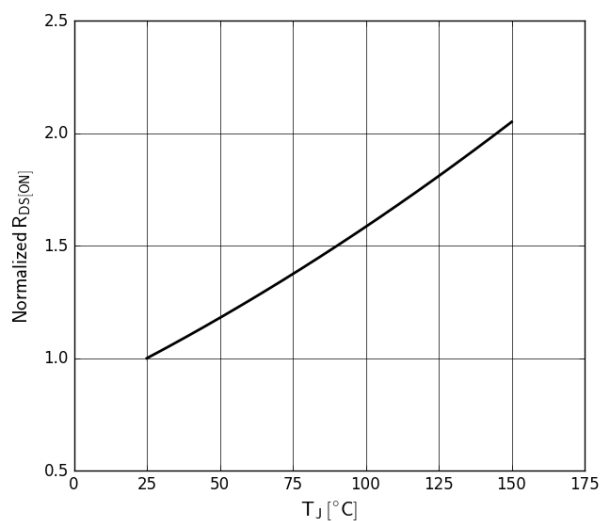


Figure 4. Normalized On-resistance
 $I_D=16\text{A}$, $V_{GS}=10\text{V}$

Typical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise stated)

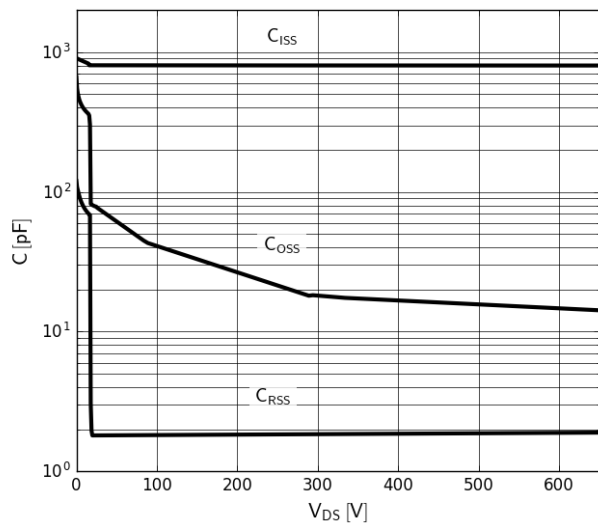


Figure 5. Typical Capacitance

$V_{GS}=0V$, $f=1\text{MHz}$

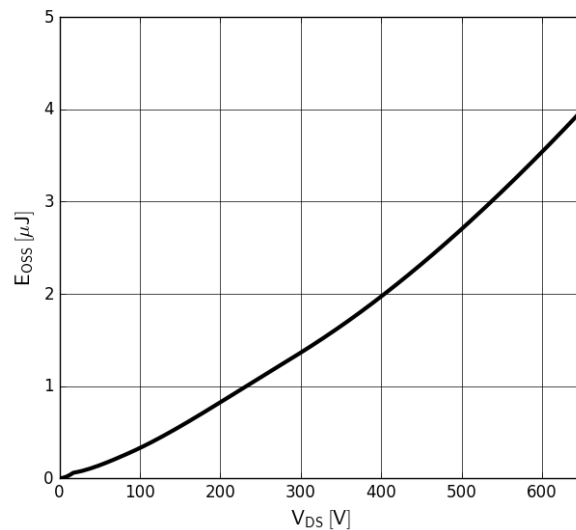


Figure 6. Typical C_{OSS} Stored Energy

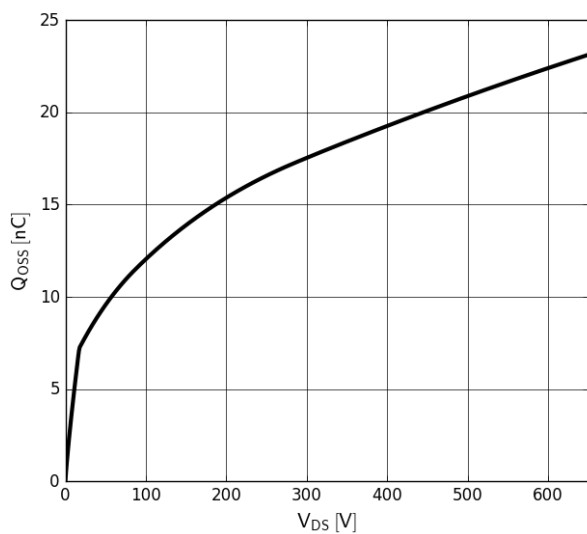


Figure 7. Typical Q_{OSS}

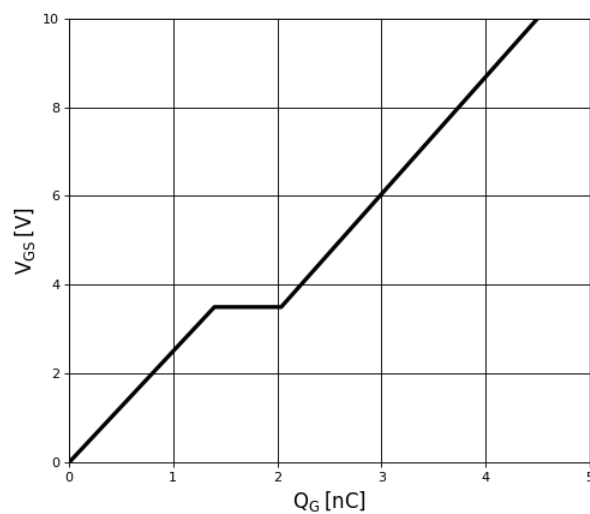
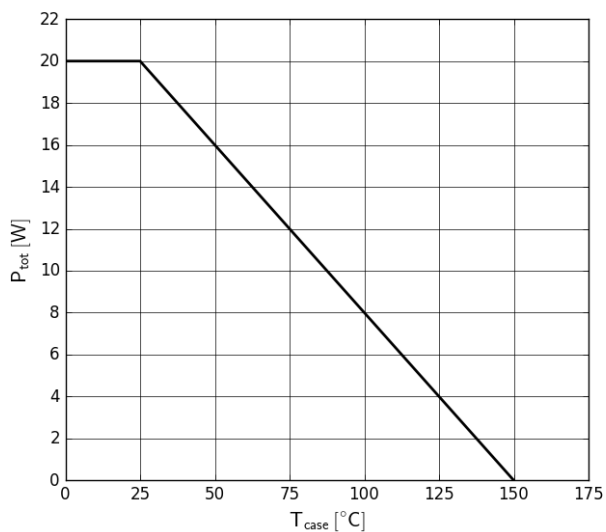
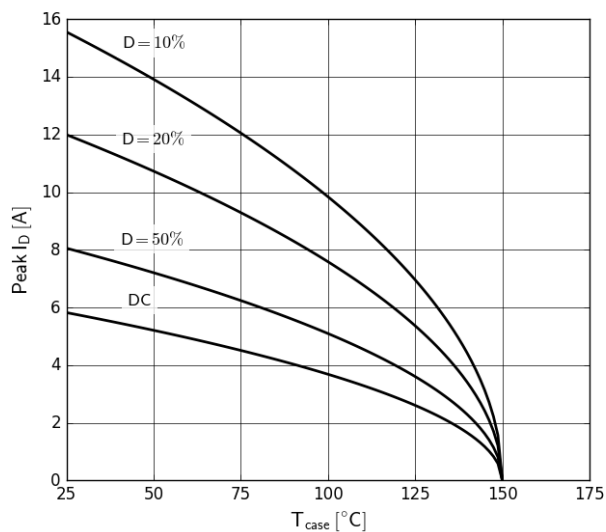
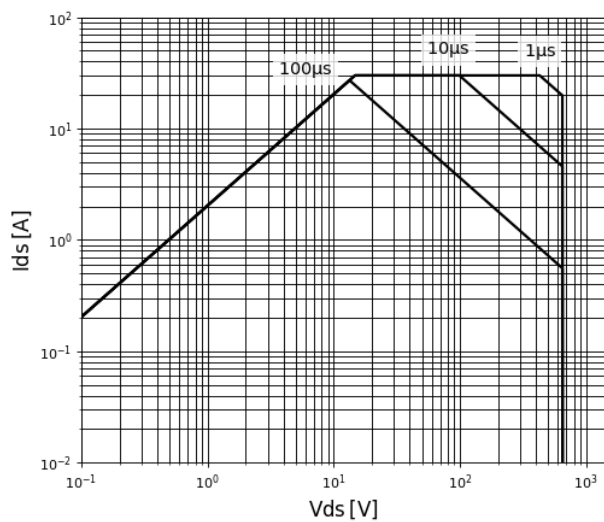
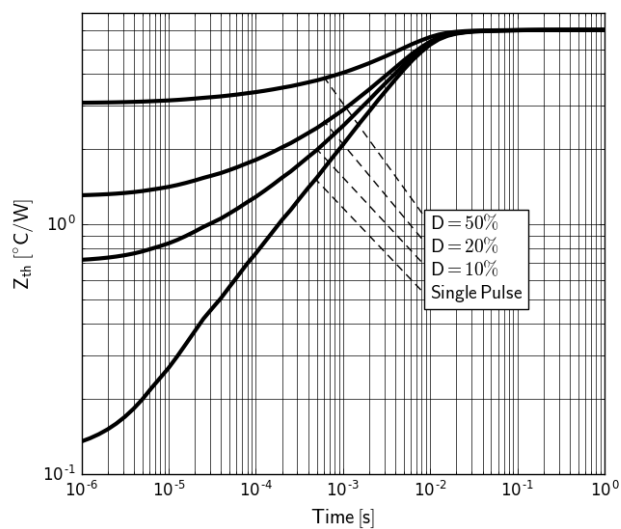
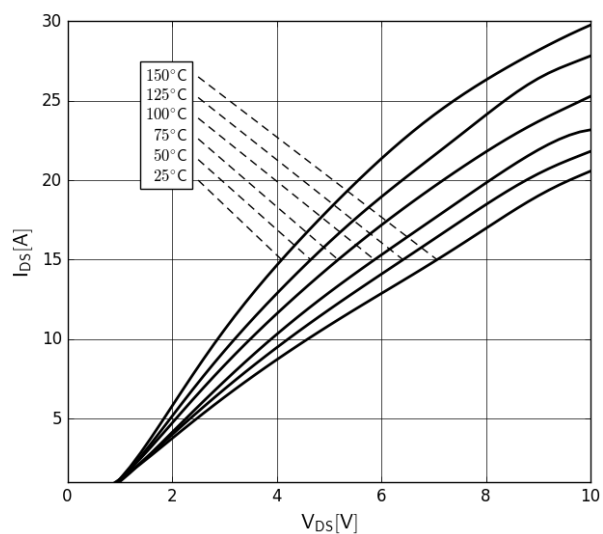


Figure 8. Typical Gate Charge

$I_{DS}=10A$, $V_{DS}=400V$

Typical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise stated)**Figure 9. Power Dissipation****Figure 10. Current Derating**Pulse width $\leq 10\mu\text{s}$, $V_{GS} \geq 10\text{V}$ **Figure 11. Forward Characteristics of Rev. Diode** $I_S=f(V_{SD})$, parameter: T_J **Figure 12. Transient Thermal Resistance**

Typical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise stated)**Figure 13. Safe Operating Area TC=25°C**

Test Circuits and Waveforms

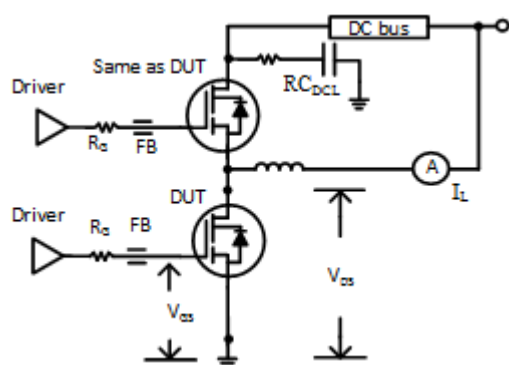


Figure 14. Switching Time Test Circuit

(see circuit implementation on page 3 for methods to ensure clean switching)

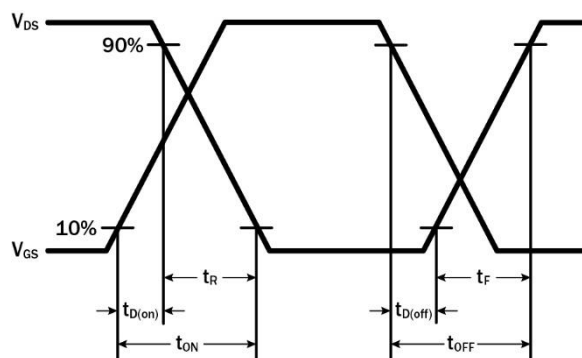


Figure 15. Switching Time Waveform

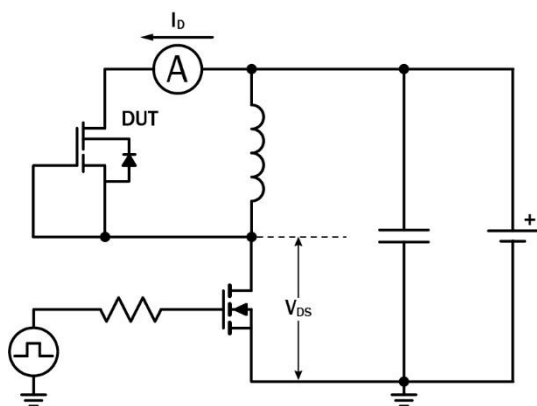


Figure 16. Diode Characteristics Test Circuit

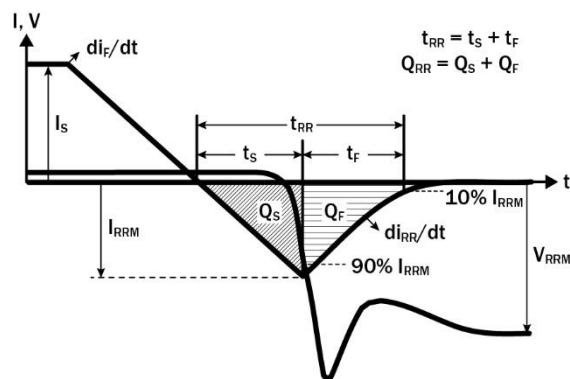


Figure 17. Diode Recovery Waveform

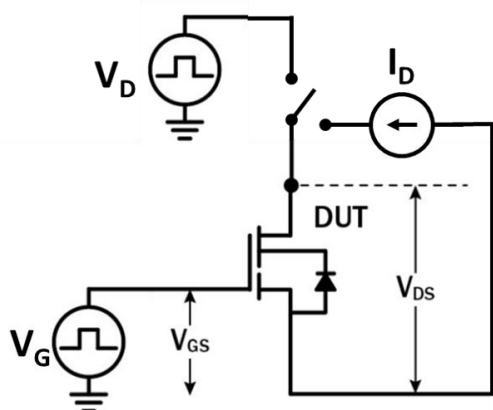


Figure 18. Dynamic $R_{DS(on)eff}$ Test Circuit

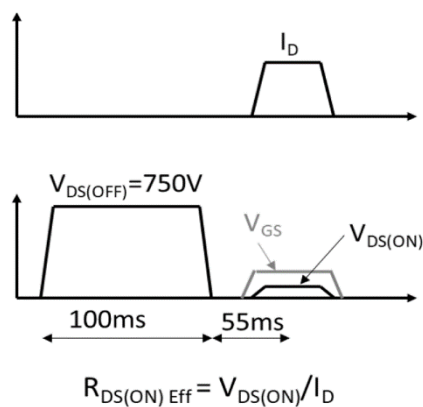


Figure 19. Dynamic $R_{DS(on)eff}$ Waveform

Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Renesas GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Renesas GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See Printed Circuit Board Layout and Probing	

GaN Design Resources

The complete technical library of GaN design tools can be found at [Renesasusa.com/design](https://www.renesas.com/design):

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

Mechanical

8x8 PQFN Package

