

TP65H100G4LSGB

650V SuperGaN® GaN FET in PQFN 8 × 8 Industry Standard Package (source tab)

Description

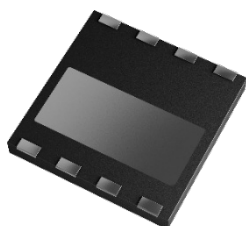
The TP65H100G4LSGB 650V, 85mΩ Gallium Nitride (GaN) FET is a normally-off device using Renesas' Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance while enabling reduced system size and cost.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

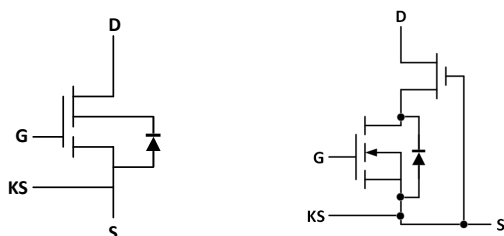
Benefits

- Achieves increased efficiency in both hard-switched and soft-switched circuits
 - Increased power density
 - Reduced system size and weight
 - Overall lower system cost
- Easy to drive with commonly used gate drivers

Product and Schematic Diagrams



TP65H100G4LSGB PQFN 8 × 8 mm IP



Cascode Schematic Symbol

Cascode Device Structure

(MOSFET has integrated ESD Protection Circuit)

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
 - Transient over-voltage capability
 - Operation with E-mode Gate drivers without need for Zener protection.
- Reduced crossover loss
- Negligible Q_{rr}
- RoHS compliant and Halogen-free packaging

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting



Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$ (V) maximum	800
$R_{DS(on)}$ (mΩ) maximum ^[1]	102
Q_{OSS} (nC) typical	56
Q_G (nC) typical	14.4

1. Dynamic $R_{DS(on)}$; see Figure 17 and Figure 18.

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1. Pin Information

1.1 Pin Assignments

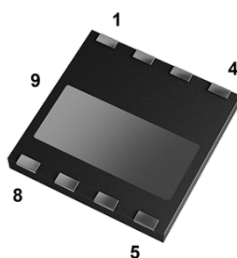


Figure 1. Pin Assignments – Bottom View

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3, 4	D	Drain.
5, 6	S	Source.
7	KS	Kelvin source.
8	G	Gate.
9	S	Source.

2. Specifications

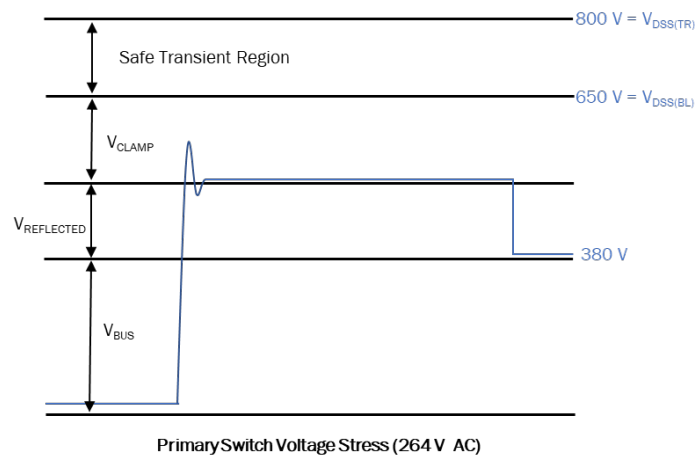
2.1 Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$ unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Unit
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)	-	650	V
$V_{DSS(TR)}$, non-repetitive	Transient drain to source voltage, non-repetitive ^[1]	-	800	
$V_{DSS(TR)}$, repetitive	Transient drain to source voltage, repetitive ^[2]	-	750	
V_{GSS}	Gate to source voltage	-20	+20	
P_D	Maximum power dissipation at $T_c = 25^\circ\text{C}$	-	65.8	W
I_D	Continuous drain current at $T_c = 25^\circ\text{C}$	-	18.9	A
	Continuous drain current at $T_c = 100^\circ\text{C}$	-	12	A
I_{DM}	Pulsed drain current (pulse width: 10 μs)	-	95	A
T_J	Junction operating temperature	-55	+150	$^\circ\text{C}$
T_S	Storage temperature	-55	+150	$^\circ\text{C}$
T_{SOLD}	Reflow soldering temperature ^[3]	-	260	$^\circ\text{C}$

1. In off-state, spike duration < 30 μs , non-repetitive.
2. Off-state, spike duration < 5 μs , repetitive.
3. Reflow MSL3.



2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\theta JC}$	Junction-to-case	1.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-ambient ^[1]	50	

1. Device on one layer epoxy PCB for source connection (vertical and without air stream cooling, with 6cm² copper area and 70 μm thickness).

2.3 Electrical Specifications – Forward Device

$T_J = 25^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	$V_{GS} = 0V$	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 0.5mA$	3.2	3.65	4.1	V
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient		-	-5.8	-	mV/°C
$R_{DS(on)eff}$	Drain-source on-resistance ^[1]	$V_{GS} = 10V, I_D = 12A, T_J = 25^\circ\text{C}$	-	85	102	mΩ
		$V_{GS} = 10V, I_D = 12A, T_J = 150^\circ\text{C}$	-	184	-	
I_{DSS}	Drain-to-source leakage current	$V_{DS} = 650V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	-	2.5	25	μA
		$V_{DS} = 650V, V_{GS} = 0V, T_J = 150^\circ\text{C}$	-	5	-	
I_{GSS}	Gate-to-source forward leakage current	$V_{GS} = 20V$	-	-	100	nA
	Gate-to-source reverse leakage current	$V_{GS} = -20V$	-	-	-100	
C_{iss}	Input capacitance	$V_{GS} = 0V, V_{DS} = 400V, f = 500kHz$	-	818	-	pF
C_{oss}	Output capacitance		-	53	-	
C_{rss}	Reverse transfer capacitance		-	3.6	-	
$C_{O(er)}$	Output capacitance, energy related ^[2]	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$	-	78	-	pF
$C_{O(tr)}$	Output capacitance, time related ^[3]		-	139	-	
Q_G	Total gate charge	$V_{DS} = 400V, V_{GS} = 0V \text{ to } 10V, I_D = 12A$	-	14.4	-	nC
Q_{GS}	Gate-source charge		-	4.7	-	
Q_{GD}	Gate-drain charge		-	5.2	-	
Q_{oss}	Output charge	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$	-	56	-	nC
$t_{D(on)}$	Turn-on delay	$V_{DS} = 400V, V_{GS} = 0V \text{ to } 12V, I_D = 13A, R_{G\_on} = 36\Omega, Z_{FB} = 120\Omega \text{ at } 100MHz \text{ (see Figure 15)}$	-	23	-	ns
t_R	Rise time		-	7.1	-	
$t_{D(off)}$	Turn-off delay		-	58	-	
t_F	Fall time		-	7.5	-	

1. Dynamic $R_{DS(on)}$, 100% tested; see [Figure 17](#) and [Figure 18](#) for conditions.
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

2.4 Electrical Specifications – Reverse Device

$T_J = 25^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	$V_{GS} = 0V$, $T_C = 100^\circ\text{C}$, $\leq 25\%$ duty cycle	-	-	12	A
V_{SD}	Reverse voltage ^[1]	$V_{GS} = 0V$, $I_S = 12A$	-	1.7	-	V
		$V_{GS} = 0V$, $I_S = 8A$	-	1.4	-	

1. Includes dynamic $R_{DS(on)}$ effect.

Note: Reverse recovery charge is negligible, enabled by the LV Si FET technology

3. Typical Performance Graphs

$T_C = 25^\circ\text{C}$ unless otherwise stated.

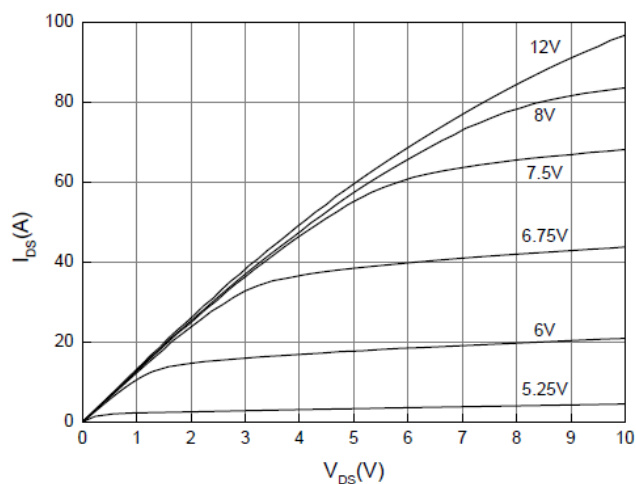


Figure 2. Typical Output Characteristics, $T_J = 25^\circ\text{C}$

Parameter: V_{GS}

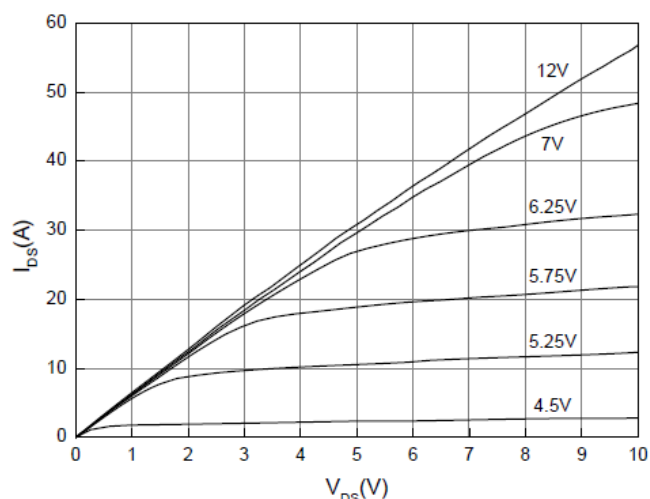


Figure 3. Typical Output Characteristics, $T_J = 150^\circ\text{C}$

Parameter: V_{GS}

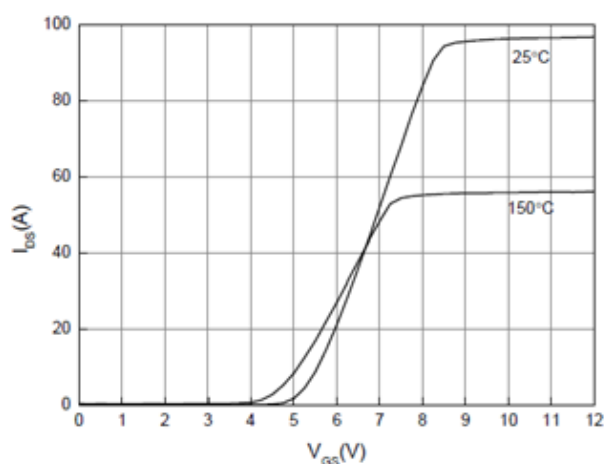


Figure 4. Typical Transfer Characteristics

$V_{DS} = 10\text{V}$, Parameter: T_J

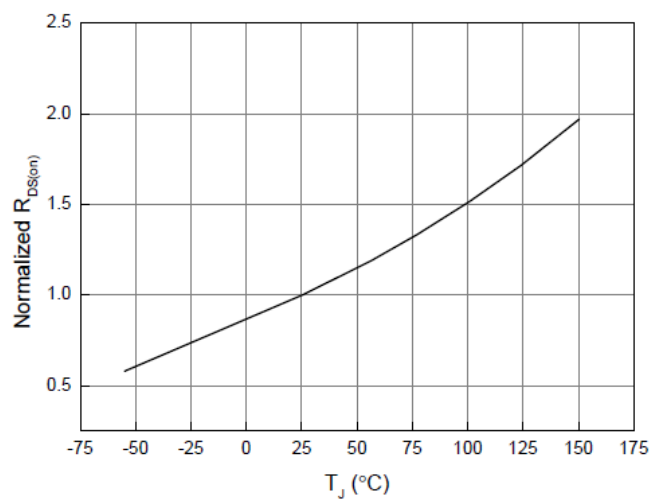


Figure 5. Normalized On-resistance

$I_D = 12\text{A}$, $V_{GS} = 10\text{V}$

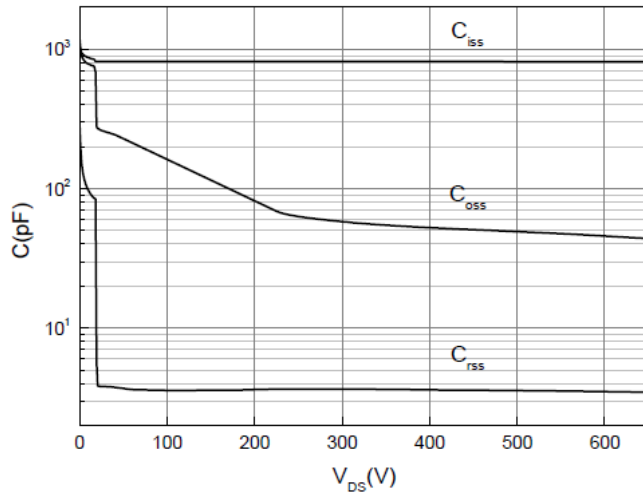


Figure 6. Typical Capacitance
 $V_{GS} = 0V$, $f = 1MHz$

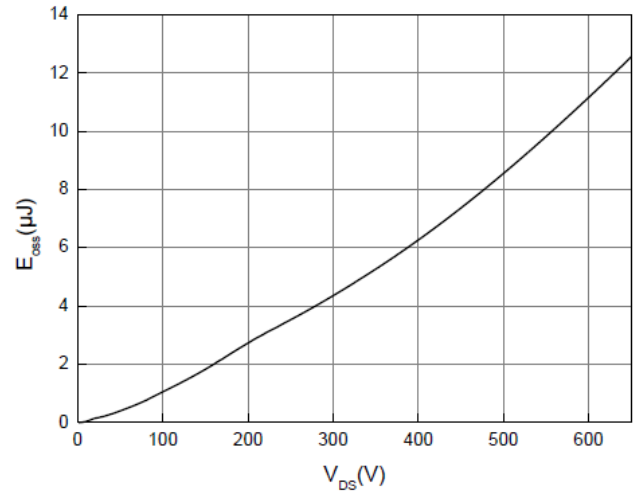


Figure 7. Typical Coss Stored Energy

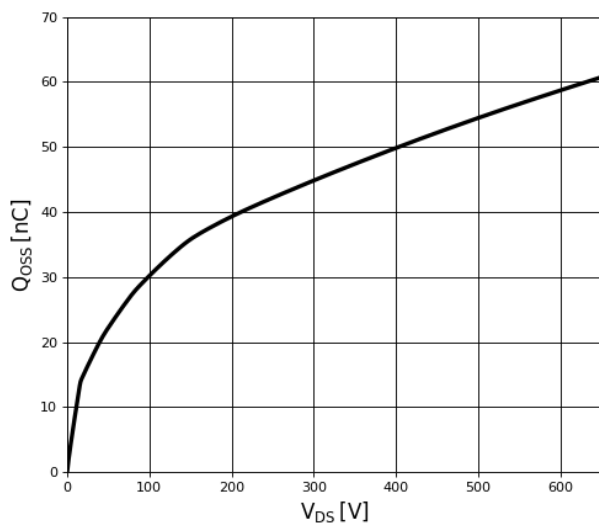


Figure 8. Typical Qoss

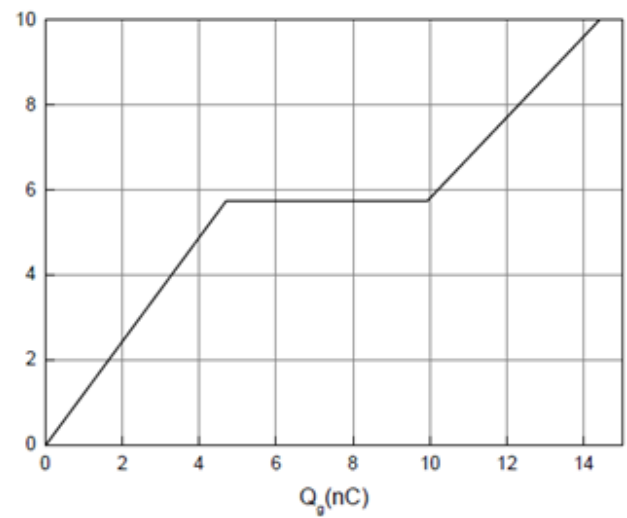


Figure 9. Typical Gate Charge
 $I_{DS} = 12A$, $V_{DS} = 400V$

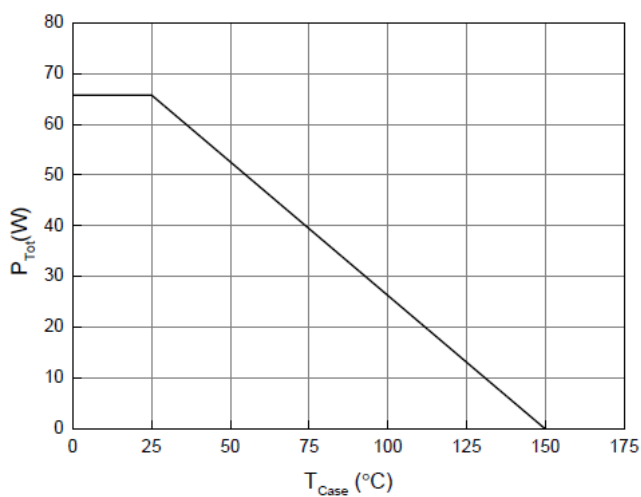


Figure 10. Power Dissipation

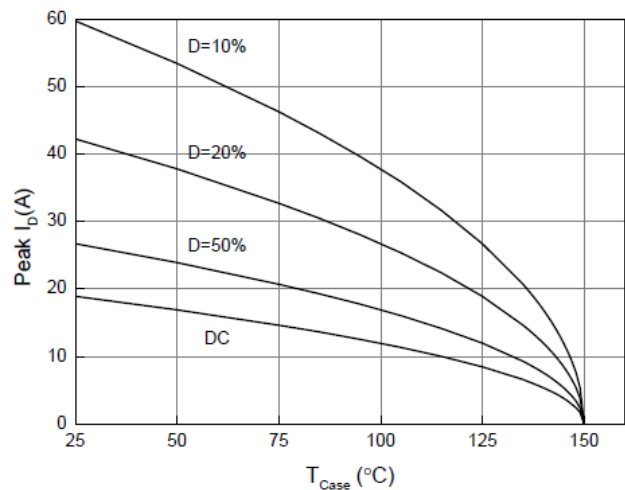


Figure 11. Current Derating
 Pulse width $\leq 10\mu s$, $V_{GS} \geq 10V$

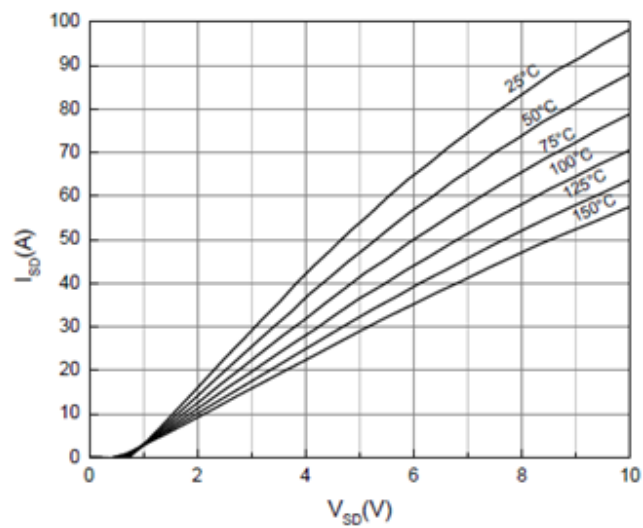


Figure 12. Forward Characteristics of Rev. Diode

$I_S = f(V_{SD})$, Parameter: T_J

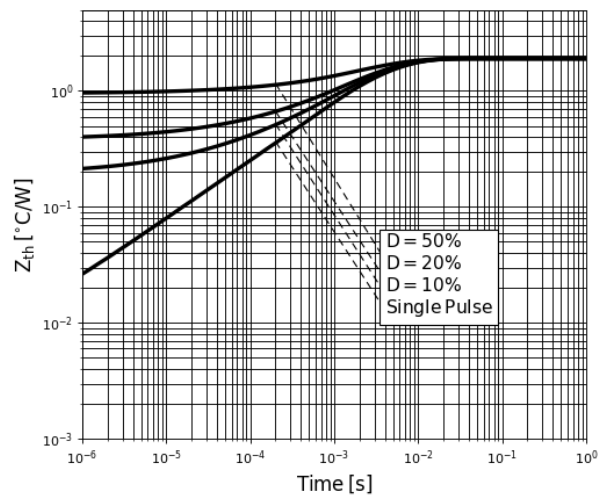


Figure 13. Transient Thermal Resistance

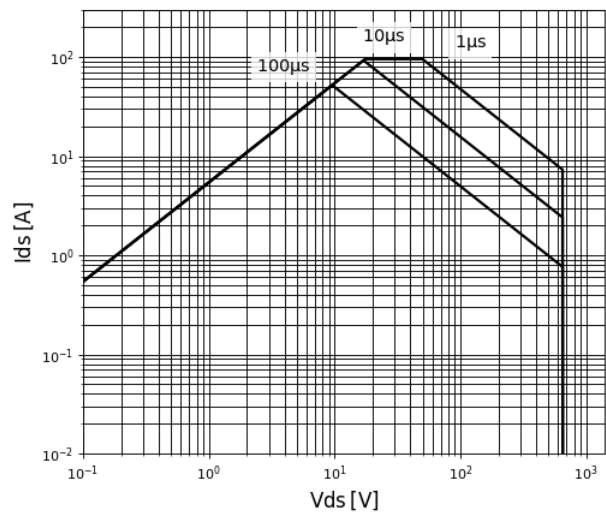


Figure 14. Safe Operating Area $T_c = 25^\circ\text{C}$

4. Test Circuits and Waveforms

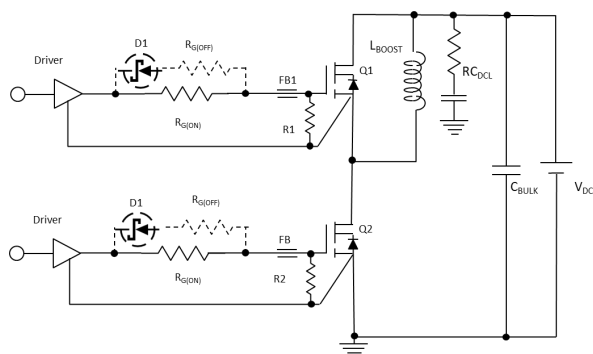


Figure 15. Switching Time Test Circuit

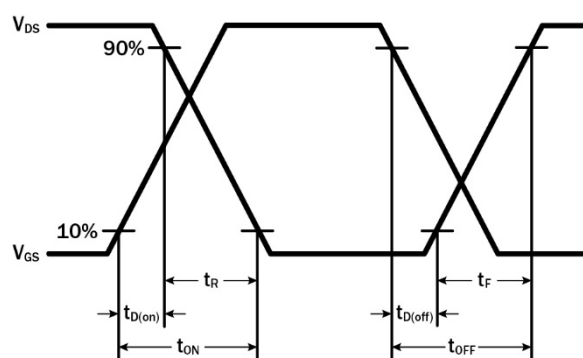


Figure 16. Switching Time Waveform

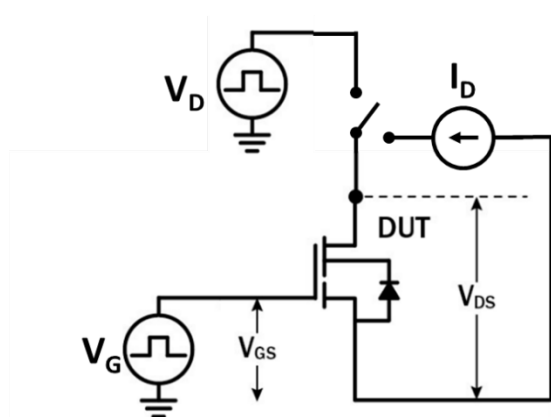


Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit

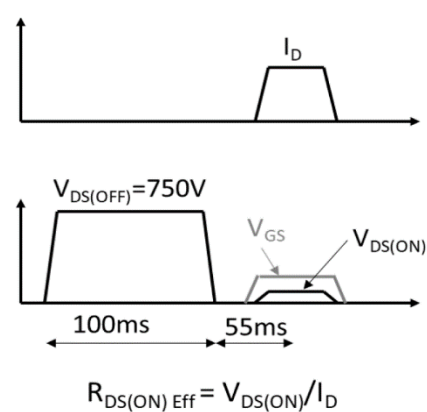


Figure 18. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings

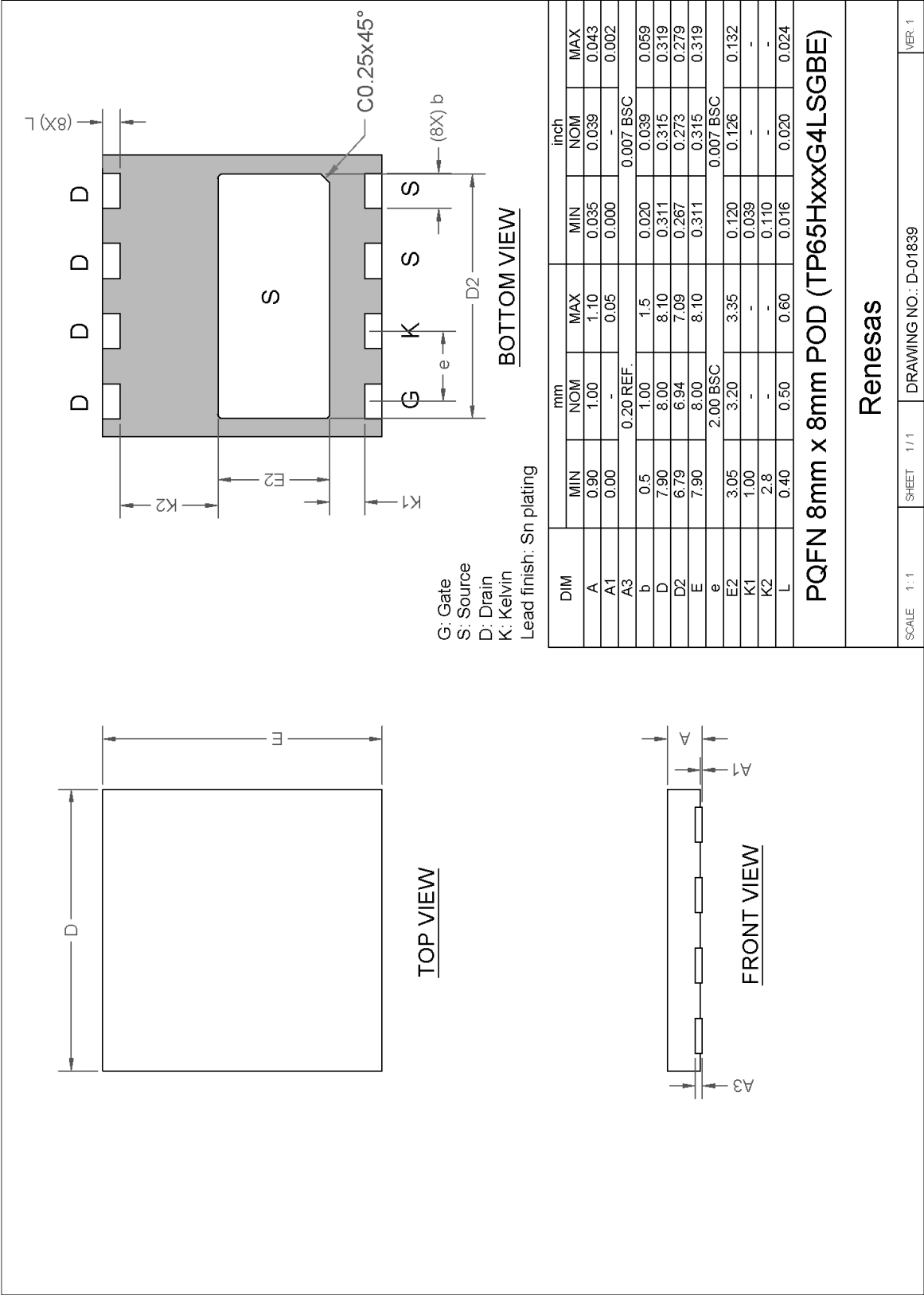


Figure 19. 8 × 8 mm PQFN Package Outline Drawing

6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the [GaN Power Solutions](#) page.

7. Ordering Information

Part Number	Package Description	Package Configuration
TP65H100G4LSGB-TR ^[1]	8 × 8 mm PQFN IP	Source

1. "-TR" suffix refers to tape and reel.

8. Revision History

Revision	Date	Description
2.00	Nov 25, 2025	Updated the document's formatting; no technical changes were completed.
1.01	Jun 13, 2025	Updated Package Outline Drawings (POD).
1.00	Apr 3, 2024	Initial release.

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