

TP65H100G4LSGB

650V SuperGaN® GaN FET in PQFN (source tab)

Description

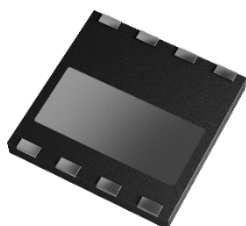
The TP65H100G4LSGB 650V, 85mΩ Gallium Nitride (GaN) FET is a normally-off device using Renesas' Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

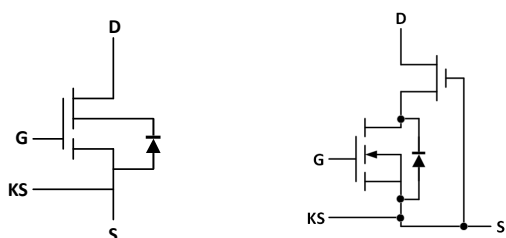
Benefits

- Achieves increased efficiency in both hard-switched and soft-switched circuits
 - Increased power density
 - Reduced system size and weight
 - Overall lower system cost
- Easy to drive with commonly used gate drivers

Product and Schematic Diagrams



TP65H100G4LSGB PQFN



Cascode Schematic Symbol

Cascode Device Structure

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
 - Transient over-voltage capability
 - Operation with E-mode Gate drivers without need for Zener protection.
- Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting



Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$ (V) maximum	800
$R_{DS(on)}$ (mΩ) maximum ^[1]	102
Q_{OSS} (nC) typical	56
Q_G (nC) typical	14.4

1. Dynamic $R_{DS(on)}$; see Figure 21 and Figure 22.

Contents

1. Pin Information	3
1.1 Pin Assignments	3
1.2 Pin Descriptions	3
2. Specifications	4
2.1 Absolute Maximum Ratings	4
2.2 Thermal Specifications	4
2.3 Circuit Implementation	5
2.4 Electrical Specifications – Forward Device	6
2.5 Electrical Specifications – Reverse Device	7
3. Typical Performance Graphs	8
4. Test Circuits and Waveforms	12
5. Package Outline Drawings	13
6. Design Considerations	14
7. Related Information	14
8. Ordering Information	14
9. Revision History	14

Figures

Figure 1. Pin Assignments – Bottom View	3
Figure 2. Simplified Half-Bridge Schematic	5
Figure 3. Simplified Single-Ended Schematic	5
Figure 4. Typical Output Characteristics, $T_J = 25^{\circ}\text{C}$	8
Figure 5. Typical Output Characteristics, $T_J = 150^{\circ}\text{C}$	8
Figure 6. Typical Transfer Characteristics	8
Figure 7. Normalized On-resistance	8
Figure 8. Typical Capacitance	9
Figure 9. Typical C_{oss} Stored Energy	9
Figure 10. Typical Q_{oss}	9
Figure 11. Typical Gate Charge	9
Figure 12. Power Dissipation	10
Figure 13. Current Derating	10
Figure 14. Forward Characteristics of Rev. Diode	10
Figure 15. Transient Thermal Resistance	10
Figure 16. Safe Operating Area $T_C = 25^{\circ}\text{C}$	11
Figure 17. Switching Time Test Circuit	12
Figure 18. Switching Time Waveform	12
Figure 19. Diode Characteristics Test Circuit	12
Figure 20. Diode Recovery Waveform	12
Figure 21. Dynamic $R_{DS(on)eff}$ Test Circuit	12
Figure 22. Dynamic $R_{DS(on)eff}$ Waveform	12

1. Pin Information

1.1 Pin Assignments

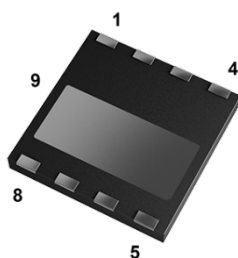


Figure 1. Pin Assignments – Bottom View

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3, 4	D	Drain.
5, 6	S	Source.
7	KS	Kelvin source.
8	G	Gate.
9	S	Source.

2. Specifications

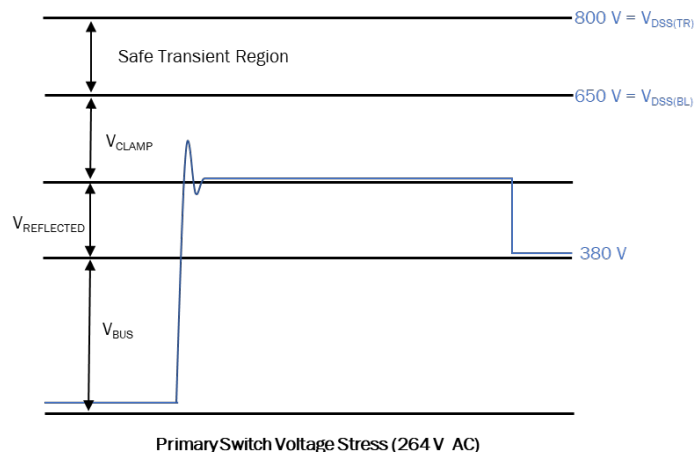
2.1 Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$ unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Unit
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)	-	650	V
$V_{DSS(TR), \text{non-repetitive}}$	Transient drain to source voltage, non-repetitive ^[1]	-	800	
$V_{DSS(TR), \text{repetitive}}$	Transient drain to source voltage, repetitive ^[2]	-	750	
V_{GSS}	Gate to source voltage	-20	+20	
P_D	Maximum power dissipation at $T_c = 25^\circ\text{C}$	-	65.8	W
I_D	Continuous drain current at $T_c = 25^\circ\text{C}$ ^[3]	-	18.9	A
	Continuous drain current at $T_c = 100^\circ\text{C}$ ^[3]	-	12	A
I_{DM}	Pulsed drain current (pulse width: 10 μs)	-	95	A
T_J	Junction operating temperature	-55	+150	$^\circ\text{C}$
T_S	Storage temperature	-55	+150	$^\circ\text{C}$
T_{SOLD}	Reflow soldering temperature ^[4]	-	260	$^\circ\text{C}$

1. In off-state, spike duration < 30 μs , non-repetitive.
2. Off-state, spike duration < 5 μs , repetitive.
3. For increased stability at high current operation, see [Circuit Implementation](#).
4. Reflow MSL3.



2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\theta JC}$	Junction-to-case	1.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-ambient ^[1]	50	

1. Device on one layer epoxy PCB for source connection (vertical and without air stream cooling, with 6cm² copper area and 70 μm thickness).

2.3 Circuit Implementation

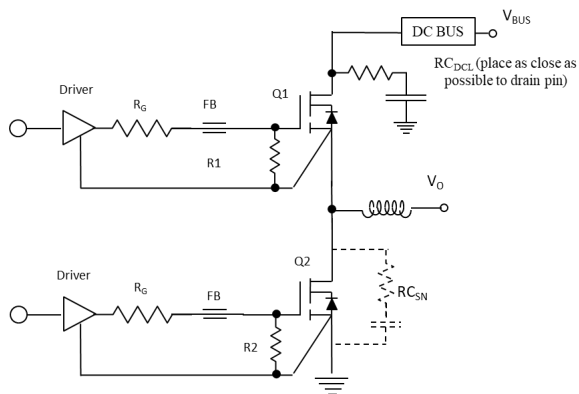


Figure 2. Simplified Half-Bridge Schematic

Recommended gate drive: (0V, 10–12V) with $R_{G(\text{tot})} = 36\Omega$ ^[1]

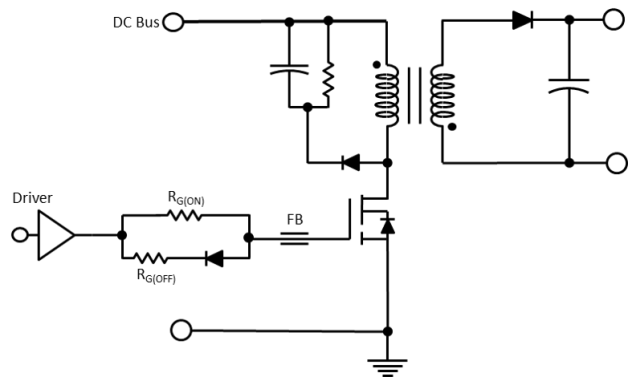


Figure 3. Simplified Single-Ended Schematic

Recommended gate drive:
(0V, 10–12V): $R_{G(\text{ON})} = 50$ to 150Ω ; $R_{G(\text{OFF})} = 0$ to 10Ω

Gate Ferrite Bead (FB1)	Recommended DC Link RC Snubber (RC_{DCL}) ^[2]
100–330 Ω at 100MHz	$[10\text{nF} + 10\Omega] \times 2$

1. For bridge topologies only. R_G could be much smaller in single-ended topologies.
2. RC_{DCL} should be placed as close as possible to the drain pin.

For additional driver configurations/options, see application note [Recommended External Circuitry for Renesas GaN FETs](#).

2.4 Electrical Specifications – Forward Device

$T_J = 25^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	$V_{GS} = 0V$	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 0.5mA$	3.2	3.65	4.1	V
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient		-	-5.8	-	mV/ $^\circ\text{C}$
$R_{DS(on)eff}$	Drain-source on-resistance ^[1]	$V_{GS} = 10V, I_D = 12A, T_J = 25^\circ\text{C}$	-	85	102	m Ω
		$V_{GS} = 10V, I_D = 12A, T_J = 150^\circ\text{C}$	-	184	-	
I_{DSS}	Drain-to-source leakage current	$V_{DS} = 650V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	-	2.5	25	μA
		$V_{DS} = 650V, V_{GS} = 0V, T_J = 150^\circ\text{C}$	-	5	-	
I_{GSS}	Gate-to-source forward leakage current	$V_{GS} = 20V$	-	-	100	nA
	Gate-to-source reverse leakage current	$V_{GS} = -20V$	-	-	-100	
C_{iss}	Input capacitance	$V_{GS} = 0V, V_{DS} = 400V, f = 500kHz$	-	818	-	pF
C_{oss}	Output capacitance		-	53	-	
C_{rss}	Reverse transfer capacitance		-	3.6	-	
$C_{O(er)}$	Output capacitance, energy related ^[2]	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$	-	78	-	pF
$C_{O(tr)}$	Output capacitance, time related ^[3]		-	139	-	
Q_G	Total gate charge	$V_{DS} = 400V, V_{GS} = 0V \text{ to } 10V, I_D = 12A$	-	14.4	-	nC
Q_{GS}	Gate-source charge		-	4.7	-	
Q_{GD}	Gate-drain charge		-	5.2	-	
Q_{oss}	Output charge	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$	-	56	-	nC
$t_{D(on)}$	Turn-on delay	$V_{DS} = 400V, V_{GS} = 0V \text{ to } 12V, I_D = 13A, R_{G_on} = 36\Omega, Z_{FB} = 120\Omega \text{ at } 100MHz \text{ (see Figure 17)}$	-	23	-	ns
t_R	Rise time		-	7.1	-	
$t_{D(off)}$	Turn-off delay		-	58	-	
t_F	Fall time		-	7.5	-	

1. Dynamic $R_{DS(on)}$, 100% tested; see [Figure 21](#) and [Figure 22](#) for conditions.
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

2.5 Electrical Specifications – Reverse Device

$T_J = 25^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	$V_{GS} = 0V$, $T_C = 100^\circ\text{C}$, $\leq 25\%$ duty cycle	-	-	12	A
V_{SD}	Reverse voltage ^[1]	$V_{GS} = 0V$, $I_S = 12A$	-	1.7	-	V
		$V_{GS} = 0V$, $I_S = 8A$	-	1.4	-	
t_{RR}	Reverse recovery time	$I_S = 13A$, $V_{DD} = 400V$, $di/dt = 1000A/\mu s$	-	17.9	-	ns
Q_{RR}	Reverse recovery charge ^[2]		-	0	-	nC

1. Includes dynamic $R_{DS(on)}$ effect.
2. Excludes Q_{oss} .

3. Typical Performance Graphs

$T_c = 25^\circ\text{C}$ unless otherwise stated.

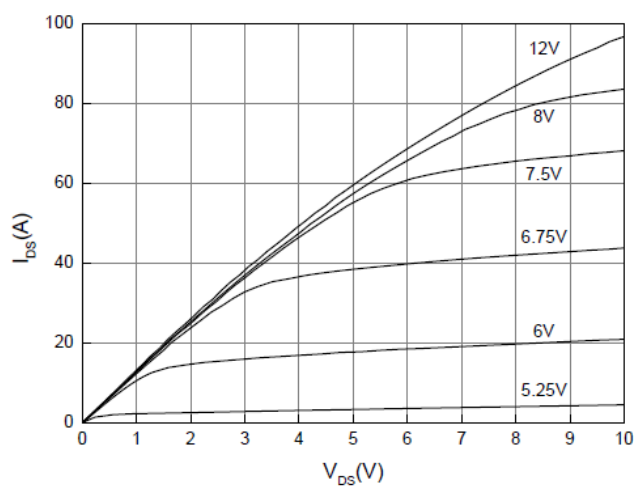


Figure 4. Typical Output Characteristics, $T_J = 25^\circ\text{C}$

Parameter: V_{GS}

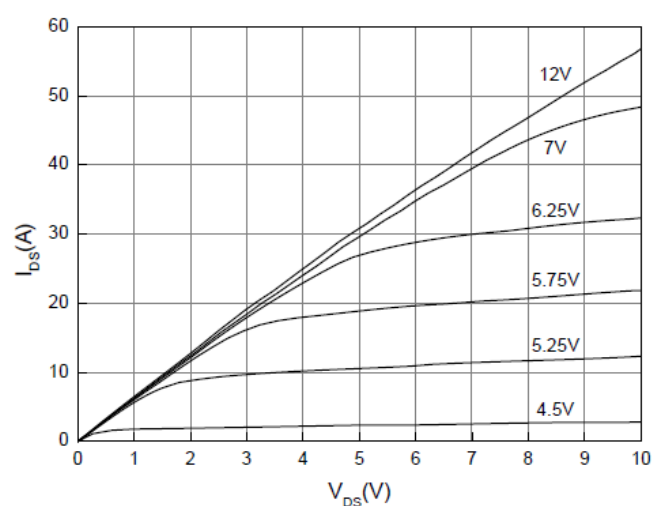


Figure 5. Typical Output Characteristics, $T_J = 150^\circ\text{C}$

Parameter: V_{GS}

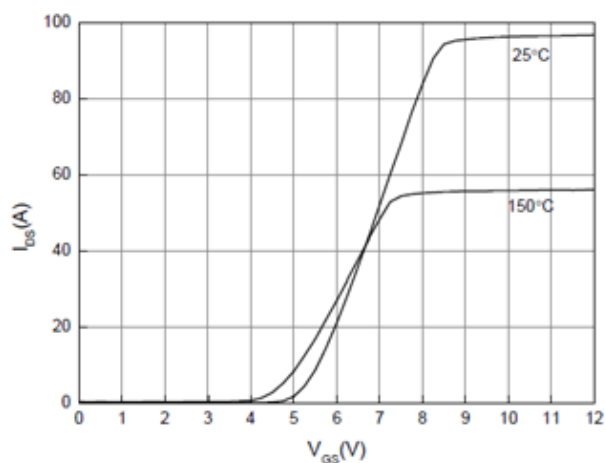


Figure 6. Typical Transfer Characteristics

$V_{DS} = 10\text{V}$, parameter: T_J

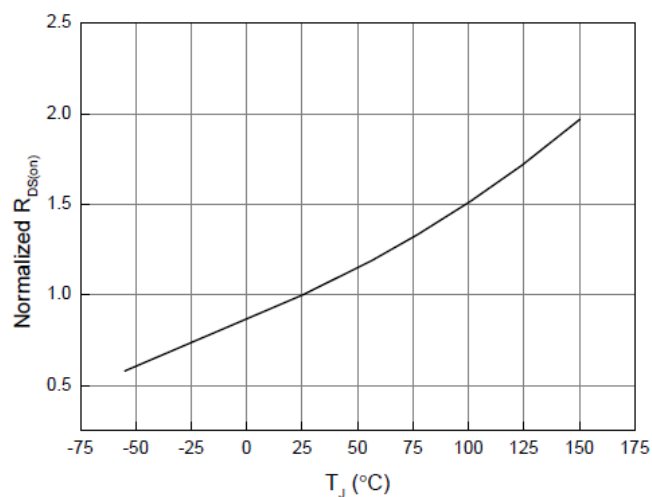


Figure 7. Normalized On-resistance

$I_D = 12\text{A}$, $V_{GS} = 10\text{V}$

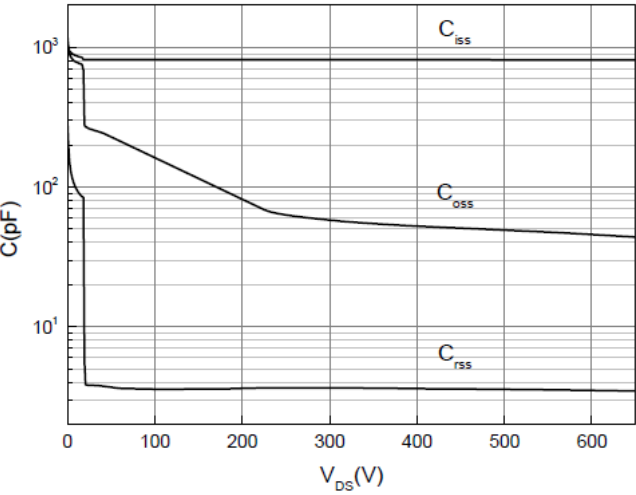


Figure 8. Typical Capacitance
V_{GS} = 0V, f = 500kHz

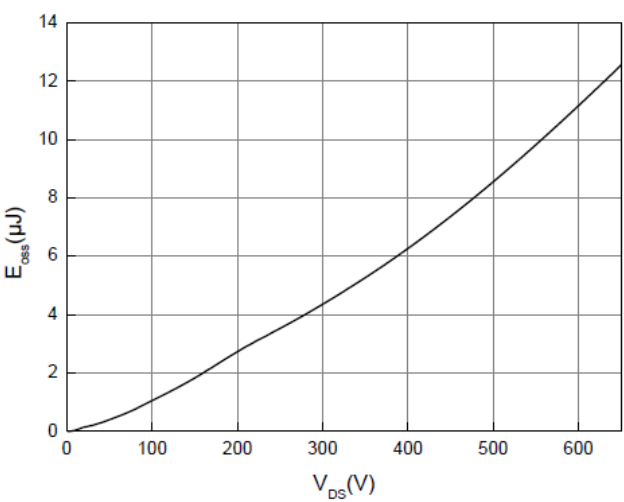


Figure 9. Typical Coss Stored Energy

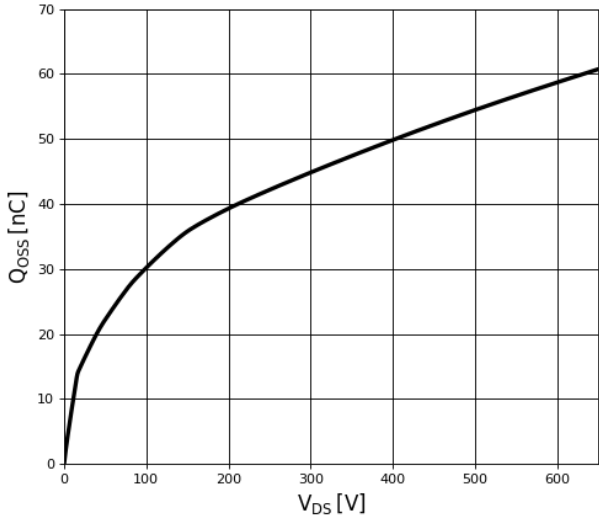


Figure 10. Typical Qoss

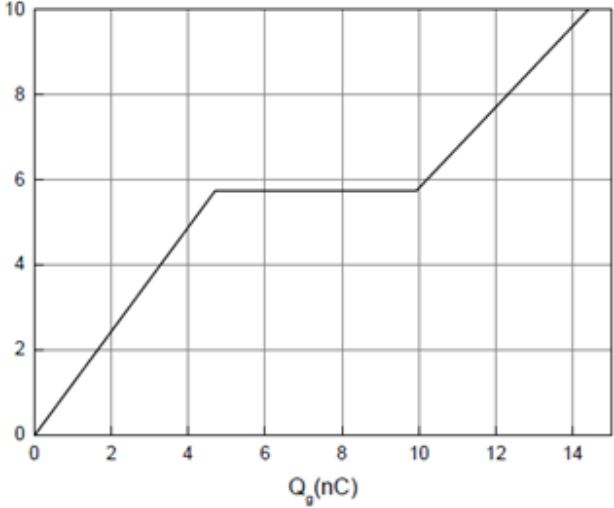


Figure 11. Typical Gate Charge
I_{DS} = 12A, V_{DS} = 400V

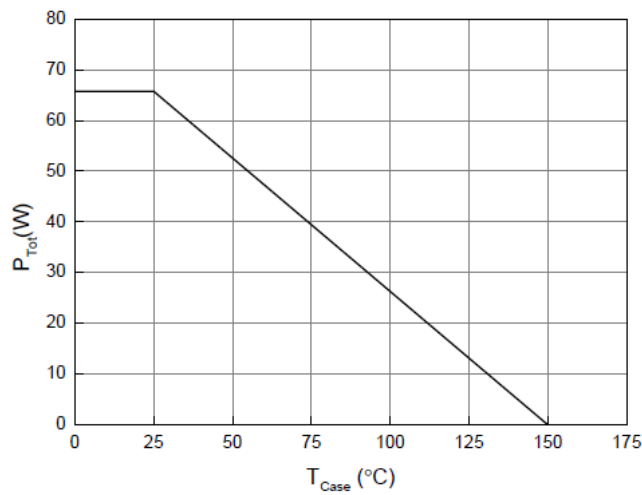


Figure 12. Power Dissipation

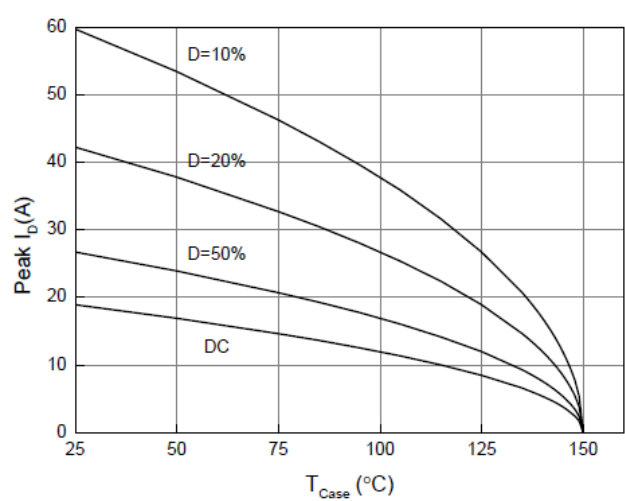


Figure 13. Current Derating
Pulse width ≤ 10μs, V_{GS} ≥ 10V

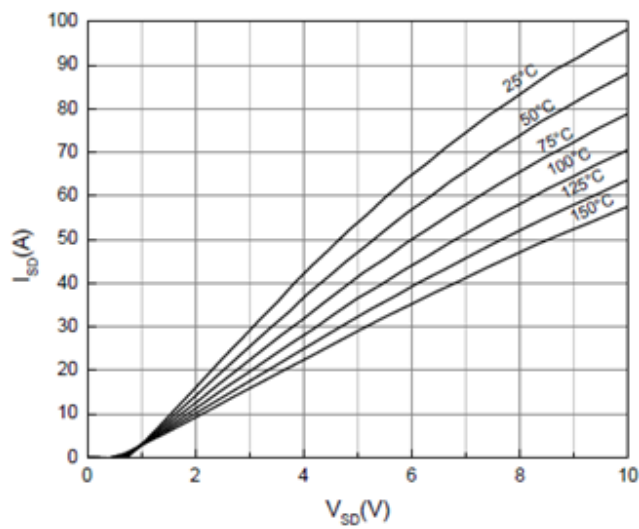


Figure 14. Forward Characteristics of Rev. Diode
I_S = f(V_{SD}), parameter: T_J

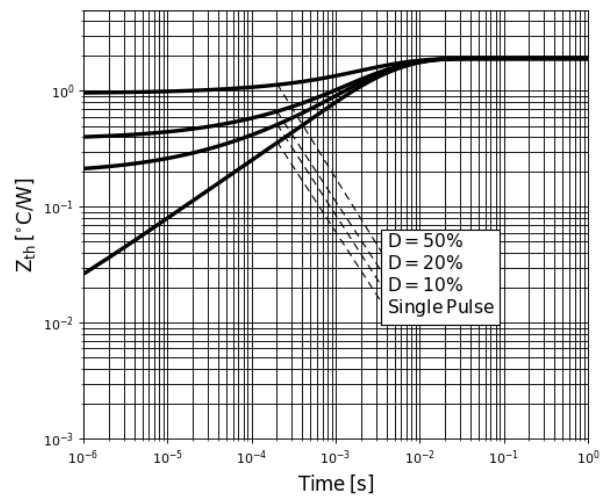


Figure 15. Transient Thermal Resistance

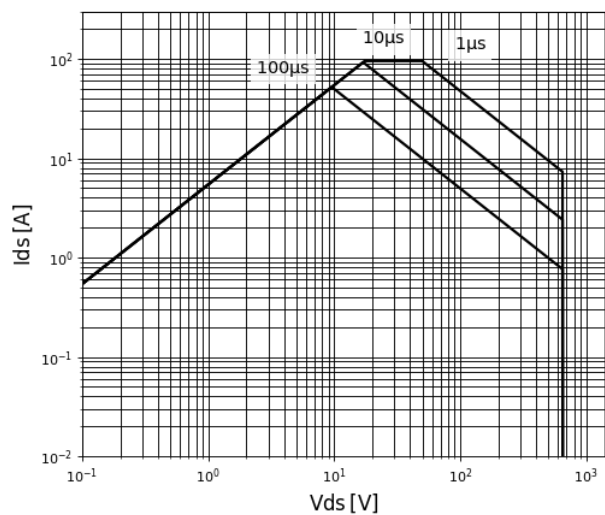


Figure 16. Safe Operating Area $T_c = 25^\circ\text{C}$

4. Test Circuits and Waveforms

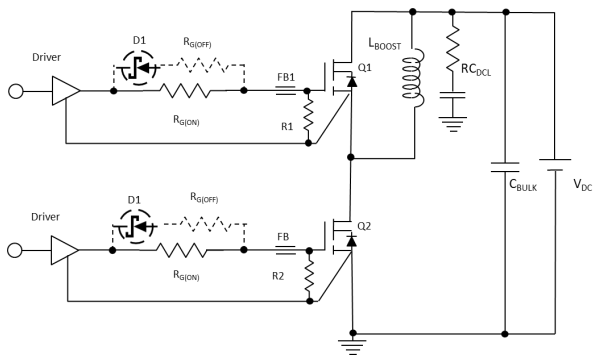


Figure 17. Switching Time Test Circuit

(For methods to ensure clean switching, see [Circuit Implementation](#))

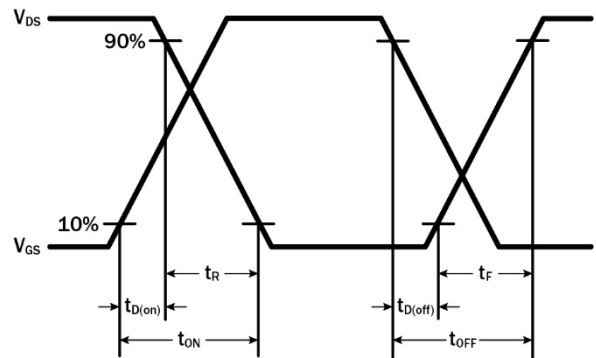


Figure 18. Switching Time Waveform

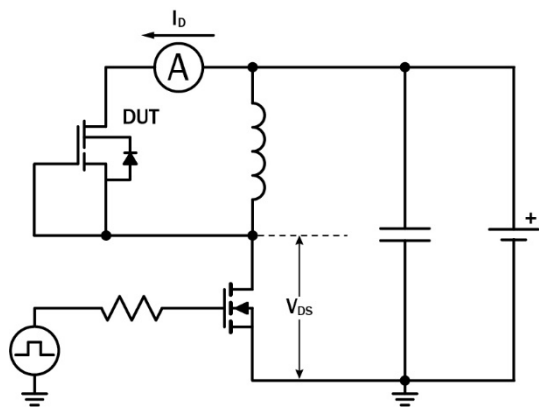


Figure 19. Diode Characteristics Test Circuit

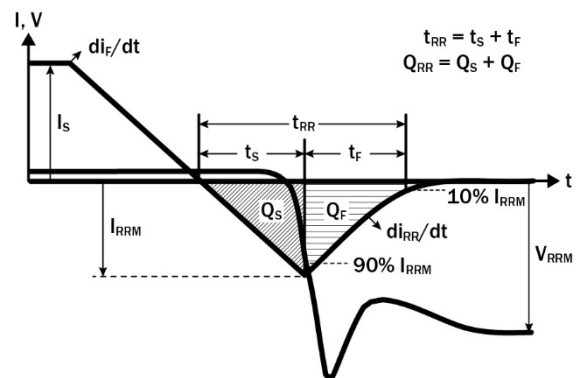


Figure 20. Diode Recovery Waveform

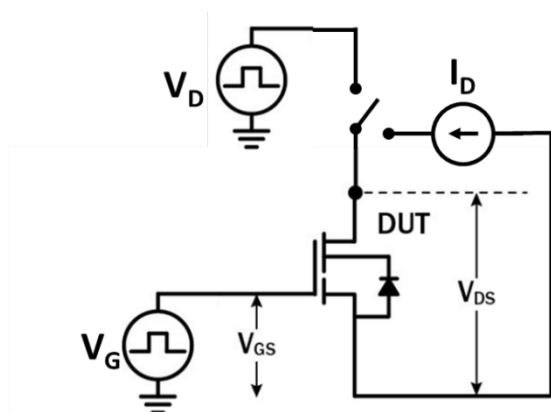


Figure 21. Dynamic $R_{DS(on)eff}$ Test Circuit

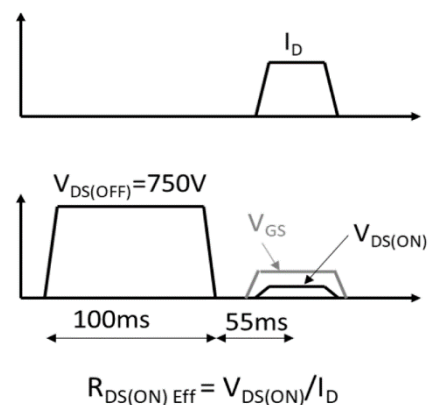
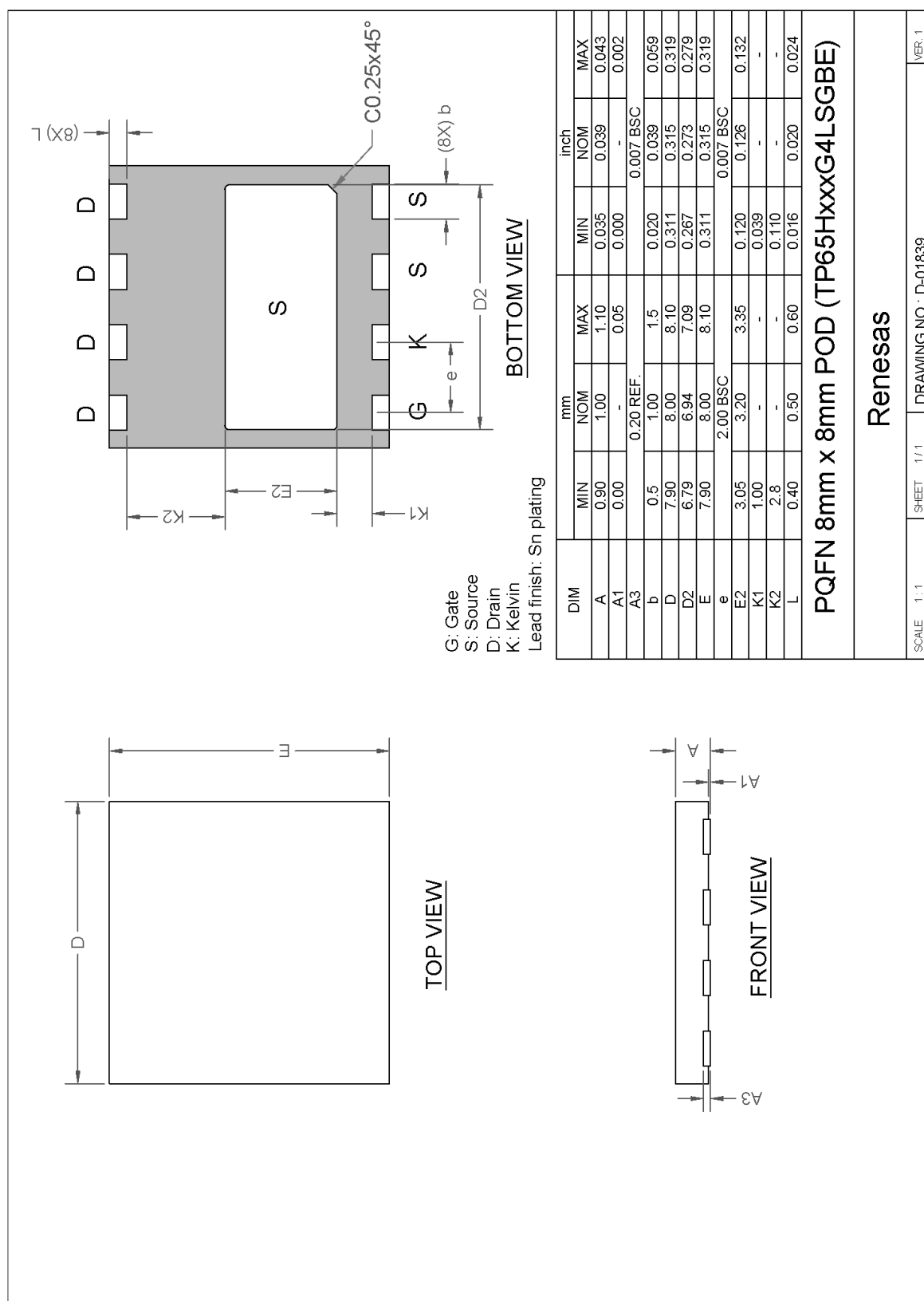


Figure 22. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings



6. Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high-frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Renesas GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The following table provides some practical rules that should be followed during the evaluation.

When Evaluating Renesas GaN Devices:	
DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop.	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout.
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB.	Use long traces in drive circuit, long lead length of the devices.
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points.	Use differential mode probe or probe ground clip with long wire.

7. Related Information

The complete technical library of GaN design tools can be found at [Renesas](#):

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

Specific resources include:

- [Printed Circuit Board Layout and Probing for GaN Power Switches](#)
- [Recommendations for Vapor Phase Reflow](#)
- [Recommended External Circuitry for GaN FETs](#)
- [PQFN Tape and Reel Information](#)

8. Ordering Information

Part Number	Package Description	Package Configuration
TP65H100G4LSGB-TR ^[1]	8 × 8 PQFN	Source

1. "-TR" suffix refers to tape and reel.

9. Revision History

Revision	Date	Description
1.01	Jun 13, 2025	Updated Package Outline Drawings (POD).
1.00	Apr 3, 2024	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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