Datasheet

TP65H030G4PRS

650V SuperGaN® GaN FET in TOLT (source tab)

Description

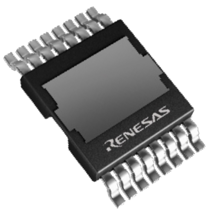
The TP65H030G4PRS 650V, 30mΩ Gallium Nitride (GaN) FET is a normally-off device using Renesas' Gen IV plus platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior performance, standard drive, ease of adoption and reliability.

The Gen IV plus SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

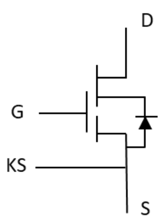
Benefits

- Superior normally off architecture with D-mode GaN HEMT
- Compatible with standard silicon drivers
- Enhanced noise immunity with a 4V threshold voltage with no negative gate drive required
- Enables high-efficiency, high power density, and reliable power conversion
- Facilitates cost-effective GaN adoption reducing system size, weight, and costs

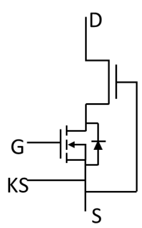
Product and Schematic Diagrams



TP65H030G4PRS TOLT



Cascode Schematic Symbol



Cascode Device Structure

Features

- Ultra-fast switching Gen IV plus GaN
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Zero reverse recovery charge
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Applications

- AI datacenter and telecom power supplies
- E-mobility charging
- PV inverter
- UPS
- BESS

Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$(V) maximum	800
$R_{DS(on)}$ (mΩ) maximum [1]	41
Q_{OSS} (nC) typical	135
Q_G (nC) typical	24.5

1. Dynamic $R_{DS(on)}$ (see Figure 20 and Figure 21)

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1. Pin Information

1.1 Pin Assignments

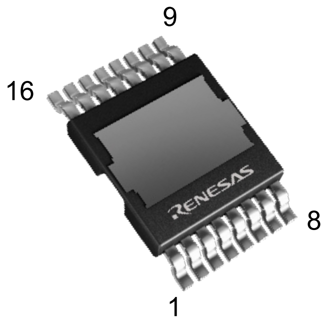


Figure 1. Pin Assignments

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3, 4, 5, 6, 7, 8	D	Drain.
9	G	Gate.
10	KS	Kelvin Source.
11, 12, 13, 14, 15, 16	S	Source.

2. Specifications

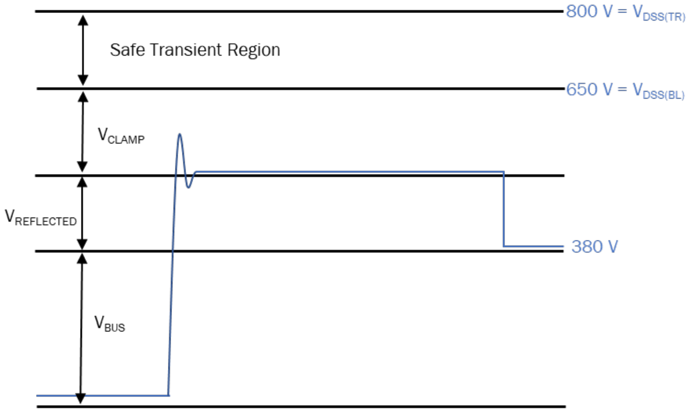
2.1 Absolute Maximum Ratings

T_c = 25°C unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)	-	650	V
$V_{DSS(TR)\text{, non-repetitive}}$	Transient drain to source voltage, non-repetitive [1]	-	800	
$V_{DSS(TR)\text{, repetitive}}$	Transient drain to source voltage, repetitive [2]	-	750	
V_{GSS}	Gate to source voltage	-20	+20	
P_D	Maximum power dissipation at T_C = 25°C	-	192	W
I_D	Continuous drain current at T_C = 25°C [3]	-	55.7	A
	Continuous drain current at T_C = 100°C [3]	-	35	A
I_{DM}	Pulsed drain current (pulse width: 10µs)	-	230	A
T_J	Operating temperature junction	-55	+150	°C
T_S	Storage temperature	-55	+150	°C
T_{SOLD}	Reflow soldering temperature [4]	-	260	°C

1. In off-state, spike duration < 30µs, non-repetitive.
2. Off-state, spike duration < 5µs.
3. For increased stability at high current operation, see Circuit Implementation.
4. Reflow MSL3.



Primary Switch Voltage Stress (264 V AC)

2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\theta JC}$	Junction-to-case	0.65	°C/W
$R_{\theta JA}$	Junction-to-ambient	40	

2.3 Circuit Implementation

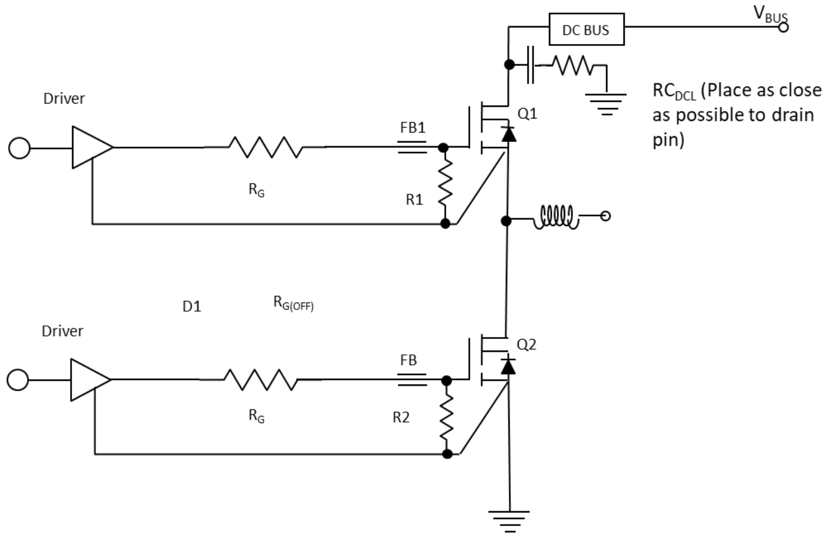


Figure 2. Simplified Half-Bridge Schematic

Recommended gate drive: (0V, 12V) with $R_{G(tot)}$ = 30Ω [1]

Gate Ferrite Bead (FB1)	Recommended DC Link RC Snubber (RC_{DCL}) [2]
120Ω at 100MHz	10nF + 2.3Ω

1. For bridge topologies only.
2. Place RC_{DCL} as close as possible to the drain pin.

For additional driver configurations/options, see application note Recommended External Circuitry for Renesas GaN FETs.

2.4 Electrical Specifications – Forward Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	V_{GS} = 0V	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, I_D = 1mA	3.3	4	4.8	V
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient		-	-6.5	-	mV/°C
$R_{DS(on)eff}$	Drain-source on-resistance [1]	V_{GS} = 12V, I_D = 30A, T_J = 25°C	-	30	41	mΩ
		V_{GS} = 12V, I_D = 30A, T_J = 150°C	-	62	-	
I_{DSS}	Drain-to-source leakage current	V_{DS} = 650V, V_{GS} = 0V, T_J = 25°C	-	3	30	µA
		V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C	-	20	-	
I_{GSS}	Gate-to-source forward leakage current	V_{GS} = 20V	-	-	400	µA
	Gate-to-source reverse leakage current	V_{GS} = -20V	-	-	-400	
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 400V, f = 1MHz	-	1500	-	pF
C_{OSS}	Output capacitance		-	127	-	
C_{RSS}	Reverse transfer capacitance		-	4.6	-	
$C_{O(er)}$	Output capacitance, energy related [2]	V_{GS} = 0V, V_{DS} = 0V to 400V	-	183	-	pF
$C_{O(tr)}$	Output capacitance, time related [3]		-	339	-	
Q_G	Total gate charge	V_{DS} = 400V, V_{GS} = 0V to 12V, I_D = 30A	-	24.5	-	nC
Q_{GS}	Gate-source charge		-	8.4	-	
Q_{GD}	Gate-drain charge		-	6.6	-	
Q_{OSS}	Output charge	V_{GS} = 0V, V_{DS} = 0V to 400V	-	135	-	nC
$t_{D(on)}$	Turn-on delay	V_{DS} = 400V, V_{GS} = 0V to 12V, $R_{G(on)}$ = 10Ω, $R_{G(off)}$ = 30Ω, I_D = 30A, Z_{FB} = 180Ω at 100MHz (see Figure 16)	-	26.4	-	ns
t_R	Rise time		-	6.4	-	
$t_{D(off)}$	Turn-off delay		-	63.6	-	
t_F	Fall time		-	5.2	-	

1. Dynamic $R_{DS(on)}$, 100% tested; see Figure 20 and Figure 21 for conditions.
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

2.5 Electrical Specifications – Reverse Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	V_{GS} = 0V, T_C = 100°C, ≤ 25% duty cycle	-	-	32	A
V_{SD}	Reverse voltage [1]	V_{GS} = 0V, I_S = 32A	-	1.8	-	V
		V_{GS} = 0V, I_S = 16A	-	1.3	-	
t_{RR}	Reverse recovery time	I_S = 10A, V_{DD} = 400V, di/dt = 1000A/µs	-	36	-	ns
Q_{RR}	Reverse recovery charge [2]		-	0	-	nC

1. Includes dynamic $R_{DS(on)}$ effect.
2. Excludes Q_{OSS}.

3. Typical Performance Graphs

T_C = 25°C unless otherwise stated.

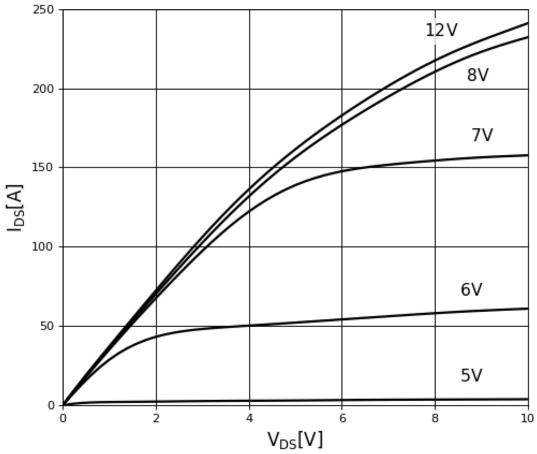


Figure 3. Typical Output Characteristics, T_J = 25°C

Parameter: V_{GS}

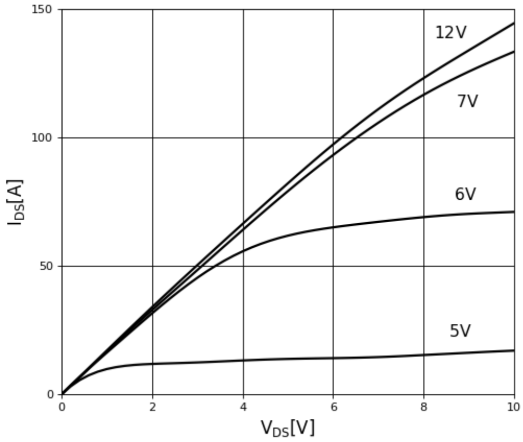


Figure 4. Typical Output Characteristics, T_J = 150°C

Parameter: V_{GS}

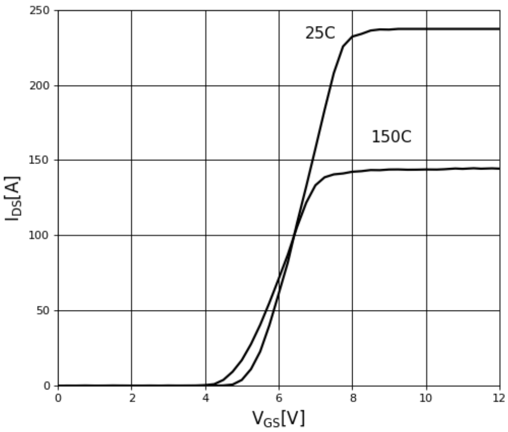


Figure 5. Typical Transfer Characteristics

V_{DS} = 10V, parameter: T_J

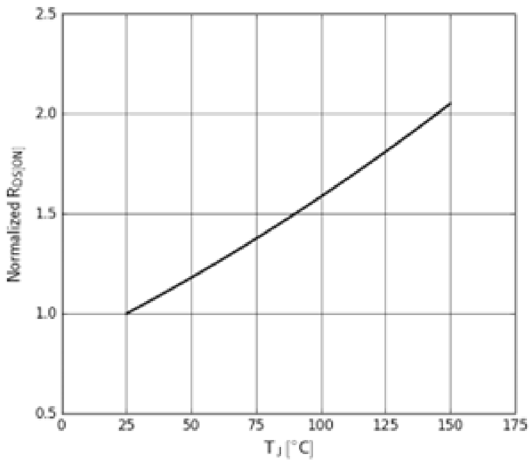


Figure 6. Normalized On-Resistance

I_D = 30A, V_{GS} = 12V

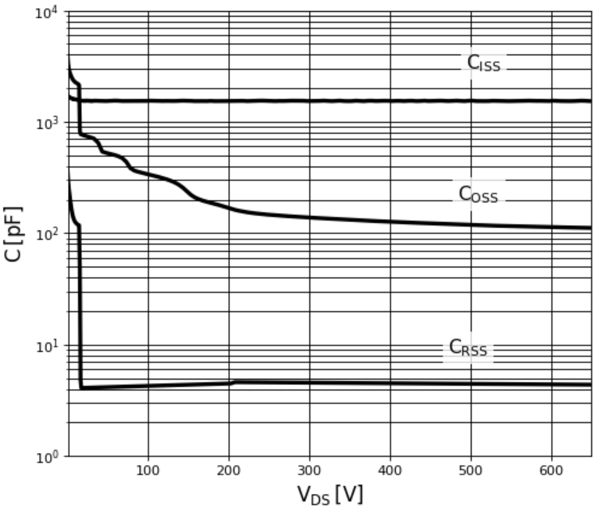


Figure 7. Typical Capacitance

V_{GS} = 0V, f = 1MHz

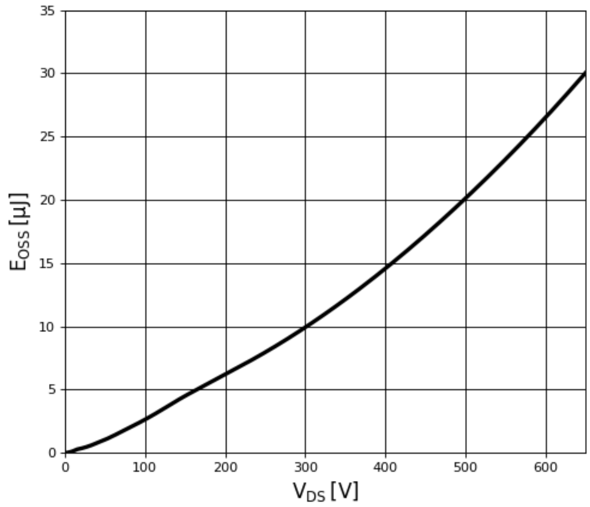


Figure 8. Typical C_{OSS} Stored Energy

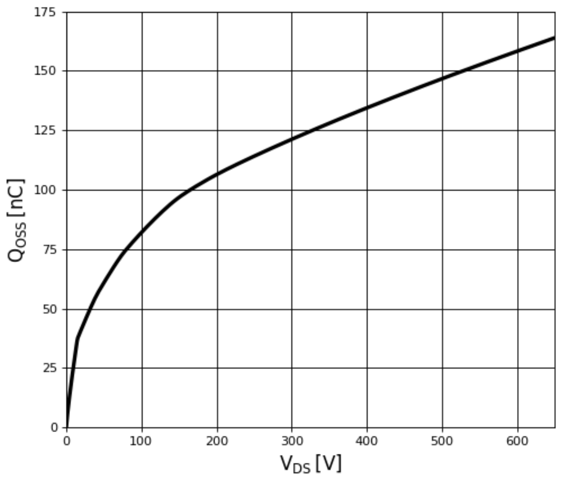


Figure 9. Typical QOSS

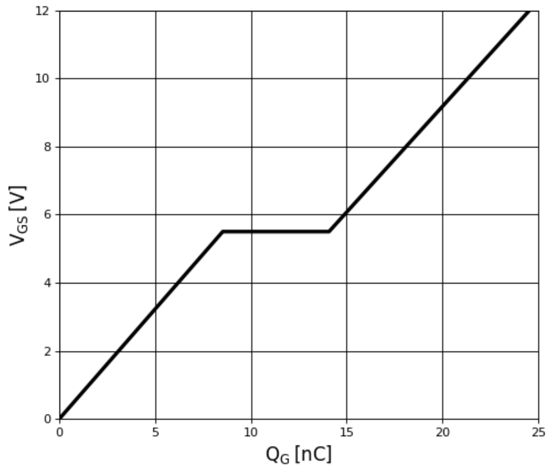


Figure 10. Typical Gate Charge

I_{DS} = 30A, V_{DS} = 400V

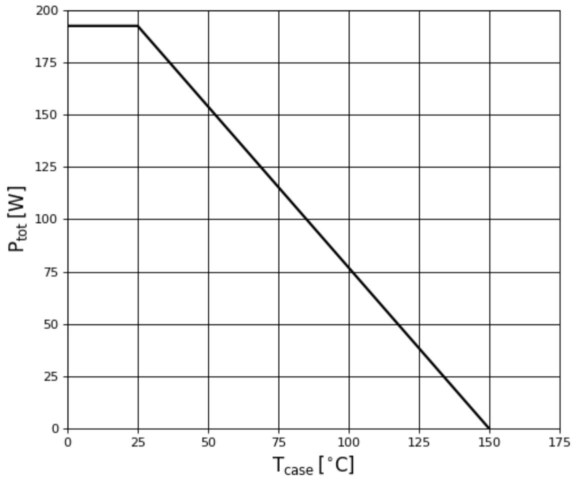


Figure 11. Power Dissipation

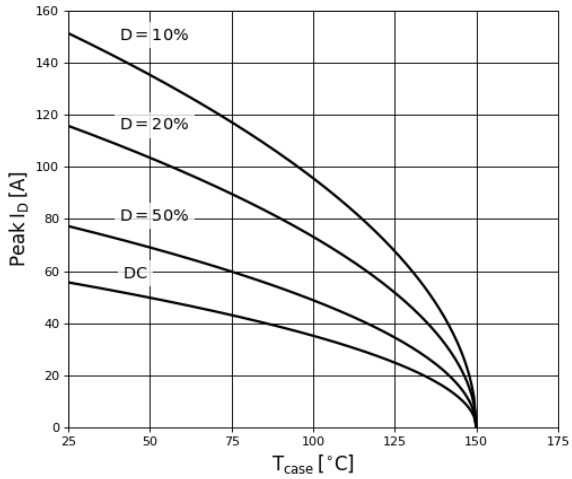


Figure 12. Current Derating

Pulse width ≤ 10µs, V_{GS} ≥ 12V

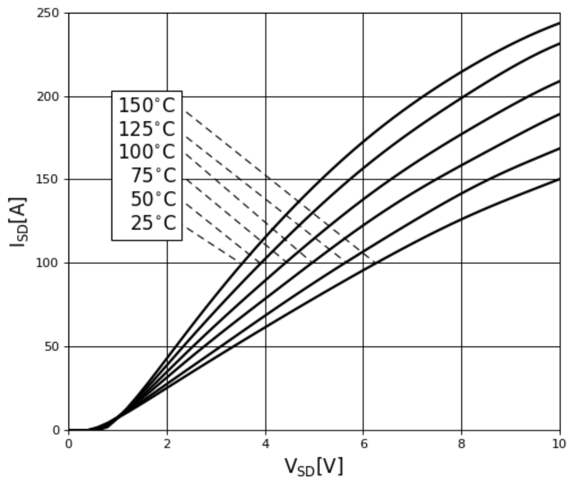


Figure 13. Forward Characteristics of Rev. Diode

$I_S = f(V_{SD})$, parameter: T_J

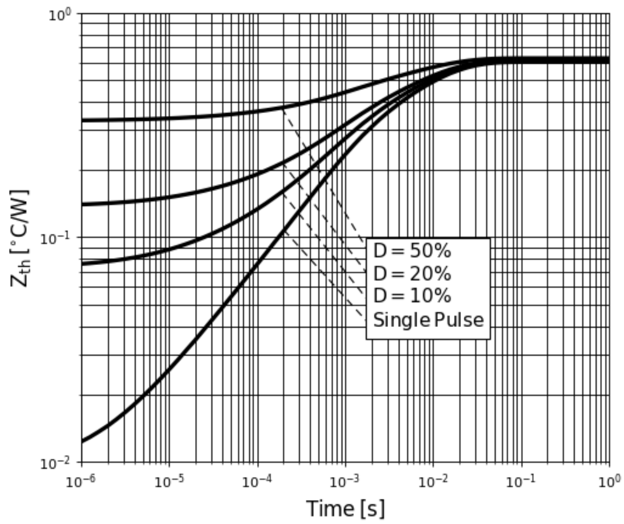


Figure 14. Transient Thermal Resistance

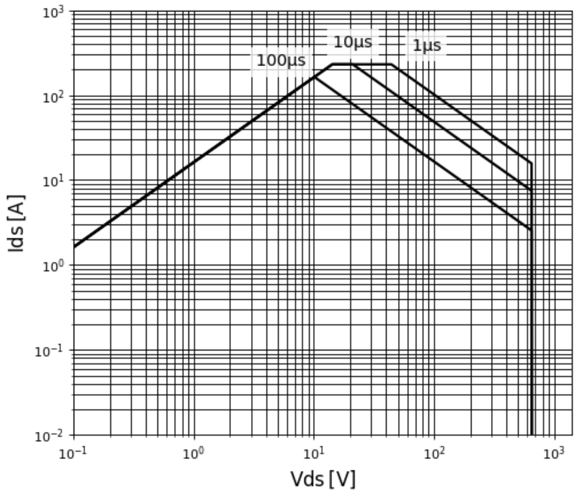


Figure 15. Safe Operating Area T_C = 25°C

4. Test Circuits and Waveforms

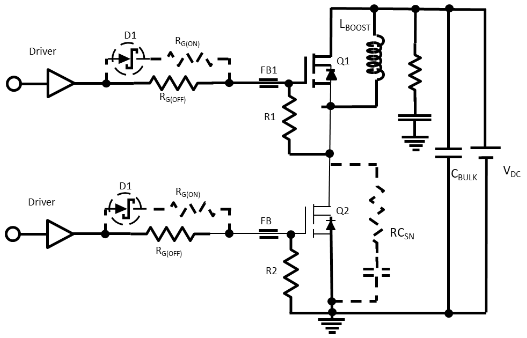


Figure 16. Switching Time Test Circuit

(For methods to ensure clean switching, see Circuit Implementation)

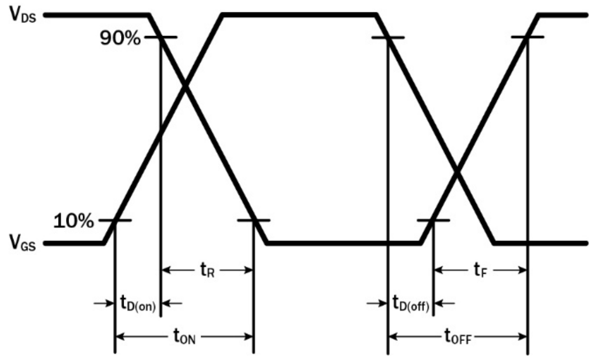


Figure 17. Switching Time Waveform

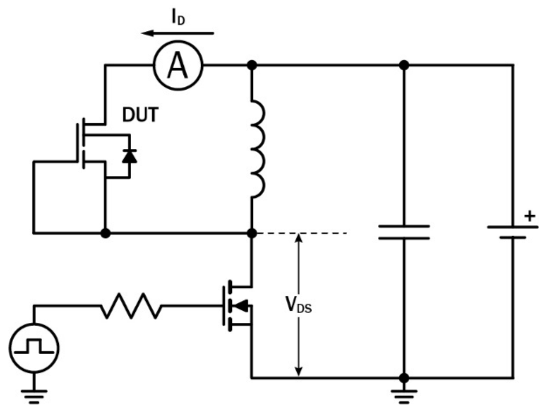


Figure 18. Diode Characteristics Test Circuit

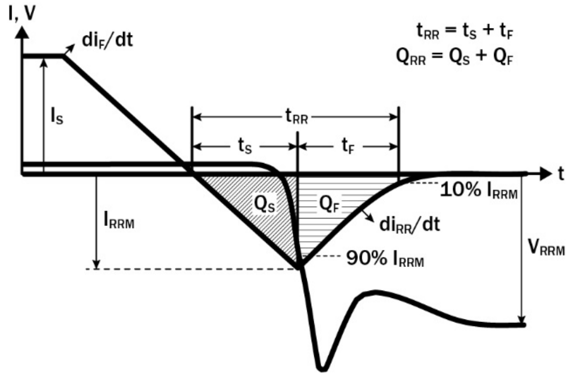


Figure 19. Diode Recovery Waveform

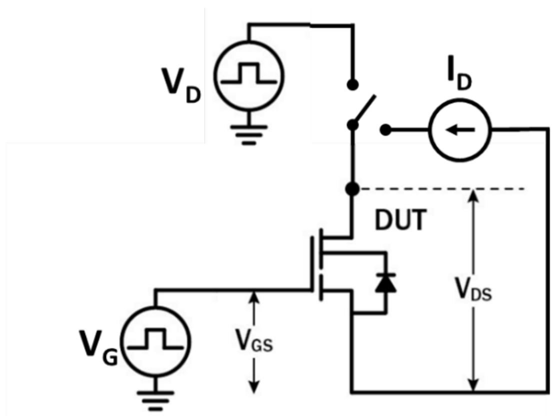


Figure 20. Dynamic $R_{DS(on)eff}$ Test Circuit

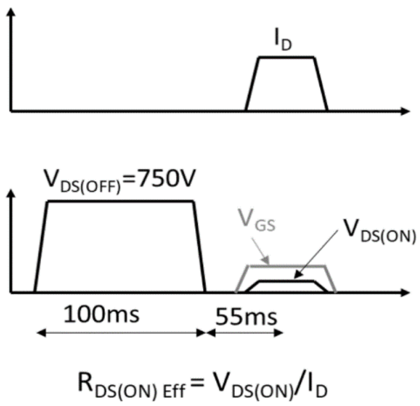
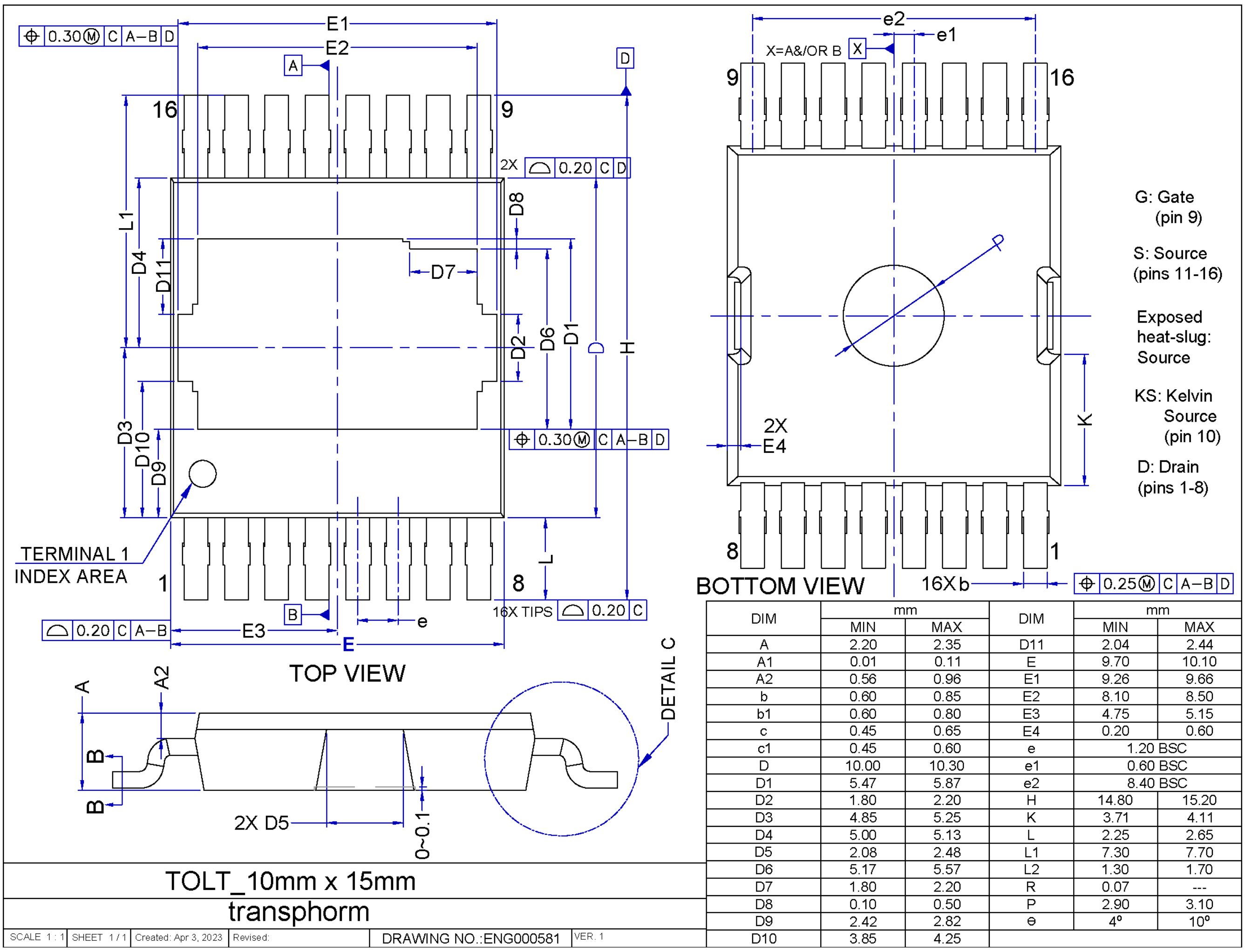


Figure 21. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings



DIM	mm MIN	mm MAX	DIM	mm MIN	mm MAX
A	2.20	2.35	D11	2.04	2.44
A1	0.01	0.11	E	9.70	10.10
A2	0.56	0.96	E1	9.26	9.66
b	0.60	0.85	E2	8.10	8.50
b1	0.60	0.80	E3	4.75	5.15
c	0.45	0.65	E4	0.20	0.60
c1	0.45	0.60	e	1.20 BSC	
D	10.00	10.30	e1	0.60 BSC	
D1	5.47	5.87	e2	8.40 BSC	
D2	1.80	2.20	H	14.80	15.20
D3	4.85	5.25	K	3.71	4.11
D4	5.00	5.13	L	2.25	2.65
D5	2.08	2.48	L1	7.30	7.70
D6	5.17	5.57	L2	1.30	1.70
D7	1.80	2.20	R	0.07	---
D8	0.10	0.50	P	2.90	3.10
D9	2.42	2.82	θ	4°	10°
D10	3.85	4.25			

6. Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high-frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Renesas GaN devices, see application note *Printed Circuit Board Layout and Probing for GaN Power Switches*. The following table provides some practical rules to follow during the evaluation.

When Evaluating Renesas GaN Devices:	
DO	**DO NOT**
Minimize circuit inductance by keeping traces short, both in the drive and power loop.	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout.
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB.	Use long traces in drive circuit, long lead length of the devices.
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points.	Use differential mode probe or probe ground clip with long wire.

7. Related Information

The complete technical library of GaN design tools can be found at Renesas:

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

Specific resources include:

- *Printed Circuit Board Layout and Probing for Gan Power Switches*
- *Recommendations for Vapor Phase Reflow*
- *Recommended External Circuitry for GaN FETs*

8. Ordering Information

Part Number	Package Description
TP65H030G4PRS	TOLT

9. Revision History

Revision	Date	Description
1.00	Jun 25, 2025	Initial release.

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