PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

µPD65977S1-xxx-B6

SYSTEM-ON-CHIP LITE
GATE ARRAY WITH ARM7TDMI SUBSYSTEM
HARDWARE

DESCRIPTION

The System-on-Chip Lite ("SoCLite") is based on standard ASIC technology and consists of two blocks: an ARM7TDMI based subsystem and a sea-of-gates area. The ARM subsystem is fully designed and verified as a supermacro. It frees the user from the task of developing a complete RISC computer system. The sea-of-gates area allows the user to implement custom logic or special peripheral functions.

The SoCLite is designed for embedded control applications. To maintain flexibility, SoCLite is not realized as an ASSP (Application Specific Standard Product), this means that it can be used for a wide range of different applications. Once the customer functions are implemented into the sea-of-gates, it becomes a custom SoC.

The ARM7TDMI based subsystem of SoCLite offers a basic combination of general purpose peripheral functions, like a serial communication interface (UART), Timer (32-bit), Interrupt Controller, Watchdog, internal RAM and ROM (only as boot-ROM).

Functions in detail are described in the following user's manual. Be sure to read this manual when you design your systems.

System-on-Chip Lite User's Manual - Hardware : A15402EE1V0UM00

FEATURES

- 32-bit RISC CPU with Von Neumann Architecture
- Internal 2 Kbyte ROM (boot ROM only)
- Internal 8 Kbyte RAM
- Serial Interface
  - UART mode: 1 channel
- Timer
  - 32-bit timer with load register: 1 channel
  - Watchdog timer: 1 channel
- Interrupt Controller with 32 prioritized interrupt sources
- External Bus Interface (32-bit data / 26-bit address bus)
- On-chip debug capability via JTAG
- Built-in power saving mode
- Power supply voltage range: 3.0 V ≤ V_{DD} ≤ 3.6 V
- Frequency range: up to 35 MHz for ARM subsystem
- Crystal frequency range: 4 MHz ≤ $f_{CRYSTAL}$ ≤ 16 MHz
- Built-in clock oscillator circuit with internal PLL
  - PLL output: 6.25 MHz to 115 MHz
- Temperature range: -40 °C to +85 °C
- Package: 256 Plastic BGA, (27 x 27 mm)
- Process: CMOS-9HD
- Sea-of-Gates: 190K raw gates for user defined logic

ORDERING INFORMATION

Device	Part Number	Package	ROM	RAM	Oper. Freq.
SoCLite	µPD65977S1-xxx-B6	256 PBGA 27 x 27 mm	2 K boot ROM	8 K	35 MHz

The information contained in this document is released in advance of the production cycle for the device. The parameters for the device may change before final production, or NEC Corporation may, at its own discretion, withdraw the device prior to production.

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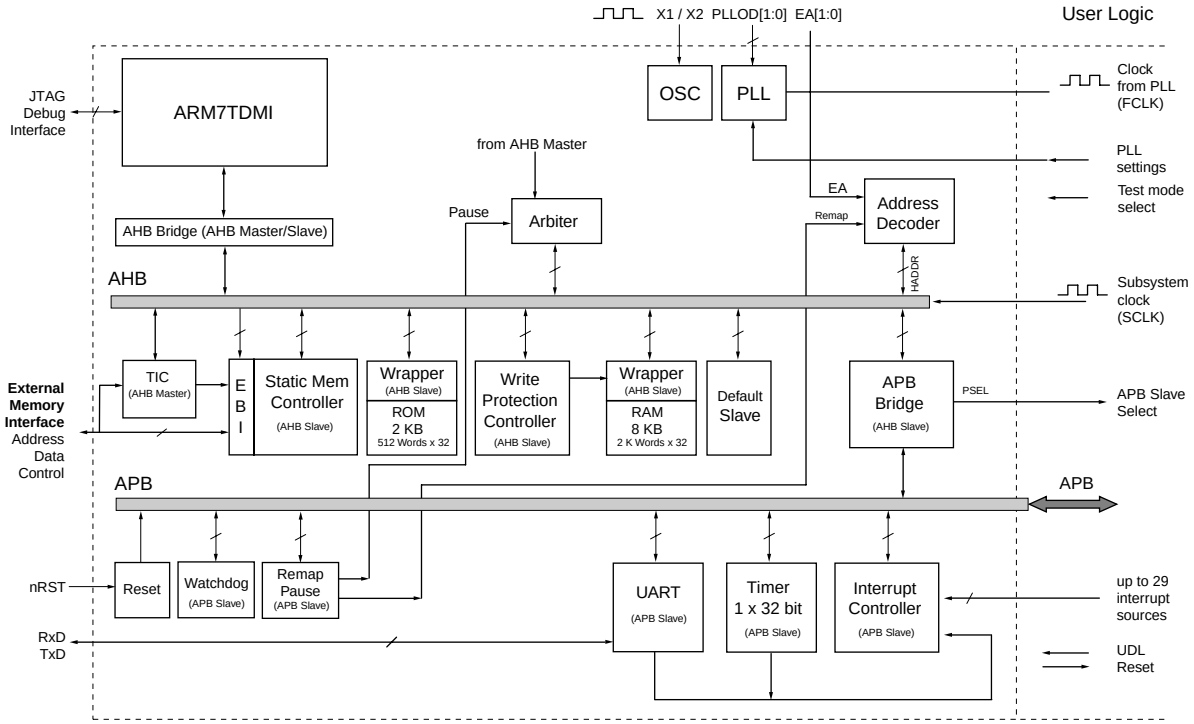
Data Published: July 2002

INTERNAL BLOCK DIAGRAM

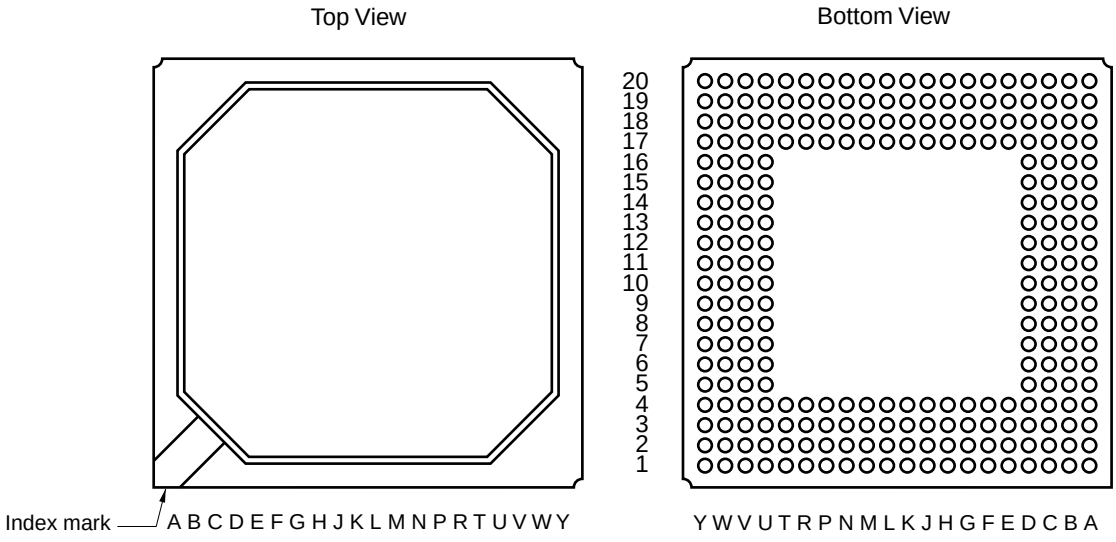


PIN IDENTIFICATION

XADDR0 to XADDR25	: Memory Address Bus	AV_{DD}	: Analog Power Supply for PLL
XDATA0 to XDATA31	: Memory Data Bus	DV_{DD}	: Digital Power Supply for PLL
nXCS0 to nXCS7	: Memory Chip (Bank) Select	AV_{SS}	: Analog Ground for PLL
nXBLS0 to nXBLS3	: Memory Byte Lane Select	DV_{SS}	: Digital Ground for PLL
nXOE	: Memory Output Enable	V_{DD0} to V_{DD11}	: Power Supply
nXWEN	: Memory Read / Write	V_{SS0} to V_{SS12}	: Ground Power Supply
nXWAIT	: Memory Wait	IC1	: Internal connection
RXD	: Receive Data Input	TEST	: Internal connection
TXD	: Transmit Data Output		
X1	: Crystal		
X2	: Crystal		
nRST	: Reset		
EA0	: Enable signal for external or internal boot memory		
EA1	: Enable signal for external or internal boot memory		
DBGEN	: Debug enable		
PLLOD0	: Frequency range of PLL output		
PLLOD1	: Frequency range of PLL output		
JTAG_TDI	: JTAG data in		
JTAG_TDO	: JTAG data out		
JTAG_TCK	: JTAG clock		
JTAG_TMS	: JTAG mode select		
JTAG_TRST	: JTAG reset		
TCLK	: Clock for test purposes		

PIN CONFIGURATION

- 256-Pin Plastic BGA (27 mm × 27 mm)



(1/3)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A1	V_{SS0}	D5	nXCS5	L1		U17	V_{SS7}
A2	XDATA31	D6	V_{DD11}	L2		U18	
A3	XDATA29	D7	nXCS0	L3		U19	
A4	XDATA27	D8	V_{SS12}	L4		U20	
A5	nXCS2	D9	XADDR22	L17	V_{DD7}	V1	
A6	XDATA25	D10	XADDR20	L18	IC1**Note1**	V2	
A7	XDATA24	D11	V_{DD10}	L19	nXBLS1	V3	
A8	XDATA22	D12	XADDR16	L20	nXBLS0	V4	
A9	XDATA20	D13	V_{SS11}	M1		V5	
A10	XDATA18	D14	PLLOD0	M2		V6	
A11	XDATA17	D15	V_{DD9}	M3		V7	
A12	XDATA15	D16	IC1**Note1**	M4		V8	
A13	XDATA14	D17	V_{SS10}	M17	JTAG_TDO	V9	
A14	XDATA13	D18	XADDR10	M18	JTAG_TDI	V10	
A15	XDATA12	D19	XADDR9	M19	TXD	V11	
A16	IC1**Note1**	D20	XDATA8	M20	RXD	V12	

(2/3)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A17	AV_{SS}	E1		N1		V13	
A18	DV_{DD}	E2		N2		V14	
A19	X1	E3		N3		V15	
A20	nRST	E4		N4	V_{SS3}	V16	
B1		E17	XADDR8	N17	V_{SS8}	V17	
B2	TCLK	E18	XADDR7	N18	JTAG_TRST	V18	
B3	XDATA30	E19	XDATA7	N19	JTAG_TMS	V19	
B4	XDATA28	E20	XDATA6	N20	JTAG_TCK	V20	
B5	nXCS3	F1		P1		W1	
B6	XDATA26	F2		P2		W2	
B7	XADDR24	F3		P3		W3	
B8	XDATA23	F4	V_{DD0}	P4		W4	
B9	XDATA21	F17	V_{DD8}	P17		W5	
B10	XDATA19	F18	XADDR6	P18		W6	
B11	XADDR17	F19	XADDR5	P19		W7	
B12	XDATA16	F20	XDATA5	P20		W8	
B13	XADDR13	G1		R1		W9	
B14	XADDR11	G2		R2		W10	
B15	PLLOD1	G3		R3		W11	
B16	DV_{SS}	G4		R4	V_{DD2}	W12	
B17	EA1	G17	XADDR4	R17	V_{DD6}	W13	
B18	X2	G18	XADDR3	R18		W14	
B19	TEST**Note2**	G19	XDATA4	R19		W15	
B20	XDATA11	G20	XDATA3	R20		W16	
C1		H1		T1		W17	
C2		H2		T2		W18	
C3	nXCS7	H3		T3		W19	
C4	nXCS6	H4	V_{SS2}	T4		W20	
C5	nXCS4	H17	V_{SS9}	T17		Y1	
C6	nXCS1	H18	XADDR2	T18		Y2	
C7	XADDR25	H19	XDATA2	T19		Y3	
C8	XADDR23	H20	XDATA1	T20		Y4	
C9	XADDR21	J1		U1		Y5	

(3/3)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
C10	XADDR19	J2		U2		Y6	
C11	XADDR18	J3		U3		Y7	
C12	XADDR15	J4		U4	V_{SS4}	Y8	
C13	XADDR14	J17	XADDR1	U5		Y9	
C14	XADDR12	J18	XADDR0	U6	V_{DD3}	Y10	
C15	IC1[Note1]	J19	XDATA0	U7		Y11	
C16	AV_{DD}	J20	nXWAIT	U8	V_{SS5}	Y12	
C17	EA0	K1		U9		Y13	
C18	DBGEN	K2		U10	V_{DD4}	Y14	
C19	XDATA10	K3		U11		Y15	
C20	XDATA9	K4	V_{DD1}	U12		Y16	
D1		K17	nXOE	U13	V_{SS6}	Y17	
D2		K18	nXWEN	U14		Y18	
D3		K19	nXBLS3	U15	V_{DD5}	Y19	
D4	V_{SS1}	K20	nXBLS2	U16		Y20	

Notes: 1. Not connected, leave pin open.

2. For internal use only, must be pulled low always.

Remark: All free pins are available for UDL.

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1. PIN FUNCTIONS

1.1 List of Pin Functions

(1) External Pins

Table 1-1: External Pins (1/2)

Pin Name	I/O	Function	Interface
nXOE	Output	Data output enable	External Bus Interface
nXWEN	Output	Write enable signal output	
nXWAIT	Input	Control signal input to insert wait in bus cycle	
nXBLS0	Output	Byte lane select signal output	
nXBLS1			
nXBLS2			
nXBLS3			
nXCS0	Output	Chip select signal output	
nXCS1			
nXCS2			
nXCS3			
nXCS4			
nXCS5			
nXCS6			
nXCS7			
XADDR0 to XADDR25	Output	26-bit address bus for external memory	
XDATA0 to XDATA31	I/O	32-bit data bus for external memory	
RXD	Input	Serial receive data input	Serial Interface
TXD	Output	Serial transmit data output	
X1	Input	Connects the crystal resonator for system clock oscillation. In the case of an external source supplying the clock, it is input to X2 (direct clock input).	Oscillator Interface
X2	-		
TCLK**Note 1**	Input	Clock input for test purpose	System Configuration Interface
nRST	Input	System reset input	
EA0**Note 4**	Input	Enable external boot memory	
EA1**Note 4**	Input		
DBGEN**Note 4**	Input	Debug enable input	
PLLOD0**Note 4**	Input	Frequency of PLL output clock (FCLK)	
PLLOD1**Note 4**	Input		
IC1**Note 2**	-	Internal connected	
TEST**Note 3**	-	Internal connection	

Table 1-1: External Pins (2/2)

Pin Name	I/O	Function	Interface
AV_{DD}	Input	Positive analog power supply for PLL	Power Supply Interface
DV_{DD}	Input	Positive digital power supply for PLL	
AV_{SS}	Input	Analog ground potential for PLL	
DV_{SS}	Input	Digital ground potential for PLL	
V_{DD0} to V_{DD11}	Input	Positive power supply	
V_{SS0} to V_{SS12}	Input	Ground potential	
JTAG_TDI	Input	Data in for debugging or boundary scan	Debug and Boundary Scan Interface
JTAG_TDO	Output	Data out for debugging or boundary scan	
JTAG_TCK	Input	Clock input for debugging or boundary scan	
JTAG_TMS	Input	Mode select input for debugging or boundary scan	
JTAG_TRST	Input	Reset input for debugging or boundary scan	

Notes: 1. Must be kept low in normal operating mode.

2. Not connected, leave pin open.

3. Must be pulled low always.

4. Must be kept unchanged during operation.

(2) Internal Pins between ARM subsystem and UDL

Table 1-2: Internal Pins between ARM subsystem and UDL

Pin Name	Direction	Function	Interface
PRESETn	to UDL	APB bus reset signal	APB Bus Interface
PSELUDL	to UDL	APB bus slave select signal	
PENABLE	to UDL	APB bus strobe signal	
PWRITE	to UDL	APB bus write signal	
PADDR0 to PADDR28	to UDL	APB address bus	
PRDATA0 to PRDATA31	from UDL	APB read data bus	
PWDATA0 to PWDATA31	to UDL	APB write data bus	
FCLK	to UDL	PLL output frequency	Clock Interface
SCLK	from UDL	Clock for ARM subsystem	
INT0 to INT28	from UDL	Interrupt lines to interrupt controller	Interrupt/Exception Interface
nRESUDL	from UDL	Reset signal from UDL to reset controller	
nFIRQ	from UDL	FIQ signal directly routed to ARM CPU	
PLL_M0 to PLL_M4	from UDL	M value for M-counter of PLL	PLL Configuration Interface
PLL_N0 to PLL_N6	from UDL	N value for N-counter of PLL	
PLL_S0 to PLL_S1	from UDL	VCO frequency range selection	
TARMSS	from UDL	Set ARM subsystem into test mode	
BS_TCK	to UDL	Boundary scan signals for UDL	Boundary Scan Interface
BS_TMS			
BS_TRST			

1.2 Types of Pin I/O Circuit and Recommended Connection of Pins

Table 1-3: Types of Pin I/O Circuit and Recommended Connection of Pins (1/2)

Pin	I/O Buffer Type[Note]	Recommended Connection
nXOE	BV08	Output: Leave open (if unused)
nXWEN		
nXWAIT	FIV1	Input: Connect to V_{DD} via a resistor (if unused)
nXBLS0	BV08	Output: Leave open (if unused)
nXBLS1		
nXBLS2	BW03	Output: Leave open (if unused)
nXBLS3		
nXCS0	BV08	Output: Leave open (if unused)
nXCS1		
nXCS2		
nXCS3		
nXCS4		
nXCS5		
nXCS6		
nXCS7		
XADDR0 to XADDR25		
XDATA0 to XDATA31	BW03	Input: Connect to V_{DD} or V_{SS} via a resistor (if unused) Output: Leave open (if unused)
RXD	FIV1	Input: Connect to V_{DD} or V_{SS} via a resistor (if unused)
TXD	BV08	Output: Leave open (if unused)
X1	OSI1 / OSO1	Connect to V_{SS} (when external clock is input to X2 pin)
X2		
TCLK	FIV1	Must be kept low in normal operation mode
nRST	FIF1	Schmitt-Trigger input
EA0	FIV1	Must be set to an appropriate value to guarantee correct operation
EA1		
DBGEN	FDV1	internal pull-down (50K)
PLLOD0	FIV1	Must be set to an appropriate value to guarantee correct operation
PLLOD1		
JTAG_TDI		Connect to V_{DD} (pull-up)
JTAG_TDO	BV08	
JTAG_TCK	FIV1	Connect to V_{DD} (pull-up)
JTAG_TMS		
JTAG_TRST		
AV_{DD}	-	Default power supply (analog) for PLL
DV_{DD}	-	Default power supply (digital) for PLL
AV_{SS}	-	Default ground (analog) for PLL

Table 1-3: Types of Pin I/O Circuit and Recommended Connection of Pins (2/2)

Pin	I/O Buffer Type[Note]	Recommended Connection
DV_{SS}	-	Default ground (digital) for PLL
V_{DD0} to V_{DD11}	-	Default power supply
V_{SS0} to V_{SS12}	-	Default ground

Note: For buffer type information, please refer to document “Block Library CMOS-9HD Family, EA-9HD Family” (Document No. A13052EJ6V0BL00).

2. ELECTRICAL SPECIFICATIONS

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter		Symbol	Test Conditions	Ratings	Unit
Supply voltage		V_{DD}, DV_{DD}, AV_{DD}		-0.5 ~ +4.6	V
Input voltage	except X1	V_I	$V_I < V_{DD}$ + 3.0 V	-0.5 ~ +6.6	V
Output voltage	except X2	V_O	$V_O < V_{DD}$ + 3.0 V	-0.5 ~ +6.6	V
Output current	except X2	I_O		30	mA
Operating ambient temperature		T_A		-40 ~ +85	°C
Storage temperature		T_{STG}		-65 ~ +150	°C

Cautions: 1. Do not directly connect output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open drain pins or open collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

2.2 Operating Conditions

Table 2-2: Operating Conditions

Clock Input	Operating Ambient Temperature (T_A)	Supply Voltage (V_{DD})	Operation Clock Frequency
Oscillator Input (crystal frequency range)**Note 2**	-40 ~ +85°C	3.0 V ~ 3.6 V	4 MHz ≤ $f_{Crystal}$ ≤ 16 MHz
ARM Subsystem Input (SCLK frequency range)			f_{SCLK} ≤ 35 MHz**Note 1**

Notes: 1. ARM subsystem operating frequency, as derived from PLL output clock (FCLK).

2. Input frequency for oscillator at external pins X1 and X2 or external pin X2, if a direct clock source is used.

2.3 Oscillator Characteristics

(a) Crystal or Ceramic Resonator Connection

Figure 2-1: Crystal or Ceramic Resonator Connection

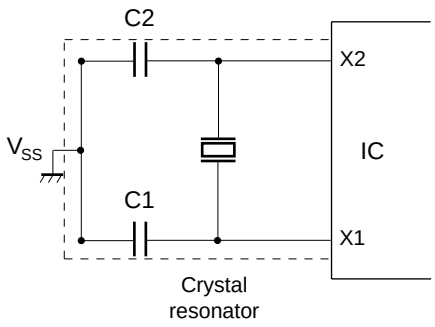


Table 2-3: Oscillator Characteristics (T_A = -40 to +85°C, V_{DD} = 3.3 V ± 0.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	fxx	V_{DD} = 3.0 V to 3.6 V	4		16	MHz
Oscillation stabilization time	t_{OST}			10		ms

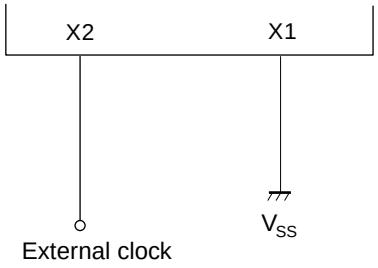
Note: The value of the oscillation stabilization time is just a typical value. It greatly depends on the application (external components, PCB layout).

Caution: Ensure that the duty cycle of oscillation waveform is between 45% and 55%.

Remark: PCB layout recommendations are listed in sub-chapter (c).

(b) External Clock Input

Figure 2-2: External Clock Input



The external clock shall be connected to the X2 output while clamping X1 to ground (V_{SS}).

Table 2-4: Oscillator Characteristics (T_A = -40 to +85°C, V_{DD} = 3.3 V ± 0.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fxx	V_{DD} = 3.0 V to 3.6 V	4		16	MHz

(c) PCB layout recommendations for crystal oscillator wiring

Since crystal oscillators are very EMI sensitive, it is strongly recommended to design the PCB board for the oscillator part very carefully according to the below listed recommendations.

The oscillator consists of an inverter inside SOClite ASIC that is connected to a quartz-crystal. The inverter is bridged by an internal feedback resistor. The inverter within SOClite ASIC has a high input impedance (X1 pin) and high output impedance (X2 pin). The output pin X2 has a low drive capability in order not to overdrive or damage the crystal. Internally, the oscillator signal is fed via a buffer chain to a 2:1 pre-scaler inside the PLL. The pre-scaler divides the oscillator input by two, which ensures a stable 50% duty cycle clock as PLL input signal.

In case of a poor PCB layout, noise injection into the on-chip oscillator may cause unintended noise spikes at the output of the internal oscillator buffer stage. The spiky signal will be divided by two and then further be filtered by the PLL characteristics. In case of an injected noise spike, a slowly decaying frequency disturbance at the PLL output would be observable.

The PCB layout recommendations for the oscillator part are as follows:

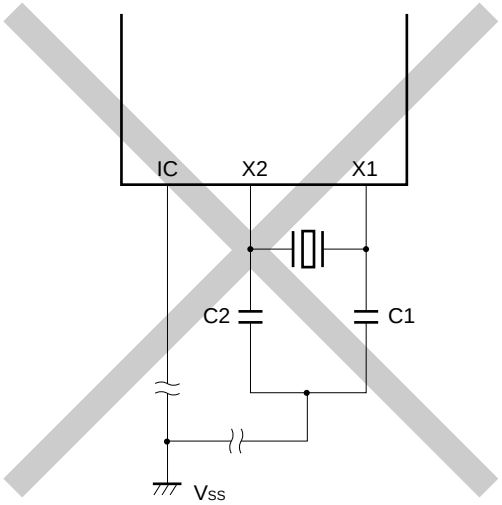
- **Ground path distance between the capacitors C1 and C2 and the ground pin V_{SS10} should be as short as possible.**
- **The oscillator must not share its ground trace with other signals (please refer to Figure 2-3 d).**
- **Place the crystal resonator and the capacitors C1 and C2 as close as possible to the X1 and X2 pins.**
- **Keep the wiring lengths as short as possible.**
- **Ensure that no other signals cross or/and accompany the crystal wiring (please refer to Figure 2-3 b/c).**
- **Enclose the oscillator circuitry with a ground guard ring as much as possible. Even a very thin guard ring due to PCB routing restrictions, is much better than having no guard ring at all.**
- **Apply an as complete as possible ground shielding to X1 and X2 oscillator signals. Shielding tracks on both sides of X1 and X2 oscillator signals must be connected to the ground plane at both ends and at least every 5 to 10 mm. Further, a local ground plane on the adjacent layers may be required.**
- **Keep any fast switching and/or high fluctuating current flows away from the oscillator lines.**
- **Do not fetch signals directly from the oscillator (please refer to Figure 2-3 e)**
- **Choose the capacitance C2 attached to X2 pin as big as possible. A value of at least 68 pF is strongly recommended. It may be necessary to use a dedicated crystal for achieving the target center oscillation frequency. Please contact your crystal vendor for that purpose for further details.**
- **As starting value, C1 should be chosen equal to C2. It must be ensured by appropriate measurements that the X1 input signal does not exceed the maximum ratings. The input level can be decreased, by increasing C1 appropriately.**
- **Do not insert a series resistor Rs in your final PCB-layout.**

NEC strongly recommends to prove the effectiveness of these measures after E/S silicon availability in an early stage of the project.

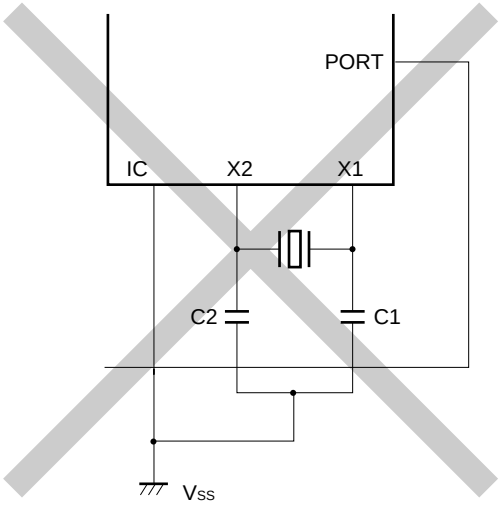
If your system is sensitive to sporadic frequency disturbances due to injected noise, we recommend to use an external crystal oscillator instead, that is hooked up to the X2 output pin, while X1 input clamped to GND (see Figure 2-2). Keep the wiring between external oscillator and X2 pin short.

Figure 2-3: Examples of Incorrect Resonator Connection (1/2)

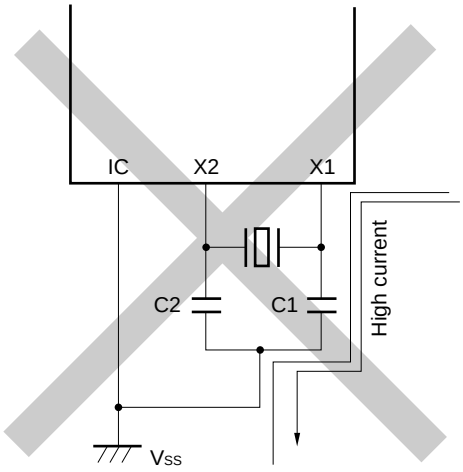
(a) Too long wiring



(b) Crossed signal line



(c) Wiring near high alternating current



(d) Current flowing through ground line of *oscillator (potential at points A, B and C fluctuates)*

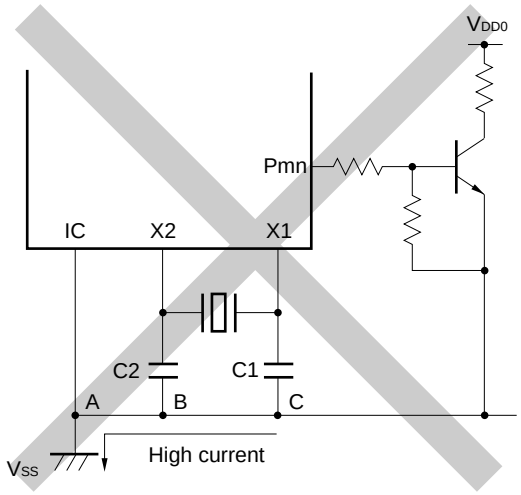
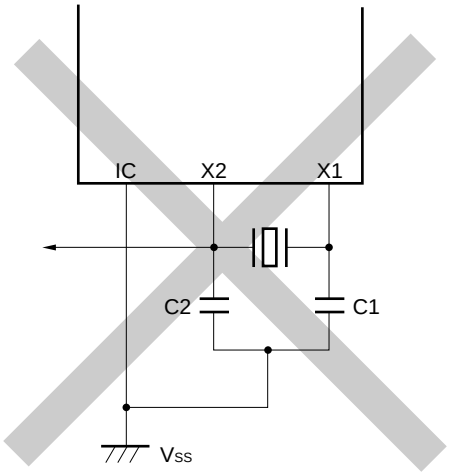


Figure 2-3: Examples of Incorrect Resonator Connection (2/2)

(d) Signals are fetched



2.4 PLL Characteristics

Table 2-5: PLL Recommended Operating Range (T_A = -40 to +85°C, AV_{DD} = 3.3 V ± 0.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	AV_{DD}		3.0	3.3	3.6	V
PLL input frequency	f_{STD}		4		160	MHz
Divided ratio	m	Multiplication rate = n / (m x p)	2		32	
	n		2		128	
	p		2		8	

Table 2-6: PLL Specification (T_A = -40 to +85°C, AV_{DD} = 3.3 V ± 0.3 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{ADD}				20	mA
VCO output frequency	f_{VCO}	frequency range set by parameters PLL_S[1:0]	50		230	MHz
PLL output clock	f_{FCLK}	set by parameters PLLOD[1:0]	6.25		115	MHz
PLL output ratio	duty	p = 2,4 or 8	45		55	%
Output period jitter	t_{pj}	peak to peak			0.4	ns
Output long term jitter	t_{lj}	peak to peak			2.0	ns
PLL lock time	tLock				1	ms

2.5 DC Characteristics

Table 2-7: DC Characteristics (T_A = -40 to +85°C; V_{DD}, DV_{DD}, AV_{DD} = 3.3 V ± 0.3 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	all except: nRST, X1	V_{IH}		2.0		5.5	V
Low-level input voltage	all except: nRST, X1	V_{IL}		0.0		0.8	V
High-level input voltage	X1	V_{IHX}		2.0		V_{DD}	V
Low-level input voltage	X1	V_{ILX}		0		0.8	V
Positive trigger voltage	nRST	V_P		1.4		2.4	V
Negative trigger voltage	nRST	V_N		0.8		1.6	V
Hysteresis voltage	nRST	V_H		0.3		1.5	V
Low-level output voltage		V_{OL}	I_{OL} = 0 mA			0.1	V
High-level output voltage		V_{OH}	I_{OH} = 0 mA	V_{DD} - 0.2			V
Static current consumption		I_{DDS}	$V_I = V_{DD}$ or GND		tbd	tbd	µA
OFF-state output current		I_{OZ}	$V_O = V_{DD}$ or GND			± 10	µA
Output short-circuit current **Note 1**		I_{OS}	V_O = GND			- 250	mA
Input leakage current	all except: TEST, DBGEN, X1	I_{LI1}	$V_I = V_{DD}$ or GND			± 1	µA
	TEST, DBGEN	I_{LI2}	$V_I = V_{DD}$	28	83	190	µA
Pull-down resistor (50 KΩ) **Note 2**	TEST, DBGEN	R_{PD}	$V_I = V_{DD}$	18.9	39.8	107.1	KΩ
Low-level output current		I_{OL}	V_{OL} = 0.4 V	9.0			mA
High-level output current		I_{OH}	V_{OH} = 2.4 V	- 3.0			mA

Notes: 1. The output short circuit time is 1 second or less per pin of SoCLite.

2. The pull-down resistance varies depending on the input and output voltage.

2.6 AC Characteristics

2.6.1 General

Table 2-8: Conditions for AC Characteristics

	UDL Signals	External Signals (Pins)
Ambient temperature	T_A = -40 to +85°C	
Operating voltage	V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V	
Input signal rise/fall time	ideal (= 0 ns)	
Output signal load capacitance	C_L = 1 pF	C_L = 50 pF

Figure 2-4: AC Test Input Measurement Points (external signals)

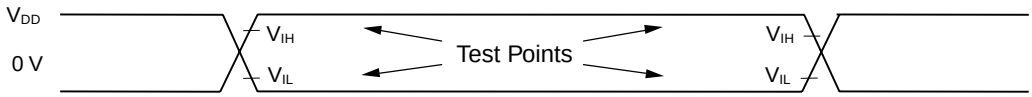


Figure 2-5: AC Test Output Measurement Points (external signals)

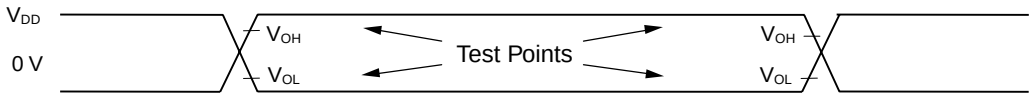
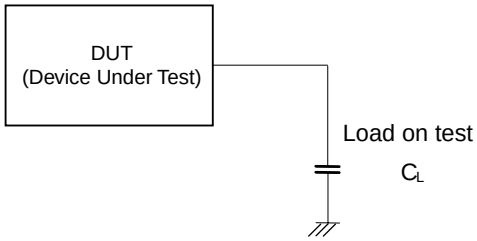


Figure 2-6: AC Test Load Condition



Caution: If the load capacitance of external signals (pins) exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

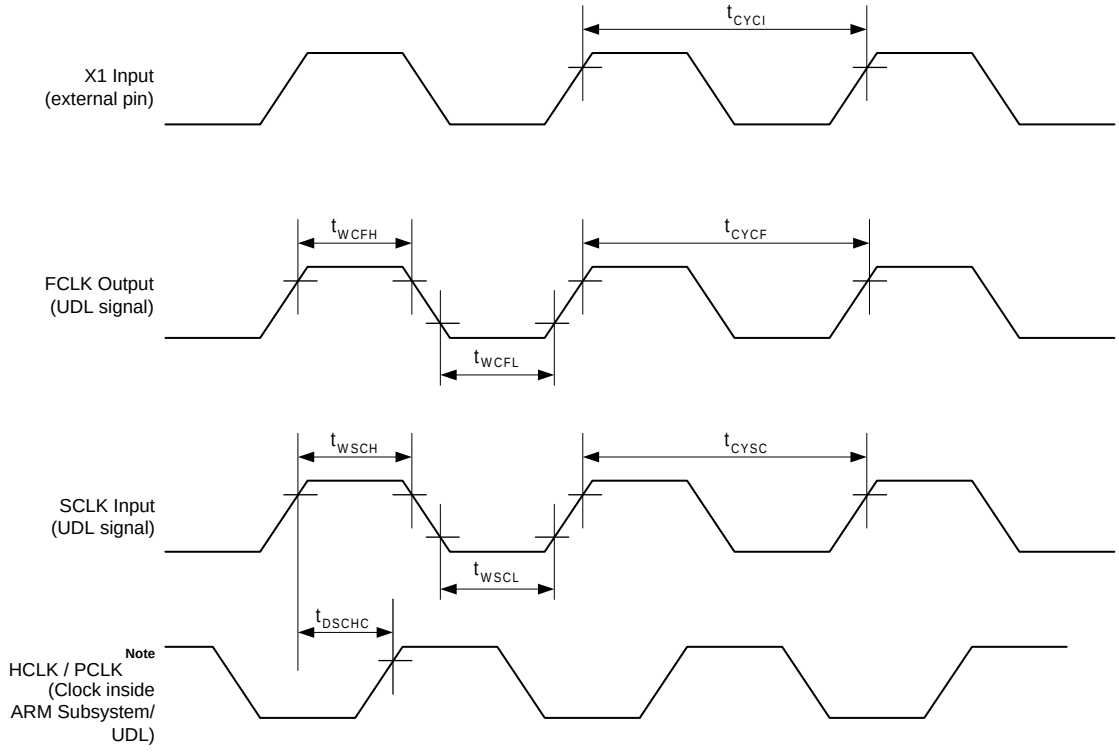
2.6.2 Clock Timing

Table 2-9: Clock AC Characteristics (T_A = -40 to +85°C, V_{DD} = 3.3 V ± 0.3 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
X1 input cycle	t_{CYCI}		62.5	250	ns
SCLK input cycle	t_{CYSC}		28.6		ns
SCLK input high-level width	t_{WSCH}		12.9		ns
SCLK input low-level width	t_{WSCL}		12.9		ns
SCLK to PCLK/HCLK delay **Note**	t_{DSCHC}		4.15	10.69	ns
FCLK output cycle	t_{CYCF}		8.7	160	ns
FCLK output high-level width	t_{WFIH}		3.9	88	ns
FCLK output low-level width	t_{WCFL}		3.9	88	ns

Note: For synchronous APB connection only.

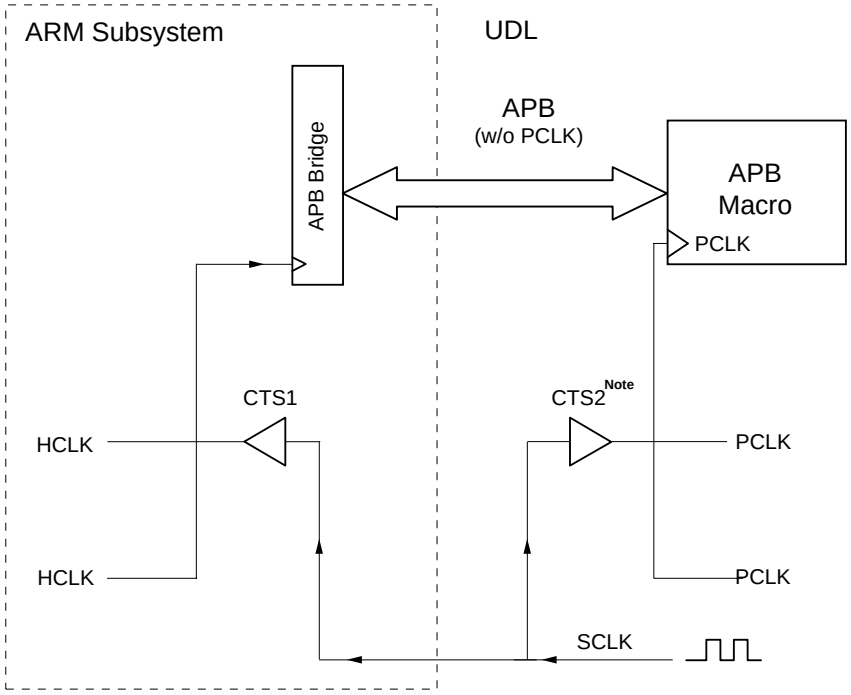
Figure 2-7: Clock Waveforms



Note: For synchronous APB connection only.

2.6.3 APB Bus Timing

Figure 2-8: Clock Structure



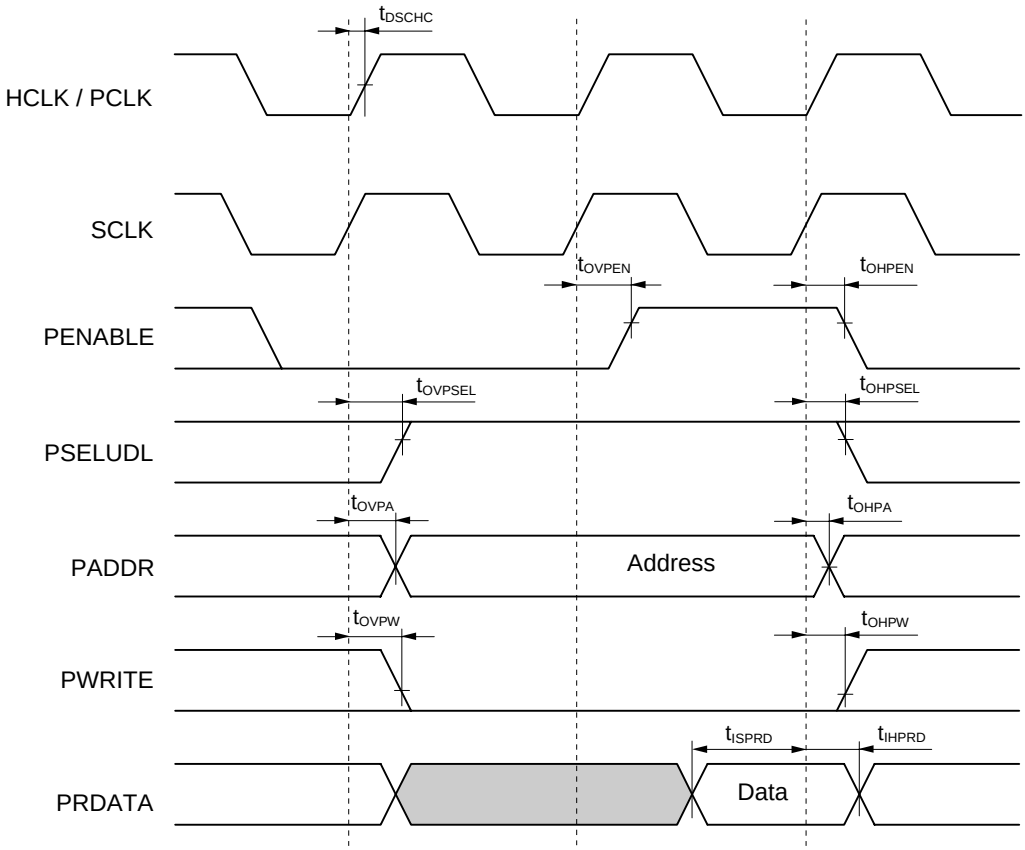
Note: For synchronous operation of APB bus, adjust CTS2 (SCLK to PCLK delay) to CTS1 (SCLK to HCLK delay).

Table 2-10: APB Bus AC Characteristics (T_A = -40 to +85°C, V_{DD} = 3.3 V ± 0.3 V)

Parameter	Symbol	related to HCLK/PCLK		related to SCLK		Unit
		MIN.	MAX.	MIN.	MAX.	
PENABLE valid after rising clock	t_{OVPEN}		2.9		13.5	ns
PENABLE hold after rising clock	t_{OHPEN}	0.9		5.1		ns
PSELUDL valid after rising clock	t_{OVPSEL}		2.7		13.4	ns
PSELUDL hold after rising clock	t_{OHPSEL}	0.9		5.0		ns
PADDR valid after rising clock	t_{OVPA}		3.3		14.0	ns
PADDR hold after rising clock	t_{OHPA}	0.6		4.8		ns
PWRITE valid after rising clock	t_{OVPW}		2.9		13.6	ns
PWRITE hold after rising clock	t_{OHPW}	1.0		5.1		ns
PRDATA setup to rising clock	t_{ISPRD}	16.7		8.2		ns
PRDATA hold after rising clock	t_{IHPRD}	0		0		ns
PWDATA valid after rising clock	t_{OVPWD}		4.6		15.3	ns
PWDATA hold after rising clock	t_{OHPWD}	1.0		5.2		ns

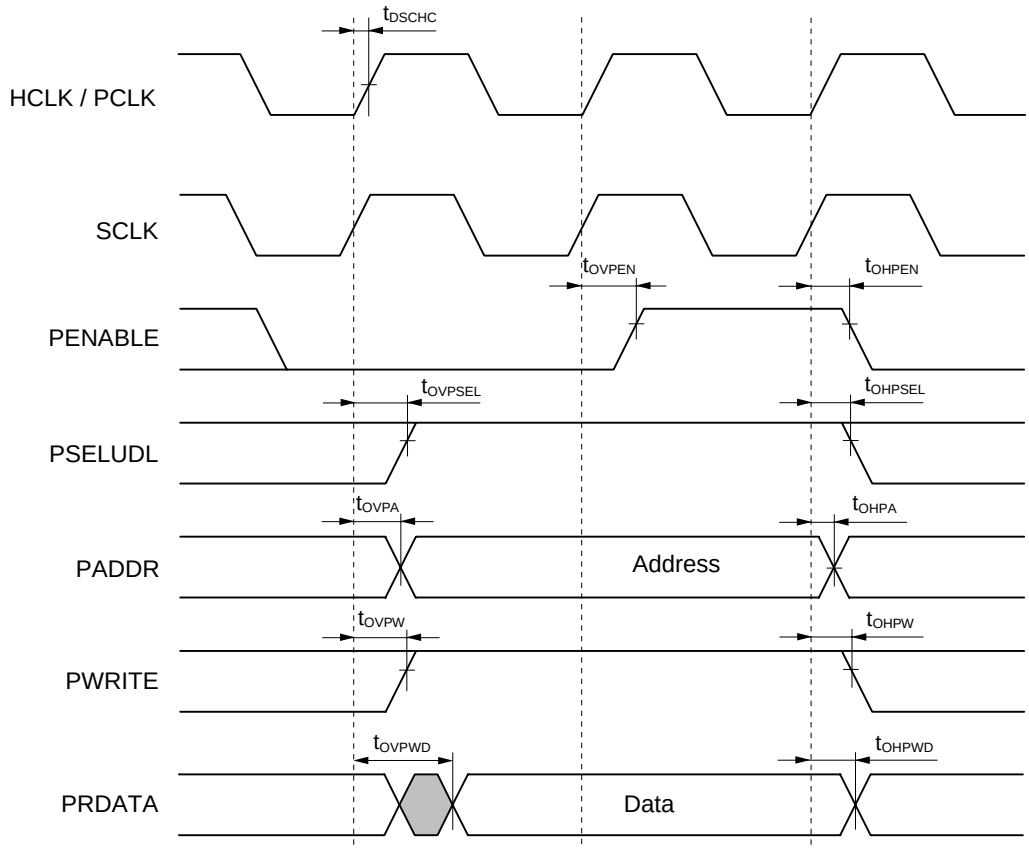
Remark: If the APB bus is connected synchronously to the ARM subsystem use the min. and max. values related to HCLK/PCLK, if it is connected asynchronously use the min. and max. values related to SCLK.

Figure 2-9: APB Read Cycle



Remark: If the APB bus is connected synchronously to the ARM subsystem use the min. and max. values related to HCLK/PCLK, if it is connected asynchronously use the min. and max. values related to SCLK.

Figure 2-10: APB Write Cycle



Remark: If the APB bus is connected synchronously to the ARM subsystem use the min. and max. values related to HCLK/PCLK, if it is connected asynchronously use the min. and max. values related to SCLK.

2.6.4 External Memory Bus Timing

Table 2-11: External Memory Bus AC Characteristics (T_A = -40 to +85°C, V_{DD} = 3.3 V ± 0.3 V) (1/2)

	Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Read	Address setup time before nXCS↓	t_{SACS}		T - 1.6		ns
	Delay time from nXCS↓ to nXOE↓	t_{DCSO}			5.9	ns
	nXCS low level width (single read)	t_{WCSL}		(WST1 + n + 3) T - 1.2		ns
	nXCS low level width (page mode) **Note 3**	t_{WPCSL}		(WST1 + 2)T + (3 WST2 + 7)T - 1.2		ns
	Data input valid after nXOE↓ (single read)	t_{VOID}			(WST1 + n + 2)T - 22.8	ns
	Data input valid after nXOE↓ (page mode) **Note 3**	t_{VPOID}			(WST1 + 2)T - 22.8	ns
	Data input valid after address (inside page) **Note 3**	t_{VPAID}			(WST2 + 1)T - 18.6	ns
	Data input hold time (from nXCS↑)	t_{HCID}		0		ns
	Delay time from nXCS↑ to nXOE↑	t_{DCOE}			6.2	ns
	Data input valid after address (sequential read)	t_{VSAID}			(WST1 + n + 2)T - 18.6	ns
Wait	nXWAIT valid after chip select (read)	t_{VRCWT}			(WST1 - 1)T - 13.0	ns
	nXWAIT hold time (from chip select)	t_{HCWT}		n x T		ns
	nXWAIT valid after chip select (write)	t_{VWCWT}			(WST2 - 2)T - 13.0	ns
Write	Delay time from nXCS↓ to nXWEN↓ / nXBLS↓	t_{DCSW}			7.5	ns
	nXWEN / nXBLS low level width	t_{WWEL}		(WST2 + n + 1)T - 0.7		ns
	Delay time from nXWEN↑ / nXBLS↑ to nXCS↑ **Note 1**	t_{DWCS}		T - 7.3		ns
	Delay time from nXCS↓ to data output	t_{DCDO}			5.7	ns
	Data output hold time (from nXWEN↑ / nXBLS↑) **Note 1**	t_{HWED}		T - 9.6		ns
	nXCS low level width **Note 2**	t_{WWCSL}		(WST2 + n + 1)T - 1.2		ns
	Delay time from nXCS↑ to nXWEN↑ / nXBLS↑ **Note 2**	t_{DCWE}		1.6		ns
	Data output hold time (from nXCS↑) **Note 2**	t_{HCSD}		2T - 4.0		ns
	Delay time from nXWEN↓ / nXBLS↓ to next nXWEN↓ / nXBLS↓	t_{DSWE}		(WST2 + n + 3)T		ns
	Address hold time (from nXWEN↑ / nXBLS↑) **Note 1**	t_{HWAD}		T - 8.6		ns

Table 2-11: External Memory Bus AC Characteristics (T_A = -40 to +85°C, V_{DD} = 3.3 V ± 0.3 V) (2/2)

	Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Write	Address hold time (from nXCS↑)**Note 2**	t_{HCAD}		T - 5.2		ns
Turn Around	nXCS high level width (turn around inside the same memory bank)	t_{WCSH1}		(IDCY + 1)T - 1.2		ns
	nXCS high level width (turn around to a different memory bank)	t_{WCSH2}		(IDCY + 1)T - 4.1		ns

Notes: 1. Write access inside the same memory bank.

2. Consecutive write access to a different memory bank.

3. It is assumed that nXWAIT input is kept HIGH during page mode. Therefore n is not considered in the equation.

Remarks: 1. T : Clock period of SCLK.

2. WST1 : Content of WST1 inside the appropriate SMCBCRx register, (WST1 shall be greater than value 2).

3. WST2 : Content of WST2 inside the appropriate SMCBCRx register, (WST2 shall be greater than value 3).

4. n : Number of wait states inserted into the bus cycle by nXWAIT input.

Figure 2-11: External Memory Bus Single Read Cycle

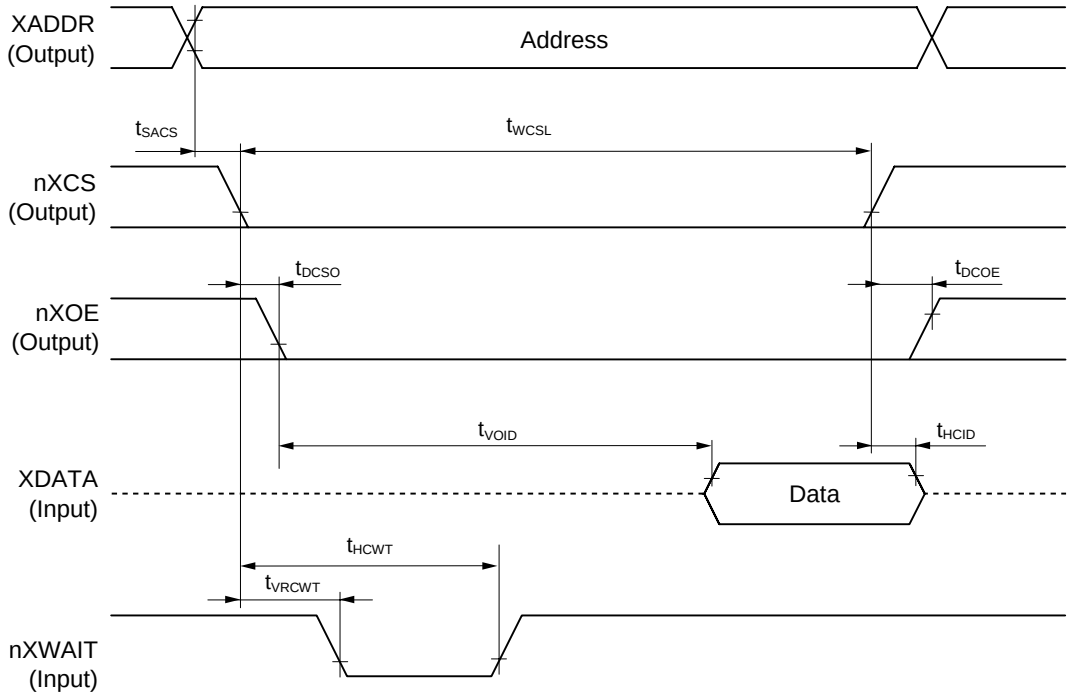


Figure 2-12: External Memory Bus Sequential Read Cycle

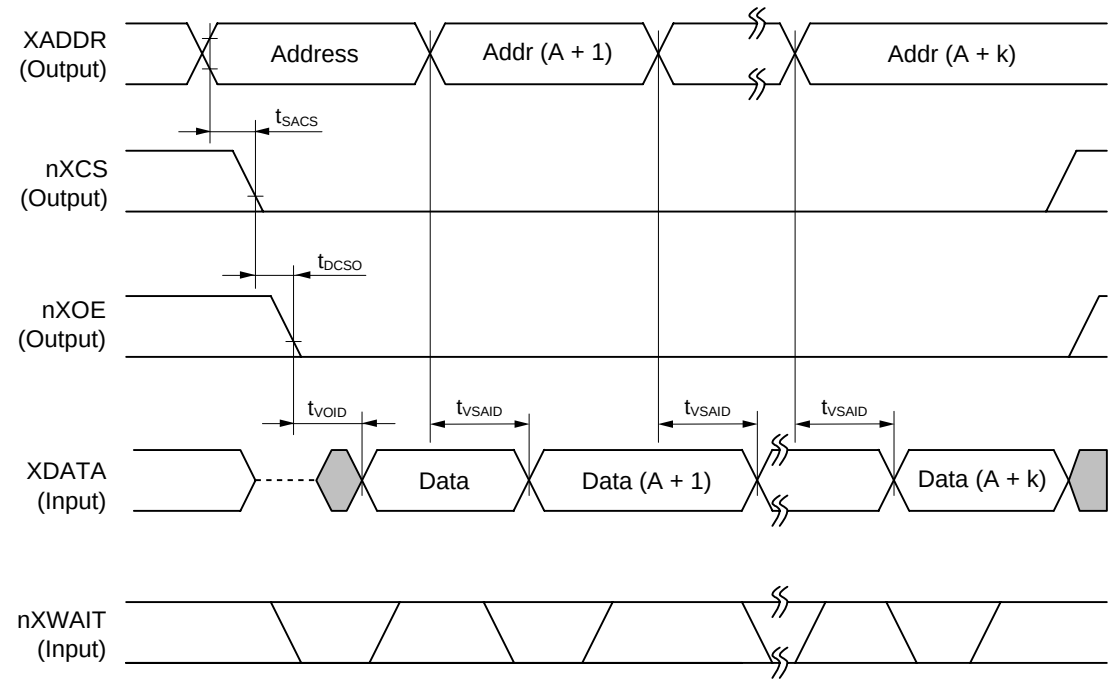


Figure 2-13: External Memory Bus Page Mode Read Cycle (32-bit wide)

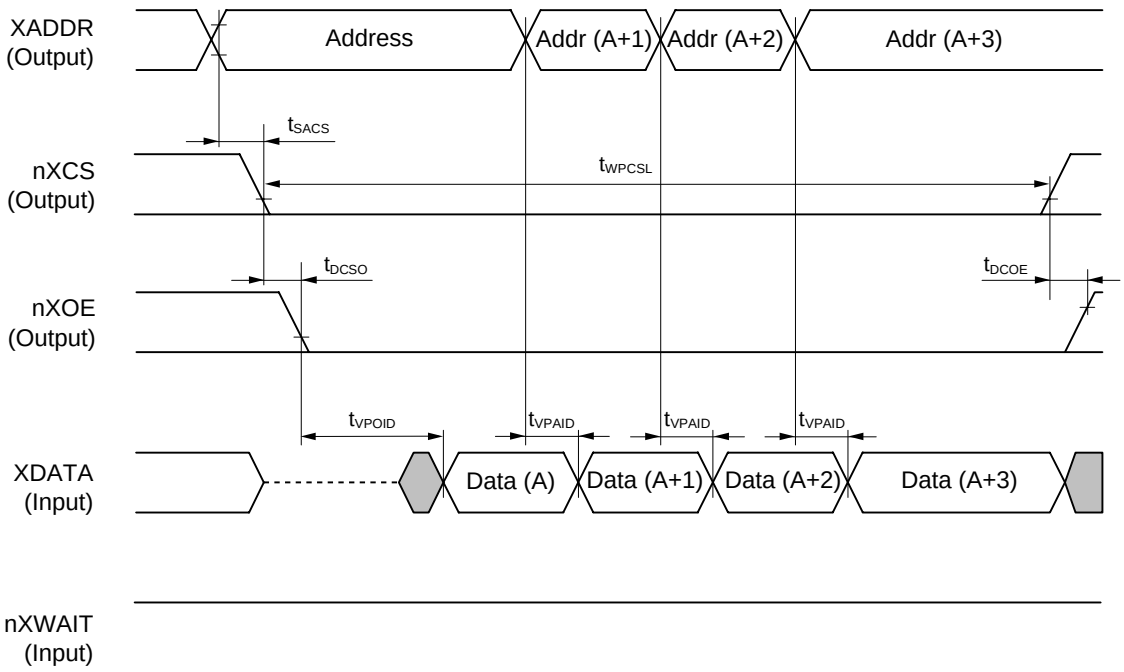


Figure 2-14: External Memory Bus Single Write Cycle

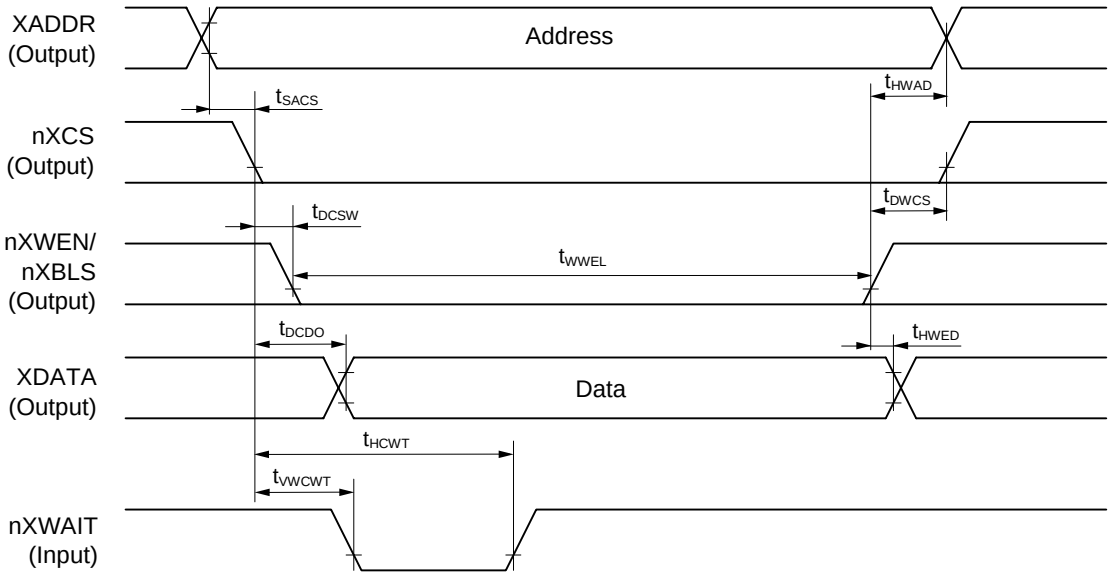


Figure 2-15: External Memory Bus Single Write Cycle to different Memory Banks

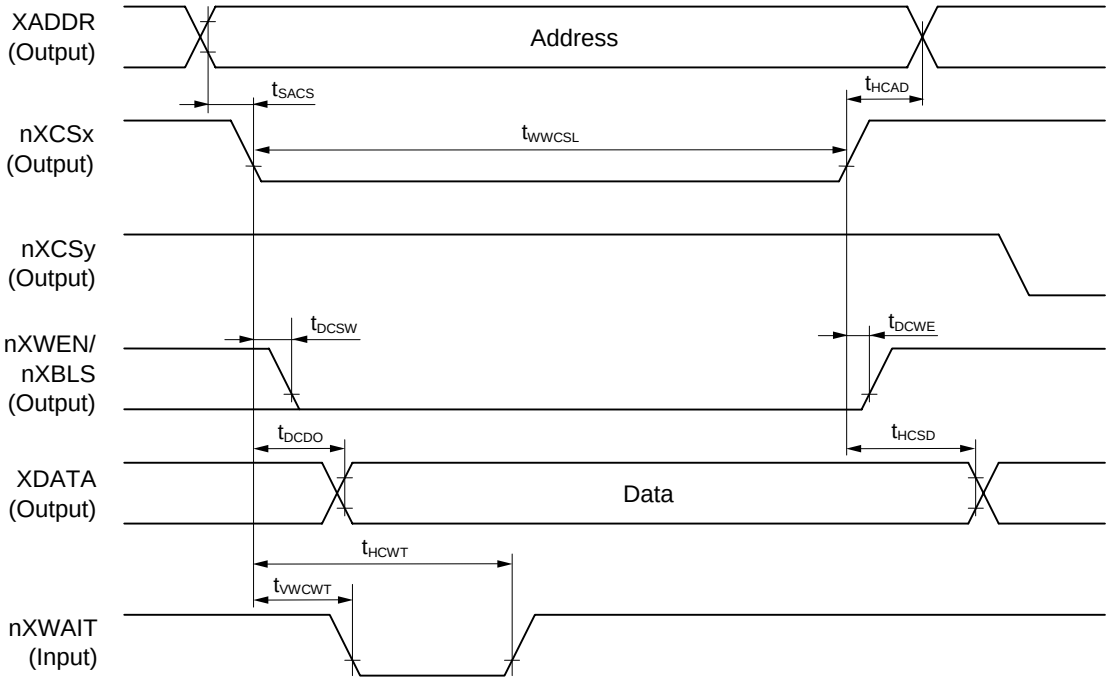


Figure 2-16: External Memory Bus Sequential Write Cycle

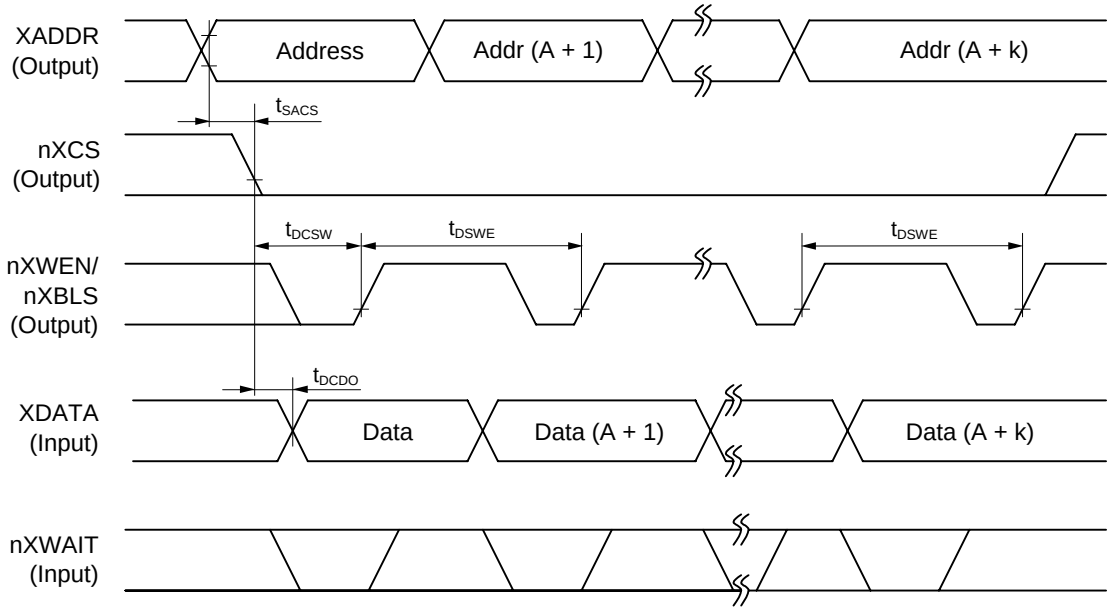
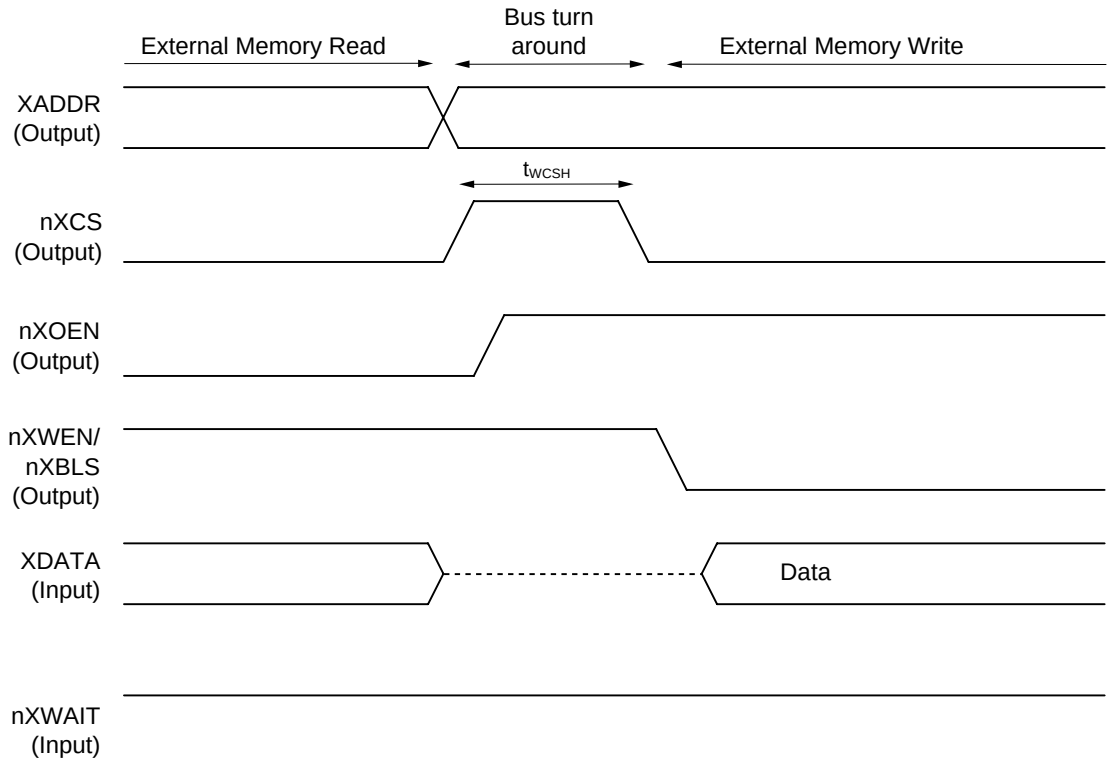


Figure 2-17: External Memory Bus Turn Around Cycle



2.6.5 Reset Timing

Table 2-12: Reset AC Characteristics (T_A = -40 to +85°C, V_{DD} = 3.3 V ± 0.3 V)

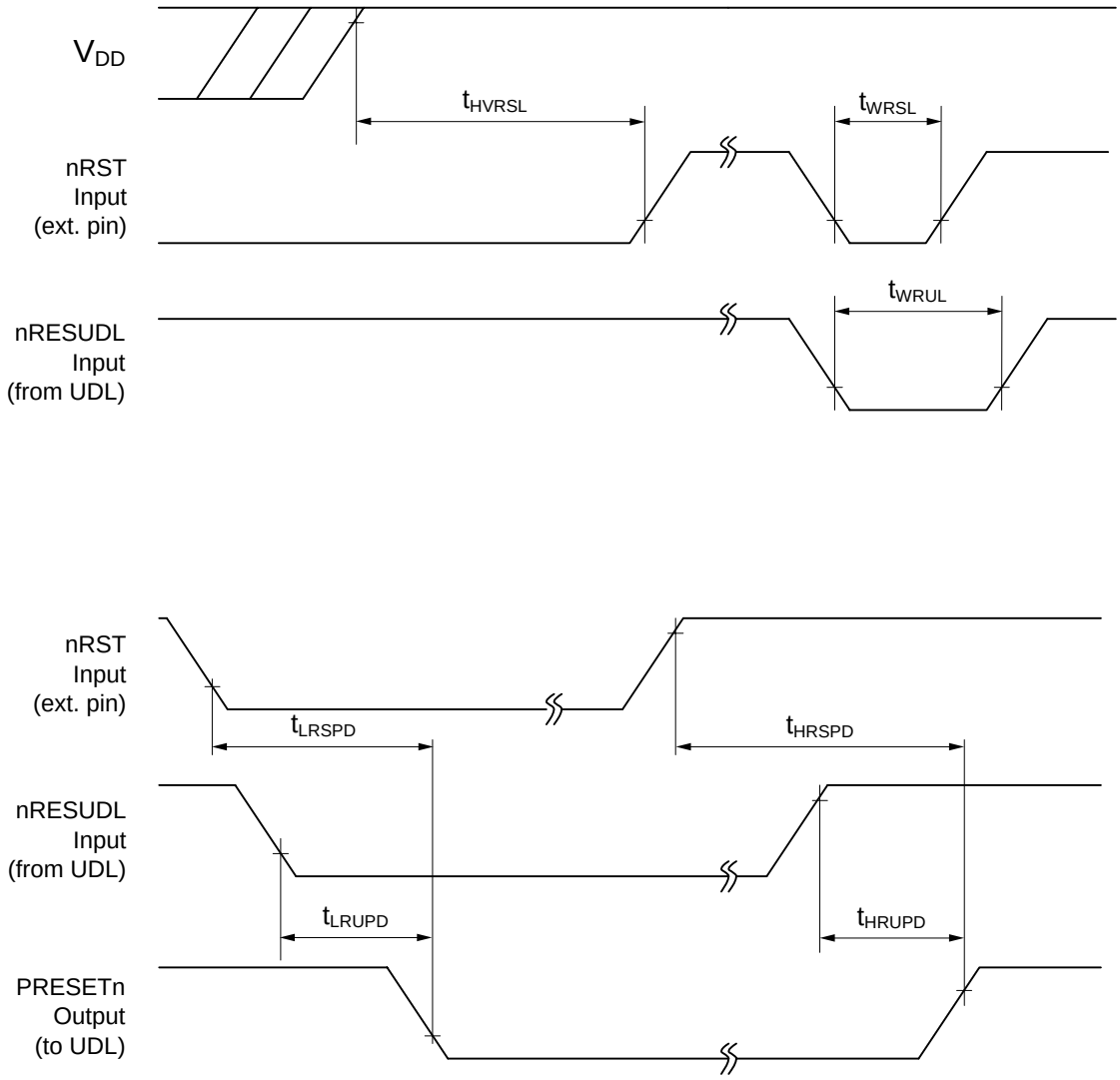
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
nRST low-level width	t_{WRSL}		2 T_{OSC} + 70		ns
nRESUDL low-level width	t_{WRUL}		2 T_{SCLK}		ns
nRST hold time from V_{DD}	t_{HVRSL}		2 T_{OST} + 1		µs
PRESETn delay from nRST falling edge	t_{LRSPD}			2 T_{OSC} + 70	ns
PRESETn delay from nRST rising edge	t_{HRSPD}			2^{14} x T_{OSC}	ns
PRESETn delay from nRESUDL falling edge	t_{LRUPD}			4 T_{SCLK}	ns
PRESETn delay from nRESUDL rising edge	t_{HRUPD}			7 T_{SCLK}	ns

Remarks: 1. T_{SCLK} : Clock period of SCLK.

2. T_{OSC} : Clock period of oscillator.

3. T_{OST} : Oscillation stabilization time.

Figure 2-18: Reset Cycle



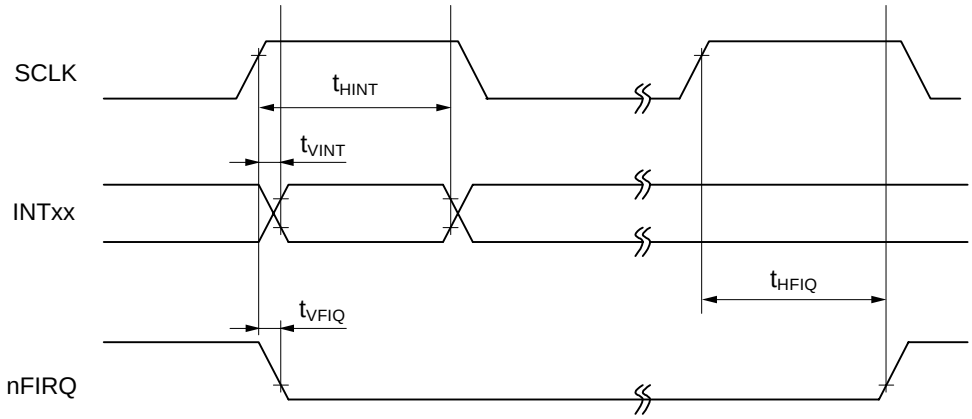
2.6.6 Interrupt Timing

Table 2-13: Interrupt AC Characteristics (T_A = -40 to +85°C, V_{DD} = 3.3 V ± 0.3 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
INTxx input valid after rising edge of SCLK	t_{VINT}			2.5	ns
INTxx input hold time	t_{HINT}		10.4		ns
nFIRQ input valid after rising edge of SCLK	t_{VFIQ}			3.1	ns
nFIRQ input hold time	t_{HFIQ}		9.0		ns

Remark: The min. and max. values are related to SCLK.

Figure 2-19: Interrupt Cycle

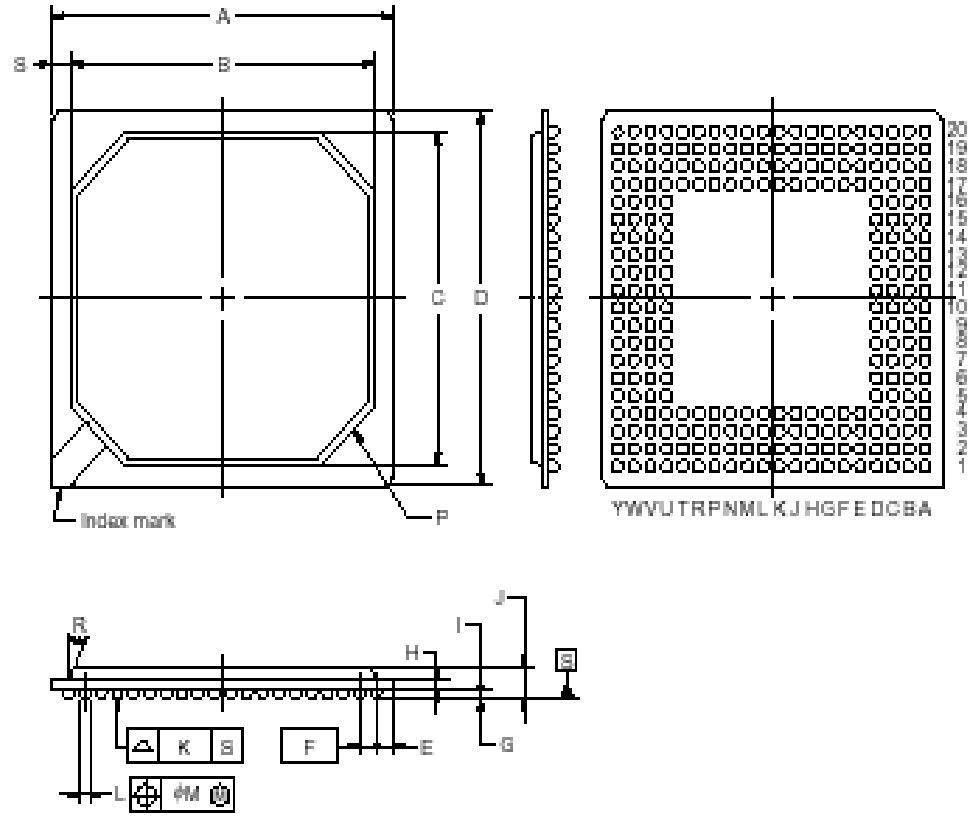


nFIRQ should be active until exception handler is executed

3. PACKAGE DRAWING

Figure 3-1: Package Drawing

256-PIN PLASTIC BGA (27x27)



NOTE

Each ball centerline is located within φ0.3 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	27.0±0.2
B	24.0
C	24.0
D	27.0±0.2
E	1.48
F	1.27 (T.P.)
G	0.6±0.1
H	0.36
I	1.53±0.15
J	2.13±0.25
K	0.15
L	φ0.75±0.15
M	0.3
P	C3.95
R	30°
S	1.5

S25651-137-BG-2

4. RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions.
For details of the recommended soldering conditions, refer to information document **Semiconductor Device Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended, consult NEC.

Table 4-1: Soldering Conditions

Soldering Method	Soldering Condition	Symbol Code of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 230°C Time of temperature higher than 210°C: 30 seconds max. Number of reflows: 3 max. Number of storage days after opening of dry pack: 3 **Note**	IR30-203-3
VPS	Package peak temperature: 215°C Time of temperature higher than 200°C: 40 seconds max. Number of reflows: 3 max. Number of storage days after opening of dry pack: 3 **Note**	VP15-203-3

Note: The number of days refers to storage at 25°C, 65% RH MAX after the dry pack has been opened. After that, prebaking is necessary at 125°C for 20 hours (min.), 72 hours (max.).

Caution: Do not use two or more soldering methods in combination (except partial heating method).

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
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