

6-Channel Power Sequencer with PG and Fault Monitoring

General Description

Overview

Renesas SLG7SQ50562-E is a low power and small form device. The mixed-signal IC is housed in a 4mm x 4mm STQFN package which is optimal for using with small devices.

This device can be further customized to meet your specific application requirements. Custom designs can be created using the free GUI-based Go Configure™ Software Hub, available for download at [renesas.com](https://www.renesas.com), where example projects are also included. Contact your local Renesas representative or email greenpak@renesas.com for support.

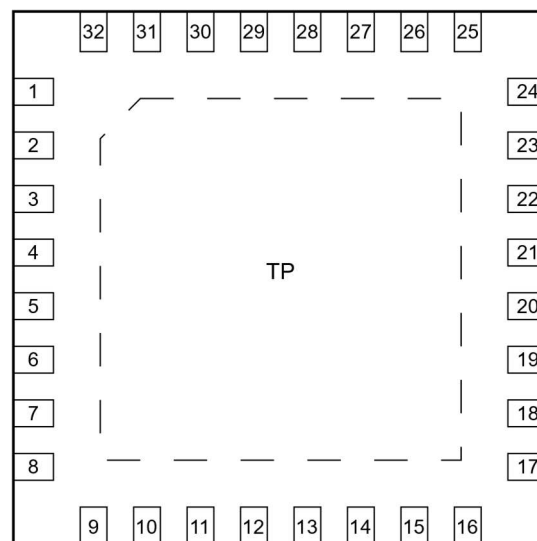
Features

- Low Power Consumption
- RoHS Compliant / Halogen-Free
- 32-pin STQFN: 4.0 mm x 4.0 mm x 0.55 mm, 0.4 mm pitch

Output Summary

7 Outputs - Push Pull 1X

Pin Configuration



STQFN-32
(Top View)

Pin Name

Pin #	Pin name	Pin #	Pin name
1	Group2_EN	17	Group6_EN
2	VIN_PG	18	OVERT*
3	NC	19	NC
4	PG/Group1	20	NC
5	PG/Group3	21	PG/Group4
6	PG/Group5	22	NC
7	SDA	23	NC
8	SCL	24	NC
9	NC	25	NC
10	PG/Group2	26	AVCC1
11	System_PWR_EN	27	NC
12	Group3_EN	28	AVCC2
13	Group4_EN	29	SYS_PWR_GD
14	GND2	30	GND
15	VDD2	31	VDD
16	Group5_EN	32	Group1_EN

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Pin Configuration

Pin	Pin Name	Type	Pin Description	Internal Resistors
1	Group2_EN	Digital Output	Push Pull 1X	floating
2	VIN_PG	Digital Input	Digital Input with Schmitt trigger	100 kΩ pull-down
3	NC	--	Keep Floating or connect to GND	--
4	PG/Group1	Digital Input	Digital Input with Schmitt trigger	floating
5	PG/Group3	Digital Input	Digital Input with Schmitt trigger	floating
6	PG/Group5	Digital Input	Digital Input with Schmitt trigger	floating
7	SDA	Bi-directional	Digital Input without Schmitt trigger / Open Drain NMOS	floating
8	SCL	Digital Input	Digital Input without Schmitt trigger	floating
9	NC	Digital Input	Digital Input without Schmitt trigger	1 MΩ pull-down
10	PG/Group2	Digital Input	Low Voltage Digital Input	floating
11	System_PWR_EN	Digital Input	Low Voltage Digital Input	100 kΩ pull-down
12	Group3_EN	Digital Output	Push Pull 1X	floating
13	Group4_EN	Digital Output	Push Pull 1X	floating
14	GND2	GND	Ground	--
15	VDD2	PWR	Supply Voltage	--
16	Group5_EN	Digital Output	Push Pull 1X	floating
17	Group6_EN	Digital Output	Push Pull 1X	floating
18	OVERT*	Digital Input	Low Voltage Digital Input	floating
19	NC	Digital Input	Digital Input without Schmitt trigger	1 MΩ pull-down
20	NC	--	Keep Floating or connect to GND	--
21	PG/Group4	Digital Input	Digital Input with Schmitt trigger	floating
22	NC	--	Keep Floating or connect to GND	--
23	NC	--	Keep Floating or connect to GND	--
24	NC	--	Keep Floating or connect to GND	--
25	NC	--	Keep Floating or connect to GND	--
26	AVCC1	Analog Input/Output	Analog Input/Output	floating
27	NC	--	Keep Floating or connect to GND	--
28	AVCC2	Analog Input/Output	Analog Input/Output	floating
29	SYS_PWR_GD	Digital Output	Push Pull 1X	floating
30	GND	GND	Ground	--
31	VDD	PWR	Supply Voltage	--
32	Group1_EN	Digital Output	Push Pull 1X	floating

Ordering Information

Part number	Package type
SLG7SQ50562-EV	32-pin STQFN - Tape and Reel (5k units)

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Absolute Maximum Conditions

Parameter	Min	Max	Unit
Supply Voltage on V _{DD} relative to GND	-0.3	7	V
DC Input Voltage	GND - 0.5	V _{DD} + 0.5	V
Maximum Average or DC Current (Through V _{DD} or GND pin)	--	90	mA
Current at Input Pin	-1.0	1.0	mA
Input Leakage Current (Absolute Value)	--	1000	nA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{DD}	Supply Voltage		2.30	3.30	5.50	V
V _{DD2}	Supply Voltage 2	V _{DD2} ≤ V _{DD}	2.30	3.30	5.50	V
T _A	Operating Temperature		-40	25	125	°C
C _{VDD}	Capacitor Value at V _{DD}		0.1	--	--	μF
C _{IN}	Input Capacitance		--	4	--	pF
I _Q	Quiescent Current	Static inputs and floating outputs PIN8-7 are High. PIN4-6, PIN10, PIN18, PIN26, PIN28 are Low	--	57	--	μA
V _O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V _{DD} +0.3 (Note 1)	V
V _{IH}	HIGH-Level Input Voltage	Logic Input without Schmitt trigger (Note 2)	0.7xV _{DD} (Note 1)	--	V _{DD} +0.3 (Note 1)	V
		Logic Input with Schmitt Trigger	0.8xV _{DD} (Note 1)	--	V _{DD} +0.3 (Note 1)	V
		Low-Level Logic Input (Note 2)	1.25	--	V _{DD} +0.3 (Note 1)	V
V _{IL}	LOW-Level Input Voltage	Logic Input without Schmitt trigger (Note 2)	GND-0.3	--	0.3xV _{DD} (Note 1)	V
		Logic Input with Schmitt Trigger	GND-0.3	--	0.2xV _{DD} (Note 1)	V
		Low-Level Logic Input (Note 2)	GND-0.3	--	0.5	V
V _{OH}	HIGH-Level Output Voltage (Note 1)	Push-Pull 1X, V _{DD} = V _{DD2} = 2.3 V to 3 V, I _{OH} = 100 μA	2.288	2.593	--	V
		Push-Pull 1X, V _{DD} = V _{DD2} = 3 V to 4 V, I _{OH} = 3 mA	2.696	3.244	--	V
		Push-Pull 1X, V _{DD} = V _{DD2} = 4 V to 5.5 V, I _{OH} = 5 mA	3.608	4.588	--	V

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V _{OL}	LOW-Level Output Voltage (Note 1)	Push-Pull 1X, V _{DD} = V _{DD2} = 2.3 V to 3 V, I _{OL} = 100 µA	--	0.007	0.009	V
		Push-Pull 1X, V _{DD} = V _{DD2} = 3 V to 4 V, I _{OL} = 3 mA	--	0.161	0.232	V
		Push-Pull 1X, V _{DD} = V _{DD2} = 4 V to 5.5 V, I _{OL} = 5 mA	--	0.215	0.313	V
I _{OH}	HIGH-Level Output Current (Note 1, Note 3)	Push-Pull 1X, V _{DD} = V _{DD2} = 2.3 V to 3 V, V _{OH} = V _{DD} - 0.2 V	1.49	2.30	--	mA
		Push-Pull 1X, V _{DD} = V _{DD2} = 3 V to 4 V, V _{OH} = 2.4 V	5.28	11.70	--	mA
		Push-Pull 1X, V _{DD} = V _{DD2} = 4 V to 5.5 V, V _{OH} = 2.4 V	14.59	27.30	--	mA
I _{OL}	LOW-Level Output Current (Note 1, Note 3)	Push-Pull 1X, V _{DD} = V _{DD2} = 2.3 V to 3 V, V _{OL} = 0.15 V	1.48	2.30	--	mA
		Push-Pull 1X, V _{DD} = V _{DD2} = 3 V to 4 V, V _{OL} = 0.4 V	4.72	7.30	--	mA
		Push-Pull 1X, V _{DD} = V _{DD2} = 4 V to 5.5 V, V _{OL} = 0.4 V	5.97	9.30	--	mA
R _{PULL_DOWN}	Internal Pull-Down Resistance	Pull-down on PINs 2, 11	--	100	--	kΩ
		Pull-down on PINs 9, 19	--	1	--	MΩ
T _{DLY0_0 #1}	Delay Time	At temperature +25 °C	0.8	1.2	3.0	µs
		At temperature -40 +125 °C (Note 4)	0.3	1.2	4.3	µs
T _{DLY0_0 #2}	Delay Time	At temperature +25 °C	9.84	10.12	10.44	ms
		At temperature -40 +125 °C (Note 4)	9.77	10.12	10.65	ms
T _{DLY0_0 #3}	Delay Time	At temperature +25 °C	0.8	1.2	3.0	µs
		At temperature -40 +125 °C (Note 4)	0.3	1.2	4.3	µs
T _{DLY0_0 #4}	Delay Time	At temperature +25 °C	0.8	1.2	3.0	µs
		At temperature -40 +125 °C (Note 4)	0.3	1.2	4.3	µs
T _{DLY0_0 #5}	Delay Time	At temperature +25 °C	60	80	320	ns
		At temperature -40 +125 °C (Note 4)	60	80	340	ns
T _{DLY0_1 #0}	Delay Time	At temperature +25 °C	0.8	1.2	3.0	µs
		At temperature -40 +125 °C (Note 4)	0.3	1.2	4.3	µs
T _{OSH0_1 #1}	Pulse Width	At temperature +25 °C	0.8	1.2	3.0	µs
		At temperature -40 +125 °C (Note 4)	0.3	1.2	4.3	µs
T _{DLY0_1 #2}	Delay Time	At temperature +25 °C	4.92	5.01	5.13	ms
		At temperature -40 +125 °C (Note 4)	4.88	5.01	5.23	ms
T _{DLY0_1 #3}	Delay Time	At temperature +25 °C	60	80	320	ns
		At temperature -40 +125 °C (Note 4)	60	80	340	ns
T _{DLY1}	Delay Time	At temperature +25 °C	98.64	100.34	103.59	ms
		At temperature -40 +125 °C (Note 4)	98.15	100.34	118.90	ms
T _{DLY1_0 #1}	Delay Time	At temperature +25 °C	4.92	5.01	5.13	ms
		At temperature -40 +125 °C (Note 4)	4.88	5.01	5.23	ms
T _{DLY1_0 #2}	Delay Time	At temperature +25 °C	0.8	1.2	3.0	µs

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		At temperature -40 +125 °C (Note 4)	0.3	1.2	4.3	us
T _{DLY1_0 #3}	Delay Time	At temperature +25 °C	0.8	1.2	3.0	us
		At temperature -40 +125 °C (Note 4)	0.3	1.2	4.3	us
T _{DLY1_0 #4}	Delay Time	At temperature +25 °C	0.8	1.2	3.0	us
		At temperature -40 +125 °C (Note 4)	0.3	1.2	4.3	us
T _{DLY1_1 #0}	Delay Time	At temperature +25 °C	0.8	1.2	3.0	us
		At temperature -40 +125 °C (Note 4)	0.3	1.2	4.3	us
T _{DLY1_1 #1}	Delay Time	At temperature +25 °C	4.92	5.01	5.13	ms
		At temperature -40 +125 °C (Note 4)	4.88	5.01	5.23	ms
T _{DLY1_1 #2}	Delay Time	At temperature +25 °C	4.92	5.01	5.13	ms
		At temperature -40 +125 °C (Note 4)	4.88	5.01	5.23	ms
T _{DLY1_1 #3}	Delay Time	At temperature +25 °C	0.8	1.2	3.0	us
		At temperature -40 +125 °C (Note 4)	0.3	1.2	4.3	us
T _{DLY1_1 #4}	Delay Time	At temperature +25 °C	0.8	1.2	3.0	us
		At temperature -40 +125 °C (Note 4)	0.3	1.2	4.3	us
V _{ACMP0H}	Analog Comparator Threshold Voltage	Low to High transition, at temperature +25 °C	1710	--	1741	mV
		Low to High transition, at temperature -40 +125 °C (Note 4)	1701	--	1748	mV
		High to Low transition, at temperature +25 °C	1710	--	1741	mV
		High to Low transition, at temperature -40 +125 °C (Note 4)	1701	--	1748	mV
V _{ACMP1H}	Analog Comparator Threshold Voltage	Low to High transition, at temperature +25 °C	180	--	202	mV
		Low to High transition, at temperature -40 +125 °C (Note 4)	179	--	202	mV
		High to Low transition, at temperature +25 °C	180	--	202	mV
		High to Low transition, at temperature -40 +125 °C (Note 4)	179	--	202	mV
V _{ACMP2L}	Analog Comparator Threshold Voltage	Low to High transition, at temperature +25 °C	372	--	395	mV
		Low to High transition, at temperature -40 +125 °C (Note 4)	370	--	397	mV
		High to Low transition, at temperature +25 °C	372	--	395	mV
		High to Low transition, at temperature -40 +125 °C (Note 4)	370	--	397	mV
V _{ACMP3L}	Analog Comparator Threshold Voltage	Low to High transition, at temperature +25 °C	86	--	105	mV
		Low to High transition, at temperature -40 +125 °C (Note 4)	85	--	105	mV
		High to Low transition,	86	--	105	mV

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		at temperature +25 °C				
		High to Low transition, at temperature -40 +125 °C (Note 4)	85	--	105	mV
T _{SU}	Startup Time	From V _{DD} rising past PON _{THR}	--	1.22	2.09	ms
PON _{THR}	Power-On Threshold	V _{DD} Level Required to Start Up the Chip	1.64	1.85	2.06	V
POFF _{THR}	Power-Off Threshold	V _{DD} Level Required to Switch Off the Chip	0.81	1.26	1.55	V
Note 1 GPIs 0, 1, 2, 3, 4, 5, 6, 7, GPIOs 0, 1, 2, 3, 8, 9, 10, 11, GPOs 0, 5, 6, 7 are powered from V _{DD} and GPIOs 4, 5, 6, 7, GPOs 1, 2, 3, 4 are powered from V _{DD2} . Note 2 No hysteresis. Note 3 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions. Note 4 Guaranteed by Design.						

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Asynchronous State Machine (ASM) Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
t _{st_out_delay}	Asynchronous State Machine Output Delay Time	V _{DD} = 2.5 V ± 8%	133	--	277	ns
		V _{DD} = 3.3 V ± 10%	96	--	190	ns
		V _{DD} = 5.0 V ± 10%	70	--	123	ns
t _{st_out}	Asynchronous State Machine Output Transition Time	V _{DD} = 2.5 V ± 8%	--	--	165	ns
		V _{DD} = 3.3 V ± 10%	--	--	70	ns
		V _{DD} = 5.0 V ± 10%	--	--	46	ns
t _{st_pulse}	Asynchronous State Machine Input Pulse Acceptance Time	V _{DD} = 2.5 V ± 8%	28	--	--	ns
		V _{DD} = 3.3 V ± 10%	19	--	--	ns
		V _{DD} = 5.0 V ± 10%	12	--	--	ns
t _{st_comp}	Asynchronous State Machine Input Compete Time	V _{DD} = 2.5 V ± 8%	--	--	10	ns
		V _{DD} = 3.3 V ± 10%	--	--	7	ns
		V _{DD} = 5.0 V ± 10%	--	--	5	ns
t _{st_sequential_delay}	Asynchronous State Machine Sequential Output Delay Time	V _{DD} = 2.5 V ± 8%	229	--	485	ns
		V _{DD} = 3.3 V ± 10%	162	--	330	ns
		V _{DD} = 5.0 V ± 10%	119	--	208	ns
t _{st_dmlatch_delay}	Asynchronous State Machine Dynamic Memory Latch Delay	V _{DD} = 2.5 V ± 8%	229	--	485	ns
		V _{DD} = 3.3 V ± 10%	162	--	330	ns
		V _{DD} = 5.0 V ± 10%	119	--	208	ns

I²C Specifications

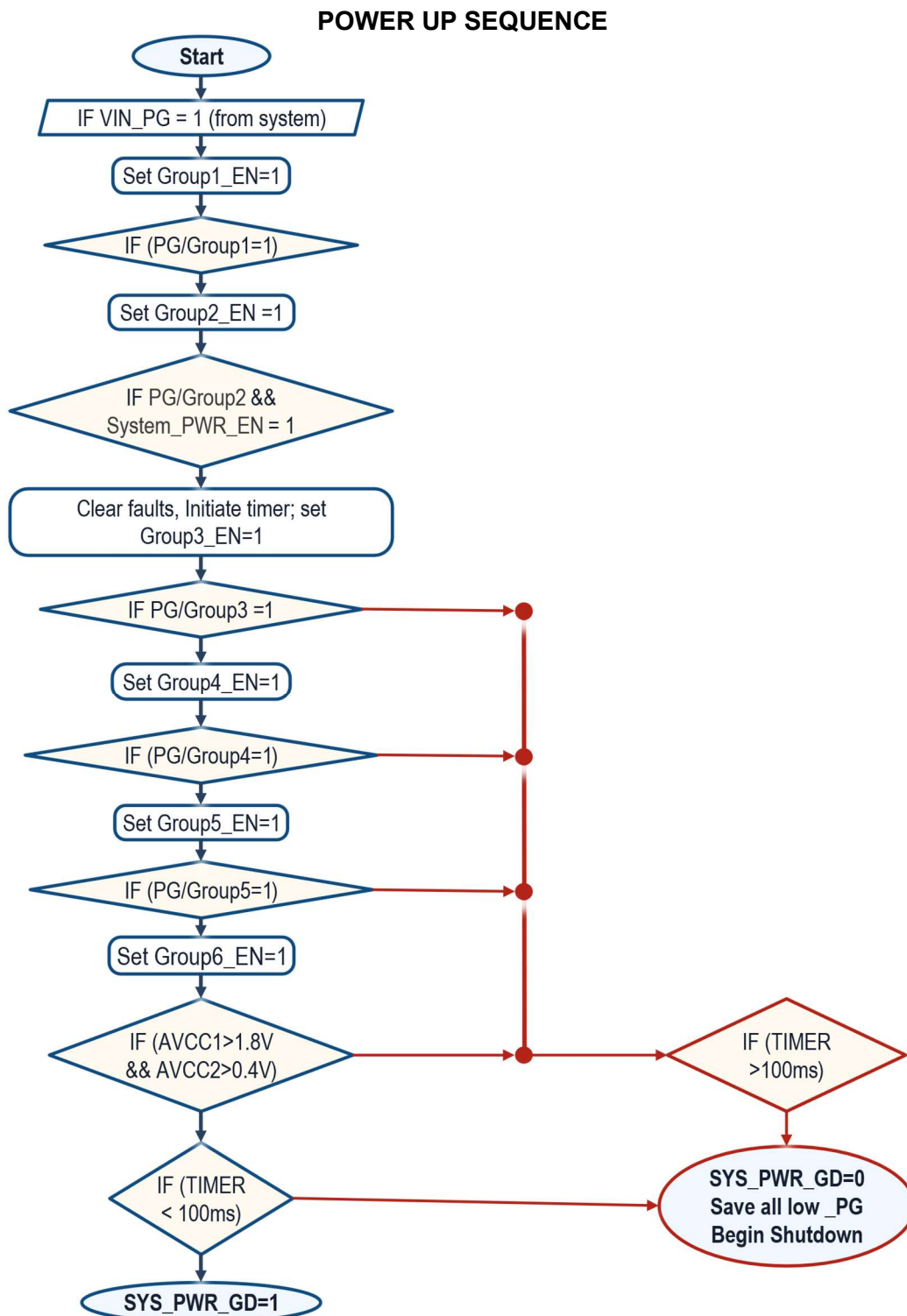
Symbol	Parameter	Condition/Note	Min	Typ	Max	Unit
F _{SCL}	Clock Frequency, SCL		--	--	1000	kHz
t _{LOW}	Clock Pulse Width Low		500	--	--	ns
t _{HIGH}	Clock Pulse Width High		260	--	--	ns
t _{AA}	Clock Low to Data Out Valid		--	--	450	ns
t _{BUF}	Bus Free Time between Stop and Start		500	--	--	ns
t _{HD_STA}	Start Hold Time		260	--	--	ns
t _{SU_STA}	Start Set-up Time		260	--	--	ns
t _{HD_DAT}	Data Hold Time		0	--	--	ns
t _{SU_DAT}	Data Set-up Time		50	--	--	ns
t _R	Inputs Rise Time		--	--	120	ns
t _F	Inputs Fall Time		--	--	129	ns
t _{SU_STO}	Stop Set-up Time		260	--	--	ns
t _{VD_DAT}	Data Valid Time		--	--	450	ns

Chip Address

HEX	BIN	DEC	Memory Space
0x08	0001000	8	0x000..0FF
0x09	0001001	9	0x100..1FF

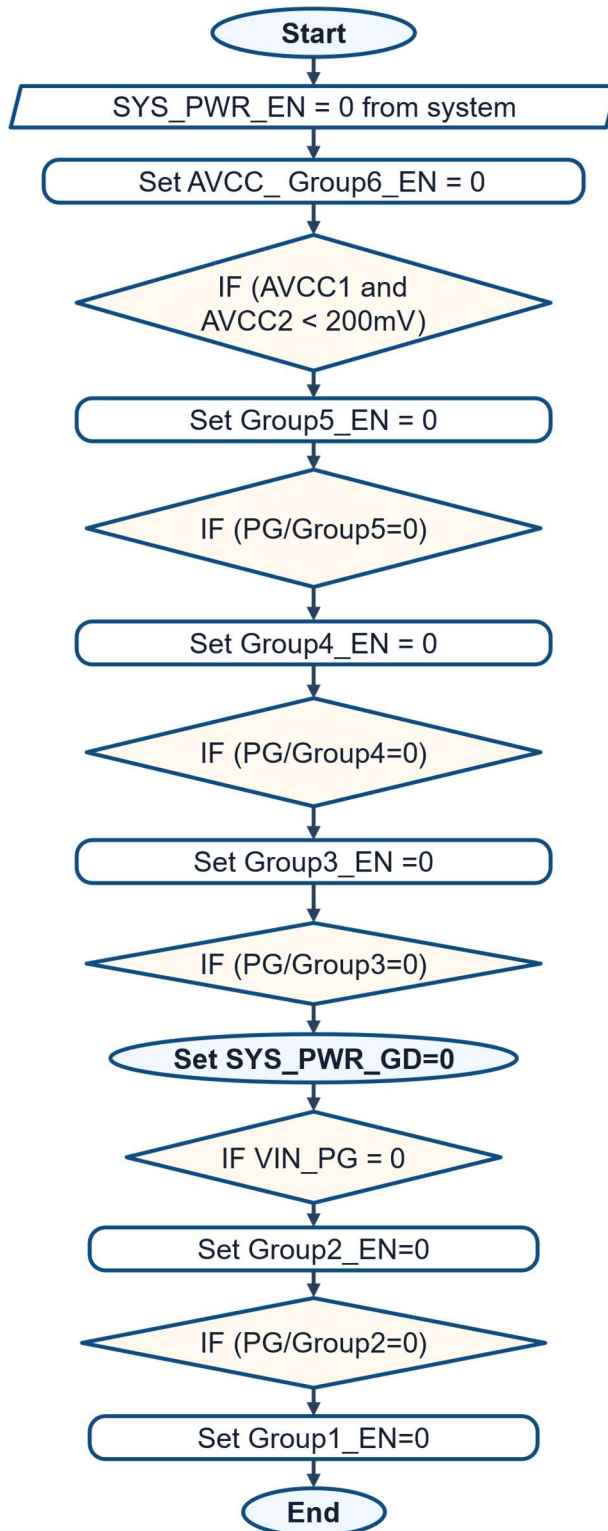
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Description



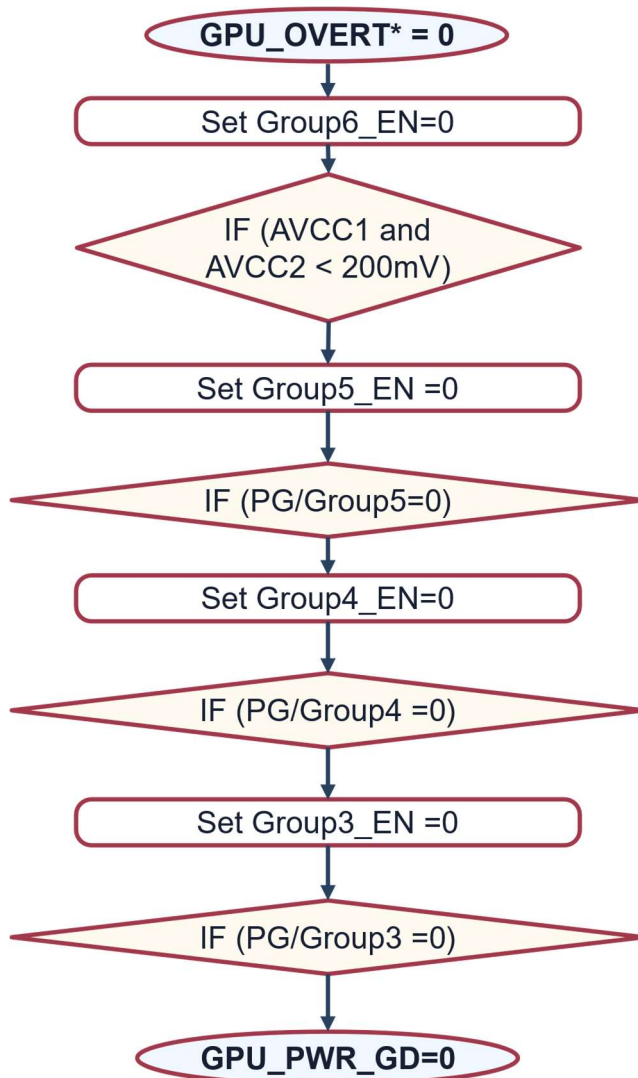
6-Channel Power Sequencer with PG and Fault Monitoring

SHUTDOWN SEQUENCE (CONTROLLED)



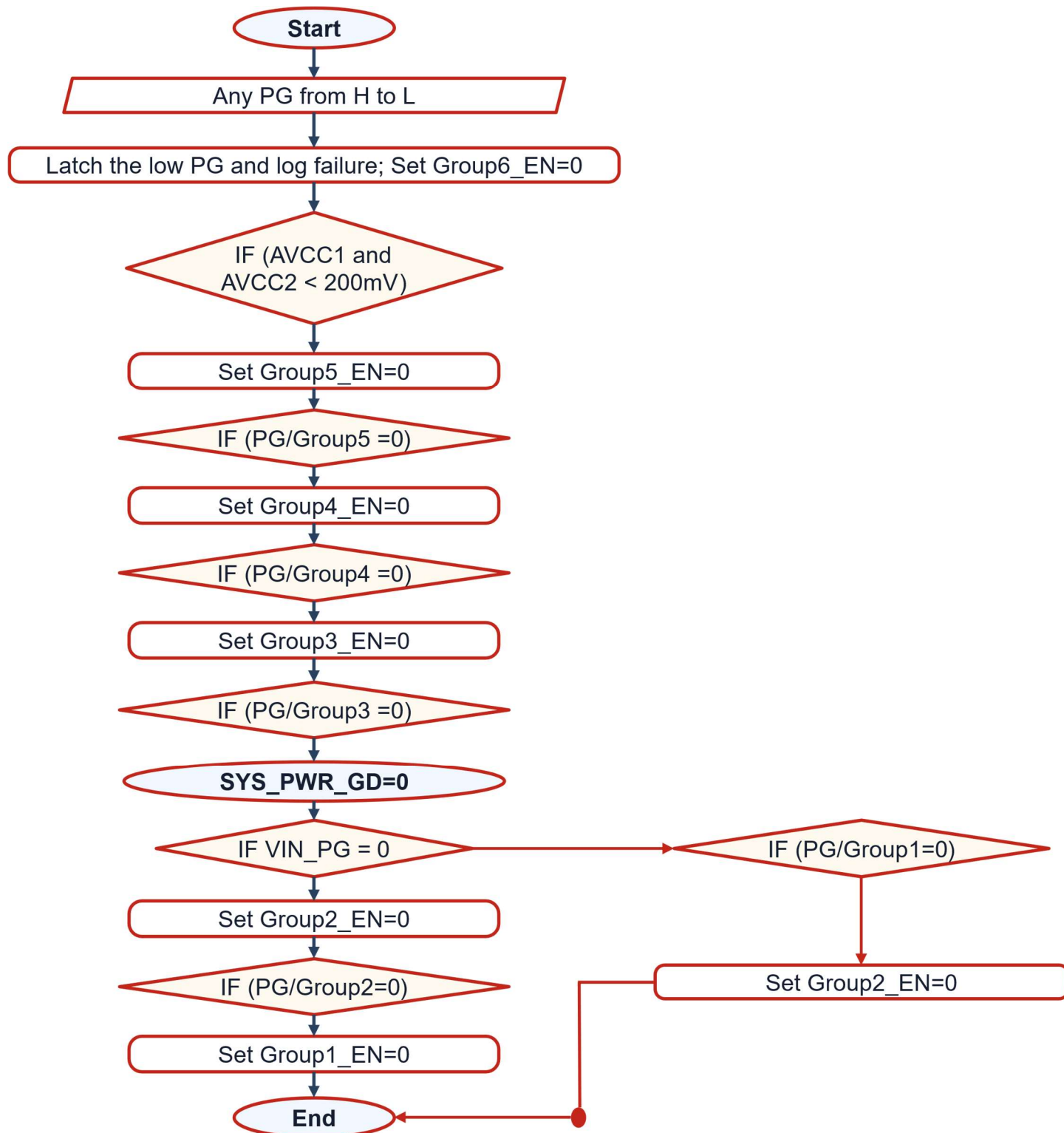
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OVER_TEMPERATURE SEQUENCE



6-Channel Power Sequencer with PG and Fault Monitoring

SHUTDOWN SEQUENCE (SUPRISE/UNCONTROLLED)



6-Channel Power Sequencer with PG and Fault Monitoring

I²C Description

I²C Basic Command Structure

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the START condition, the first four bits are a control code, which can be set by the user in registers [4083:4080] or value defined externally by GPIs GPI4, GPI5, GPI6, and GPI7. The LSB of the control code is defined by the value of GPI4, while the MSB is defined by the value of GPI7. The address source is selected by register [4087]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a '1' selecting for a Read command, and a '0' selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device chooses to set the Control Code to either '1111' or '0000' in a system with other target device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to insure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG7SQ50562-E are in the range from 0 (00H) to 511 (1FFH). The upper two address bits (A10 and A9) will be '0' for all commands to the SLG7SQ50562-E. The value of Address bit A8 will depend on whether the Bus Controller is addressing the upper or lower half of the 4K bit address space.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address.

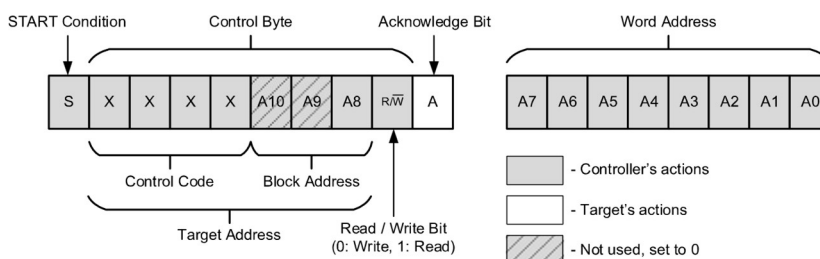


Figure 1. Basic Command Structure

Table 1: I²C Block Addressing

I ² C Address	Address bits		
	A10	A9	A8
0x08	0	0	0
0x09	0	0	1

I²C Serial General Timing

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 2. Timing specifications can be found in I²C Specifications section

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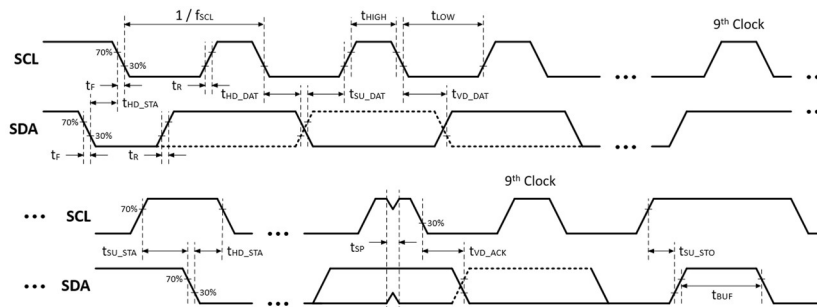


Figure 2. I²C General Timing Characteristics

Byte Write Command

Following the START condition from the controller, the Control Code [4 bits], the Block address [3 bits], and the $\overline{R/\overline{W}}$ bit (set to "0") are placed onto the I²C bus by the controller. After the SLG7SQ50562-E sends an Acknowledge bit (ACK), the next byte transmitted by the controller is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG7SQ50562-E, where the data byte is to be written. After the SLG7SQ50562-E sends another Acknowledge bit, the Controller will transmit the data byte to be written into the addressed memory location. The SLG7SQ50562-E again provides an Acknowledge bit and then the controller generates a STOP condition. The internal write cycle for the data will take place at the time that the SLG7SQ50562-E generates the Acknowledge bit.

It is possible to latch all IOs during I²C write command, register [4065] = 1 - Enable. It means that IOs will remain their state until the write command is done.

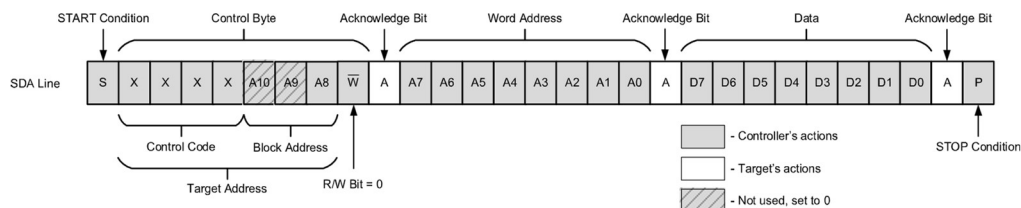


Figure 3. Byte Write Command, $\overline{R/\overline{W}} = 0$

Random Read Command

The Random Read Command allows to read data at an arbitrary address. The Random Read command starts with a Control Byte (with $\overline{R/\overline{W}}$ bit set to '0', indicating a write command) and Word Address to set the internal byte address, followed by a START condition, and then the Control Byte for the read (exactly the same as the Byte Write command). The START condition in the middle of the command will halt the decoding of a Write command but will set the internal address counter in preparation for the second half of the command. After the START condition, the Bus controller issues a second control byte with the $\overline{R/\overline{W}}$ bit set to '1', after which the SLG7SQ50562-E issues an Acknowledge bit, followed by the requested eight data bits.

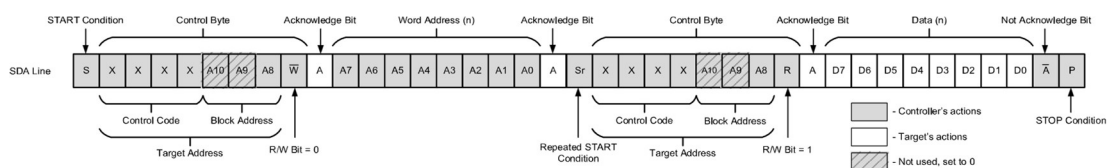


Figure 4. Random Read Command

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I²C register control data

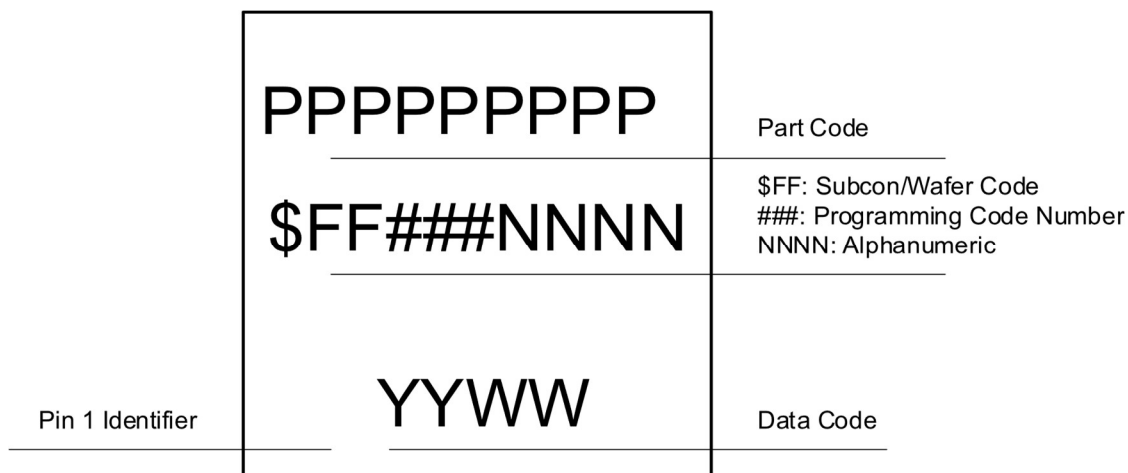
Address Byte	Register Bit	Block	Function
0x198	reg<3271:3264>	F1 stack memory, lower byte	Monitor PG signals after GPU_PWR_GD is H
0x1E1	reg<3855:3848>	CNT2 Counter Value	Monitor power up states

I²C Commands

1. [start] [0x09] [w] [0x98] [start] [0x09] [R] [xxxxxxx] [stop] // read F1 stack memory
2. [start] [0x09] [w] [0xE1] [start] [0x09] [R] [xxxxxxx] [stop] // read CNT2 Counter Value

6-Channel Power Sequencer with PG and Fault Monitoring

Package Top Marking



Datasheet revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	001	U	0xCC5FA8A1	SQ50562-EV	A	09/11/2026

Memory Lock Options

Option	Status
Registers	Unlocked

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

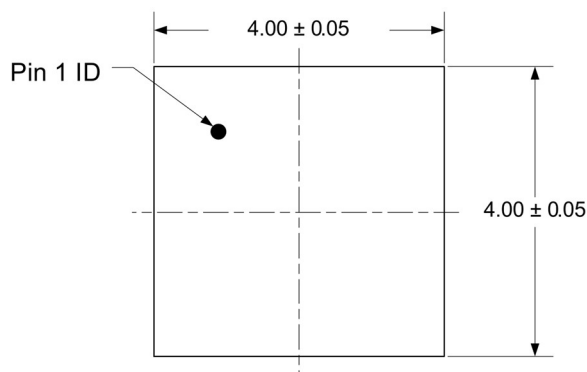
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Package Drawing and Dimensions

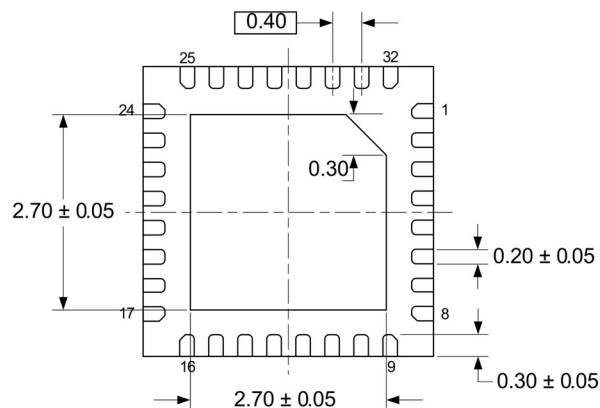
STQFN-32 (4.0 mm x 4.0 mm x 0.55 mm, 0.4 mm Pitch)

JEDEC MO-220, Variation WECE

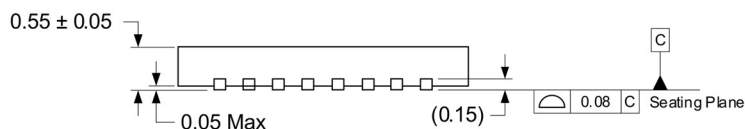
IC Net Weight: 0.028 g



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Note 1: JEDEC compatible.

Note 2: All dimensions are in mm and angles are in degrees.

Note 3: Use ± 0.05 mm for the non-toleranced dimensions.

Note 4: Numbers in () are for references only.

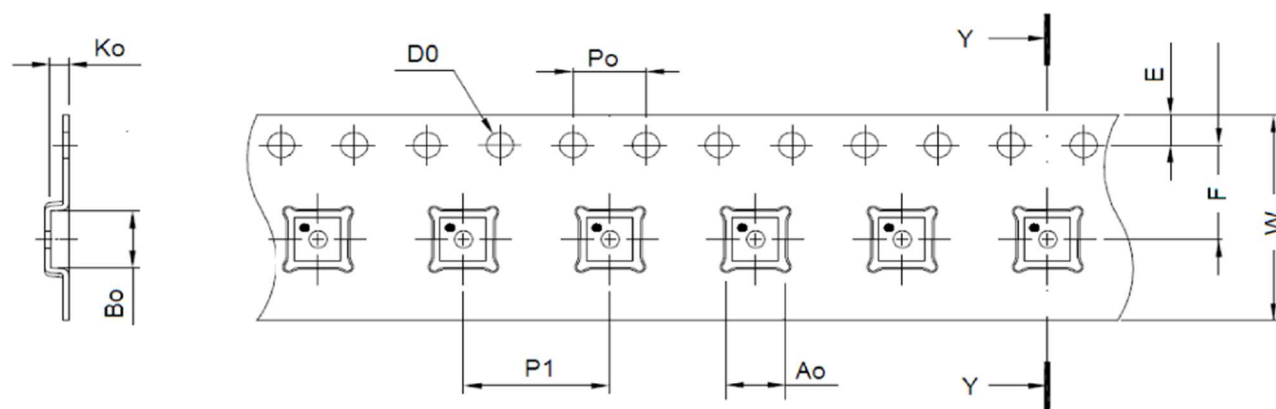
6-Channel Power Sequencer with PG and Fault Monitoring

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader [min]		Trailer [min]		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 32L 4 mm x 4 mm 0.4P Green	32	4x4x0.55	5000	10000	330/100	42	336	42	336	12	8

Carrier Tape Drawing and Dimensions

Package Type	PocketB™ Length [mm]	PocketB™ Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 32L 4 mm x 4 mm 0.4P Green	4.25	4.25	0.75	4	8	1.5	1.75	5.5	12

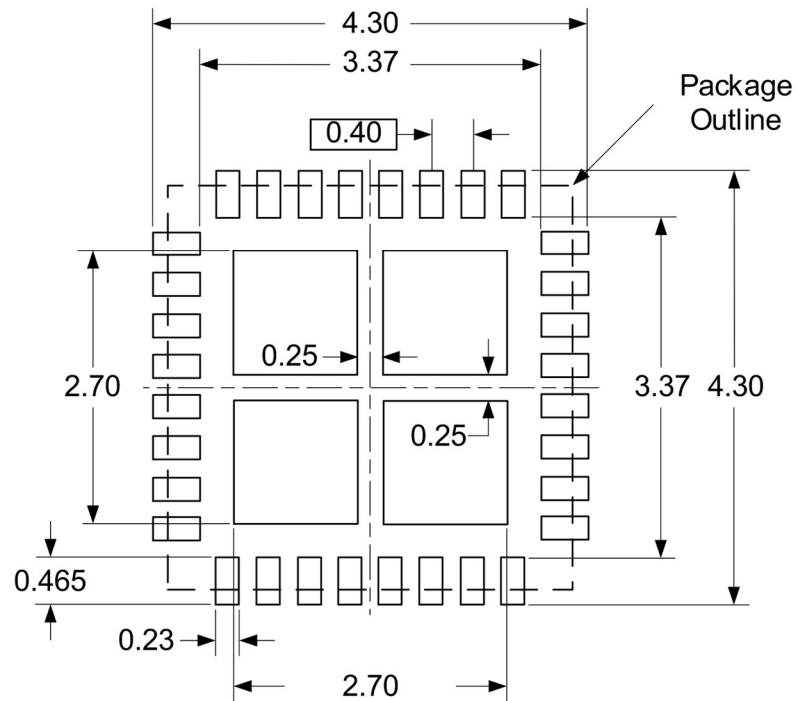


Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.85 mm³ (nominal). More information can be found at www.jedec.org.

6-Channel Power Sequencer with PG and Fault Monitoring

Recommended Land Pattern



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

Note 1: JEDEC compatible.

Note 2: All dimensions are in mm and angles are in degrees.

Note 3: Use ± 0.05 mm for the non-toleranced dimensions.

Note 4: Numbers in () are for references only.

6-Channel Power Sequencer with PG and Fault Monitoring

Datasheet Revision History

Date	Version	Change
07/31/2026	0.10	New Design
09/11/2026	0.11	Updated DRS Table
09/11/2026	1.00	Production Release