

8-Rail Cascaded Power Sequencer

General Description

Renesas SLG7SQ50538 is a low power and small form device. The mixed-signal IC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

This device can be further customized to meet your specific application requirements. Custom designs can be created using the free GUI-based Go Configure™ Software Hub, available for download at [renesas.com](https://www.renesas.com), where example projects are also included. Contact your local Renesas representative or email greenpak@renesas.com for support.

Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

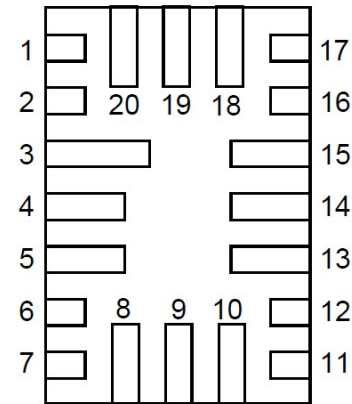
Output Summary

4 Outputs - Open Drain NMOS 1X
3 Outputs - Push Pull 1X

Pin Name

Pin #	Pin name	Pin #	Pin name
1	VDD	11	GND
2	ON	12	SET3
3	NC	13	SET4
4	SET2	14	FAULT_External
5	OFF	15	VCC
6	SET1	16	FAULT OUT
7	OUT1	17	DONE
8	OUT2	18	OUT4
9	NC	19	OUT3
10	POK	20	NC

Pin Configuration



**STQFN-20
(Top View)**

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Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	ON	Digital Input	Digital Input without Schmitt trigger	floating
3	NC	--	Keep Floating or Connect to GND	--
4	SET2	Analog Input/Output	Analog Input/Output	floating
5	OFF	Digital Input	Digital Input without Schmitt trigger	floating
6	SET1	Analog Input/Output	Analog Input/Output	floating
7	OUT1	Digital Output	Push Pull 1X	floating
8	OUT2	Digital Output	Push Pull 1X	floating
9	NC	--	Keep Floating or Connect to GND	--
10	POK	Digital Output	Open Drain NMOS 1X	10kΩ pullup
11	GND	GND	Ground	--
12	SET3	Analog Input/Output	Analog Input/Output	floating
13	SET4	Analog Input/Output	Analog Input/Output	floating
14	FAULT_External	Digital Input	Digital Input without Schmitt trigger	floating
15	VCC	Analog Input/Output	Analog Input/Output	1MΩ pulldown
16	FAULT OUT	Digital Output	Open Drain NMOS 1X	10kΩ pullup
17	DONE	Digital Output	Push Pull 1X	floating
18	OUT4	Digital Output	Open Drain NMOS 1X	10kΩ pullup
19	OUT3	Digital Output	Open Drain NMOS 1X	10kΩ pullup
20	NC	--	Keep Floating or Connect to GND	--

Ordering Information

Part Number	Package Type
SLG7SQ50538V	20-pin STQFN - Tape and Reel (3k units)

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Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	10	mA
	OD 1x	--	14	
Current at Input Pin		-1.0	1.0	mA
ACMP Input Leakage	Vin = 0 V	--	1.38	nA
	Vin = VDD	--	1.40	
Logic Input without Schmitt Trigger(Floating) Leakage	Vin = 0 V	--	2.11	nA
	Vin = VDD	--	172.97	
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		2.9	3.3	5.5	V
T _A	Operating Temperature		-40	25	85	°C
C _{VDD}	Capacitor Value at VDD		--	0.1	--	μF
C _{IN}	Input Capacitance		--	4	--	pF
I _Q	Quiescent Current	PINs 2, 4, 6, 12 and 14 are HIGH, PINs 5, 13 are LOW	--	70	--	μA
V _O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I _{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T _J = 85°C	--	--	45	mA
		T _J = 110°C	--	--	21	mA
I _{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T _J = 85°C	--	--	69	mA
		T _J = 110°C	--	--	33	mA
V _{IH}	HIGH-Level Input Voltage	Logic Input at VDD = 1.8 V ± 5 %	1.087	--	VDD	V
		Logic Input at VDD = 3.3 V ± 10 %	1.949	--	VDD	V
		Logic Input at VDD = 5.0 V ± 10 %	2.930	--	VDD	V
V _{IL}	LOW-Level Input Voltage	Logic Input at VDD = 1.8 V ± 5 %	0	--	0.759	V
		Logic Input at VDD = 3.3 V ± 10 %	0	--	1.286	V
		Logic Input at VDD = 5.0 V ± 10 %	0	--	1.910	V
V _{OH}	HIGH-Level Output Voltage	Push-Pull 1X, I _{OH} =100μA, at VDD = 1.8 V ± 5 %	1.680	1.788	--	V
		Push-Pull 1X, I _{OH} =3mA, at VDD = 3.3 V ± 10 %	2.713	3.095	--	V
		Push-Pull 1X, I _{OH} =5mA, at VDD = 5.0 V ± 10 %	4.159	4.750	--	V
V _{OL}	LOW-Level Output Voltage	Push-Pull 1X, I _{OL} =100μA, at VDD = 1.8 V ± 5 %	--	0.010	0.015	V
		Push-Pull 1X, I _{OL} =3mA, at VDD = 3.3 V ± 10 %	--	0.148	0.228	V

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		Push-Pull 1X, $I_{OL}=5\text{mA}$, at $V_{DD} = 5.0\text{ V} \pm 10\%$	--	0.189	0.270	V
		Open Drain NMOS 1X, $I_{OL}=100\mu\text{A}$, at $V_{DD} = 1.8\text{ V} \pm 5\%$	--	0.007	0.010	V
		Open Drain NMOS 1X, $I_{OL}=3\text{mA}$, at $V_{DD} = 3.3\text{ V} \pm 10\%$	--	0.080	0.147	V
		Open Drain NMOS 1X, $I_{OL}=5\text{mA}$, at $V_{DD} = 5.0\text{ V} \pm 10\%$	--	0.102	0.180	V
I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 1X, $V_{OH}=V_{DD}-0.2\text{V}$, at $V_{DD} = 1.8\text{ V} \pm 5\%$	1.027	1.703	--	mA
		Push-Pull 1X, $V_{OH}=2.4\text{V}$, at $V_{DD} = 3.3\text{ V} \pm 10\%$	5.608	10.774	--	mA
		Push-Pull 1X, $V_{OH}=2.4\text{V}$, at $V_{DD} = 5.0\text{ V} \pm 10\%$	20.337	30.010	--	mA
I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 1X, $V_{OL}=0.15\text{V}$, at $V_{DD} = 1.8\text{ V} \pm 5\%$	0.917	1.660	--	mA
		Push-Pull 1X, $V_{OL}=0.4\text{V}$, at $V_{DD} = 3.3\text{ V} \pm 10\%$	4.875	7.795	--	mA
		Push-Pull 1X, $V_{OL}=0.4\text{V}$, at $V_{DD} = 5.0\text{ V} \pm 10\%$	6.996	10.438	--	mA
		Open Drain NMOS 1X, $V_{OL}=0.15\text{V}$, at $V_{DD} = 1.8\text{ V} \pm 5\%$	1.375	2.534	--	mA
		Open Drain NMOS 1X, $V_{OL}=0.4\text{V}$, at $V_{DD} = 3.3\text{ V} \pm 10\%$	7.313	12.370	--	mA
		Open Drain NMOS 1X, $V_{OL}=0.4\text{V}$, at $V_{DD} = 5.0\text{ V} \pm 10\%$	10.820	17.380	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PINs 10, 16, 18, 19	--	10	--	k Ω
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PIN 15	--	1	--	M Ω
T_{DLY0}	Delay time	At temperature +25°C	8.00	9.00	11.00	μs
		At temperature -40 +85°C (Note 4)	8.00	9.00	11.00	μs
T_{DLY1}	Delay time	At temperature +25°C	74.00	80.00	86.00	μs
		At temperature -40 +85°C (Note 4)	74.00	80.00	89.00	μs
T_{DLY2}	Delay time	At temperature +25°C	18.00	20.00	22.00	μs
		At temperature -40 +85°C (Note 4)	18.00	20.00	23.00	μs
T_{DLY3}	Delay time	At temperature +25°C	400	500	1120	ns
		At temperature -40 +85°C (Note 4)	400	500	1220	ns
T_{DLY4}	Delay time	At temperature +25°C	13.00	15.00	17.00	μs
		At temperature -40 +85°C (Note 4)	13.00	15.00	18.00	μs
T_{DLY5}	Delay time	At temperature +25°C	19.15	20.08	20.91	ms
		At temperature -40 +85°C (Note 4)	18.87	20.08	21.62	ms
T_{DLY6}	Delay time	At temperature +25°C	13.00	15.00	17.00	μs
		At temperature -40 +85°C (Note 4)	13.00	15.00	18.00	μs
T_{DLY7}	Delay time	At temperature +25°C	13.00	15.00	17.00	μs
		At temperature -40 +85°C (Note 4)	13.00	15.00	18.00	μs
T_{DLY8}	Delay time	At temperature +25°C	13.00	15.00	17.00	μs
		At temperature -40 +85°C (Note 4)	13.00	15.00	18.00	μs
T_{DLY9}	Delay time	At temperature +25°C	13.00	15.00	17.00	μs
		At temperature -40 +85°C (Note 4)	13.00	15.00	18.00	μs
V_{ACMP0}	Analog Comparator0 Threshold Voltage	Low to High transition, at temperature +25°C	475	--	525	mV

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		Low to High transition, at temperature -40 +85°C (Note 4)	467	--	535	mV
		High to Low transition, at temperature +25°C	473	--	524	mV
		High to Low transition, at temperature -40 +85°C (Note 4)	464	--	532	mV
V _{ACMP1}	Analog Comparator1 Threshold Voltage	Low to High transition, at temperature +25°C	474	--	524	mV
		Low to High transition, at temperature -40 +85°C (Note 4)	465	--	535	mV
		High to Low transition, at temperature +25°C	473	--	521	mV
		High to Low transition, at temperature -40 +85°C (Note 4)	464	--	531	mV
V _{ACMP2}	Analog Comparator2 Threshold Voltage	Low to High transition, at temperature +25°C	474	--	525	mV
		Low to High transition, at temperature -40 +85°C (Note 4)	467	--	532	mV
		High to Low transition, at temperature +25°C	473	--	523	mV
		High to Low transition, at temperature -40 +85°C (Note 4)	466	--	529	mV
V _{ACMP3}	Analog Comparator3 Threshold Voltage	Low to High transition, at temperature +25°C	2332	--	2476	mV
		Low to High transition, at temperature -40 +85°C (Note 4)	2306	--	2495	mV
		High to Low transition, at temperature +25°C	2330	--	2474	mV
		High to Low transition, at temperature -40 +85°C (Note 4)	2303	--	2492	mV
V _{ACMP5}	Analog Comparator5 Threshold Voltage	Low to High transition, at temperature +25°C	487	--	515	mV
		Low to High transition, at temperature -40 +85°C (Note 4)	482	--	519	mV
		High to Low transition, at temperature +25°C	485	--	514	mV
		High to Low transition, at temperature -40 +85°C (Note 4)	480	--	518	mV
T _{SU}	Startup Time (see Note 3)	From VDD rising past PON _{THR}	0.526	1.4	5.148	ms
PON _{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	0.953	1.462	1.707	V
POFF _{THR}	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.935	1.103	1.281	V

Note:

- DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
- The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 14, 15, 16, 17, 18, 19 and 20 to another.
- VDD ramp rising speed must be less than 0.6 V/μs after power on. Violating this specification may cause chip to restart.
- Guaranteed by design.

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Package Top Marking



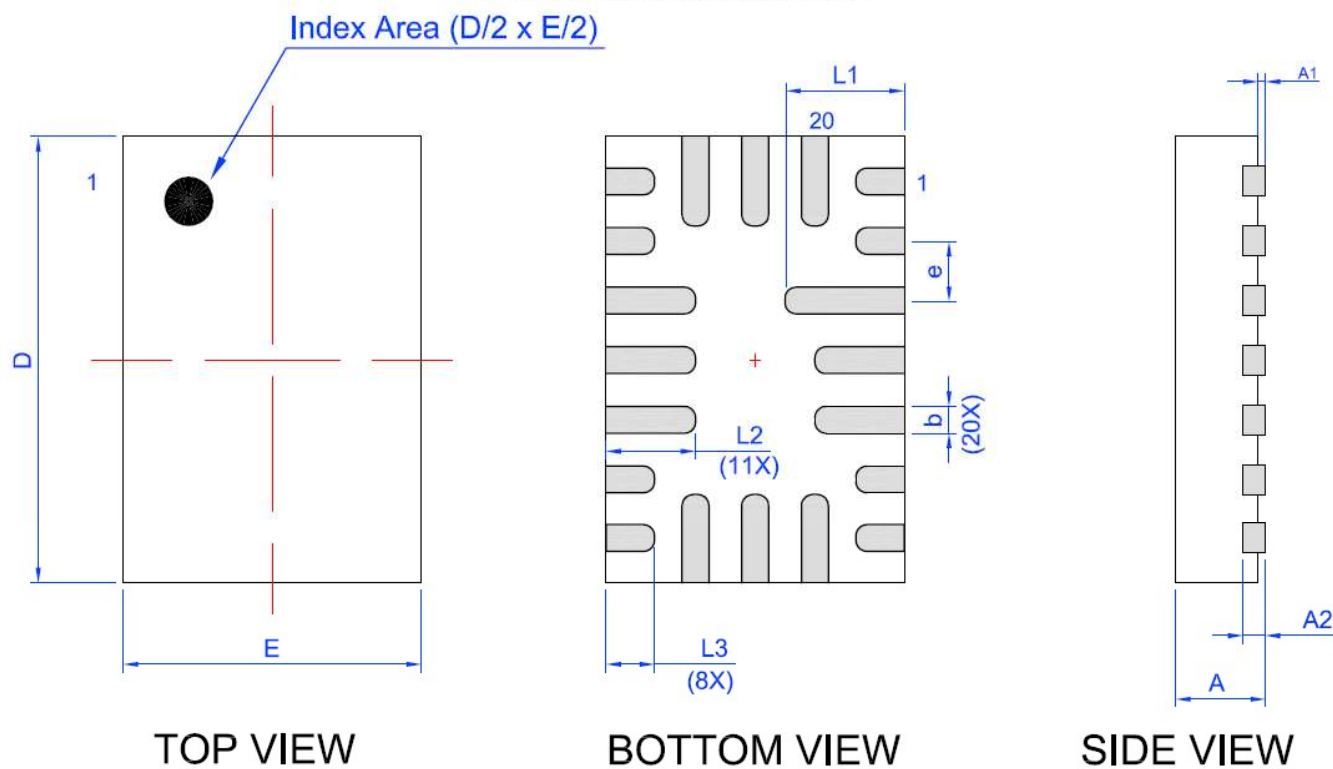
Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	003	U	0x60393004	50538	AA	08/21/2026

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

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Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P COL Package
JEDEC MO-220, Variation WECE



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

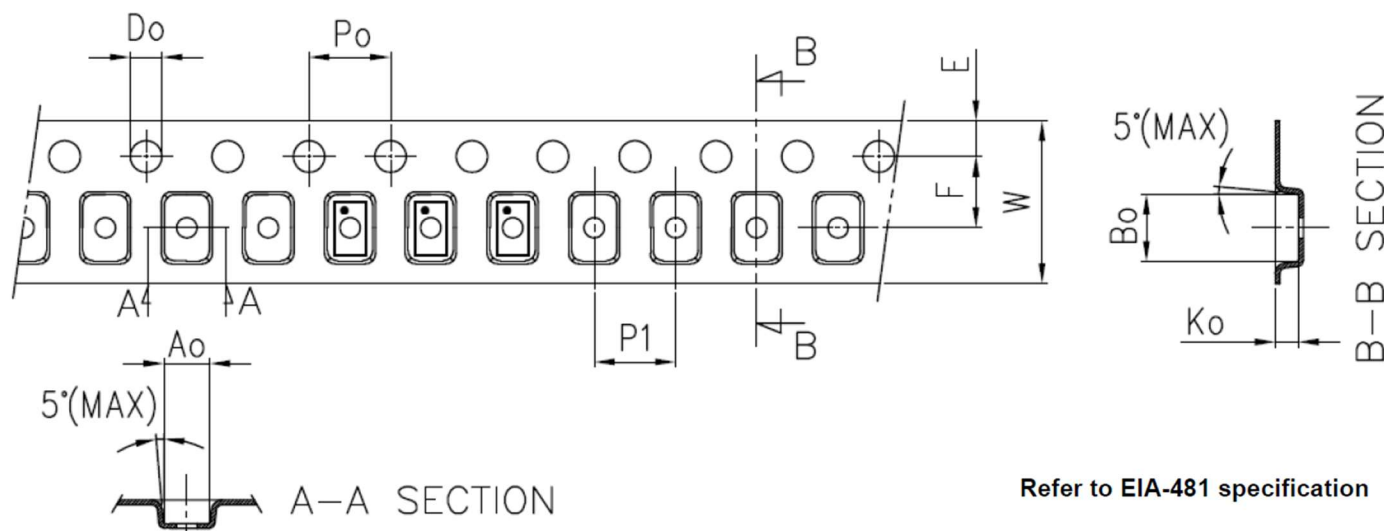
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Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3 mm 0.4P COL	20	2 x 3 x 0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3 mm 0.4P COL	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm³ (nominal). More information can be found at www.jedec.org.

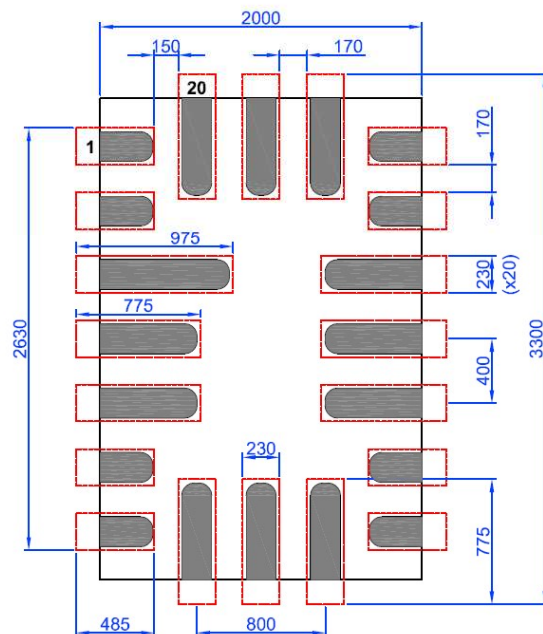
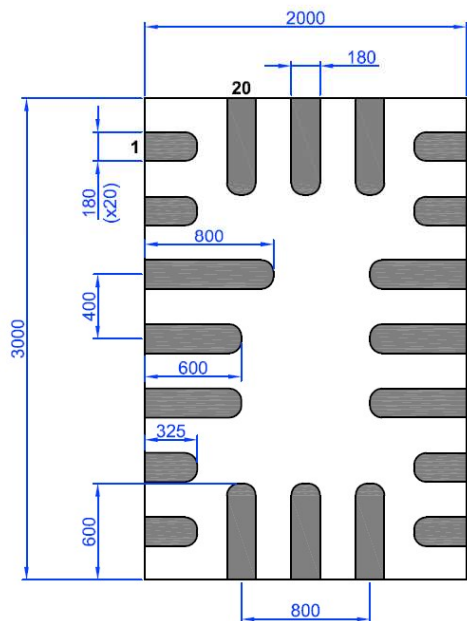
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Recommended Land Pattern

 Exposed Pad
(Top View)

 Recommended Land Pattern
(Top View)

Units: μm



Datasheet Revision History

Date	Version	Change
07/24/2026	0.10	New design
07/28/2026	0.11	Updated VDD range
08/13/2026	0.12	Updated design functionality
08/19/2026	0.13	Updated Device Revision Table
08/21/2026	1.00	Production Release

