

6-Channel Sequencer with PG

General Description

Renesas SLG7SQ50535 is a low power and small form device. The mixed-signal IC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

This device can be further customized to meet your specific application requirements. Custom designs can be created using the free GUI-based Go Configure™ Software Hub, available for download at [renesas.com](https://www.renesas.com), where example projects are also included. Contact your local Renesas representative or email greenpak@renesas.com for support.

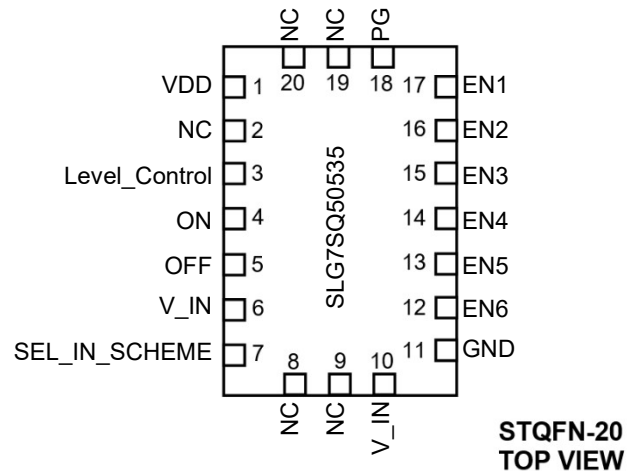
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

Output Summary

7 Outputs - Open Drain NMOS 1X

Pin Configuration



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Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	Level_Control	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
4	ON	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
5	OFF	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
6	V_IN	Analog Input/Output	Analog Input/Output	floating
7	SEL_IN_SCHEME	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
8	NC	--	Keep Floating or Connect to GND	--
9	NC	--	Keep Floating or Connect to GND	--
10	V_IN	Analog Input/Output	Analog Input/Output	floating
11	GND	GND	Ground	--
12	EN6	Digital Output	Open Drain NMOS 1X	1MΩ pullup
13	EN5	Digital Output	Open Drain NMOS 1X	1MΩ pullup
14	EN4	Digital Output	Open Drain NMOS 1X	1MΩ pullup
15	EN3	Digital Output	Open Drain NMOS 1X	1MΩ pullup
16	EN2	Digital Output	Open Drain NMOS 1X	1MΩ pullup
17	EN1	Digital Output	Open Drain NMOS 1X	1MΩ pullup
18	PG	Digital Output	Open Drain NMOS 1X	1MΩ pullup
19	NC	--	Keep Floating or Connect to GND	--
20	NC	--	Keep Floating or Connect to GND	--

Ordering Information

Part Number	Package Type
SLG7SQ50535V	VTR=STQFN-20 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5	VDD + 0.5	V
Maximum Average or DC Current (Through pin)	OD 1x	--	8	mA
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		3.9	3.9	5.5	V
T _A	Operating Temperature		-40	25	85	°C
C _{VDD}	Capacitor Value at VDD		--	0.1	--	μF
C _{IN}	Input Capacitance		--	4	--	pF
I _Q	Quiescent Current	VDD=5.5V; inputs LOW; floating outputs	--	120	--	μA
V _O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD + 0.3	V
I _{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T _J = 85 °C	--	--	45	mA
		T _J = 110 °C	--	--	22	mA
I _{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T _J = 85 °C	--	--	84	mA
		T _J = 110 °C	--	--	40	mA
V _{IH}	HIGH-Level Input Voltage	Logic Input at VDD = 3.3 V ± 10 %	1.78	--	--	V
		Logic Input at VDD = 5.0 V ± 10 %	2.64	--	--	V
V _{IL}	LOW-Level Input Voltage	Logic Input at VDD = 3.3 V ± 10 %	--	--	1.21	V
		Logic Input at VDD = 5.0 V ± 10 %	--	--	1.84	V
V _{OL}	LOW-Level Output Voltage	Open Drain NMOS 1X, I _{OL} = 3 mA, at VDD = 3.3 V ± 10 %	--	0.08	0.147	V
		Open Drain NMOS 1X, I _{OL} = 5 mA, at VDD = 5.0 V ± 10 %	--	0.102	0.18	V
I _{OL}	LOW-Level Output Current (see Note 1)	Open Drain NMOS 1X, V _{OL} = 0.4 V, at VDD = 3.3 V ± 10 %	7.313	12.37	--	mA
		Open Drain NMOS 1X, V _{OL} = 0.4 V, at VDD = 5.0 V ± 10 %	10.82	17.38	--	mA

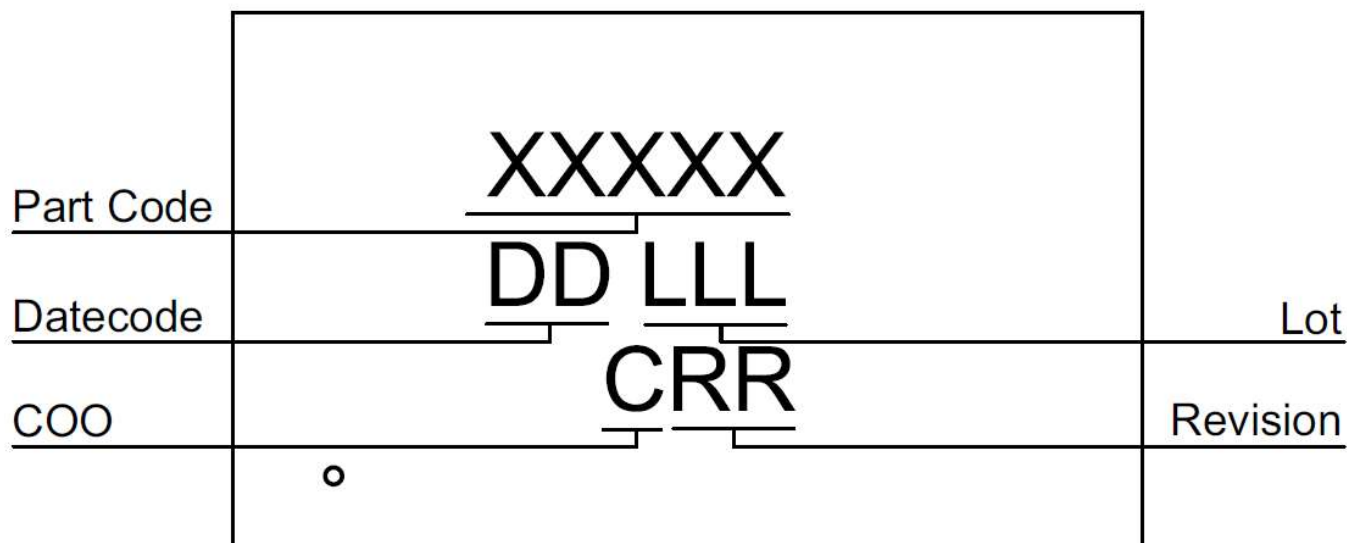
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R _{PULL_UP}	Internal Pull Up Resistance	Pull up on PINs 12, 13, 14, 15, 16, 17, 18	--	1	--	MΩ
R _{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PINs 3, 4, 5, 7	--	1	--	MΩ
T _{DLY0}	Delay time	At temperature +25°C	18.74	20.00	21.29	ms
		At temperature -40 +85°C (Note 3)	17.66	20.00	24.50	ms
T _{DLY1}	Delay time	At temperature +25°C	18.74	20.00	21.29	ms
		At temperature -40 +85°C (Note 3)	17.66	20.00	24.50	ms
T _{DLY2}	Delay time	At temperature +25°C	18.74	20.00	21.29	ms
		At temperature -40 +85°C (Note 3)	17.66	20.00	24.50	ms
T _{DLY3}	Delay time	At temperature +25°C	18.74	20.00	21.29	ms
		At temperature -40 +85°C (Note 3)	17.66	20.00	24.50	ms
T _{DLY4}	Delay time	At temperature +25°C	18.74	20.00	21.29	ms
		At temperature -40 +85°C (Note 3)	17.66	20.00	24.50	ms
T _{DLY5}	Delay time	At temperature +25°C	18.74	20.00	21.29	ms
		At temperature -40 +85°C (Note 3)	17.66	20.00	24.50	ms
T _{DLY6}	Delay time	At temperature +25°C	18.74	20.00	21.29	ms
		At temperature -40 +85°C (Note 3)	17.66	20.00	24.50	ms
V _{ACMP0}	Analog Comparator0 Threshold Voltage	Low to High transition, at temperature +25°C	--	--	2680	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	--	--	2697	mV
		High to Low transition, at temperature +25°C	2511	--	--	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	2446	--	--	mV
V _{ACMP1}	Analog Comparator1 Threshold Voltage	Low to High transition, at temperature +25°C	--	--	3409	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	--	--	3429	mV
		High to Low transition, at temperature +25°C	3180	--	--	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	3094	--	--	mV
T _{SU}	Startup Time	from VDD rising past P _{ON} _{THR}	--	0.3	--	ms
P _{ON} _{THR}	Power On Threshold	V _{DD} Level Required to Start Up the Chip	1.18	1.353	1.516	V
P _{OFF} _{THR}	Power Off Threshold	V _{DD} Level Required to Switch Off the Chip	0.73	0.914	1.103	V

Note:

1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 14, 15, 16, 17, 18, 19 and 20 to another.
3. Guaranteed by Design.

Package Top Marking



XXXXXX – Part ID Field: identifies the specific device configuration
 DD – Date Code Field: Coded date of manufacture
 LLL – Lot Code: Designates Lot #
 C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
 RR – Revision Code: Device Revision

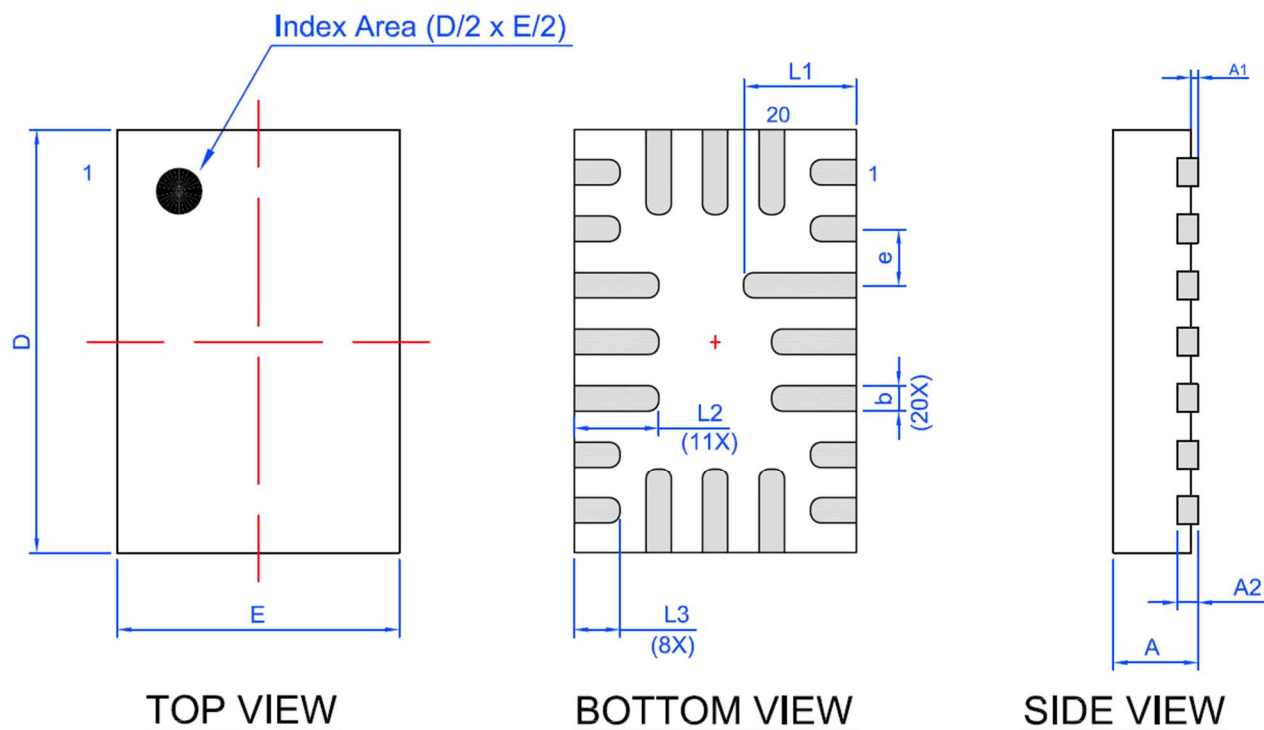
Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	002	U	0xE121335	50535	AA	08/04/2026

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

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Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P COL Package
JEDEC MO-220, Variation WECE



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

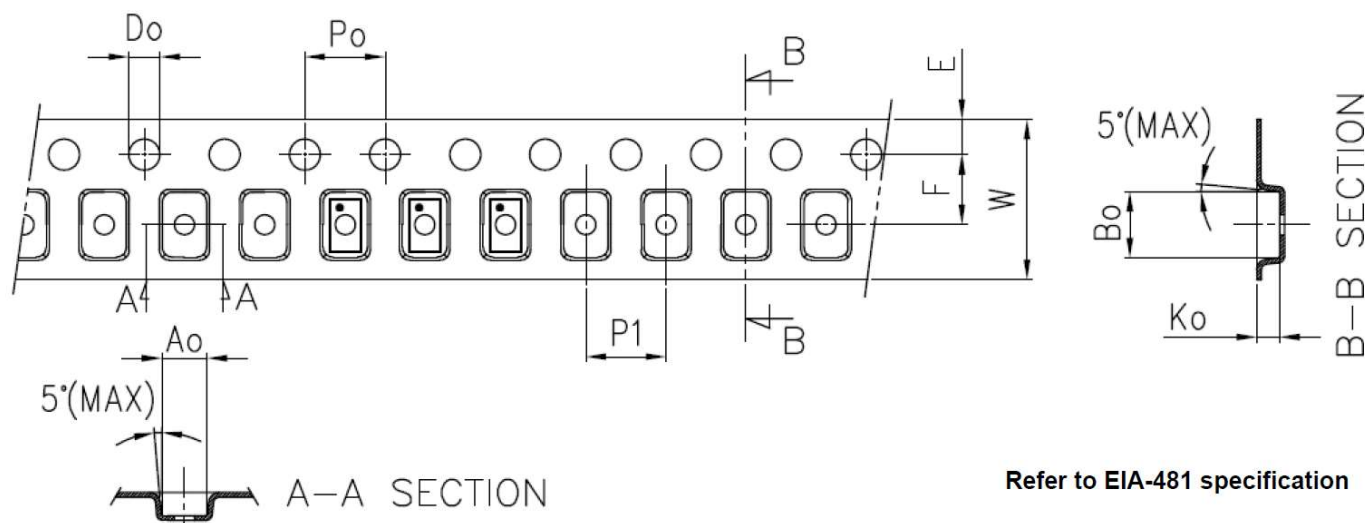
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Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm³ (nominal). More information can be found at www.jedec.org.

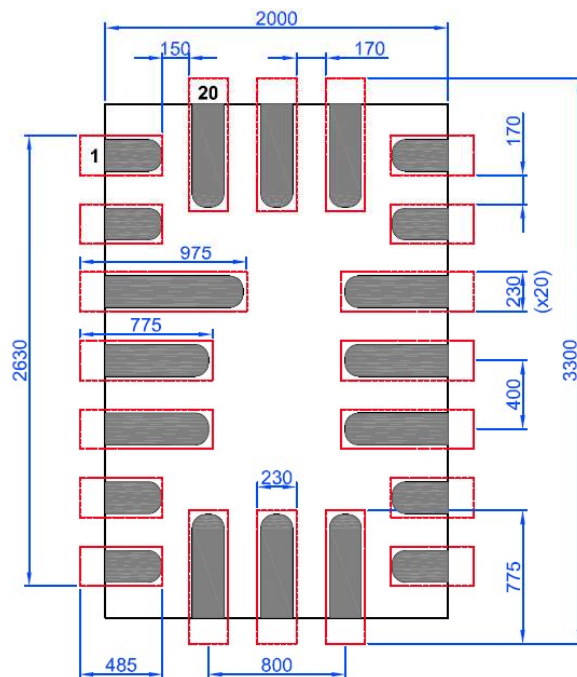
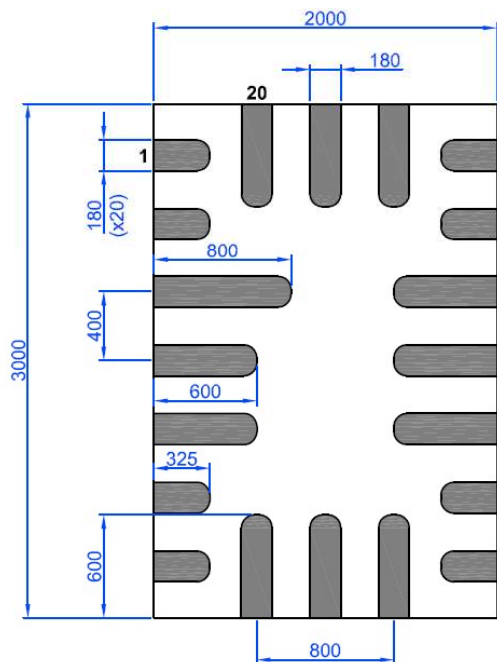
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Recommended Land Pattern

 Exposed Pad
(Top View)

 Recommended Land Pattern
(Top View)

Units: μm



Datasheet Revision History

Date	Version	Change
07/24/2026	0.10	New design
07/28/2026	0.11	Updated VDD range
08/01/2026	0.12	Updated DRS Table
08/04/2026	1.00	Production Release

