

3-Channel Power Sequencer

General Description

Overview

Renesas SLG7SQ50521 is a low power and small form device. The mixed-signal IC is housed in a 1.6mm x 2.0mm STQFN package which is optimal for using with small devices.

This device can be further customized to meet your specific application requirements. Custom designs can be created using the free GUI-based Go Configure™ Software Hub, available for download at [renesas.com](https://www.renesas.com), where example projects are also included. Contact your local Renesas representative or email greenpak@renesas.com for support.

Features

- Low Power Consumption
- RoHS Compliant / Halogen-Free
- 14-pin STQFN: 1.6 mm x 2.0 mm x 0.55 mm, 0.4 mm Pitch

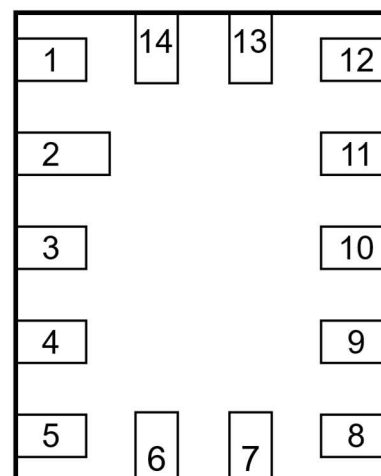
Output Summary

3 Outputs - Push Pull 1X

Pin Name

Pin #	Pin name	Pin #	Pin name
1	VDD	8	GND
2	NC	9	EN
3	SCL	10	FLAG3
4	SDA	11	FLAG2
5	NC	12	FLAG1
6	NC	13	NC
7	NC	14	NC

Pin Configuration



STQFN-14
(Top View)

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Pin Configuration

Pin	Pin Name	Type	Pin Description	Internal Resistors
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or connect to GND	--
3	SCL	Digital Input	Digital Input without Schmitt trigger	floating
4	SDA	Bi-directional	Digital Input without Schmitt trigger / Open Drain NMOS	floating
5	NC	--	Keep Floating or connect to GND	--
6	NC	--	Keep Floating or connect to GND	--
7	NC	--	Keep Floating or connect to GND	--
8	GND	GND	Ground	--
9	EN	Analog Input/Output	Analog Input/Output	floating
10	FLAG3	Digital Output	Push Pull 1X	floating
11	FLAG2	Digital Output	Push Pull 1X	floating
12	FLAG1	Digital Output	Push Pull 1X	floating
13	NC	--	Keep Floating or connect to GND	--
14	NC	--	Keep Floating or connect to GND	--

Ordering Information

Part number	Package type
SLG7SQ50521V	14-pin STQFN - Tape and Reel (3k units)

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Absolute Maximum Conditions

Parameter	Min	Max	Unit
Supply Voltage on V _{DD} relative to GND	-0.3	7	V
DC Input Voltage	GND - 0.5	V _{DD} + 0.5	V
Maximum Average or DC Current (Through V _{DD} or GND pin)	--	90	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	11	mA
Current at Input Pin	-1.0	1.0	mA
Input Leakage Current (Absolute Value)	--	1000	nA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{DD}	Supply Voltage		2.30	3.30	5.50	V
T _A	Operating Temperature		-40	25	85	°C
C _{VDD}	Capacitor Value at V _{DD}		0.1	--	--	μF
C _{IN}	Input Capacitance		--	4	--	pF
I _Q	Quiescent Current	Short Pin9 to GND, Pin3,4 to VDD and floating outputs	--	40	--	μA
V _O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V _{DD} +0.3	V
V _{IH}	HIGH-Level Input Voltage	Logic Input without Schmitt trigger (Note 1)	0.7xV _{DD}	--	V _{DD} +0.3	V
V _{IL}	LOW-Level Input Voltage	Logic Input without Schmitt trigger (Note 1)	GND-0.3	--	0.3xV _{DD}	V
V _{OH}	HIGH-Level Output Pulse Voltage	Push-Pull 1X, V _{DD} = 2.5 V ± 8%, I _{OH} = 1 mA	2.15	--	--	V
		Push-Pull 1X, V _{DD} = 3.3 V ± 10%, I _{OH} = 3 mA	2.70	--	--	V
		Push-Pull 1X, V _{DD} = 5 V ± 10%, I _{OH} = 5 mA	4.16	--	--	V
V _{OL}	LOW-Level Output Pulse Voltage	Push-Pull 1X, V _{DD} = 2.5 V ± 8%, I _{OL} = 1 mA	--	--	0.103	V
		Push-Pull 1X, V _{DD} = 3.3 V ± 10%, I _{OL} = 3 mA	--	--	0.218	V
		Push-Pull 1X, V _{DD} = 5 V ± 10%, I _{OL} = 5 mA	--	--	0.270	V
I _{OH}	HIGH-Level Output Pulse Current (Note 2)	Push-Pull 1X, V _{DD} = 2.5 V ± 8%, V _{OH} = V _{DD} - 0.2	1.37	--	--	mA
		Push-Pull 1X, V _{DD} = 3.3 V ± 10%, V _{OH} = 2.4 V	5.61	--	--	mA
		Push-Pull 1X, V _{DD} = 5 V ± 10%, V _{OH} = 2.4 V	20.42	--	--	mA
I _{OL}	LOW-Level Output Pulse Current (Note 2)	Push-Pull 1X, V _{DD} = 2.5 V ± 8%, V _{OL} = 0.15 V	1.52	--	--	mA
		Push-Pull 1X, V _{DD} = 3.3 V ± 10%, V _{OL} = 0.4 V	5.42	--	--	mA
		Push-Pull 1X, V _{DD} = 5 V ± 10%, V _{OL} = 0.4 V	7.36	--	--	mA
T _{DLY1}	Delay Time	At temperature +25 °C	11.53	11.96	13.44	ms
		At temperature -40 +85 °C (Note 3)	11.46	11.96	14.26	ms
T _{DLY2}	Delay Time	At temperature +25 °C	11.53	11.96	13.44	ms

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		At temperature -40 +85 °C (Note 3)	11.46	11.96	14.26	ms
T _{DLY3}	Delay Time	At temperature +25 °C	11.53	11.96	13.44	ms
		At temperature -40 +85 °C (Note 3)	11.46	11.96	14.26	ms
		At temperature +25 °C	11.53	11.96	13.44	ms
V _{ACMP0H}	Analog Comparator Threshold Voltage	Low to High transition, at temperature +25 °C	1225	--	1263	mV
		Low to High transition, at temperature -40 +85 °C (Note 3)	1223	--	1263	mV
		High to Low transition, at temperature +25 °C	1225	--	1263	mV
		High to Low transition, at temperature -40 +85 °C (Note 3)	1223	--	1263	mV
T _{SU}	Startup Time	From V _{DD} rising past PON _{THR}	--	1	2	ms
PON _{THR}	Power-On Threshold	V _{DD} Level Required to Start Up the Chip	1.6	1.85	2.05	V
POFF _{THR}	Power-Off Threshold	V _{DD} Level Required to Switch Off the Chip	0.85	1.25	1.5	V

Note 1 No hysteresis.

Note 2 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

Note 3 Guaranteed by Design.

I²C Specifications

Parameter	Description	Condition	Min	Typ	Max	Unit
F _{SCL}	Clock Frequency, SCL		--	--	400	kHz
t _{LOW}	Clock Pulse Width Low		1300	--	--	ns
t _{HIGH}	Clock Pulse Width High		600	--	--	ns
t _i	Input Filter Spike Suppression (SCL, SDA)	V _{DD} = 2.5 V ± 8%	--	--	95	ns
		V _{DD} = 3.3 V ± 10%	--	--	95	ns
		V _{DD} = 5.0 V ± 10%	--	--	111	ns
t _{AA}	Clock Low to Data Out Valid		--	--	900	ns
t _{BUF}	Bus Free Time between Stop and Start		1300	--	--	ns
t _{HD_STA}	Start Hold Time		600	--	--	ns
t _{SU_STA}	Start Set-up Time		600	--	--	ns
t _{HD_DAT}	Data Hold Time		0	--	--	ns
t _{SU_DAT}	Data Set-up Time		100	--	--	ns
t _R	Inputs Rise Time		--	--	300	ns
t _F	Inputs Fall Time		--	--	300	ns
t _{SU_STO}	Stop Set-up Time		600	--	--	ns
t _{DH}	Data Out Hold Time		50	--	--	ns

Chip Address

HEX	BIN	DEC
0x08	0001000	8

I2C Description

I2C Serial Communications Device Addressing

Each command to the I2C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code. Each bit in a control code can be sourced independently from the register or by value defined externally by GPIO, GPIO5, GPIO4, and GPIO2. The LSB of the control code is defined by the value of GPIO, while the MSB is defined by the value of GPIO5. The address source (either register bit or Pin) for each bit in the control code is defined by registers [2027:2024]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I2C bus. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the $R/\overline{W}$ bit, which selects whether a read command or write command is requested, with a “1” selecting for a Read command, and a “0” selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I2C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device chooses to set the Control Code to either “1111” or “0000” in a system with other target device, please consult the I2C-bus specification and user manual to understand the addressing and implementation of these special functions, to ensure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I2C Macrocell on the SLG7SQ50521 are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9, and A8) will be “0” for all commands to the SLG7SQ50521.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. Figure 1 shows this basic command structure.

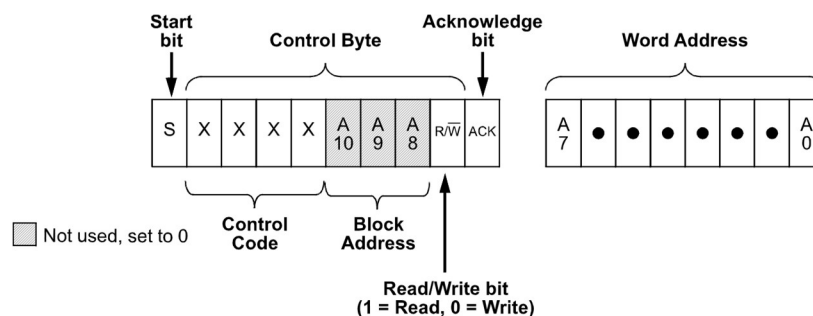


Figure 1. Basic Command Structure

I2C Serial General Timing

General timing characteristics for the I2C Serial Communications macrocell are shown in Figure 2. Timing specifications can be found in I2C Specifications section.

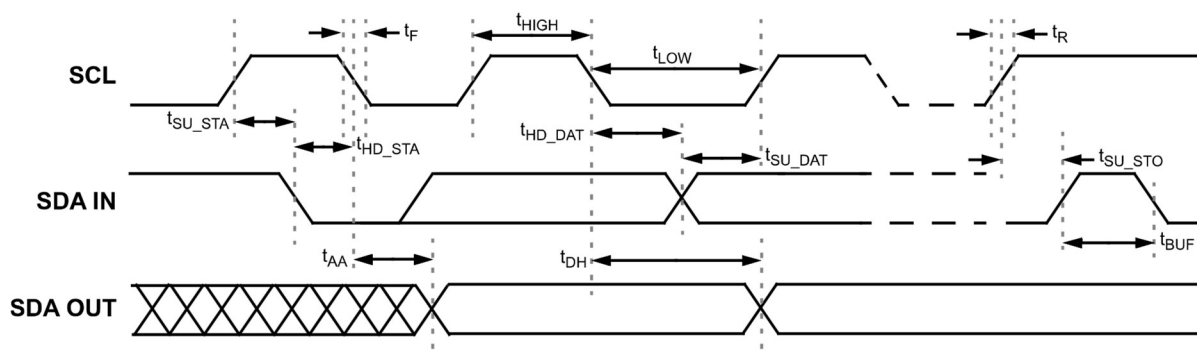


Figure 2. I²C General Timing Characteristics

Byte Write Command

Following the Start condition from the Controller, the Control Code [4 bits], the Block Address [3 bits], and the $\overline{R/\overline{W}}$ bit (set to "0") are placed onto the I²C bus by the Controller. After the SLG7SQ50521 sends an Acknowledge bit (ACK), the next byte transmitted by the Controller is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG7SQ50521, where the data byte is to be written. After the SLG7SQ50521 sends another Acknowledge bit, the Controller will transmit the data byte to be written into the addressed memory location. The SLG7SQ50521 again provides an Acknowledge bit and then the Controller generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7SQ50521 generates the Acknowledge bit.

It is possible to LATCH all IOs during I²C write command, register [1961] = 1 - Enable. It means that IOs will remain their state until the write command is done.

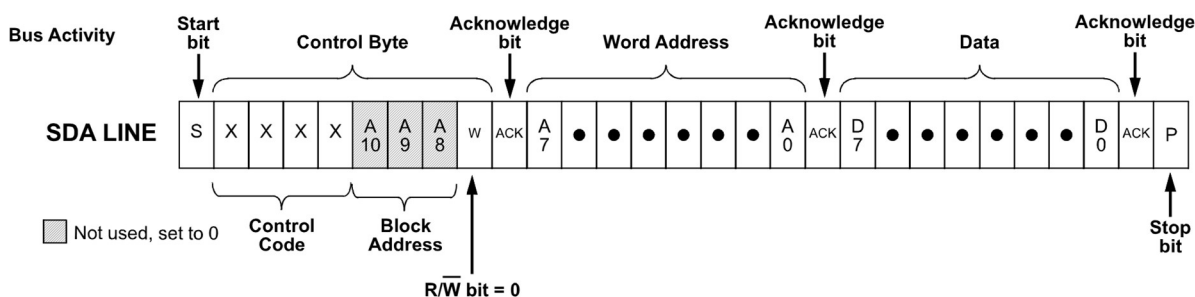


Figure 3. Byte Write Command, $\overline{R/\overline{W}} = 0$

Random Read Command

The Random Read Command starts with a Control Byte (with $\overline{R/\overline{W}}$ bit set to "0", indicating a Write Command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Controller issues a second control byte with the $\overline{R/\overline{W}}$ bit set to "1", after which the SLG7SQ50521 issues an Acknowledge bit, followed by the requested eight data bits.

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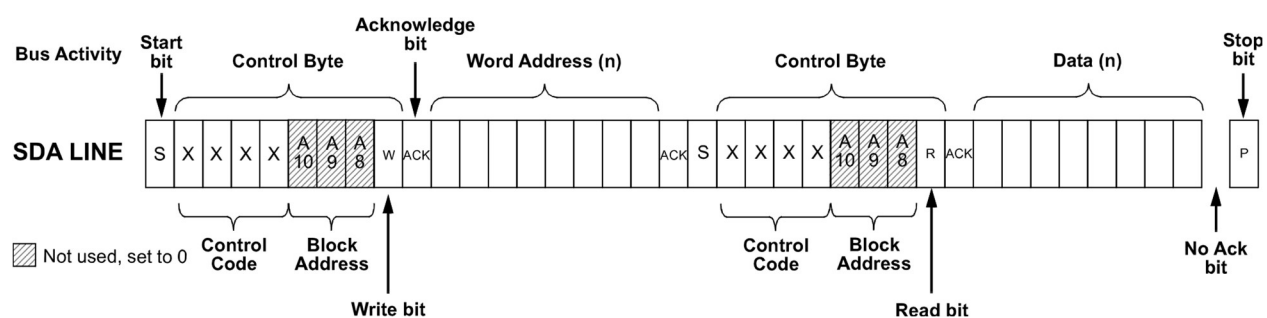
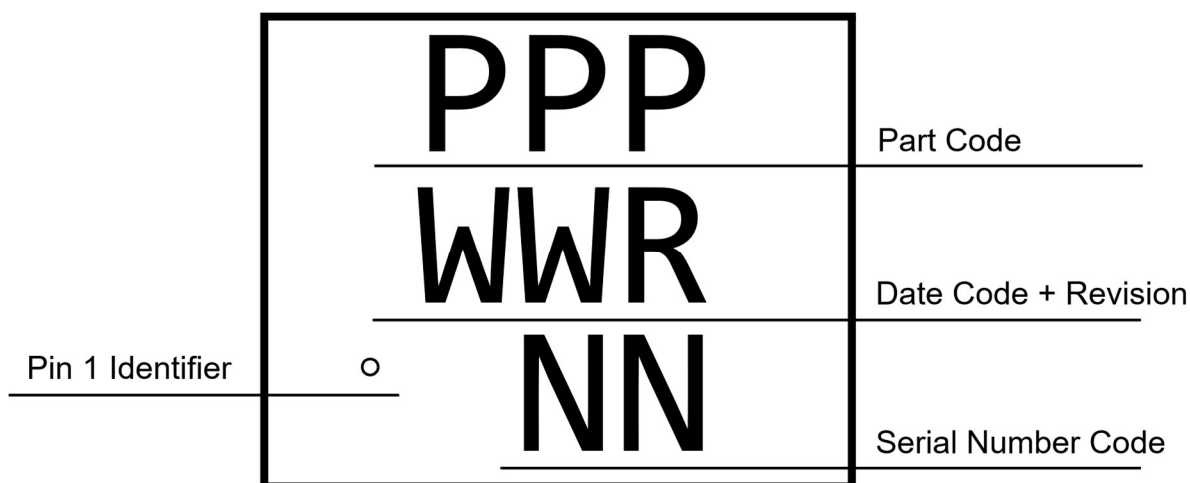


Figure 4. Random Read Command

Package Top Marking



Datasheet revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	001	U	0x359B7DD	1XA	A	08/07/2026

Memory Lock Options

Option	Status
Registers	Unlocked

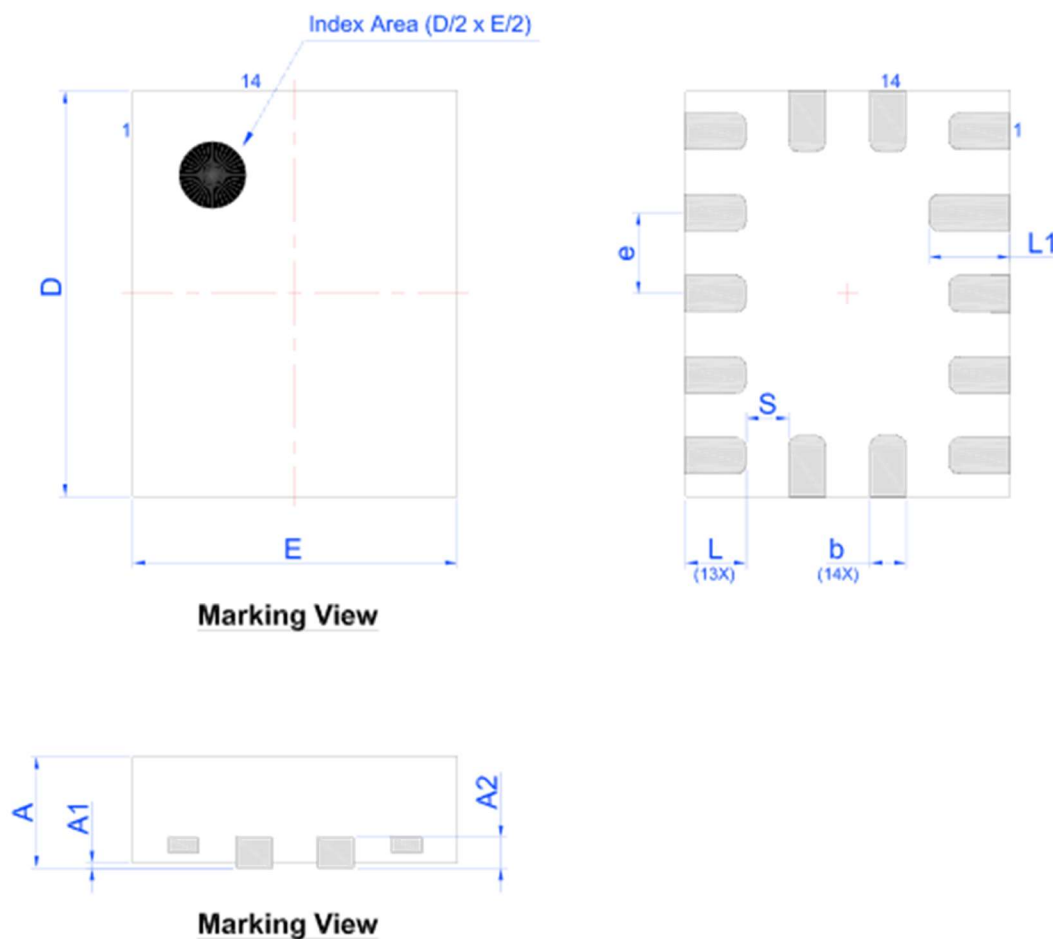
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

Package Outlines for STQFN 14L 1.6 mm x 2.0 mm x 0.55 mm 0.4P FC Package

JEDEC MO-220

IC Net Weight: 0.0045 g



Unit: mm

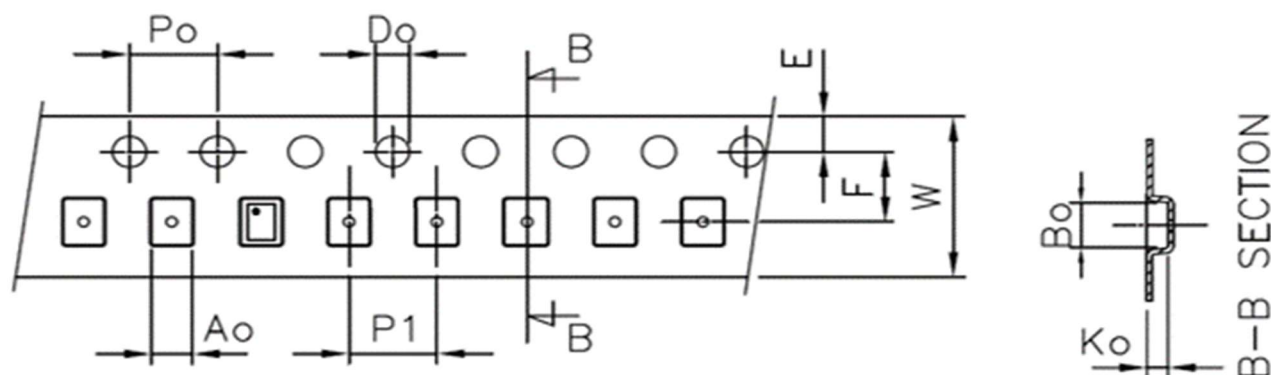
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.95	2.00	2.05
A1	0.005	-	0.050	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.35	0.40	0.45
e	0.40 BSC			S	0.21 REF		

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
STQFN 14L 1.6 mm x 2 mm 0.4P FC Green	14	1.6x2.0x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

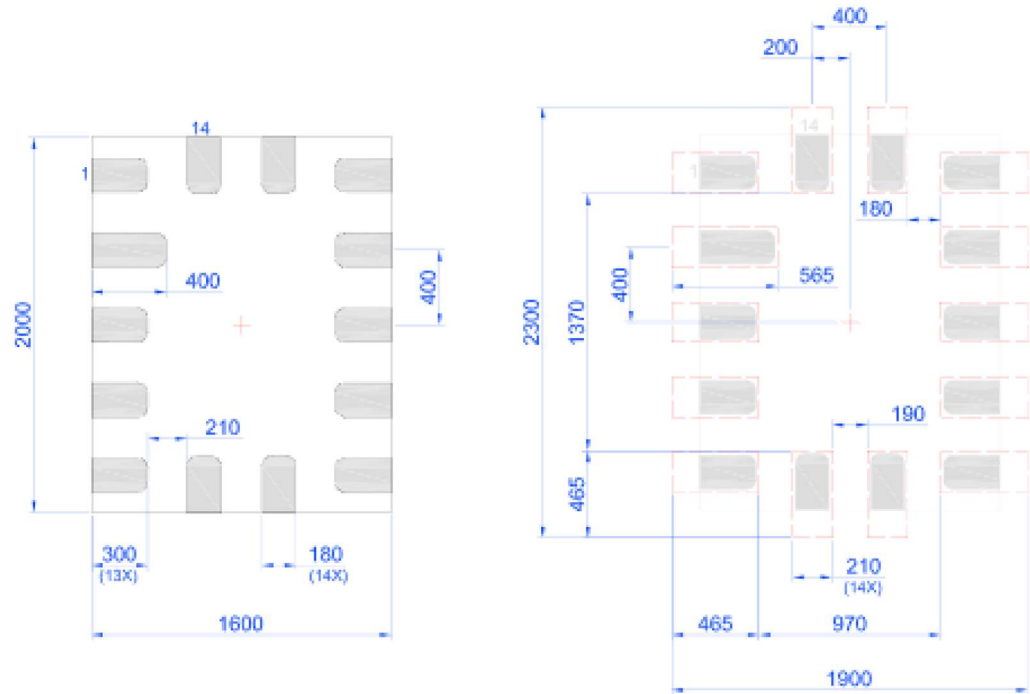
Package Type	Pocket BTM length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 1.6 mm x 2 mm 0.4P FC Green	1.8 ± 0.05	2.2 ± 0.05	0.76	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm³ (nominal) for STQFN 14L Package. More information can be found at www.jedec.org.

Recommended Land Pattern



Unit: μm

Datasheet Revision History

Date	Version	Change
07/21/2026	0.10	New Design
08/06/2026	0.11	Updated Device Revision Table
08/07/2026	1.00	Production Release