

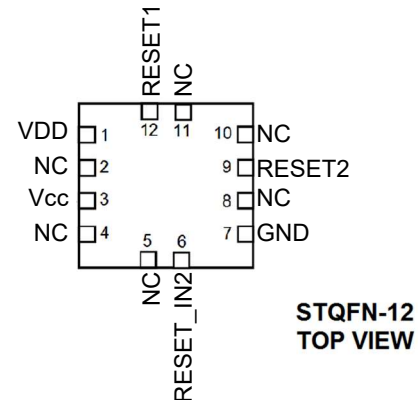
Dual Reset Voltage Monitor

General Description

Renesas SLG7SQ50520 is a low power and small form device. The mixed-signal IC is housed in a 1.6mm x 1.6mm STQFN package which is optimal for using with small devices.

This device can be further customized to meet your specific application requirements. Custom designs can be created using the free GUI-based Go Configure™ Software Hub, available for download at [renesas.com](https://www.renesas.com), where example projects are also included. Contact your local Renesas representative or email greenpak@renesas.com for support.

Pin Configuration



Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 12 Package

Output Summary

2 Outputs - Push Pull 1X

Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	Vcc	Analog Input/Output	Analog Input/Output	floating
4	NC	--	Keep Floating or Connect to GND	--
5	NC	--	Keep Floating or Connect to GND	--
6	RESET_IN2	Analog Input/Output	Analog Input/Output	floating
7	GND	GND	Ground	--
8	NC	--	Keep Floating or Connect to GND	--
9	RESET2	Digital Output	Push Pull 1X	floating
10	NC	--	Keep Floating or Connect to GND	--
11	NC	--	Keep Floating or Connect to GND	--
12	RESET1	Digital Output	Push Pull 1X	floating

Ordering Information

Part Number	Package Type
SLG7SQ50520V	STQFN-12 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	12	mA
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1000	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		1.71	3.3	5.5	V
T _A	Operating Temperature		-40	25	85	°C
C _{VDD}	Capacitor Value at VDD		--	0.1	--	μF
C _{IN}	Input Capacitance		--	4	--	pF
I _Q	Quiescent Current	Static inputs and floating outputs PIN3 and PIN6 to GND	--	110	--	μA
V _O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD + 0.3	V
I _{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T _J = 85 °C	--	--	73	mA
		T _J = 110 °C	--	--	35	mA
I _{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T _J = 85 °C	--	--	92	mA
		T _J = 110 °C	--	--	44	mA
V _{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I _{OH} = 100 μA, at VDD = 1.8 V ± 5 %	1.68	1.79	--	V
		Push-Pull 1X, Open Drain PMOS 1X, I _{OH} = 3 mA, at VDD = 3.3 V ± 10 %	2.71	3.09	--	V
		Push-Pull 1X, Open Drain PMOS 1X, I _{OH} = 5 mA, at VDD = 5.0 V ± 10 %	4.15	4.73	--	V
V _{OL}	LOW-Level Output Voltage	Push-Pull 1X, I _{OL} = 100 μA, at VDD = 1.8 V ± 5 %	--	0.02	0.03	V
		Push-Pull 1X, I _{OL} = 3 mA, at VDD = 3.3 V ± 10 %	--	0.18	0.28	V
		Push-Pull 1X, I _{OL} = 5 mA, at VDD = 5.0 V ± 10 %	--	0.23	0.33	V
I _{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V _{OH} = VDD - 0.2 V, at VDD = 1.8 V ± 5 %	1.04	1.4	--	mA
		Push-Pull 1X, Open Drain PMOS 1X, V _{OH} = 2.4 V, at VDD = 3.3 V ± 10 %	5.83	10.18	--	mA
		Push-Pull 1X, Open Drain PMOS 1X, V _{OH} = 2.4 V, at VDD = 5.0 V ± 10 %	21.808	29.1	--	mA

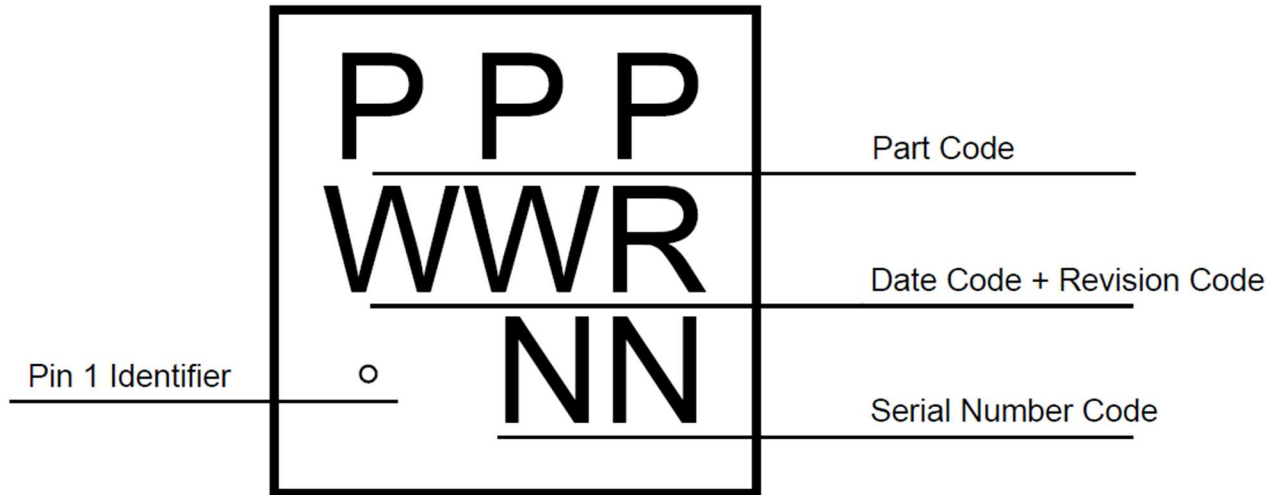
Dual Reset Voltage Monitor

I _{OL}	LOW-Level Output Current (Note 1)	Push-Pull 1X, V _{OL} = 0.15 V, at VDD = 1.8 V ± 5 %	0.76	1.34	--	mA
		Push-Pull 1X, V _{OL} = 0.4 V, at VDD = 3.3 V ± 10 %	4.06	6.44	--	mA
		Push-Pull 1X, V _{OL} = 0.4 V, at VDD = 5.0 V ± 10 %	6.01	9.73	--	mA
T _{DLY2}	Delay time	At temperature +25°C	7.64	12.00	17.40	µs
		At temperature -40 +85°C (Note 3)	7.42	12.00	22.10	µs
T _{DLY3}	Delay time	At temperature +25°C	11.46	16.00	21.76	µs
		At temperature -40 +85°C (Note 3)	11.14	16.00	27.62	µs
V _{ACMP0}	Analog Comparator0 Threshold Voltage	Low to High transition, at temperature +25°C	1563	--	1739	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	1521	--	1749	mV
		High to Low transition, at temperature +25°C	1559	--	1735	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	1513	--	1744	mV
V _{ACMP1}	Analog Comparator1 Threshold Voltage	Low to High transition, at temperature +25°C	560	--	643	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	544	--	647	mV
		High to Low transition, at temperature +25°C	560	--	637	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	545	--	642	mV
T _{SU}	Startup Time	From VDD rising past PON _{THR}	--	0.27	--	ms
PON _{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	1.182	1.346	1.505	V
POFF _{THR}	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.752	0.918	1.11	V

Note:

1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.
3. Guaranteed by Design.

Package Top Marking

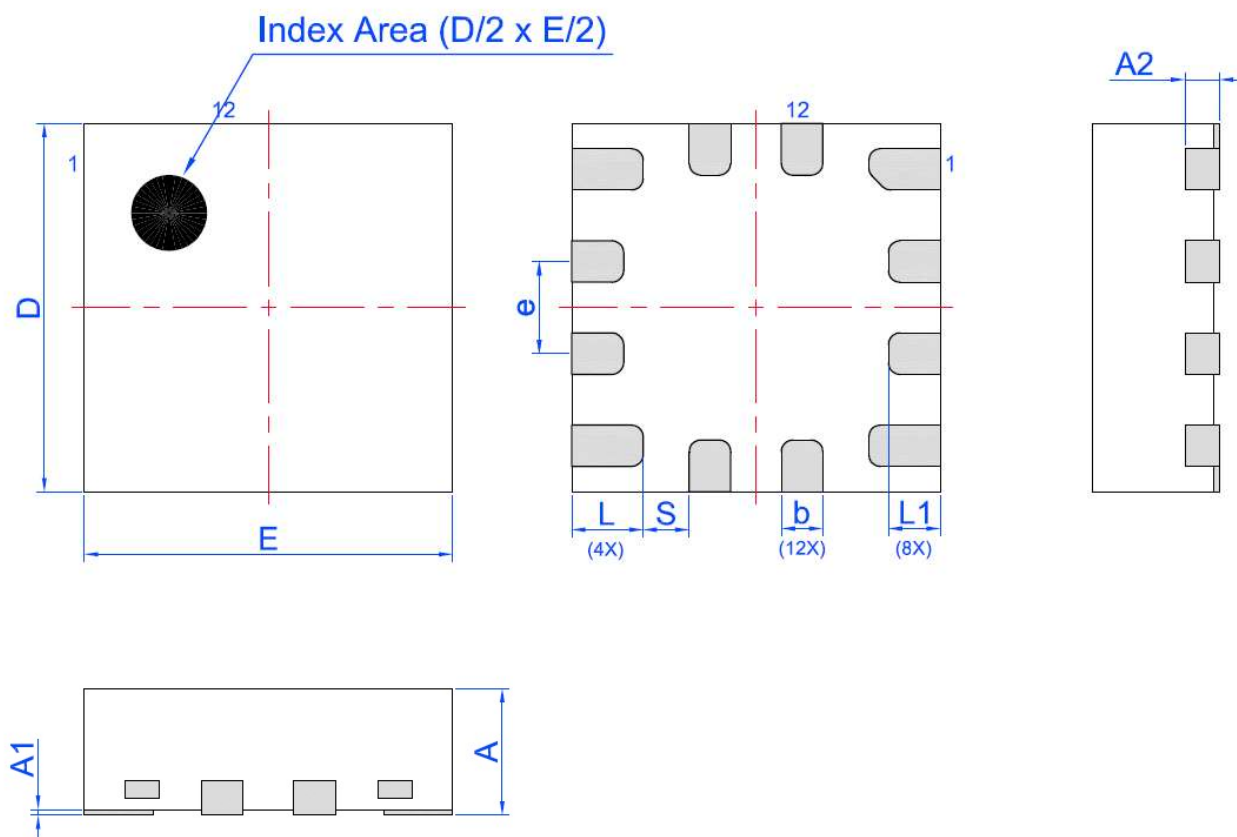


Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	001	U	0x9016E700	1X4	A	07/29/2026

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

12 Lead STQFN FC Package 1.6 x 1.6 mm
IC net weight: 0.0028 g



Unit: mm

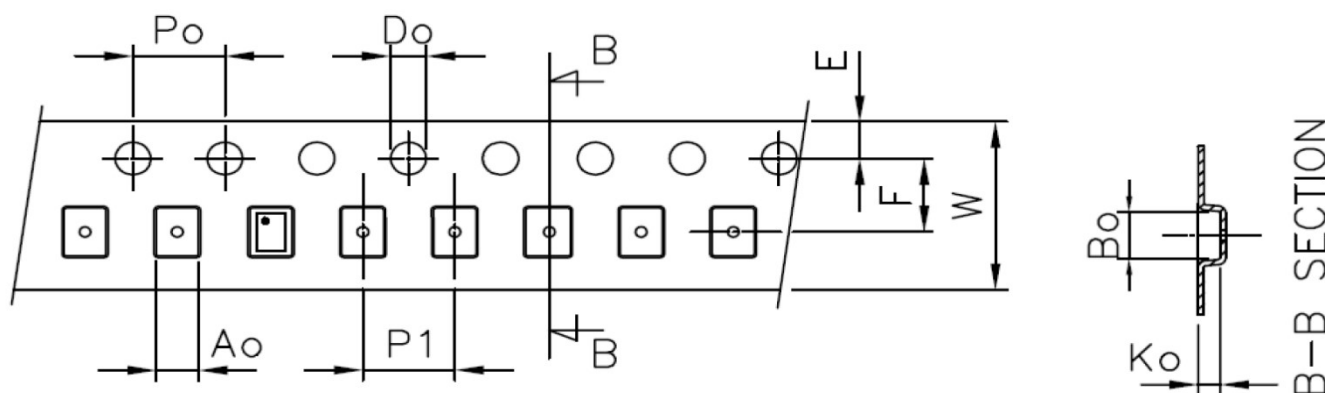
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.26	0.31	0.36
b	0.13	0.18	0.23	L1	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 12L FC 0.4P Green	12	1.6x1.6x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L FC 0.4P Green	1.9	1.9	0.8	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

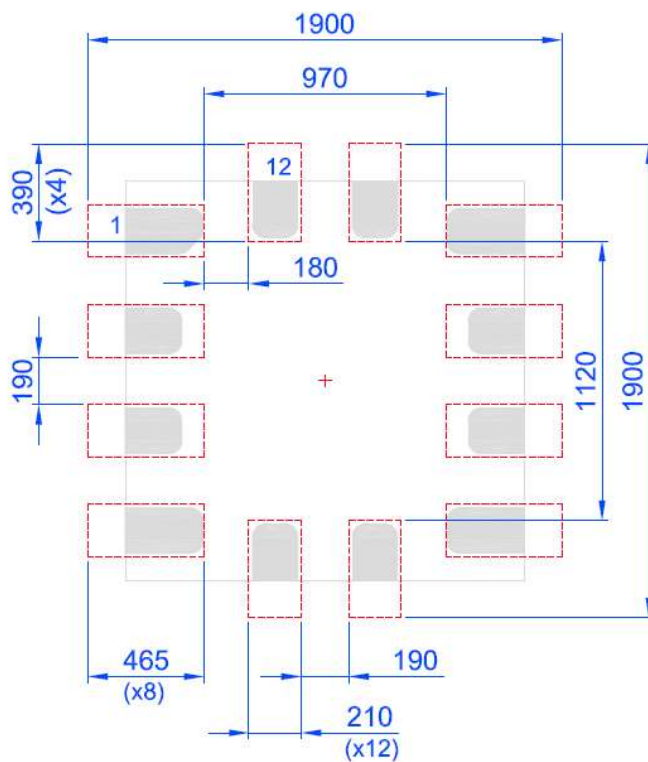
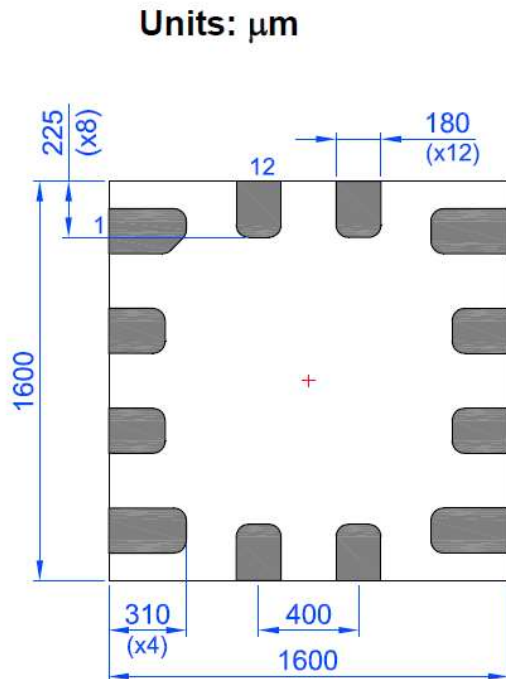
Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.408 mm³ (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern

 Exposed Pad
(PKG face down)

 Recommended Land Pattern
(PKG face down)

Units: μm



Datasheet Revision History

Date	Version	Change
07/21/2026	0.10	New design
07/28/2026	0.11	Updated Device Revision Table
07/29/2026	1.00	Production Release

