

General Purpose Watchdog timer (Push-Pull output)

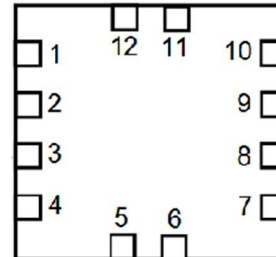
General Description

Renesas SLG7RN47285 is a low power and small form device. The SoC is housed in a 2mm x 2mm STQFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 12 Package

Pin Configuration



**STQFN-12
TOP VIEW**

Output Summary

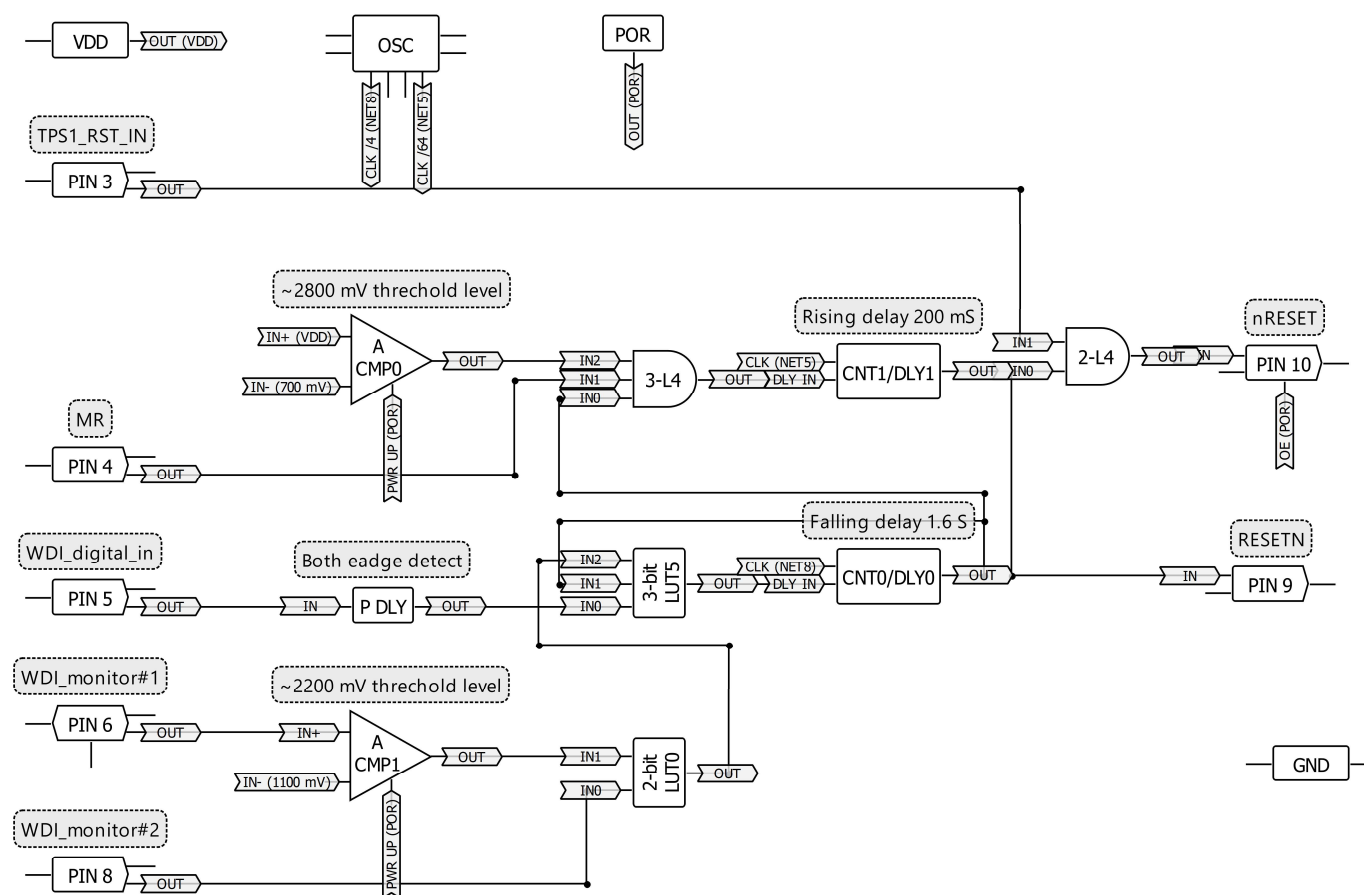
2 Outputs - Push Pull 1X

Pin Name

Pin #	Pin name	Pin #	Pin name
1	VDD	7	GND
2	NC	8	WDI_monitor#2
3	TPS1_RST_IN	9	RESETN
4	MR	10	nRESET
5	WDI_digital_in	11	NC
6	WDI_monitor#1	12	NC

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Block Diagram



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Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	TPS1_RST_IN	Digital Input	Digital Input without Schmitt trigger	100kΩ pullup
4	MR	Digital Input	Digital Input without Schmitt trigger	100kΩ pullup
5	WDI_digital_in	Digital Input	Low Voltage Digital Input	floating
6	WDI_monitor#1	Analog Input/Output	Analog Input/Output	100kΩ pullup
7	GND	GND	Ground	--
8	WDI_monitor#2	Digital Input	Low Voltage Digital Input	100kΩ pulldown
9	RESETN	Digital Output	Push Pull 1X	floating
10	nRESET	Digital Output	Push Pull 1X	floating
11	NC	--	Keep Floating or Connect to GND	--
12	NC	--	Keep Floating or Connect to GND	--

Ordering Information

Part Number	Package Type
SLG7RN47285P	12-pin STQFN - Tape and Reel (3k units)

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Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5	VDD + 0.5	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	12	mA
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	° C
Junction Temperature		--	150	° C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1000	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		1.71	3.3	3.6	V
T _A	Operating Temperature		-40	25	85	°C
C _{VDD}	Capacitor Value at VDD		--	0.1	--	μF
C _{IN}	Input Capacitance		--	4	--	pF
I _Q	Quiescent Current	Static inputs and floating outputs	--	75	--	μA
V _O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD + 0.3	V
I _{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T _J = 85 °C	--	--	73	mA
		T _J = 110 °C	--	--	35	mA
I _{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T _J = 85 °C	--	--	92	mA
		T _J = 110 °C	--	--	44	mA
V _{IH}	HIGH-Level Input Voltage	Logic Input at VDD = 1.8 V	1.100	--	VDD	V
		Logic Input at VDD = 3.3 V	1.780	--	VDD	V
		Low-Level Logic Input at VDD = 1.8 V	0.980	--	VDD	V
		Low-Level Logic Input at VDD = 3.3 V	1.130	--	VDD	V
V _{IL}	LOW-Level Input Voltage	Logic Input at VDD = 1.8 V	--	--	0.690	V
		Logic Input at VDD = 3.3 V	--	--	1.210	V
		Low-Level Logic Input at VDD = 1.8 V	--	--	0.520	V
		Low-Level Logic Input at VDD = 3.3 V	--	--	0.690	V
V _{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I _{OH} = 100 μA, at VDD = 1.8 V	1.680	1.790	--	V
		Push-Pull 1X, Open Drain PMOS 1X, I _{OH} = 3 mA, at VDD = 3.3 V	2.720	3.090	--	V

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V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, $I_{OL} = 100 \mu A$, at $V_{DD} = 1.8 V$	--	0.020	0.030	V
		Push-Pull 1X, $I_{OL} = 3 mA$, at $V_{DD} = 3.3 V$	--	0.180	0.280	V
I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD} - 0.2 V$, at $V_{DD} = 1.8 V$	1.000	1.390	--	mA
		Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = 2.4 V$, at $V_{DD} = 3.3 V$	6.010	10.150	--	mA
I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 1X, $V_{OL} = 0.15 V$, at $V_{DD} = 1.8 V$	0.760	1.340	--	mA
		Push-Pull 1X, $V_{OL} = 0.4 V$, at $V_{DD} = 3.3 V$	4.060	6.440	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PINs 3, 4, 6	--	100	--	k Ω
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PIN 8	--	100	--	k Ω
T_{DLY0}	Delay time	At temperature +25°C	1.48	1.60	1.70	s
		At temperature -40 +85°C (Note 3)	1.38	1.60	2.00	s
T_{DLY1}	Delay time	At temperature +25°C	182.46	199.68	213.92	ms
		At temperature -40 +85°C (Note 3)	170.95	199.68	251.90	ms
V_{ACMP0}	Analog Comparator0 Threshold Voltage	Low to High transition, at temperature +25°C	2714	--	2958	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	2610	--	3006	mV
		High to Low transition, at temperature +25°C	2630	--	2866	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	2545	--	2903	mV
V_{ACMP1}	Analog Comparator1 Threshold Voltage	Low to High transition, at temperature +25°C	2115	--	2319	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	2039	--	2356	mV
		High to Low transition, at temperature +25°C	2074	--	2278	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	2012	--	2308	mV
V_{HYST}	Analog Comparator Hysteresis Voltage (Note 3)	ACMP 0 at temperature +25 °C	--	25	--	mV
		ACMP 0 at temperature -40 +85°C (Note 3)	--	25	--	mV
		ACMP 1 at temperature +25 °C	--	25	--	mV
		ACMP 1 at temperature	--	25	--	mV

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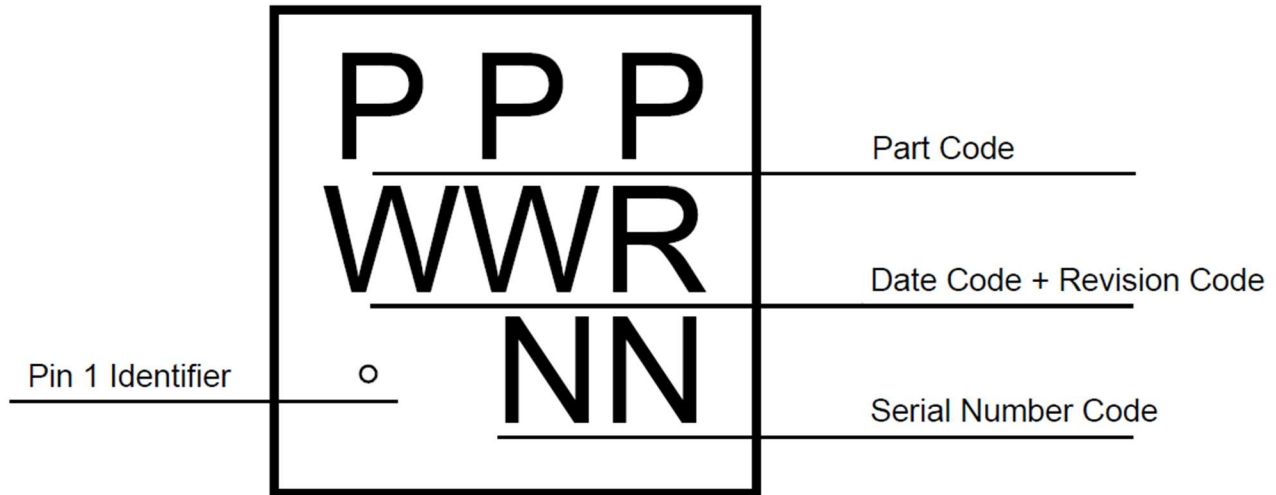
		-40 +85°C (Note 3)				
T _{SU}	Startup Time	From VDD rising past PON _{THR}	--	0.31	--	ms
PON _{THR}	Power On Threshold	V _{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
POFF _{THR}	Power Off Threshold	V _{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V

Note:

1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10, 11 and 12 to another.
3. Guaranteed by Design.

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Package Top Marking

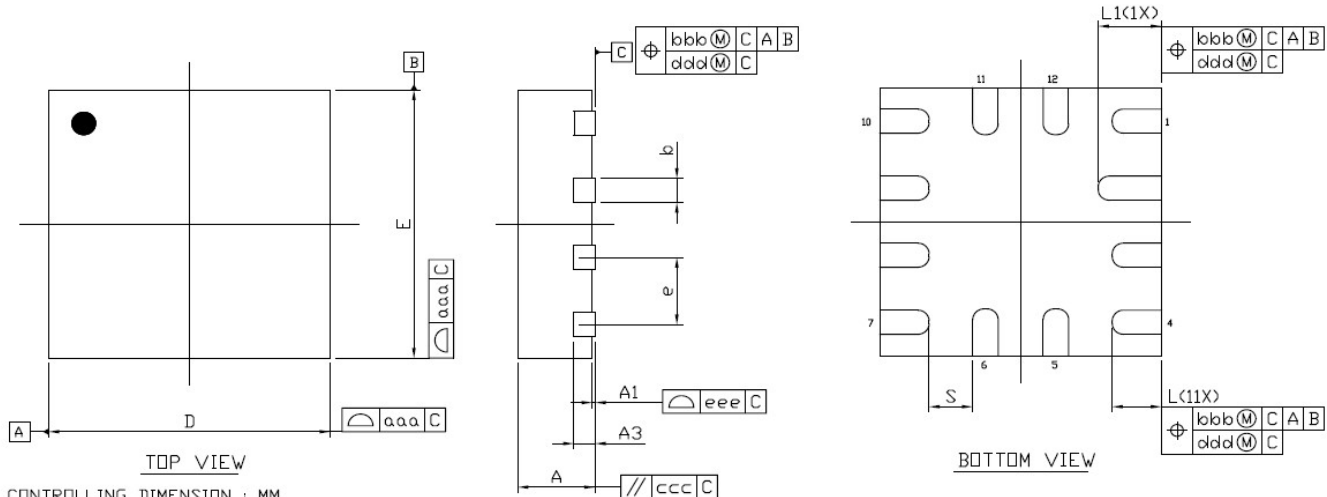


Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	001	L	0x36DA57F2	1FX	B	10/07/2025

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

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Package Drawing and Dimensions



A1 MAX LEAD COPLANARITY 0.05mm
STANDARD TOLERANCE : ±0.05

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

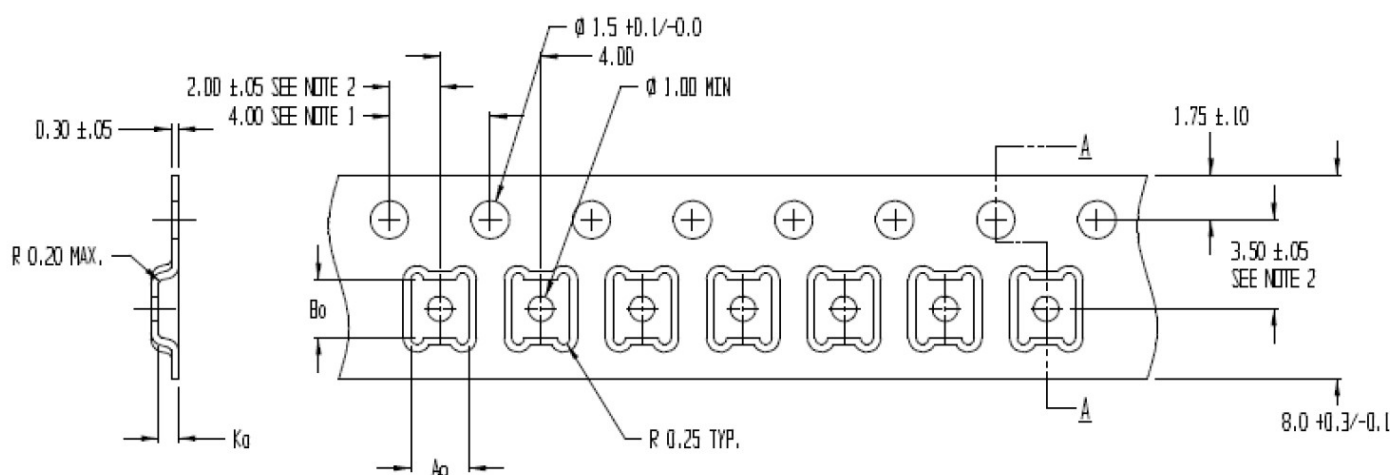
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Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 12L FCA 0.5P Green	10	2x2x0.55	3000	3000	7'-2.4'hub	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L FCA 0.5P Green	2.3	2.3	0.8	4	4	1.5	1.75	3.5	8



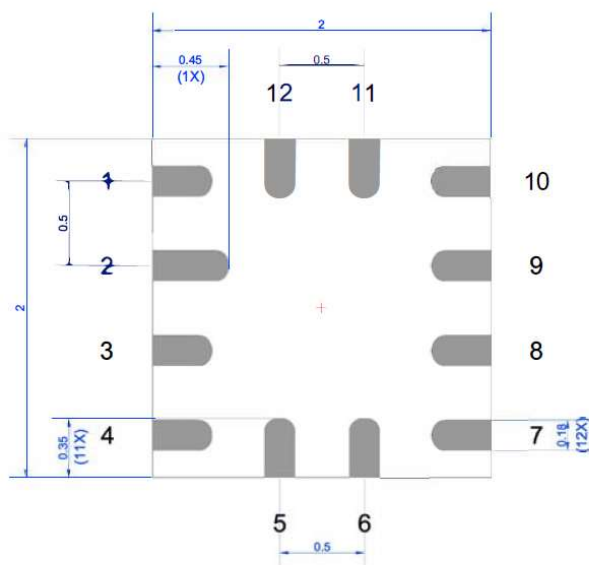
Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.2 mm³ (nominal). More information can be found at www.jedec.org.

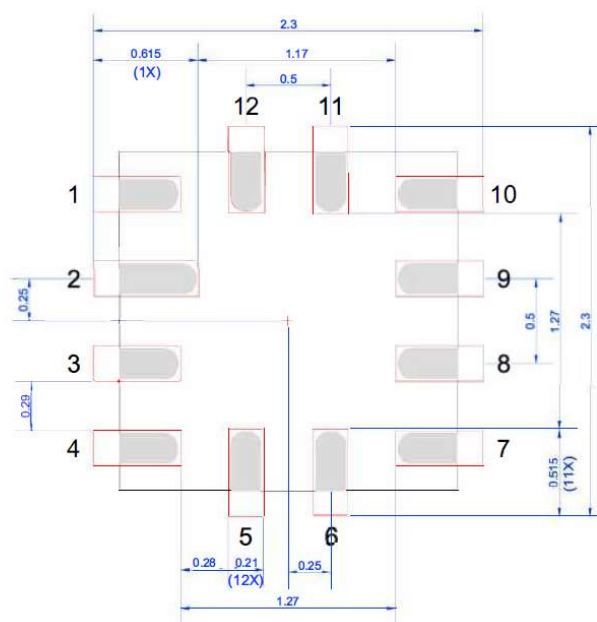
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Recommended Land Pattern

Expose Pad 
(Package face down)



Recommended Landing Pattern 
(Package face down)



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Datasheet Revision History

Date	Version	Change
01/23/2024	0.10	New design
01/25/2024	0.11	Updated Device Revision Table
09/30/2025	0.12	Lock the design
10/03/2025	0.13	Updated Device Revision Table
10/07/2025	1.00	Production Release