SLG7RN46610

GreenPAK ™

RZ/N2L reference design

General Description

Renesas SLG7RN46610 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

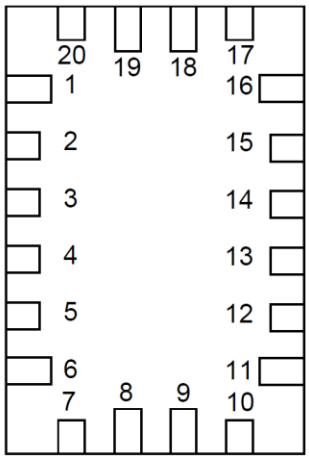
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

Output Summary

3 Outputs - Open Drain NMOS 1X
1 Output - Push Pull 1X

Pin Configuration

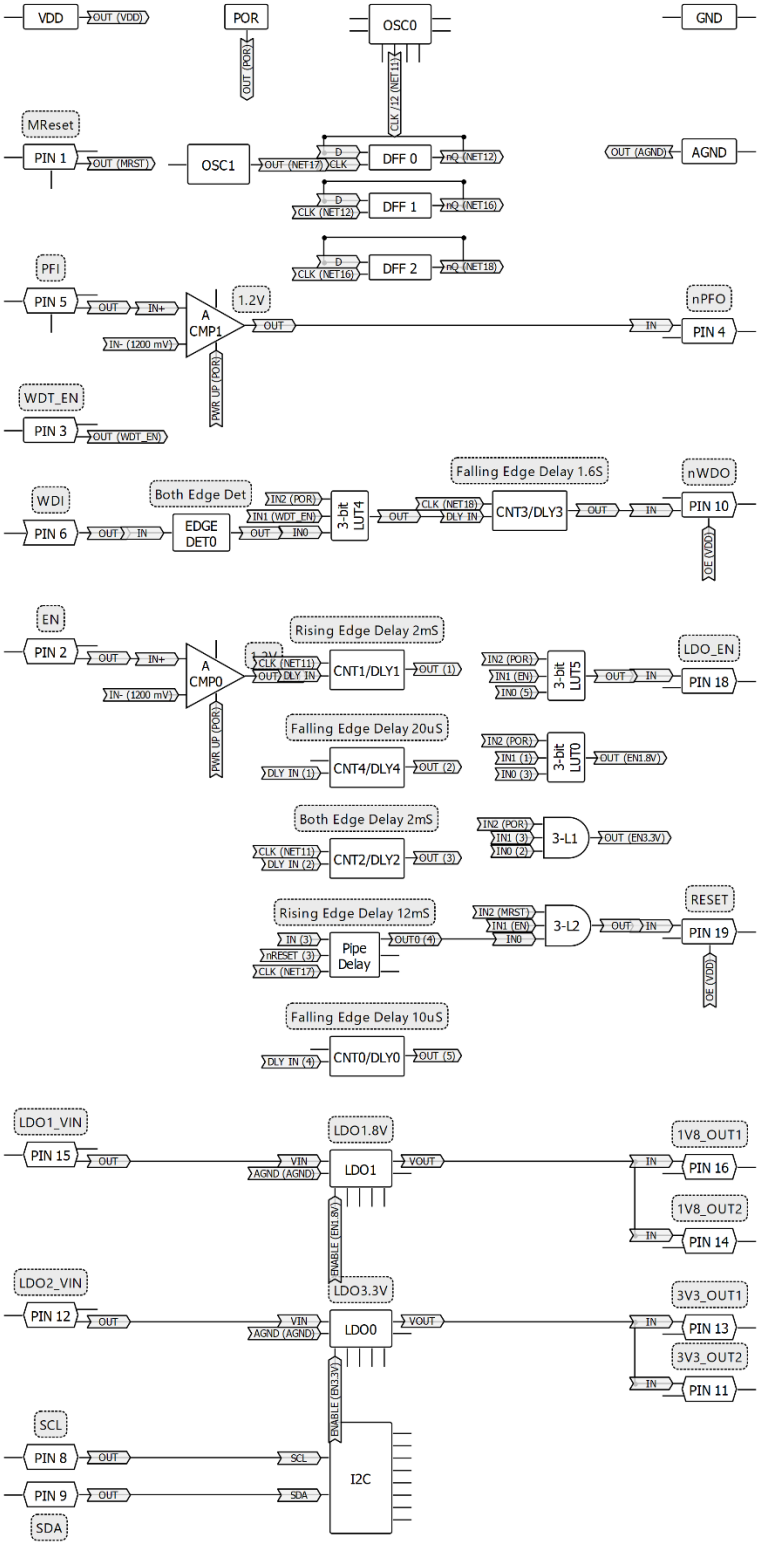


STQFN-20
(Top view)

Pin name

Pin #	Pin name	Pin #	Pin name
1	MReset	11	3V3_OUT2
2	EN	12	LDO2_VIN
3	WDT_EN	13	3V3_OUT1
4	nPFO	14	1V8_OUT2
5	PFI	15	LDO1_VIN
6	WDI	16	1V8_OUT1
7	VDD	17	AGND
8	SCL	18	LDO_EN
9	SDA	19	RESET
10	nWDO	20	GND

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	MReset	Digital Input	Digital Input without Schmitt trigger	100kΩ pullup
2	EN	Analog Input/Output	Analog Input/Output	floating
3	WDT_EN	Digital Input	Digital Input without Schmitt trigger	100kΩ pulldown
4	nPFO	Digital Output	Open Drain NMOS 1X	floating
5	PFI	Analog Input/Output	Analog Input/Output	floating
6	WDI	Digital Input	Digital Input without Schmitt trigger	100kΩ pulldown
7	VDD	PWR	Supply Voltage	--
8	SCL	Digital Input	Digital Input without Schmitt trigger	floating
9	SDA	Digital Input	Digital Input without Schmitt trigger	floating
10	nWDO	Digital Output	Open Drain NMOS 1X	floating
11	3V3_OUT2	Analog Output	LDO0 VOUT Analog Output	floating
12	LDO2_VIN	Analog Input	LDO0 VIN Analog Input	floating
13	3V3_OUT1	Analog Output	LDO0 VOUT Analog Output	floating
14	1V8_OUT2	Analog Output	LDO1 VOUT Analog Output	floating
15	LDO1_VIN	Analog Input	LDO1 VIN Analog Input	floating
16	1V8_OUT1	Analog Output	LDO1 VOUT Analog Output	floating
17	AGND	AGND	Ground	--
18	LDO_EN	Digital Output	Push Pull 1X	floating
19	RESET	Digital Output	Open Drain NMOS 1X	floating
20	GND	GND	Ground	--

Ordering Information

Part Number	Package Type
SLG7RN46610V	20-pin STQFN
SLG7RN46610V	20-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.3	7	V
DC Input Voltage		GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	31	mA
	OD 1x	--	41	
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	° C
Junction Temperature		--	150	° C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.8	5	5.5	V
T_A	Operating Temperature		-40	25	85	° C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	65	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	152	mA
		T_J = 110°C	--	--	72	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7xVDD	--	VDD+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input	GND-0.3	--	0.3xVDD	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, I_{OH}=3mA at VDD=3.3V	2.73	3.12	--	V
		Push-Pull 1X, I_{OH}=5mA at VDD=5.0V	4.19	4.78	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=3mA, at VDD=3.3V	--	0.13	0.23	V
		Push-Pull 1X, I_{OL}=5mA, at VDD=5.0V	--	0.16	0.27	V
		Open Drain NMOS 1X, I_{OL}=3mA, at VDD=3.3V	--	0.08	0.15	V
		Open Drain NMOS 1X, I_{OL}=5mA, at VDD=5.0V	--	0.10	0.18	V
I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 1X, V_{OH}=2.4V at VDD=3.3V	6.05	12.08	--	mA
		Push-Pull 1X, V_{OH}=2.4V at VDD=5.0V	22.08	34.04	--	mA

I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 1X, V_{OL}=0.4V, at VDD=3.3V	4.87	8.24	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=5.0V	7.21	11.58	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=3.3V	7.31	12.37	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=5.0V	10.82	17.38	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PIN 1	--	100	--	kΩ
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PINs 3, 6	--	100	--	kΩ
T_{DLY0}	Delay0 Time	At temperature 25°C	6.88	10.5	28.3	µs
		At temperature -40 +85°C (Note 3)	5.04	10.5	40.52	µs
T_{DLY1}	Delay1 Time	At temperature 25°C	1.77	2.01	2.09	ms
		At temperature -40 +85°C (Note 3)	1.76	2.01	2.26	ms
T_{DLY2}	Delay2 Time	At temperature 25°C	1.77	2.01	2.09	ms
		At temperature -40 +85°C (Note 3)	1.76	2.01	2.26	ms
T_{DLY4}	Delay4 Time	At temperature 25°C	15.72	20.5	38.56	µs
		At temperature -40 +85°C (Note 3)	13.86	20.5	51.54	µs
V_{ACMP0}	Analog Comparator0 Threshold Voltage	Low to High transition, at temperature 25°C	1190	--	1214	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	1182	--	1214	mV
		High to Low transition, at temperature 25°C	990	--	1012	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	984	--	1012	mV
V_{ACMP1}	Analog Comparator1 Threshold Voltage	Low to High transition, at temperature 25°C	1205	--	1230	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	1198	--	1233	mV
		High to Low transition, at temperature 25°C	1170	--	1196	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	1158	--	1193	mV
V_{HYST}	Analog Comparator Hysteresis Voltage (Note 3)	ACMP 0 at temperature 25°C	--	200	--	mV
		ACMP 0 at temperature -40 +85°C	--	200	--	mV
		ACMP 1 at temperature 25°C	--	25	--	mV
		ACMP 1 at temperature -40 +85°C	--	25	--	mV
LDO0	LDO0 output voltage	Vout0 voltage	--	3.30	--	V
		Vout1 voltage	--	3.30	--	V
LDO1	LDO1 output voltage	Vout0 voltage	--	1.80	--	V

		Vout1 voltage	--	1.80	--	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1.3	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.34	1.55	1.74	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.05	1.25	1.45	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. PINs 1, 2, 3, 4, 5 and 6 are connected to one side, PINs 8, 9, 10, 18 and 19 to another.
3. Guaranteed by Design.

LDO Regulator Thermal Limitations

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
IC_{TL}	Thermal Limitation	85 °C ambient, Total IC package	--	--	0.6	W
		70 °C ambient, Total IC package	--	--	0.8	W
		Max Watt per LDO[1]	--	--	0.5	W
Shutdown	Thermal Shutdown[2]		115	125	135	° C
	Thermal Shutdown Recovery		90	100	110	° C

Note:
1. Please note that Max Watt LDO multiplied by number of LDOs can easily exceed the Max Watt for the total IC package. In this case an external resistor should be used on LDO Vin to lower the voltage drop across the LDO Regulator.
2.Lower Thermal shutdown levels may be achieved by using the temperature sensor and comparator.

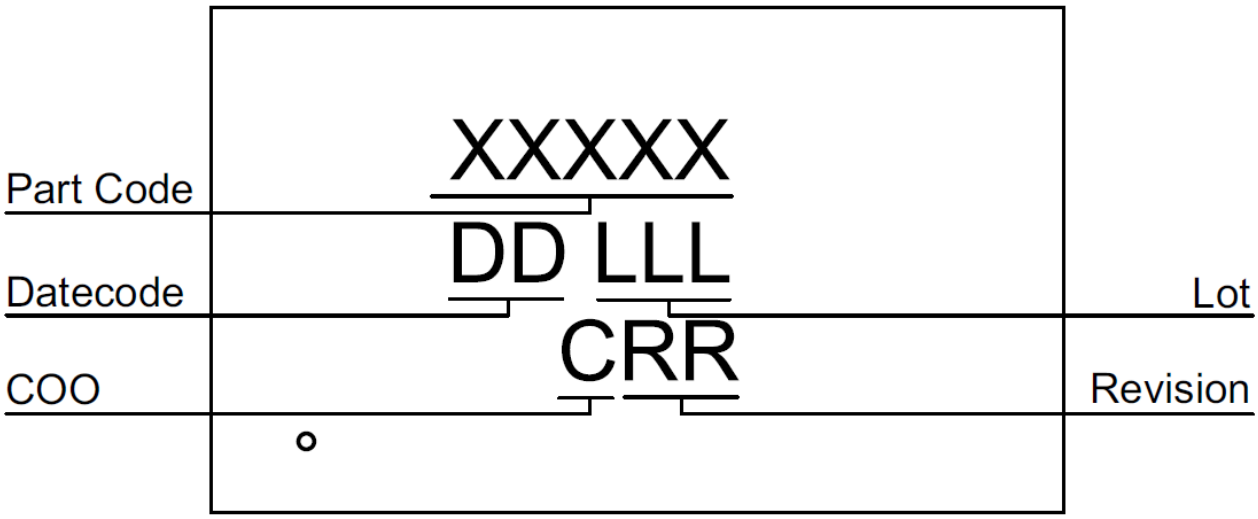
LDO HP MODE Electrical Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OUT}	Output Current Rating		--	--	300	mA
V_{IN}	Voltage Input		2.3	--	VDD	V
V_{DO}	Voltage Dropout		--	250	300	mV
ΔV_{OUT}	Output Voltage Accuracy (see Note 1)	over PVT of V_{OUT} > 1.5 V	-3	--	+3	%
		over PVT of $V_{OUT} \leqslant$ 1.5 V	-60	--	+60	mV
e_N	Noise Voltage (rms)	10 Hz to 100 kHz	--	75	--	µV
PSRR	Power Supply Rejection Ratio (see Note 2)	100 Hz to 100 kHz	TBD	50	--	dB
CTRR	Crosstalk Rejection Ratio	LDO0 to LDO1 regulation perturbation, and LDO2 to LDO3 perturbation at 0 to 150 mA at 1 kHz at 1.8 V V_{OUT}	TBD	50	--	dB
ΔV_{LINE}	Line Regulation	V_{OUT} + 0.5 V < $V_{IN} \leqslant$ 5.5 V	-1%	--	+1%	%/V
ΔV_{LOAD}	Load Regulation	1 mA < I_{OUT} < 150 mA	--	--	0.3	mV/ mA
ΔV_{TC}	V_{OUT} Temp Coefficient		--	100	--	ppm/ C
C_{IN}	External Input Capacitor (see Note 2)		2	--	--	µF

C_{OUT}	External Output Capacitor		4	--	--	µF
t_{SS_0}	Soft Start Option 0 Time	V_{OUT} 5% to 95%	-20%	10	+20%	V/ms
t_{SS_1}	Soft Start Option 1 Time	V_{OUT} 5% to 95%	-20%	20	+20%	V/ms
t_{SS_2}	Soft Start Option 2 Time	V_{OUT} 5% to 95%	-30%	1.25	+30%	V/ms
t_{SS_3}	Soft Start Option 3 Time	V_{OUT} 5% to 95%	-30%	2.50	+30%	V/ms
SC	Short Circuit Protection		TBD	TBD	TBD	mA
t_{WAIT}	Wait Time	Time from EN=1 to V_{OUT} start rise	--	500	--	µs
R_D	Output Discharge Pull-down Resistance	EN=0, Dis_EN = 1	--	300	--	Ω

Note:
1. Accuracy specifies all the effects of line regulation (ΔV_{LINE}), load regulation (ΔV_{LOAD}), and temperature coefficient (ΔV_{TC}),
2. X7R-type and X5R-type capacitors are recommended

Package Top Marking



XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.10	001	L	0xD427BB1C			05/31/2023

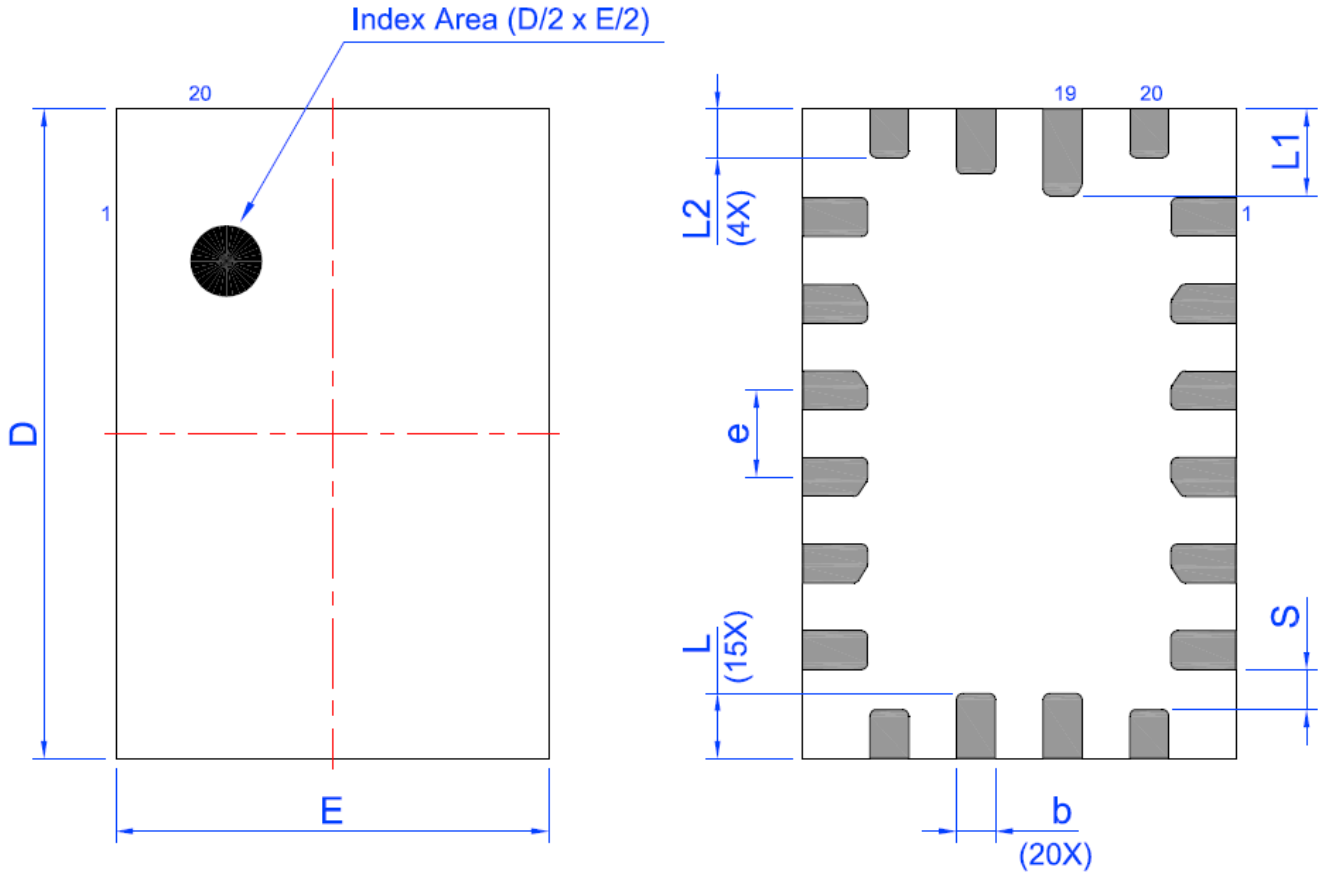
Lock coverage for this part is indicated by √, from one of the following options:

	Unlocked
	Locked for read, bits <1535:0>
	Locked for write, bits <1535:0>
	Locked for write all bits
	Locked for read and write bits <1535:0>
√	Locked for read bits <1535:0> and write of all bits

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

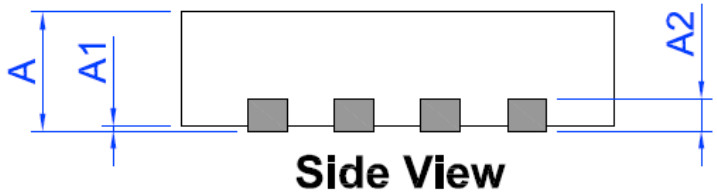
Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P FCD Package
JEDEC MO-220, Variation WECE



Marking View

BTM View



Side View

Unit: mm

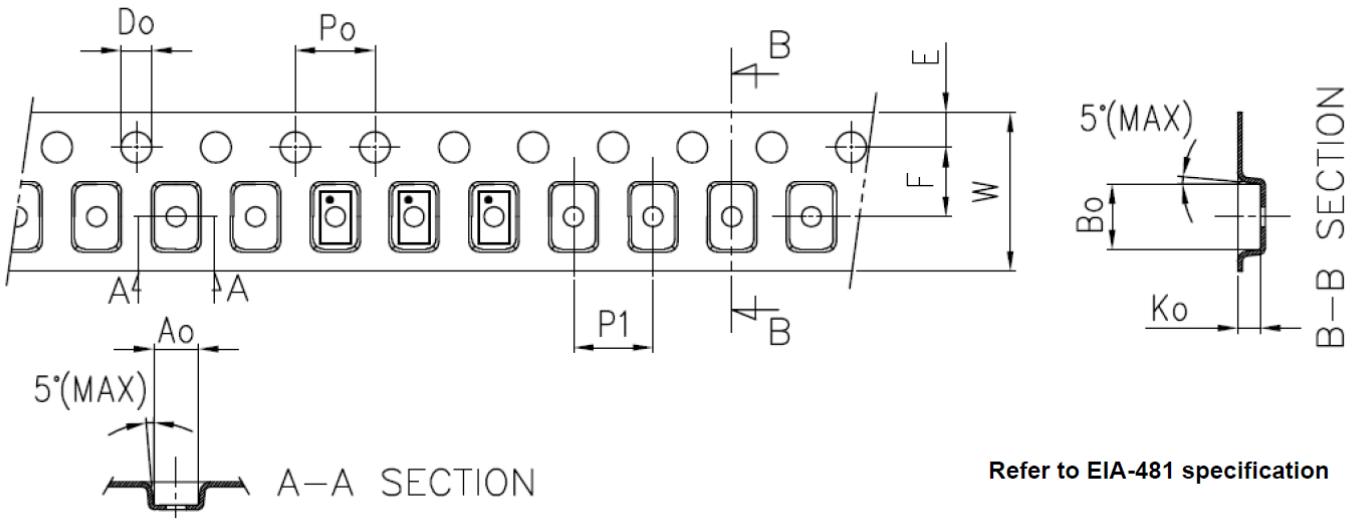
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.35	0.40	0.45
e	0.40 BSC			L2	0.175	0.225	0.275
S	0.185 TYP						

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3mm 0.4P FCD	20	2 x 3 x 0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P FCD	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

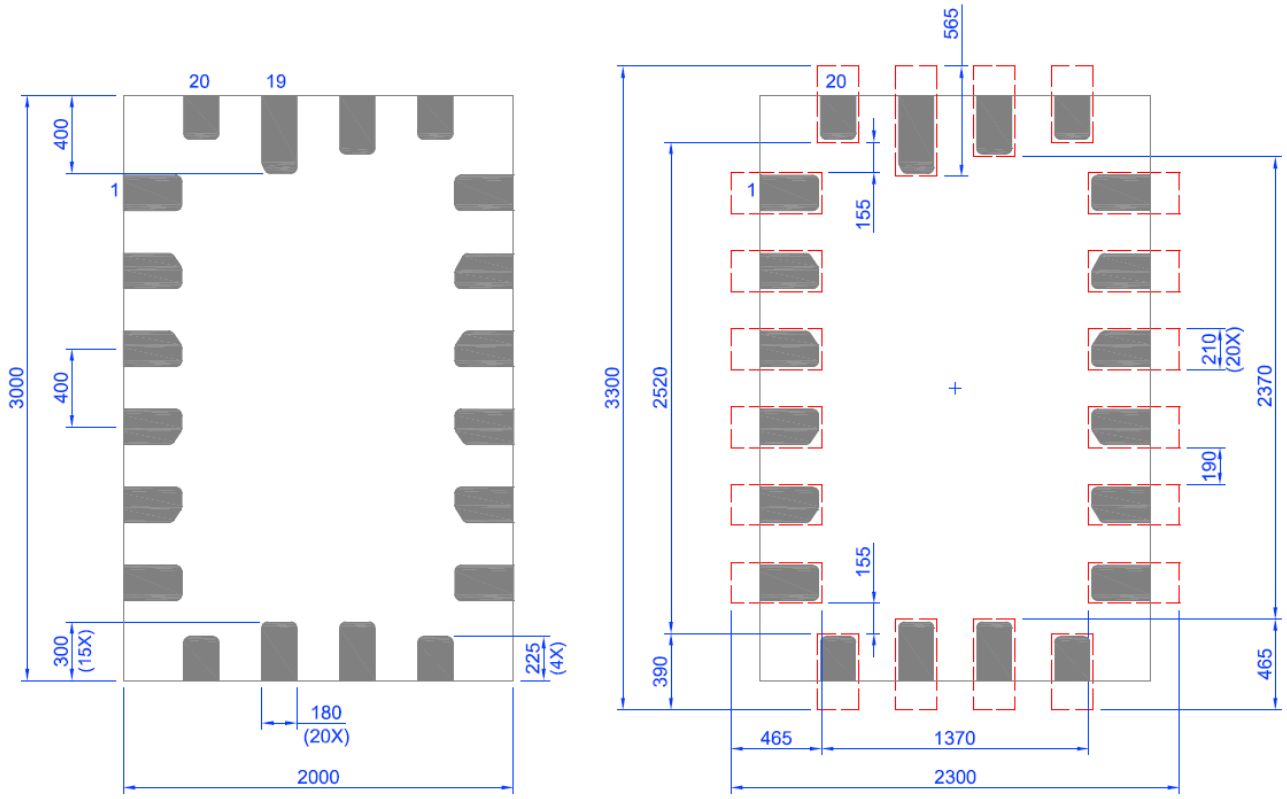
Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern

Exposed Pad
(PKG face down)

Recommended Land Pattern
(PKG face down)



Unit:um

Datasheet Revision History

Date	Version	Change
05/31/2023	0.10	New design for SLG46582 chip

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