SLG7RN46358

GreenPAK ™

RZ/G2E Power Sequence

General Description

Renesas SLG7RN46358 is a low power and small form device. The SoC is housed in a 4mm x 4mm STQFN package which is optimal for using with small devices.

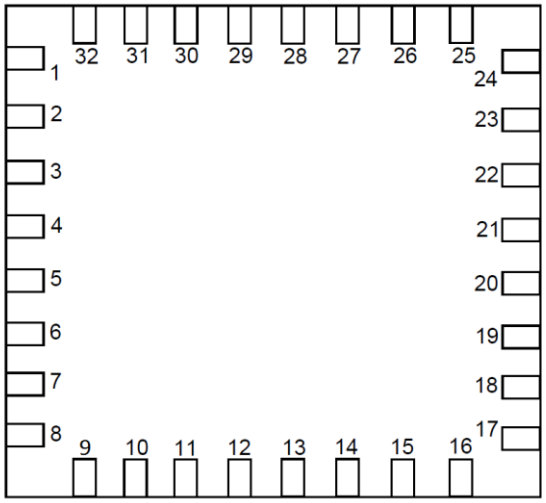
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 32 Package

Output Summary

1 Output - Open Drain NMOS 2X
4 Outputs - Push Pull 1X

Pin Configuration



STQFN-32 (Top view)

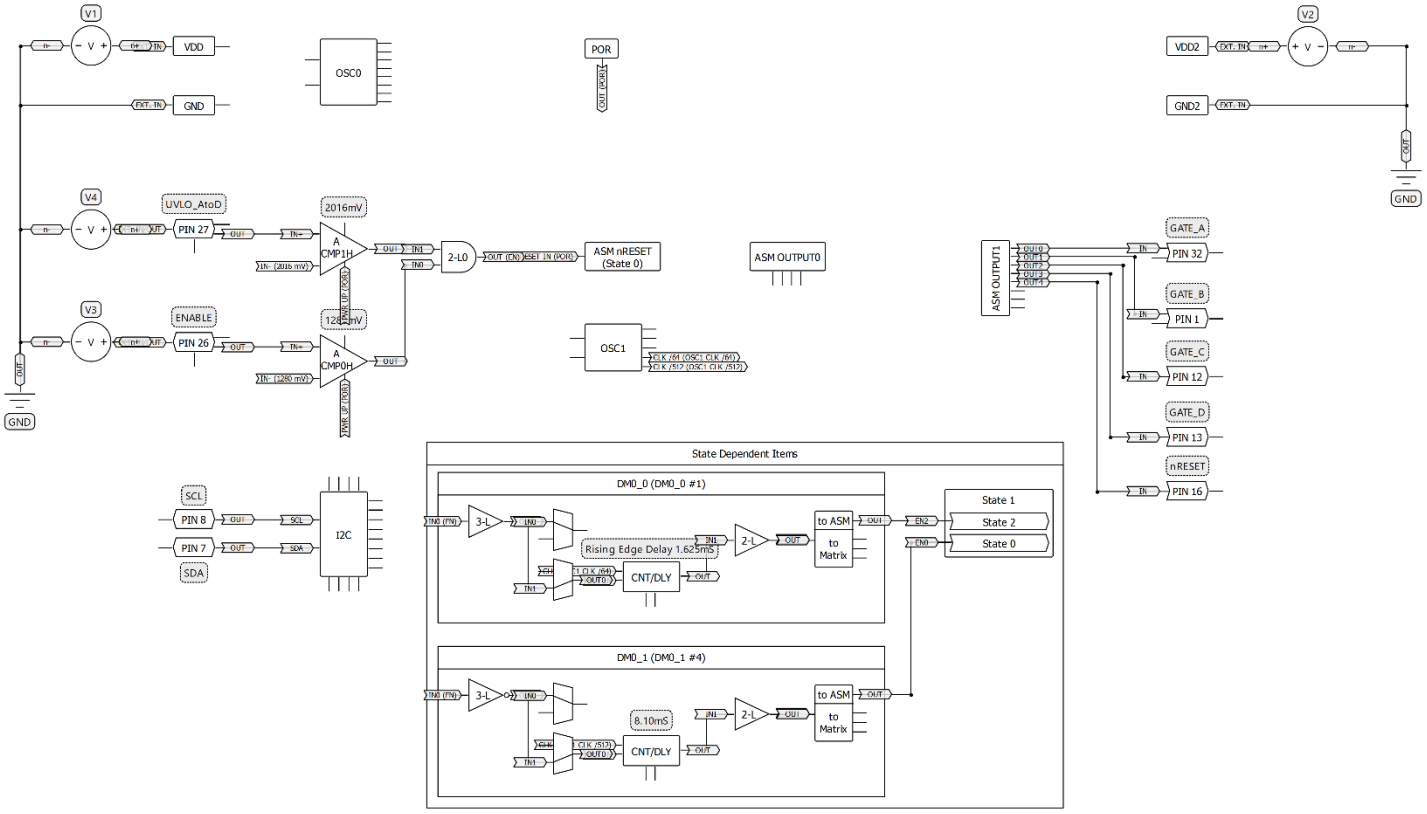
Pin name

Pin #	Pin name	Pin #	Pin name
1	GATE_B	17	NC
2	NC	18	NC
3	NC	19	NC
4	NC	20	NC
5	NC	21	NC
6	NC	22	NC
7	SDA	23	NC
8	SCL	24	NC
9	NC	25	NC
10	NC	26	ENABLE
11	NC	27	UVLO_AtoD
12	GATE_C	28	NC
13	GATE_D	29	NC
14	GND	30	GND
15	VDD2	31	VDD
16	nRESET	32	GATE_A

Block Diagram

SLG46880V (SLG7RN46358_GP_r001U_03072023.gp6)

State 1



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	GATE_B	Digital Output	Push Pull 1X	floating
2	NC	--	Keep Floating or Connect to GND	--
3	NC	--	Keep Floating or Connect to GND	--
4	NC	--	Keep Floating or Connect to GND	--
5	NC	--	Keep Floating or Connect to GND	--
6	NC	--	Keep Floating or Connect to GND	--
7	SDA	Digital Input	Digital Input without Schmitt trigger	floating
8	SCL	Digital Input	Digital Input without Schmitt trigger	floating
9	NC	--	Keep Floating or Connect to GND	--
10	NC	--	Keep Floating or Connect to GND	--
11	NC	--	Keep Floating or Connect to GND	--
12	GATE_C	Digital Output	Push Pull 1X	floating
13	GATE_D	Digital Output	Push Pull 1X	floating
14	GND	GND	Ground	--
15	VDD2	PWR	Supply Voltage	--
16	nRESET	Digital Output	Open Drain NMOS 2X	floating
17	NC	--	Keep Floating or Connect to GND	--
18	NC	--	Keep Floating or Connect to GND	--
19	NC	--	Keep Floating or Connect to GND	--
20	NC	--	Keep Floating or Connect to GND	--
21	NC	--	Keep Floating or Connect to GND	--
22	NC	--	Keep Floating or Connect to GND	--
23	NC	--	Keep Floating or Connect to GND	--
24	NC	--	Keep Floating or Connect to GND	--
25	NC	--	Keep Floating or Connect to GND	--
26	ENABLE	Analog Input/Output	Analog Input/Output	floating
27	UVLO_AtoD	Analog Input/Output	Analog Input/Output	floating
28	NC	--	Keep Floating or Connect to GND	--
29	NC	--	Keep Floating or Connect to GND	--
30	GND	GND	Ground	--
31	VDD	PWR	Supply Voltage	--
32	GATE_A	Digital Output	Push Pull 1X	floating

Ordering Information

Part Number	Package Type
SLG7RN46358V	32-pin STQFN
SLG7RN46358V	32-pin STQFN - Tape and Reel (5k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at Input Pin	GND-0.5V	VDD+0.5V	V
Maximum Average or DC Current (Through V_{DD} or GND pin)	--	90	mA
Current at Input Pin	-1.0	1.0	mA
Input leakage Current (Absolute Value)	--	1000	nA
Storage Temperature Range	-65	150	° C
Junction Temperature	--	150	° C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD} (Note 4)	Supply Voltage		4.5	5	5.5	V
V_{DD2} (Note 4)	Supply Voltage		4.5	5	5.5	V
T_A	Operating Temperature		-40	25	85	° C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	73	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7xVDD	--	VDD+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input	GND-0.3	--	0.3xVDD	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, I_{OH}=5mA at VDD=5.0V	4.154	4.247	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=5mA, at VDD=5.0V	--	0.212	0.297	V
		Open Drain NMOS 2X, I_{OL}=5mA, at VDD=5.0V	--	0.041	0.061	V
I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 1X, VOH=2.4V at VDD=5.0V	19.89	24.83	--	mA
I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 1X, V_{OL}=0.4V, at VDD=5.0V	7.15	9.76	--	mA
		Open Drain NMOS 2X, V_{OL}=0.4V, at VDD=5.0V	31.20	45.10	--	mA
V_{ACMP0}	Analog Comparator0 Threshold Voltage	Low to High transition, at temperature 25°C	1264	1280	1290	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	1261	1280	1290	mV
		High to Low transition, at temperature 25°C	1204	1216	1227	mV

		High to Low transition, at temperature -40 +85°C (Note 3)	1200	1216	1227	mV
V_{ACMP1}	Analog Comparator1 Threshold Voltage	Low to High transition, at temperature 25°C	1991	2016	2034	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	1985	2016	2034	mV
		High to Low transition, at temperature 25°C	1962	1984	2007	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	1957	1984	2007	mV
V_{HYST}	Analog Comparator Hysteresis Voltage (Note 3)	ACMP 0 at temperature 25°C	--	64	--	mV
		ACMP 0 at temperature -40 +85°C	--	64	--	mV
		ACMP 1 at temperature 25°C	--	32	--	mV
		ACMP 1 at temperature -40 +85°C	--	32	--	mV
$T_{DM0\_0\#0}$	DM0_0#0 DLY Time	At temperature 25°C	11.36	11.62	11.88	ms
		At temperature -40 +85°C (Note 3)	11.25	11.64	12.07	ms
$T_{DM0\_0\#1}$	DM0_0#1 DLY Time	At temperature 25°C	1.60	1.64	1.68	ms
		At temperature -40 +85°C (Note 3)	1.58	1.64	1.71	ms
$T_{DM0\_0\#2}$	DM0_0#2 DLY Time	At temperature 25°C	13.09	13.37	13.65	ms
		At temperature -40 +85°C (Note 3)	12.97	13.39	13.87	ms
$T_{DM0\_0\#3}$	DM0_0#3 DLY Time	At temperature 25°C	36.07	36.60	37.14	ms
		At temperature -40 +85°C (Note 3)	35.73	36.66	37.74	ms
$T_{DM0\_0\#4}$	DM0_0#4 DLY Time	At temperature 25°C	158.4	162.1	166.6	ms
		At temperature -40 +85°C (Note 3)	157.1	163.5	177.0	ms
$T_{DM0\_1\#1}$	DM0_1#1 DLY Time	At temperature 25°C	19	20	23	µs
		At temperature -40 +85°C (Note 3)	17	20	26	µs
$T_{DM0\_1\#2}$	DM0_1#2 DLY Time	At temperature 25°C	20.01	20.36	20.72	ms
		At temperature -40 +85°C (Note 3)	19.82	20.39	21.06	ms
$T_{DM0\_1\#3}$	DM0_1#3 DLY Time	At temperature 25°C	16.06	16.36	16.68	ms
		At temperature -40 +85°C (Note 3)	15.90	16.39	16.95	ms
$T_{DM0\_1\#4}$	DM0_1#4 DLY Time	At temperature 25°C	8.15	8.37	8.59	ms
		At temperature -40 +85°C (Note 3)	8.07	8.38	8.74	ms
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1.13	1.72	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.64	1.84	2.11	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.98	1.25	1.49	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides.
3. Guaranteed by Design.
4. PINs 1, 2, 3, 4, 5, 6, 7, 8, 9, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 32 are powered from VDD and PINs 10, 11, 12, 13, 16, 17, 18, 19 are powered from VDD2.

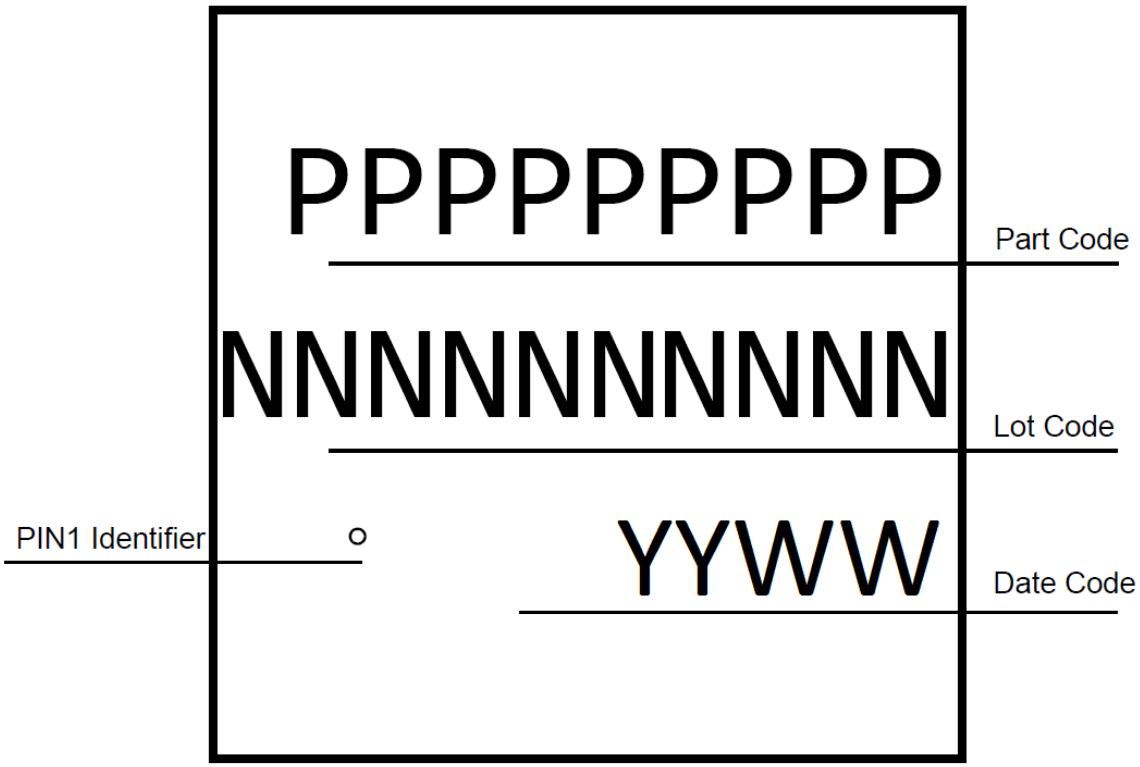
Asynchronous State Machine (ASM) Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
$t_{st\_out\_delay}$	Asynchronous State Machine Output Delay Time	VDD = 5.0V ± 10%	70	--	123	ns
t_{st_out}	Asynchronous State Machine Output Transition Time	VDD = 5.0V ± 10%	--	--	46	ns
t_{st_pulse}	Asynchronous State Machine Input Pulse Acceptance Time	VDD = 5.0V ± 10%	12	--	--	ns
t_{st_comp}	Asynchronous State Machine Input Compete Time	VDD = 5.0V ± 10%	--	--	5	ns
$t_{st\_sequential\_delay}$	Asynchronous State Machine Sequential Output Delay Time	VDD = 5.0V ± 10%	119	--	208	ns
$t_{st\_dmlatch\_delay}$	Asynchronous State Machine Dynamic Memory Latch Delay	VDD = 5.0V ± 10%	119	--	208	ns

Functionality Waveforms

Channel 1 (yellow/top line) – PIN# 27 (UVLO_AtoD)
Channel 2 (magenta /2nd line) – PIN# 26 (ENABLE)
D0 – PIN# 32 (GATE_A)
D1 – PIN# 1 (GATE_B)
D2 – PIN# 12 (GATE_C)
D3 – PIN# 13 (GATE_D)
D4 – PIN# 16 (nRESET) with external 5kΩ pull up resistor

Package Top Marking



Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	001	U	0xC54997AA	7RN46358	A	06/06/2023

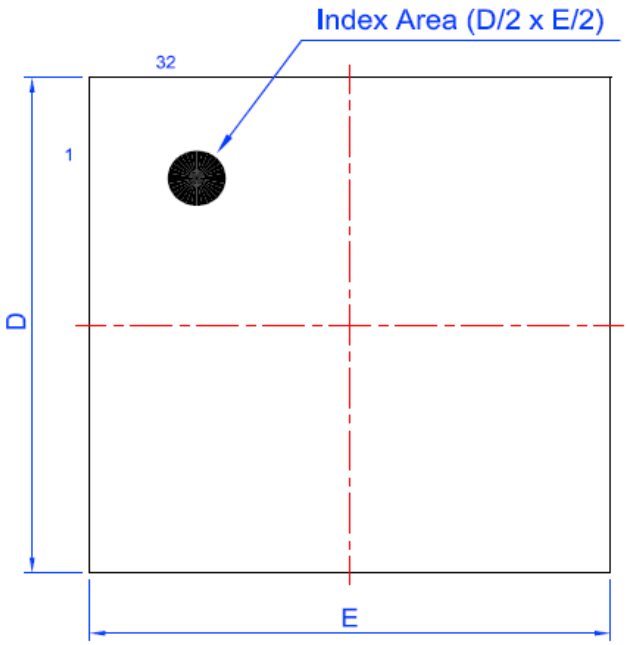
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

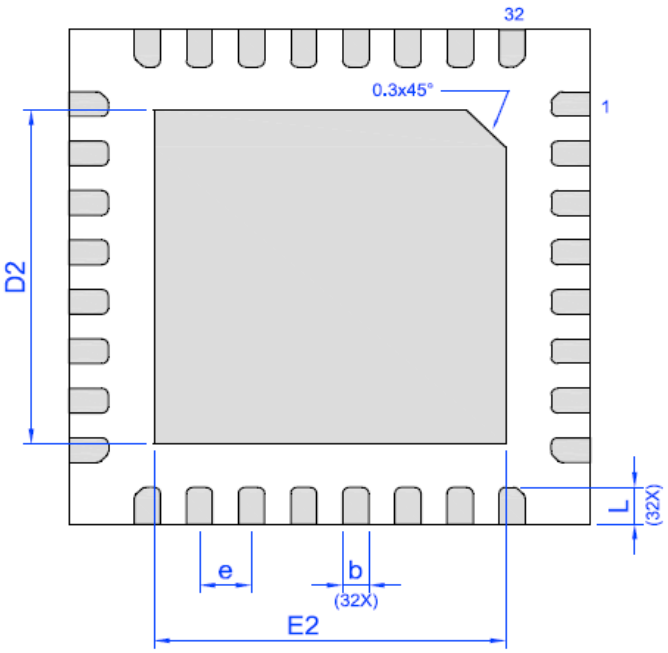
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Outlines

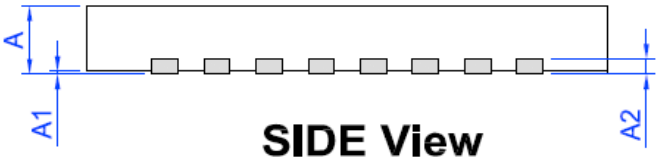
STQFN 32L 4x4mm 0.4P Package
IC Net Weight: 0.028 g



Marking View



BTM View



SIDE View

Unit: mm

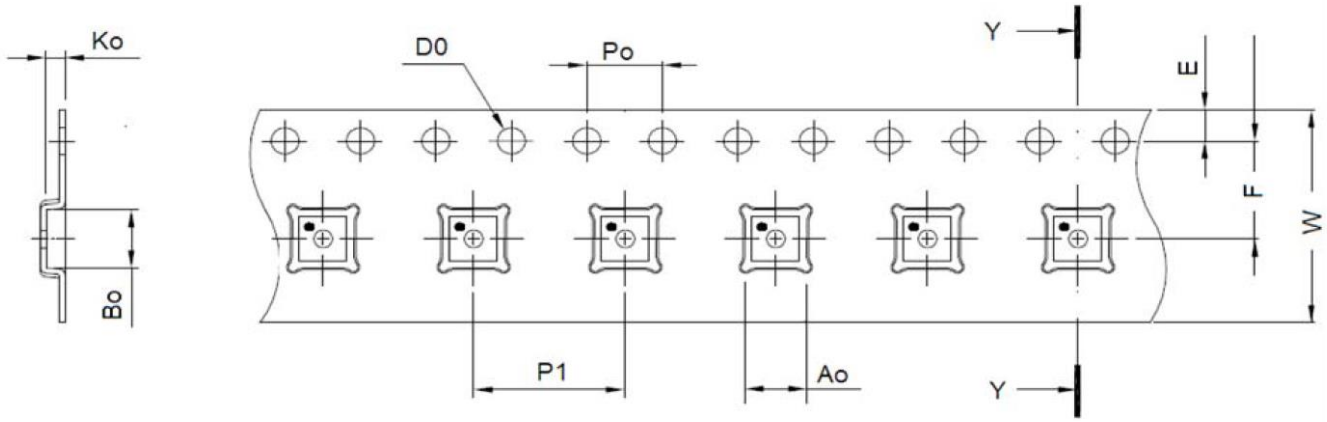
Symbol	Min.	Nom.	Max.	Symbol	Min.	Nom.	Max.
A	0.500	0.550	0.600	D	3.950	4.000	4.050
A1	0.00	-	0.050	E	3.950	4.000	4.050
A2	0.150 REF			D2	2.650	2.700	2.750
b	0.150	0.200	0.250	E2	2.650	0.270	2.750
e	0.400 BSC			L	0.250	0.300	0.350

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 32L 4x4 mm 0.4P Green	32	4 x 4 x 0.55	5000	10000	330/100	42	336	42	336	12	8

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 32L 4x4 mm 0.4P Green	4.25	4.25	0.75	4	8	1.5	1.75	5.5	12

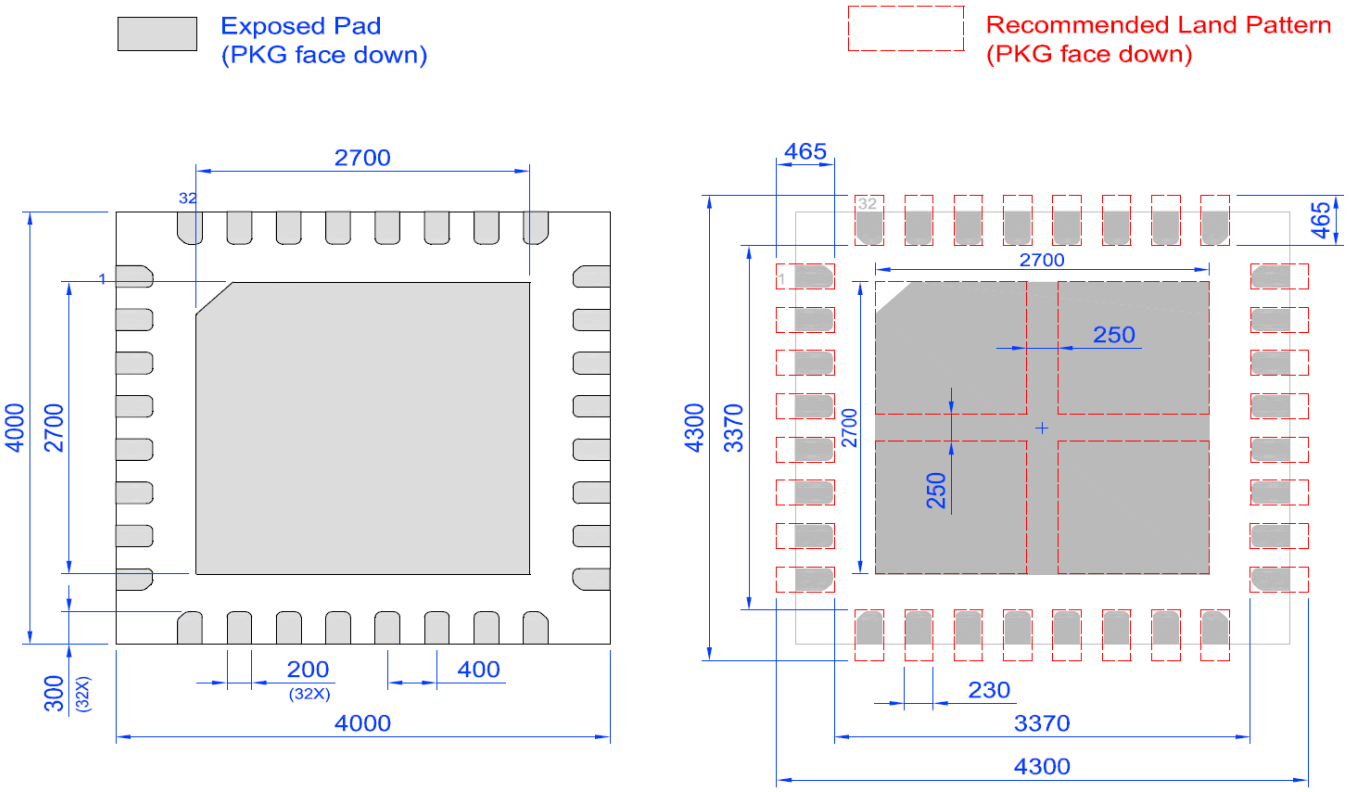


Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.85 mm^3 (nominal). More information can be found at www.jedec.org.

Layout Guidelines



Units: µm

Datasheet Revision History

Date	Version	Change
03/07/2023	0.10	New design for SLG46880 chip
06/05/2023	0.11	Updated Device Revision Table
06/06/2023	1.00	Production Release

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