



### General Description

Renesas SLG7NT4741 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

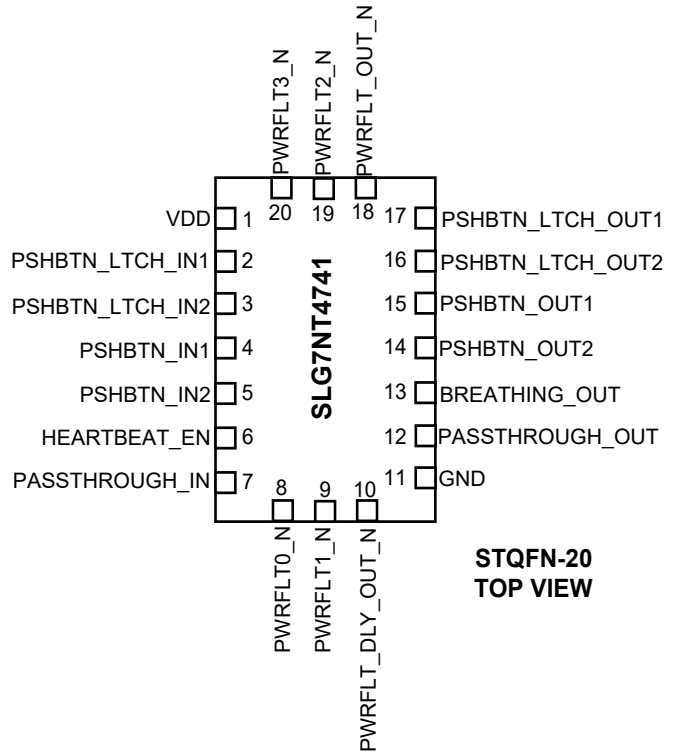
### Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-20 Package

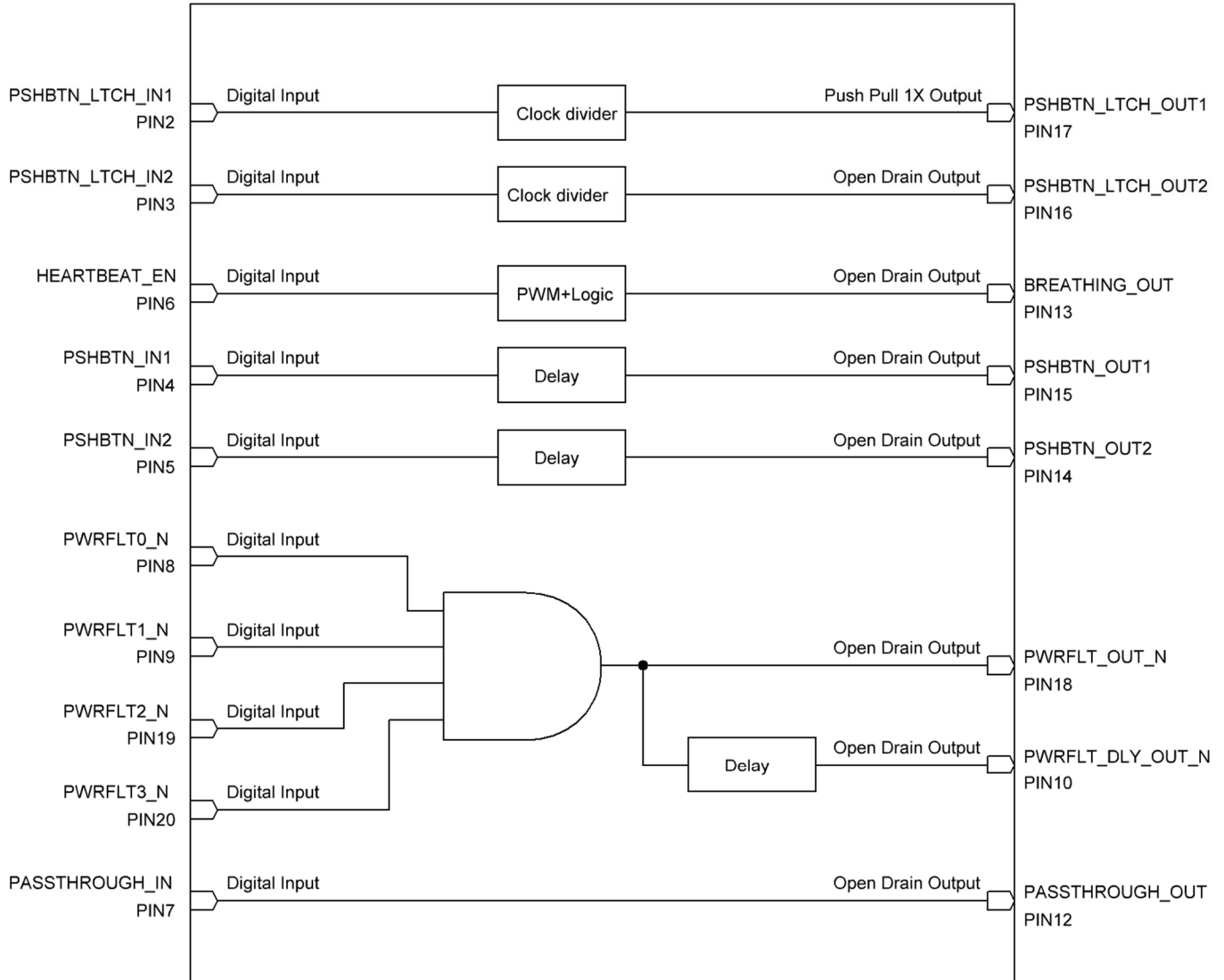
### Output Summary

- 1 Output — Push Pull 1X
- 7 Outputs — Open Drain NMOS 1X

### Pin Configuration



### Block Diagram



**Pin Configuration**

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	PSHBTN_LTCH_IN1	Digital Input	Low Voltage Digital input
3	PSHBTN_LTCH_IN2	Digital Input	Low Voltage Digital input
4	PSHBTN_IN1	Digital Input	Low Voltage Digital input
5	PSHBTN_IN2	Digital Input	Low Voltage Digital input
6	HEARTBEAT_EN	Digital Input	Low Voltage Digital input
7	PASSTHROUGH_IN	Digital Input	Low Voltage Digital input
8	PWRFLT0_N	Digital Input	Low Voltage Digital input
9	PWRFLT1_N	Digital Input	Low Voltage Digital input
10	PWRFLT_DLY_OUT_N	Digital Output	Open Drain NMOS 1X
11	GND	GND	Ground
12	PASSTHROUGH_OUT	Digital Output	Open Drain NMOS 1X
13	BREATHING_OUT	Digital Output	Open Drain NMOS 1X
14	PSHBTN_OUT2	Digital Output	Open Drain NMOS 1X
15	PSHBTN_OUT1	Digital Output	Open Drain NMOS 1X
16	PSHBTN_LTCH_OUT2	Digital Output	Open Drain NMOS 1X
17	PSHBTN_LTCH_OUT1	Digital Output	Push Pull 1X
18	PWRFLT_OUT_N	Digital Output	Open Drain NMOS 1X
19	PWRFLT2_N	Digital Input	Low Voltage Digital input
20	PWRFLT3_N	Digital Input	Low Voltage Digital input

**Ordering Information**

Part Number	Package Type
SLG7NT4741V	V=STQFN-20
SLG7NT4741VTR	VTR=STQFN-20 – Tape and Reel (3k units)

### Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V <sub>HIGH</sub> to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	125	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

### Electrical Characteristics

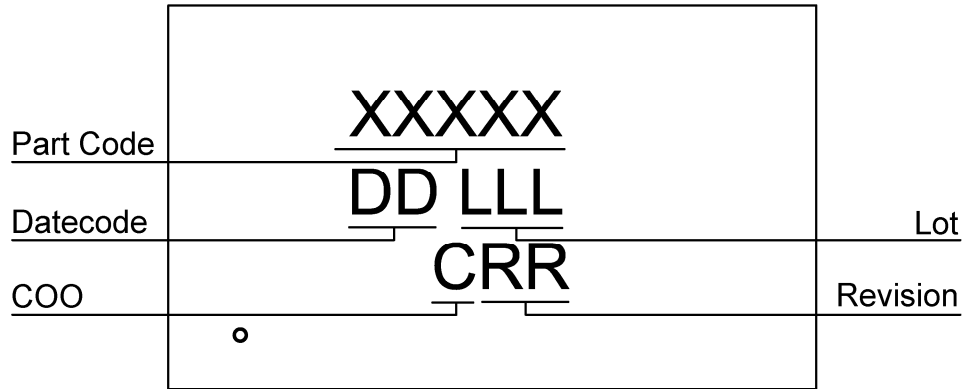
(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage		1.71	3	5.5	V
T <sub>A</sub>	Operating Temperature		-40	25	85	°C
I <sub>Q</sub>	Quiescent Current	Static inputs and outputs	--	80	--	µA
V <sub>O</sub>	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I <sub>O</sub>	Maximal Average or DC Current (note 1)	Per Each Chip Side (PIN2-PIN10, PIN12-PIN20)	--	--	90	mA
V <sub>IH</sub>	HIGH-Level Input Voltage	Low-Level Logic Input, at VDD=1.8V	0.894	--	VDD	V
		Low-Level Logic Input, at VDD=3.3V	1.059	--	VDD	
		Low-Level Logic Input, at VDD=5.0V	1.157	--	VDD	
V <sub>IL</sub>	LOW-Level Input Voltage	Low-Level Logic Input, at VDD=1.8V	0	--	0.557	V
		Low-Level Logic Input, at VDD=3.3V	0	--	0.686	
		Low-Level Logic Input, at VDD=5.0V	0	--	0.776	
I <sub>IH</sub>	HIGH-Level Input Current	Logic Input PINs; V <sub>IN</sub> = VDD	-1.0	--	1.0	µA
I <sub>IL</sub>	LOW-Level Input Current	Logic Input PINs; V <sub>IN</sub> = 0V	-1.0	--	1.0	µA
V <sub>OH</sub>	HIGH-Level Output Voltage	Push Pull & PMOS OD, I <sub>OH</sub> = 100µA, 1X Driver, at VDD=1.8 V	1.680	1.788	--	V
		Push Pull & PMOS OD, I <sub>OH</sub> = 3mA, 1X Driver, at VDD=3.3 V	2.713	3.095	--	
		Push Pull & PMOS OD, I <sub>OH</sub> = 5mA, 1X Driver, at VDD=5.0 V	4.159	4.750	--	
V <sub>OL</sub>	LOW-Level Output Voltage	Push Pull, I <sub>OL</sub> = 100µA, 1X Driver, at VDD=1.8 V	--	0.009	0.015	V
		Open Drain, I <sub>OL</sub> = 100µA, 1X Driver, at VDD=1.8 V	--	0.007	0.010	
		Push Pull, I <sub>OL</sub> = 3mA, 1X Driver, at VDD=3.3 V	--	0.148	0.228	
		Open Drain, I <sub>OL</sub> = 3mA, 1X Driver, at VDD=3.3 V	--	0.080	0.147	

		Push Pull, $I_{OL} = 5\text{mA}$ , 1X Driver, at VDD=5.0 V	--	0.189	0.270	
		Open Drain, $I_{OL} = 5\text{mA}$ , 1X Driver, at VDD=5.0 V	--	0.102	0.180	
$I_{OH}$	HIGH-Level Output Current	Push Pull & PMOS OD, $V_{OH} = VDD-0.2$ , 1X Driver at VDD=1.8 V	1.027	1.703	--	mA
		Push Pull & PMOS OD, $V_{OH} = 2.4\text{ V}$ , 1X Driver, at VDD=3.3 V	5.608	10.774	--	
		Push Pull & PMOS OD, $V_{OH} = 2.4\text{ V}$ , 1X Driver, at VDD=5.0 V	20.337	30.010	--	
$I_{OL}$	LOW-Level Output Current	Push Pull, $V_{OL} = 0.15\text{V}$ , 1X Driver, at VDD=1.8 V	0.917	1.660	--	mA
		Open Drain, $V_{OL} = 0.15\text{V}$ , 1X Driver, at VDD=1.8 V	1.375	2.534	--	
		Push Pull, $V_{OL} = 0.4\text{V}$ , 1X Driver, at VDD=3.3 V	4.875	7.795	--	
		Open Drain, $V_{OL} = 0.4\text{V}$ , 1X Driver, at VDD=3.3 V	7.313	12.370	--	
		Push Pull, $V_{OL} = 0.4\text{V}$ , 1X Driver, at VDD=5.0 V	6.996	10.438	--	
		Open Drain, $V_{OL} = 0.4\text{V}$ , 1X Driver, at VDD=5.0 V	10.820	17.380	--	
$T_{DLY1}$	Delay1 Time	At temperature 25°C	3.77	4.59	5.52	s
		At temperature -40°C +85°C (note 1)	3.73	4.67	5.86	
$T_{DLY3}$	Delay3 Time	At temperature 25°C	75,21	91,78	110,11	ms
		At temperature -40°C +85°C (note 1)	74,3	93,31	116,97	
$T_{DLY4}$	Delay4 Time	At temperature 25°C	974,61	1039,71	1177,65	ms
		At temperature -40°C +85°C (note 1)	958,02	1047,51	1189,29	
$T_{DLY5}$	Delay5 Time	At temperature 25°C	75,21	91,78	110,11	ms
		At temperature -40°C +85°C (note 1)	74,3	93,31	116,97	
$T_{DLY7}$	Delay7 Time	At temperature 25°C	75,21	91,78	110,11	ms
		At temperature -40°C +85°C (note 1)	74,3	93,31	116,97	
$T_{DLY8}$	Delay8 Time	At temperature 25°C	75,21	91,78	110,11	ms
		At temperature -40°C +85°C (note 1)	74,3	93,31	116,97	
$T_{DLY9}$	Delay9 Time	At temperature 25°C	3,89	4,16	4,72	ms
		At temperature -40°C +85°C (note 1)	3,82	4,19	4,77	
$T_{SU}$	Start up Time	From VDD rising past $PON_{THR}$	0.526	1.4	5.148	ms
$PON_{THR}$	Power On Threshold	VDD Level Required to Start Up the Chip	0.950	1.462	1.708	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.935	1.103	1.281	V

1. Guaranteed by Design.

**Package Top Marking**



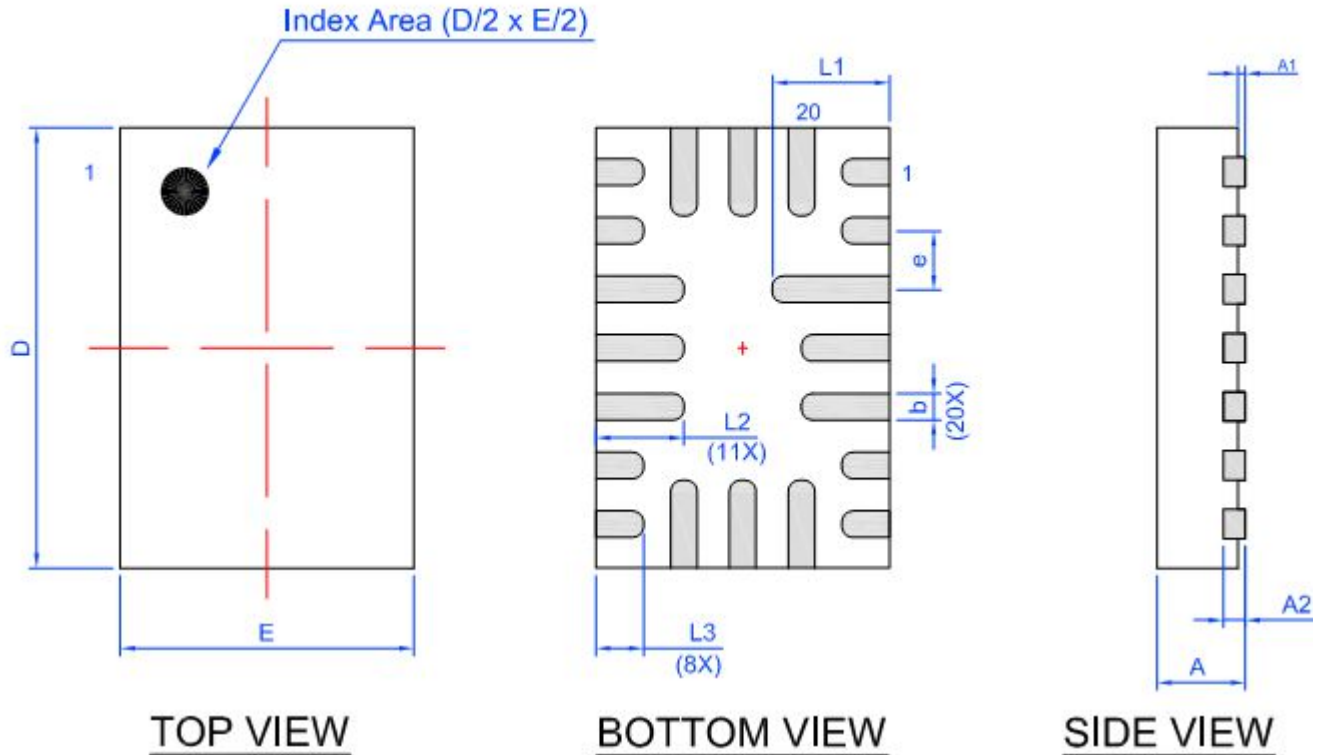
XXXXX – Part ID Field: identifies the specific device configuration  
 DD – Date Code Field: Coded date of manufacture  
 LLL – Lot Code: Designates Lot #  
 C – Assembly Site/COO: Specifies Assembly Site/Country of Origin  
 RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
1.02	002	L	4741V	AA	02/25/2022

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

**Package Drawing and Dimensions**

**20 Lead STQFN Package**  
**JEDEC MO-220, Variation WECE**  
**IC Net Weight: 0.015 g**



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

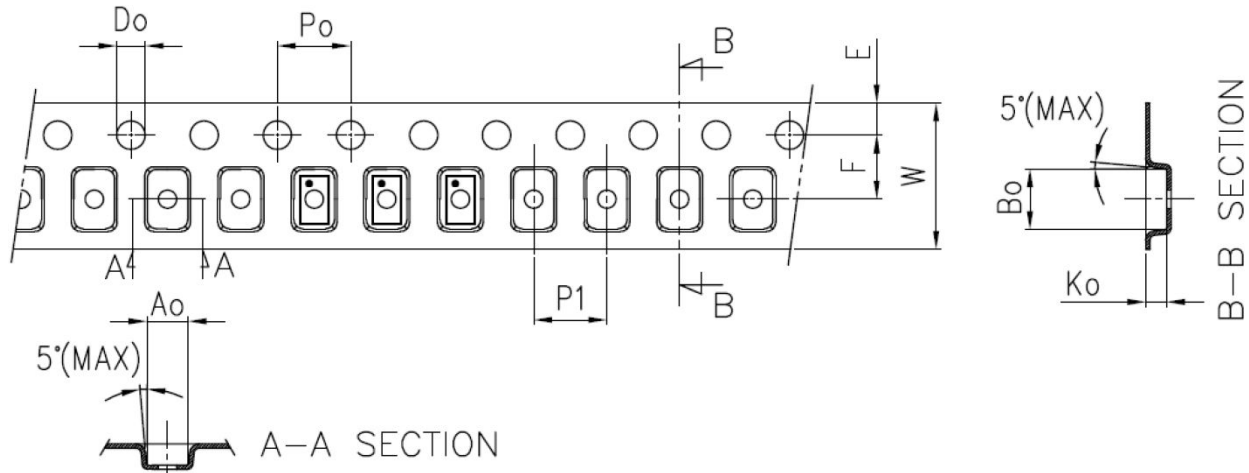
**Tape and Reel Specification**

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

**Carrier Tape Drawing and Dimensions**

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

Refer to EIA-481 Specifications


**Recommended Reflow Soldering Profile**

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).

### Datasheet Revision History

<b>Date</b>	<b>Version</b>	<b>Change</b>
04/23/2015	0.10	New design for SLG46620
04/27/2015	0.11	Changed PIN13 name and PIN20 mode to "Low Voltage"
04/27/2015	0.12	Updated Device Revision Table
10/20/2015	0.13	Corrected datasheet
10/26/2015	0.14	Updated Device Revision Table
10/29/2015	0.15	Locked NVM
11/05/2015	1.00	Production Release
03/08/2016	1.01	Updated Title Description
02/25/2022	1.02	Updated Company name and logo

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).