SLG51003

PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switch

The SLG51003 is a part of Power GreenPAK product family. This PMIC contains three compact and customizable low dropout regulators and is designed for advanced sensor applications and other battery powered equipment.

The LDO_HP is optimized to meet the requirements of high-performance analog circuits. It provides very low output voltage noise characteristics of 16 µV (rms) in addition to high PSRR of 68 dB at 1 MHz and tight output voltage accuracy of ±1 % over temperature.

The 0.8 A capable LDO_LV can be configured to operate as a load switch, which is optimized to meet the requirements of low R_{ON}. By using efficient DC/DC switching regulators upstream in conjunction with the SLG51003's linear regulators and load switch downstream, applications can leverage the best characteristics of each to simultaneously achieve low power, low noise, and low voltage dropout, respectively.

Built-in safety protection, such as undervoltage lockout, over-temperature protection, and current limit ensures that the ICs are operating under nominal conditions. The SLG51003 has an I^2C-compatible interface for flexible power control. The SLG51003 is available in a small 14-pin TQFN package with a wide ambient operating temperature range of -40 °C to +85 °C.

Features

- Input voltage range:
  - 2.8 V to 5.0 V (LDO_HP)
  - 1.7 V to 5.0 V (LDO_HV)
  - 0.8 V to 1.5 V (LDO_LV)
- Separate input supply and flexible power configurations
- Output voltage range:
  - 2.4 V to 3.3 V (LDO_HP)
  - 1.2 V to 3.75 V (LDO_HV)
  - 0.5 V to 1.4 V (LDO_LV)
- Output current range:
  - Up to 475 mA (LDO_HP)
  - Up to 500 mA (LDO_HV)
  - Up to 800 mA (LDO_LV)
- LDO_LV channel with Bypass Mode
- High PSRR of 98.5 dB at 1 kHz and 68 dB at 1 MHz (LDO_HP)
- Ultra-low output voltage noise of 16 µV (LDO_HP)
- Low dropout voltage of 10 mV per 100 mA of load (LDO_LV)
- Ultra-low R_{ON} load switch with low leakage and slew rate control for low V_{IN} supplies (LDO_LV)
- Tight output voltage accuracy of ±1 % over temperature
- Low shutdown current of 240 nA
- Low quiescent current of 14 µA
- Seven combination function macrocells
- Three delay macrocells
- One multi-function macrocell
- User-configurable settings via I^2C interface and OTP
- Soft start and soft shutdown
- Undervoltage lockout (UVLO)
- Thermal shutdown
- Configurable temperature alerts
- Wide -40 °C to +85 °C operating temperature
- 14-pin TQFN: 2.0 mm x 2.2 mm x 0.55 mm

Applications

- Advanced sensor applications
- RF applications and wireless interfaces
- Battery powered equipment

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1.1 Block Diagram

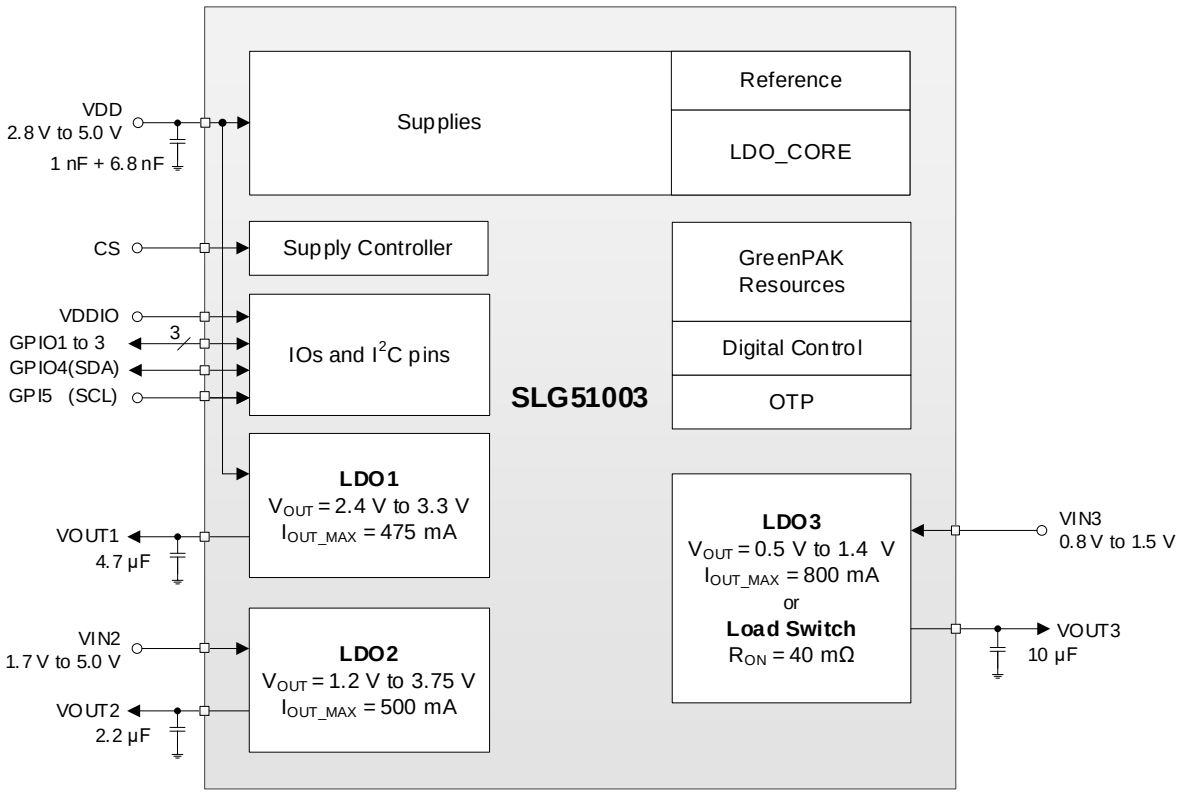


Figure 1. Block Diagram

2. Pin Information

2.1 Pin Assignment

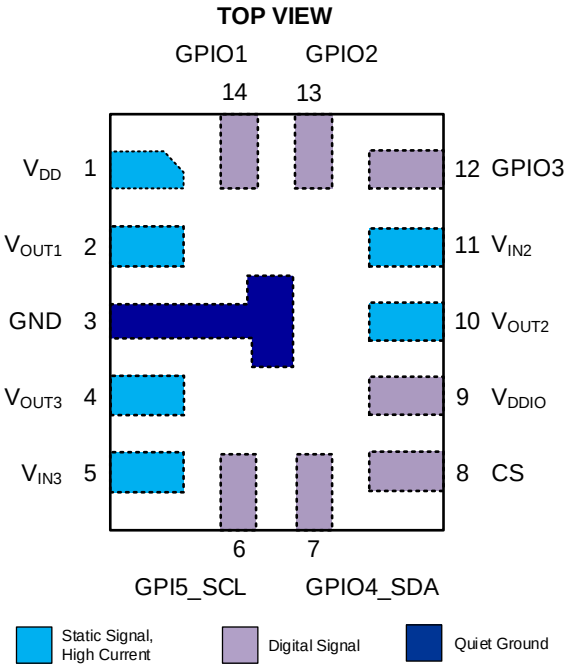


Figure 2. Pin Assignments - Top View, Face Down

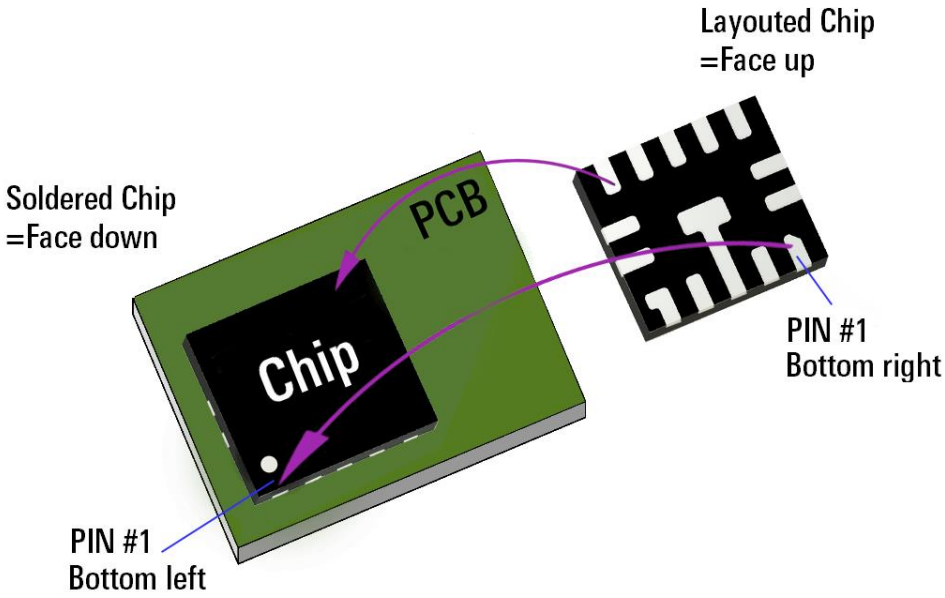


Figure 3. Chip Placement on PCB

2.2 Pin Descriptions

Table 1. TQFN-14 Pin Assignment and Description

Pin Number	Pin Name	Pin Function
3	GND	Ground
14	GPIO1	GPIO1, I2C_SA1, LDO1_SNS
13	GPIO2	GPIO2, I2C_SA2
12	GPIO3	GPIO3, I2C_SA3
7	GPIO4	GPIO4, SDA
6	GPI5_SCL	GPI5, SCL
1	V_{DD}	V_{DD} Supply & LDO1 Input
9	V_{DDIO}	V_{DDIO} Supply
8	CS	Chip Select
11	V_{IN2}	LDO2 Input
5	V_{IN3}	LDO3 Input
2	V_{OUT1}	LDO1 Output
10	V_{OUT2}	LDO2 Output
4	V_{OUT3}	LDO3 Output

Table 2. Functional Pin Description

Pin Name	Signal Name	Function	Input Options	Output Options
CS	CS	Chip Select (CS)	-	-
V_{DD}	V_{DD}	Supply Voltage for Overall Chip Control and LDO1 Input	-	-
GND	GND	Ground	-	-
V_{DDIO}	V_{DDIO}	Supply Voltage for GPIO1 - GPIO3	-	-
GPIO1	GPIO1	High Voltage General Purpose IO	Digital Input with/without Schmitt Trigger, Low Voltage Digital Input, Ultra-low Voltage Digital Input	Push-Pull, Open-Drain NMOS, Open-Drain PMOS
	I2C_SA1	I^2C Slave Address 1	-	-
	LDO1_SNS	LDO1 Remote Sense Pin	-	-
GPIO2	GPIO2	High Voltage General Purpose IO	Digital Input with/without Schmitt Trigger, Low Voltage Digital Input, Ultra-low Voltage Digital Input	Push-Pull, Open-Drain NMOS, Open-Drain PMOS
	I2C_SA2	I^2C Slave Address 2	-	-
GPIO3	GPIO3	High Voltage General Purpose IO	Digital Input with/without Schmitt Trigger, Low Voltage Digital Input, Ultra-low Voltage Digital Input	Push-Pull, Open-Drain NMOS, Open-Drain PMOS
	I2C_SA3	I^2C Slave Address 3	-	-
GPIO4	GPIO4	High Voltage General Purpose IO	Digital Input with Schmitt Trigger, Ultra-low Voltage Digital Input with Schmitt Trigger	Open-Drain NMOS
	SDA	I^2C Serial Data Line (SDA)	Digital Input with Schmitt Trigger, Ultra-low Voltage Digital Input with Schmitt Trigger	Open-Drain NMOS
GPI5_SCL	GPI5	High Voltage General Purpose Input	Digital Input with Schmitt Trigger, Ultra-low Voltage Digital Input with Schmitt Trigger	-
	SCL	I^2C Serial Clock Line (SCL)	Digital Input with Schmitt Trigger, Ultra-low Voltage Digital Input with Schmitt Trigger	-
V_{IN2}	V_{IN2}	LDO2 Input	-	-

Pin Name	Signal Name	Function	Input Options	Output Options
V_{IN3}	V_{IN3}	LDO3 Input	-	-
V_{OUT1}	V_{OUT1}	LDO1 Output	-	-
V_{OUT2}	V_{OUT2}	LDO2 Output	-	-
V_{OUT3}	V_{OUT3}	LDO3 Output	-	-

Table 3. Pin Type Definitions

Pin Type	Description	Pin Type	Description
GPI	General Purpose Input	GPIO	General Purpose Input/Output
GPO	General Purpose Output	CS	Chip Select
DIWST	Digital Input with Schmitt Trigger	DIWOSH	Digital Input without Schmitt Trigger
LVDI	Low Voltage Digital Input	ULVDI	Ultra-low Voltage Digital Input
SDA	Serial Data	PU	Pull-Up Resistor
SCL	Serial Clock	PD	Pull-Down Resistor
PWR	Power	GND	Ground

2.3 Input Pins

2.3.1. CS – Chip Select

Chip select pin (active high) is used to wake the SLG51003 from a low-power reset state (SLEEP), see section 4.1 Main Operating States.

To guarantee correct operation, the CS must be de-asserted whenever the voltage at the V_{DD} pin is out of the operating conditions boundary (that is V_{DD} < 2.8 V, or V_{DD} > 5.0 V).

When de-asserting the CS pin, it can have a programmable shutdown debounce time from 0 µs to 256 µsselected by the CS_T_DEB register.

When the CS is de-asserted, digital section is forced to shut down, and any volatile memory is reset.

While the CS pin is high, the memory status can be checked with the MEM_STATUS bit. The MEM_STATUS bit is reset upon any of UVLO, CS de-assert, POR, over-temperature detection, or software reset request event. It allows the users to write high when loading configurations via I²C, therefore giving the possibility to check for any event that may affect integrity of the I²C written data.

2.3.2. GPI5 – General Purpose Input

GPI5_SCL is always an input pin. In the LOW_IQ_RESET state, GPI5_SCL is configured as an input with no pull-up/pull-down resistor. GPI5_SCL is I²C serial interface pin. The user-configurable input levels for I²C pins are from 1.2 V up to 5.0 V.

2.3.3. SCL – I²C Clock

The SCL signal is the I²C clock.

For details of the I²C interface, see section 4.13 I2C Interface.

2.4 Bidirectional Pins

2.4.1. GPIO1 to GPIO4 – General Purpose Input/Output

General purpose input/output pins are configurable by specific registers (IO_GPIO<x>_CONF). GPIO1 to GPIO4 pins, each can be configured as an input or an open-drain NMOS output. Each of GPIO1 to GPIO3 pins can also be configured as a push-pull output or open-drain PMOS output (GPI5_SCL is always an input pin).

In the LOW_IQ_RESET state, GPIO1 to GPIO3 are configured as inputs with 1 MΩ pull-down resistors. GPIO4 and GPI5_SCL are configured as inputs with no pull-up/pull-down resistor.

GPIO4 and GPI5_SCL are I²C serial interface pins. The user-configurable input levels for I²C pins are from 1.2 V up to 5.0 V.

GPIO1 to GPIO3 are high voltage pins and are supplied by V_{DDIO}. These pins can be configured as either inputs or outputs.

There are four input modes for GPIO1 to GPIO3:

- Digital input without Schmitt trigger (recommended operation input voltage range - 1.5 V to V_{DDIO})
- Digital input with Schmitt trigger (recommended operation input voltage range - 1.5 V to V_{DDIO})
- Low voltage digital input (recommended operation input voltage range - 1.5 V to V_{DDIO})
- Ultra-low voltage digital input (recommended operation input voltage range - 1.2 V to 1.5V).

And three output modes:

- Push-pull output
- NMOS open-drain output
- PMOS open-drain output.

Digital input without Schmitt trigger, digital input with Schmitt trigger, and low voltage digital input modes are designed for 1.5 V to V_{DDIO} input voltage range. Ultra-low voltage digital input mode is designed for 1.2 V to 1.8 V input voltage range, but can also be used up to V_{DDIO} voltage. The ultra-low voltage digital input mode has fixed V_{IH} and V_{IL} thresholds, unlike other modes, which V_{IH} and V_{IL} thresholds depend on V_{DDIO} voltage.
Also, GPIO1 to GPIO3 have internal pull-up/pull-down resistors (10 kΩ, 100 kΩ, 1 MΩ).

GPIO4_SDA and GPI5 are low voltage pins and can operate from 0 V up to 5.0 V. GPIO4_SDA can be configured as either an input (default) or an output (open-drain output). GPI5_SCL can be configured only as an input. GPIO4_SDA and GPI5_SCL can operate in two types of input modes. One is ultra-low voltage digital input with Schmitt trigger (recommended operation input voltage range - 1.2 V to 1.5 V) and digital input with Schmitt trigger (recommended operation input voltage range -1.8 V to V_{DDIO}).

GPIO4_SDA and GPI5_SCL are shared with I²C and are not available when using I²C.

The electrical characteristics for all GPIOs are listed in section 3.5.2 Logic IO .

2.4.2. SDA – I²C Data

The SDA signal is the I²C data signal. It is an open-drain signal, so that either side can pull it down to a logic low level. For details of the I²C interface, see section 4.13 I2C Interface.

3. Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to the absolute maximum conditions for extended periods may affect the device reliability.

Parameter		Min	Max	Unit
Power Supply Voltage on V_{DD} Pin		-0.3	6.0	V
Power Supply Voltage on V_{DDIO} Pin		-0.3	V_{DD}	V
Power Supply Voltage on V_{IN2}, V_{OUT1}, V_{OUT2} Pins		-0.3	6.0	V
Power Supply Voltage on V_{IN3} Pin		-0.3	1.8	V
Voltage on V_{OUT3} Pin		-0.3	1.65	V
Voltage on GPIO4_SDA and GPI5_SCL Pins		-0.3	V_{DDIO} + 0.3	V
Voltage on GPIO1 to GPIO3 Pins		-0.3	V_{DDIO} + 0.3	V
Voltage on CS Pin		-0.3	V_{DD} + 0.3	V
Voltage on LDO Output Pins		-0.3	V_{IN} + 0.3	V
Maximum Average or DC Current through V_{IN3} or V_{OUT3} Pin	T_J = +100 °C	-	1.0	A
	T_J = +110 °C	-	0.9	A
Ambient Temperature		-40	+85	°C
Junction Temperature		-25	+125	°C
Storage Temperature Range		-40	+150	°C

3.1.1. Guidelines for Reliable Operation

- I²C Serial Interface Pins (GPIO4_SDA and GPI5_SCL): the I²C pins must not exceed their ABSMAX ratings, even briefly. Transients, both positive (above max) and negative (below min) can cause Electrical Overstress (EOS) damage.
- Power Sequencing: the CS pin should be held low before V_{DD} is powered up. The CS pin should also be pulled low before V_{DD} falls out of operating range. The input supplies for LDO_HP, LDO_HV, and LDO_LV channels can be safely biased, even if the V_{DD} is not present. The input supplies should be powered up before enabling their respective LDO channels. The I²C pins (GPIO4_SDA and GPI5_SCL) configured as inputs are allowed to be forced high before the V_{DD} is powered up. All other GPIOs are not allowed to be forced high before the V_{DD} and the V_{DDIO} are powered up.
- Outputs of LDOs should not exceed their respective input voltages.
- Voltage at the V_{DDIO} should not exceed the V_{DD} voltage. The V_{DDIO} and V_{DD} pins can be tied together.

3.2 ESD Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	-	2000	V
ESD Protection (Charged Device Model)	-	500	V

3.3 Recommended Operating Conditions

Parameter		Min	Max	Unit
Power Supply Voltage on V_{DD} Pin		2.8	5.0	V
Power Supply Voltage on V_{DDIO} Pin		1.2	V_{DD}	V
Power Supply Voltage on V_{IN2} Pin		1.7	5.0	V
Power Supply Voltage on V_{IN3} Pin	LDO Mode	0.8	1.5	V
	Load Switch Mode	0.5	1.4	V
Voltage on GPIO4_SDA and GPI5_SCL Pins		0	V_{DDIO}	V
Voltage on GPIO1 to GPIO3 Pins		-0.3	V_{DDIO}	V
Voltage on CS Pin		-0.3	V_{DD}	V
Operating Ambient Temperature Range		-40	+85	°C

3.4 Thermal Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Junction-to-Ambient Thermal Resistance [1]	θ_{JA}		-	55.4	-	°C/W
Continuous Power Dissipation	P_{D_CONT}	TQFN-14 (Derate 18 mW/°C above T_A = +25 ºC) JESD51-7, T_A = +25ºC	-	-	2250	mW

1. Obtained from package thermal simulation, board dimension 76.2 mm x 114.3 mm x 1.6 mm (JEDEC), 4-layer board. All layers are 35 µm thick, 60 % and 40 % of Cu thermal conductivity for external and internal layers, respectively. Nine thermal vias are applied. The geometry of thermal via is 0.3 mm diameter, 25 µm Cu plating, and 1.2 mm pitch. Natural convection (still air).

3.5 Electrical Specifications

3.5.1. CS Pin Logic IO Specifications

V_{DD} = 2.8 V to 5.0 V, T_A = -40 °C to +85 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CS Pin High-Level Input Voltage	V_{IH}		0.9	-	V_{DD}	V
CS Pin Low-Level Input Voltage	V_{IL}		0	-	0.2	V
CS Pin Input Leakage Current	I_{LKG}	CS < 2 V	-	-	1	µA
Turn-on Time from CS HIGH to Ready State	t_{ON_READY}		-	-	10	ms

3.5.2. Logic IO Specifications

V_{DD} = 2.8 V to 5.0 V, T_A = -40 °C to +85 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GPIO1 to GPIO3						
High-Level Input Voltage	V_{IH}	Digital Input without Schmitt Trigger Mode[1]	0.7 x V_{DDIO}	-	-	V
		Digital Input with Schmitt Trigger Mode [1]	0.8 x V_{DDIO}	-	-	
		Low Voltage Digital Input Mode [1]	1.25	-	-	
		Ultra-Low Voltage Digital Input Mode [1]	1.05	-	-	
Low-Level Input Voltage	V_{IL}	Digital Input without Schmitt Trigger Mode[1]	-	-	0.3 x V_{DDIO}	V
		Digital Input with Schmitt Trigger Mode [1]	-	-	0.2 x V_{DDIO}	
		Low Voltage Digital Input Mode [1]	-	-	0.5	
		Ultra-Low Voltage Digital Input Mode [1]	-	-	0.45	
High-Level Output Voltage	V_{OH}	Push-Pull, PMOS OD, I_{OH} = 100 µA, V_{DD} = 2.8 V, V_{DDIO} = 1.2 V	1.18	-	-	V
		Push-Pull, PMOS OD, I_{OH} = 100 µA, V_{DD} = 2.8 V, V_{DDIO} = 1.8 V	1.6	-	-	
		Push-Pull, PMOD OD, I_{OH} = 1 mA, V_{DD} = 2.8 V, V_{DDIO} = 2.8 V	2.71	-	-	
		Push-Pull, PMOS OD, I_{OH} = 3 mA, V_{DD} = 3.8 V, V_{DDIO} = 3.8 V	3.17	-	-	
		Push-Pull, PMOS OD, I_{OH} = 5 mA, V_{DD} = 5.0 V, V_{DDIO} = 5.0 V	4.19	-	-	
Low-Level Output Voltage	V_{OL}	Push-Pull, I_{OL} = 100 µA, V_{DD} = 2.8 V, V_{DDIO} = 1.2 V	-	-	0.005	V
		Push-Pull, I_{OL} = 100 µA, V_{DD} = 2.8 V, V_{DDIO} = 1.8 V	-	-	0.005	
		Push-Pull, I_{OL} = 1 mA, V_{DD} = 2.8 V, V_{DDIO} = 2.8 V	-	-	0.05	
		Push-Pull, I_{OL} = 3 mA, V_{DD} = 3.8 V, V_{DDIO} = 3.8 V	-	-	0.13	
		Push-Pull, I_{OL} = 5 mA, V_{DD} = 5.0 V, V_{DDIO} = 5.0 V	-	-	0.18	
		NMOS OD, I_{OL} = 100 µA, V_{DD} = 2.8 V, V_{DDIO} = 1.2 V	-	-	0.004	
		NMOS OD, I_{OL} = 100 µA, V_{DD} = 2.8 V, V_{DDIO} = 1.8 V	-	-	0.004	
		NMOS OD, I_{OL} = 1 mA, V_{DD} = 2.8 V, V_{DDIO} = 2.8 V	-	-	0.04	

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		NMOS OD, I_{OL} = 3 mA, V_{DD} = 3.8 V, V_{DDIO} = 3.8 V	-	-	0.1	
		NMOS OD, I_{OL} = 5 mA, V_{DD} = 5.0 V, V_{DDIO} = 5.0 V	-	-	0.13	
High-Level Output Current	I_{OH}	Push-Pull, PMOS OD, V_{OH} = V_{DDIO}-0.2 V, V_{DD} = 2.8 V, V_{DDIO} = 1.2 V	1.15	-	-	mA
		Push-Pull, PMOS OD, V_{OH} = V_{DDIO}-0.2 V, V_{DD} = 2.8 V, V_{DDIO} = 1.8 V	1	-	-	
		Push-Pull, PMOS OD, V_{OH} = 2.4 V, V_{DD} = 2.8 V, V_{DDIO} = 2.8 V	4.3	-	-	
		Push-Pull, PMOS OD, V_{OH} = 2.4 V, V_{DD} = 3.8 V, V_{DDIO} = 3.8 V	11.3	-	-	
		Push-Pull, PMOS OD, V_{OH} = 2.4 V, V_{DD} = 5.0 V, V_{DDIO} = 5.0 V	25.1	-	-	
Low-Level Output Current	IOL	Push-Pull, V_{OL} = 0.15 V, V_{DD} = 2.8 V, V_{DDIO} = 1.2 V	3.48	-	-	mA
		Push-Pull, V_{OL} = 0.15 V, V_{DD} = 2.8 V, V_{DDIO} = 1.8 V	3.48	-	-	
		Push-Pull, V_{OL} = 0.15 V, V_{DD} = 2.8 V, V_{DDIO} = 2.8 V	3.48	-	-	
		Push-Pull, V_{OL} = 0.4 V, V_{DD} = 3.8 V, V_{DDIO} = 3.8 V	10.03	-	-	
		Push-Pull, V_{OL} = 0.4 V, V_{DD} = 5.0 V, V_{DDIO} = 5.0 V	11.4	-	-	
		NMOS, V_{OL} = 0.15 V, V_{DD} = 2.8 V, V_{DDIO} = 1.2 V	4.64	-	-	
		NMOS, V_{OL} = 0.15 V, V_{DD} = 2.8 V, V_{DDIO} = 1.8 V	4.64	-	-	
		NMOS, V_{OL} = 0.15 V, V_{DD} = 2.8 V, V_{DDIO} = 2.8 V	4.64	-	-	
		NMOS, V_{OL} = 0.4 V, V_{DD} = 3.8 V, V_{DDIO} = 3.8 V	13.4	-	-	
		NMOS, V_{OL} = 0.4 V, V_{DD} = 5.0 V, V_{DDIO} = 5.0 V	15.2	-	-	
Pull-up or Pull-down Resistance	R_{PULL}	1 MΩ for Pull-Up: V_{IN} = GND; For Pull-Down: V_{IN} = V_{DDIO}	-	1	-	MΩ
		100 kΩ for Pull-Up: V_{IN} = GND; For Pull-Down: V_{IN} = V_{DDIO}	-	100	-	kΩ
		10 kΩ for Pull-Up: V_{IN} = GND; For Pull-Down: V_{IN} = V_{DDIO}	-	10	-	kΩ
Input Leakage	I_{LKG}		-	-	500	nA
Input Capacitance	C_{IN}		-	4	-	pF

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GPIO4_SDA and GPI5_SCL						
High-Level Input Voltage	V_{IH}	I²C Mode: V_{DDBUS} = 1.2 V [1]	0.7 x V_{DDBUS}	-	-	V
Low-Level Input Voltage	V_{IL}		-	-	0.3 x V_{DDBUS}	V
Schmitt Trigger Hysteresis	V_{HYS}		0.05 x V_{DDBUS}	-	-	V
Output Low Voltage GPIO4_SDA	V_{OL}	$I_{OUT} \le I_{OL}$, I²C Mode: V_{DDBUS} = 1.2 V	0	-	0.2	V
		$I_{OUT} \le I_{OL}$, I²C Mode: V_{DDBUS} = 1.5 V to 5.0 V	0	-	0.4	V
Output Current	I_{OL}	V_{OL} = 0.4 V	3	-	-	mA
Input Leakage	I_{LKG}		-	-	500	nA
Pin Capacitance	C_{IN}		-	-	10	pF

1. See section 2.4.1 GPIO1 to GPIO4 – General Purpose Input/Output with recommended operation input voltage range.
2. V_{DDBUS} defines the voltage thresholds for I²C pins (GPIO4_SDA, GPI5_SCL) and can be set in a range between 1.2 V to 5.0 V.

3.5.3. Estimated Typical Current Consumption

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current Consumption in SLEEP. I_{Q_SLEEP} is the I_Q in LOW_IQ_RESET State	I_{Q_SLEEP}	V_{DD} = 3.8 V, All References Disabled, I²C Interface Disabled, All Output Rails Disabled	-	0.24	-	µA
Current Consumption in READY State	$I_{Q\_READY\_DIS}$	V_{DD} = 3.8 V, All References Enabled, I²C Interface Enabled, All Output Rails Disabled	-	14	-	µA
Current Consumption in READY State	$I_{Q\_READY\_EN}$	V_{DD} = 3.8 V, All References Enabled, I²C Interface Enabled, All Output Rails Enabled, No Load	-	300	-	µA

3.5.4. Estimated Typical Delay

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Delay for Digital Input without Schmitt Trigger to PP	t_{PD}	V_{DD} = 2.8 V, Rising	-	17	-	ns
		V_{DD} = 2.8 V, Falling	-	16	-	
		V_{DD} = 3.3 V, Rising	-	15	-	
		V_{DD} = 3.3 V, Falling	-	13	-	
		V_{DD} = 5.0 V, Rising	-	14	-	
		V_{DD} = 5.0 V, Falling	-	12	-	
Delay for Digital Input with Schmitt Trigger to PP	t_{PD}	V_{DD} = 2.8 V, Rising	-	17	-	ns
		V_{DD} = 2.8 V, Falling	-	16	-	
		V_{DD} = 3.8 V, Rising	-	15	-	
		V_{DD} = 3.8 V, Falling	-	13	-	
		V_{DD} = 5.0 V, Rising	-	14	-	
		V_{DD} = 5.0 V, Falling	-	12	-	
Delay for Low Voltage Digital Input to PP	t_{PD}	V_{DD} = 2.8 V, Rising	-	34	-	ns
		V_{DD} = 2.8 V, Falling	-	149	-	
		V_{DD} = 3.8 V, Rising	-	41	-	
		V_{DD} = 3.8 V, Falling	-	67	-	
		V_{DD} = 5.0 V, Rising	-	52	-	
		V_{DD} = 5.0 V, Falling	-	38	-	
Delay for Ultra-Low Voltage Digital Input to PP	t_{PD}	V_{DD} = 2.8 V, V_{DDIO} = 1.2 V, Rising	-	29	-	ns
		V_{DD} = 2.8 V, V_{DDIO} = 1.2 V, Falling	-	32	-	
		V_{DD} = 3.8 V, V_{DDIO} = 1.2 V, Rising	-	28	-	
		V_{DD} = 3.8 V, V_{DDIO} = 1.2 V, Falling	-	30	-	
		V_{DD} = 5.0 V, V_{DDIO} = 1.2 V, Rising	-	28	-	
		V_{DD} = 5.0 V, V_{DDIO} = 1.2 V, Falling	-	29	-	
Delay for Ultra-Low Voltage Digital Input to PP	t_{PD}	V_{DD} = 2.8 V, V_{DDIO} = 1.8 V, Rising	-	30	-	ns
		V_{DD} = 2.8 V, V_{DDIO} = 1.8 V, Falling	-	32	-	
		V_{DD} = 3.8 V, V_{DDIO} = 1.8 V, Rising	-	28	-	
		V_{DD} = 3.8 V, V_{DDIO} = 1.8 V, Falling	-	30	-	
		V_{DD} = 5.0 V, V_{DDIO} = 1.8 V, Rising	-	28	-	
		V_{DD} = 5.0 V, V_{DDIO} = 1.8 V, Falling	-	29	-	
Delay for Digital Input without Schmitt Trigger to NMOS OD	t_{PD}	V_{DD} = 2.8 V, Falling	-	16	-	ns
		V_{DD} = 3.8 V, Falling	-	13	-	
		V_{DD} = 5.0 V, Falling	-	12	-	
Delay for Digital Input without Schmitt Trigger to PMOS OD	t_{PD}	V_{DD} = 2.8 V, Rising	-	17	-	ns
		V_{DD} = 3.8 V, Rising	-	15	-	
		V_{DD} = 5.0 V, Rising	-	14	-	

3.5.5. LDO_HP (LDO1) Specifications

3.5.5.1. LDO Mode Specifications

V_{DD} = 2.8 V to 5.0 V, C_{OUT1} = 4.7 µF, LDO1_SNS_REMOTE = 0x0, T_A = -40 °C to +85 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
Input Voltage	V_{DD}		2.8	-	5	V
Output Capacitance	$C_{OUT(EFF)}$	Effective Capacitance after Derating	2.2	-	10	µF
Maximum Output Current	I_{OUT_MAX}	V_{DD} = 3.3 V, V_{OUT} drops by 50 mV	475	-	-	mA
Static Parameters						
Nominal Output Voltage [1]	V_{OUT}	5 mV LSB of Programming DAC (8-bit Control)	2.4	-	3.3	V
Part to Part Output Voltage Accuracy [2]	V_{OUT_PP}	I_{OUT} = 1 mA, T_A = +25 °C	-5	-	5	mV
V_{OUT} Temperature Dependency [2]	V_{OUT_TEMP}	I_{OUT} = 1 mA	-0.65	-	0.65	%
Static Line Regulation [2]	$V_{OUT\_STATIC\_LINE}$	I_{OUT} = 1 mA, V_{DD} = V_{OUT} + $V_{DROPOUT\_MAX}$ to V_{DD_MAX}	-4.1	-	4.6	mV
Static Load Regulation [2]	$V_{OUT\_STATIC\_LD}$	2 mA < I_{OUT} < 300 mA	-9.1	-	6.0	mV
Dropout Voltage	$V_{DROPOUT}$	V_{OUT} = V_{OUT} (V_{DD_MAX}) - 10 mV, I_{OUT} = 300 mA	-	-	200	mV
Output Discharge (Pull-Down) Resistance	R_{PD_OFF}	V_{OUT} = 0.5 V, LDO Disabled	-	40	-	Ω
Functional Current Limit	$I_{OUT\_FUNC\_LIM}$		500	-	-	mA
Dynamic Parameters						
Line Transient Response	$V_{OUT\_TR\_LINE}$	V_{DD} = V_{OUT} + $V_{DROPOUT\_MAX}$ + 100 mV to V_{OUT} + $V_{DROPOUT\_MAX}$, V_{OUT} = 2.85 V, I_{OUT} = 300 mA, t_R = t_F = 1 µs	-	-	0.3	mV
Load Transient Response	$V_{OUT\_TR\_LD\_1mA}$	V_{DD} = V_{OUT} + $V_{DROPOUT\_MAX}$, V_{OUT} = 2.85 V, I_{OUT} = 1 mA to 300 mA, t_R = t_F = 1 µs	-	30	-	mV
Turn-On Time	t_{ON}	Time from LDO Enable Command to 90 % of V_{OUT}, I_{OUT} = 0 mA	-	0.4	-	ms
Turn-Off Time	t_{OFF}	Time from LDO Enable Command to 10 % of V_{OUT}, I_{OUT} = 0 mA	-	-	2	ms
AC Parameters						
Power Supply Rejection Ratio	PSRR 1kHz	f = 1 kHz, V_{DD} = 3.2 V [3], V_{OUT} = 2.85 V, I_{OUT} = 150 mA, Cin = 7.8 µF, $C_{OUT(EFF)}$ = 4.7 µF	-	98.5	-	dB
Power Supply Rejection Ratio	PSRR 100kHz	f = 100 kHz, V_{DD} = 3.2 V [3], V_{OUT} = 2.85 V, I_{OUT} = 150 mA, Cin = 7.8 µF, C_{OUT} = 4.7 µF	-	88	-	dB
Power Supply Rejection Ratio	PSRR 1MHz	f = 1 MHz, V_{DD} = 3.2 V [3], V_{OUT} = 2.85 V, I_{OUT} = 150 mA, Cin = 7.8 µF, C_{OUT} = 4.7 µF	-	68	-	dB

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Noise	V_N 100kHz	f = 10 Hz to 100 kHz, V_{IN} = 3.2 V, V_{OUT} = 2.85 V, I_{OUT} > 30 mA	-	16	-	µV
Output Noise	V_N 1MHz	f = 10 Hz to 1 MHz, V_{IN} = 3.2 V, V_{OUT} = 2.85 V, I_{OUT} > 10 mA	-	32	-	µV
Quiescent Current Specifications						
Quiescent Current	$I_{Q\_ON\_0mA}$	I_{OUT} = 0 mA	-	170	250	µA
Quiescent Current	$I_{Q\_ON\_1mA}$	I_{OUT} = 1 mA	-	200	260	µA
Quiescent Current	$I_{Q\_ON\_300mA}$	I_{OUT} = 300 mA	-	2.8	3.2	mA
1. For programmable selections, refer to section 6 I2C Serial Command Register Map. 2. The overall accuracy can be calculated by summing V_{OUT_PP} + V_{OUT_TEMP} + $V_{OUT\_STATIC\_LD}$ + $V_{OUT\_STATIC\_LINE}$. 3. For V_{DD} - V_{OUT} < 350 mV, PSRR will be degraded.						

3.5.6. LDO_HV (LDO2) Specifications

3.5.6.1. LDO Mode Specifications

V_{DD} = 2.8 V to 5.0 V, C_{OUT2} = 2.2 µF, T_A = -40 °C to +85 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
Input Voltage	V_{IN}		1.7	-	5	V
Output Capacitance	$C_{OUT(EFF)}$	Effective Capacitance after Derating	0.45	-	20	µF
Maximum Output Current	I_{OUT_MAX}	V_{OUT} drops by 50 mV [1]	500	-	-	mA
Static Parameters						
Nominal Output Voltage [2]	V_{OUT}	10 mV LSB of Programming DAC (8-bit Control)	1.2	-	3.75	V
Part to Part Output Voltage Accuracy [3]	V_{OUT_PP}	I_{OUT} = 1 mA, T_A = +25 °C	-10 [4]	-	10 [4]	mV
V_{OUT} Temperature Dependency [3]	V_{OUT_TEMP}	I_{OUT} = 1 mA [5]	-0.65	-	0.65	%
Static Line Regulation [3]	$V_{OUT\_STATIC\_LINE}$	I_{OUT} = 1 mA, V_{IN} = V_{OUT} + $V_{DROPOUT\_MAX}$ to V_{IN_MAX}	-2	-	2	mV
Static Load Regulation [3]	$V_{OUT\_STATIC\_LD}$	1 mA < I_{OUT} < I_{OUT_MAX}	-6	-	2	mV
Dropout Voltage	$V_{DROPOUT}$	V_{OUT} = V_{OUT} (V_{IN_MAX}) - 10 mV, I_{OUT} = 230 mA, V_{IN} > 1.8 V	-	-	200 [6]	mV
		V_{OUT} = V_{OUT} (V_{IN_MAX}) - 10 mV, I_{OUT} = 300 mA, V_{IN} > 1.9 V	-	-	240 [6]	mV
		V_{OUT} = V_{OUT} (V_{IN_MAX}) - 10 mV, I_{OUT} = 300 mA, V_{IN} > 3 V	-	-	120 [6]	mV
Slew Rate [2]	SR	SEL_RAMP = 0x6	20.3	25	28.7	mV/us
Output Discharge (Pull-Down) Resistance [2]	R_{PD_OFF}	SEL_PULLDN = 0x7, VOUT = 0.5 V, LDO Disabled	22	37.5	70.3	Ω
Dynamic Parameters						
Line Transient Response	$V_{OUT\_TR\_LINE}$	V_{IN} = V_{OUT} + $V_{DROPOUT\_MAX}$ + 0.6 V to V_{OUT} + $V_{DROPOUT\_MAX}$, V_{OUT} = 3.3 V, I_{OUT} = I_{OUT_MAX}, t_R = t_F = 100 mV/µs	-	2	5 [7]	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Load Transient Response	$V_{OUT\_TR\_LD\_1mA}$	V_{IN} = V_{OUT} + $V_{DROPOUT\_MAX}$, V_{OUT} = 3.3 V, I_{OUT} = 1 mA to I_{OUT_MAX} / 2, t_R = t_F = 1 µs	-	28	-	mV
Turn-On Time	t_{ON}	Time from LDO Enable Command to 90 % of V_{OUT}, I_{OUT} = 0 mA, SR = 100 mV/µs [8]	-	0.15	-	ms
Turn-Off Time	t_{OFF}	Time from LDO Enable Command to 10 % of V_{OUT}, I_{OUT} = 0 mA, R_{PD_OFF} = 100Ω	-	0.8	10	ms
AC Parameters						
Power Supply Rejection Ratio	PSRR 1kHz	f = 1 kHz, V_{IN} = V_{OUT} + 500 mV, V_{OUT} = 3.3 V, I_{OUT} = I_{OUT_MAX} / 2, C_{OUT} = 4.7 µF	-	83	-	dB
Power Supply Rejection Ratio	PSRR 100kHz	f = 100 kHz, V_{IN} = V_{OUT} + 500 mV, V_{OUT} = 3.3 V, I_{OUT} = I_{OUT_MAX} / 2, C_{OUT} = 4.7 µF	-	56	-	dB
Power Supply Rejection Ratio	PSRR 1MHz	f = 1 MHz, V_{IN} = V_{OUT} + 500 mV, V_{OUT} = 3.3 V, I_{OUT} = I_{OUT_MAX} / 2, C_{OUT} = 4.7 µF	-	47	-	dB
Power Supply Rejection Ratio	PSRR 2MHz	f = 2 MHz, V_{IN} = V_{OUT} + 500 mV, V_{OUT} = 3.3 V, I_{OUT} = I_{OUT_MAX} / 2, C_{OUT} = 4.7 µF	-	40	-	dB
Output Noise	V_N	f = 10 Hz to 100 kHz, I_{OUT} = I_{OUT_MAX} / 2	-	152	-	µV
Current Sink						
Current Sink at Over-voltage	I_{OV_SINK}	V_{OV} = V_{OUT} + 100 mV [9]	10	77	-	mA
Quiescent Current Specifications						
Quiescent Current	$I_{Q\_ON\_0mA}$	I_{OUT} = 0 mA [10]	-	13	19	µA
Quiescent Current	$I_{Q\_ON\_1mA}$	I_{OUT} = 1 mA [10]	-	36	48	µA
Quiescent Current	$I_{Q\_ON\_IMAX}$	I_{OUT} = I_{OUT_MAX} [10]	-	1.7	3.5	mA

1. Guaranteed for V_{IN} > 2.1 V. For 1.7 V ≤ V_{IN} ≤ 2.1 V, the I_{OUT_MAX} guaranteed is 200 mA.
2. For programmable selections, refer to section 6 I2C Serial Command Register Map.
3. The overall accuracy can be calculated by summing V_{OUT_PP} + V_{OUT_TEMP} + $V_{OUT\_STATIC\_LD}$ + $V_{OUT\_STATIC\_LINE}$.
4. ±10 mV accuracy applies to factory-trimmed V_{OUT} values targeted between 1.23 V to 3.72 V. V_{OUT} targets from 1.20 V to 1.22 V can be trimmed to +24 mV/-10 mV accuracy. V_{OUT} targets from 3.73 V to 3.75 V can be trimmed to +10 mV/-30 mV accuracy.
5. Guaranteed for V_{IN} ≥ 2.5 V.
6. Dropout voltage is linear for the same V_{IN} voltage with the load current, if using lower I_{OUT_MAX} than specified.
7. Guaranteed for V_{IN} > 2.1 V. Otherwise, maximum line transient is 20 mV.
8. For slew rate set at 100 mV/us, V_{OUT} = 3.3 V.
9. Guaranteed for V_{IN} > 2.35 V.
10. The internal regulator current flowing to ground.

3.5.7. LDO_LV (LDO3) Specifications

3.5.7.1. LDO Mode Specifications

V_{DD} = 2.8 V to 5.0 V, C_{OUT3} = 10 µF, T_A = -40 °C to +85 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
Input Supply (Pass Device + Part of Controller)	V_{IN}		0.8	-	1.5	V
Output Capacitance	$C_{OUT(EFF)}$	Effective Capacitance after Derating	4 [1]	-	80	µF

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Capacitor Series Inductance	ESL_{COUT}	f > 100 kHz	-	-	1	nH
Maximum Output Current	I_{OUT_MAX}	V_{OUT} drops by 50 mV	800 [2]	-	- [3]	mA
Static Parameters						
Nominal Output Voltage [4]	V_{OUT}	5 mV LSB of Programming DAC (8-bit Control)	0.5 [5]	-	1.4	V
Part to Part Output Voltage Accuracy [6]	V_{OUT_PP}	I_{OUT} = 1 mA, T_A = +25 °C	-5	-	5	mV
V_{OUT} Temperature Dependency [6]	V_{OUT_TEMP}	I_{OUT} = 1 mA	-1.1	-	1.1	%
Static Line Regulation [6]	$V_{OUT\_STATIC\_LINE}$	I_{OUT} = 1 mA, V_{IN} = V_{OUT} + $V_{DROPOUT\_MAX}$ to V_{IN_MAX}	-2	-	2	mV
Static Load Regulation [6]	$V_{OUT\_STATIC\_LD}$	1 mA < I_{OUT} < 800 mA	-11	-	1	mV
Dropout Voltage	$V_{DROPOUT}$	V_{OUT} = V_{OUT} (V_{IN_MAX}) - 10 mV, I_{OUT} = 800 mA	-	-	100 [7]	mV
Current Limit Accuracy [4]	I_{LIM_ACC}	SEL_FUNC_ILIM = 0x23 to 0x76	-30	-	40	%
Slew Rate [4]	SR	SEL_RAMP = 0x6, V_{OUT} = 1.175 V	21.1	25	28.8	mV/us
Output Discharge (Pull-Down) Resistance [4]	R_{PD_OFF}	SEL_PULLDN = 0x7, VOUT = 0.5 V, LDO Disabled	22	37.5	70.3	Ω
Dynamic Parameters						
Line Transient Response	$V_{OUT\_TR\_LINE}$	V_{IN} = V_{OUT} + $V_{DROPOUT\_MAX}$ + 100 mV to V_{OUT} + $V_{DROPOUT\_MAX}$, V_{OUT} = 1.175 V, I_{OUT} = 800 mA, t_R = t_F = 100 mV/µs	-	2	5	mV
Load Transient Response	$V_{OUT\_TR\_LD\_1mA}$	V_{IN} = V_{OUT} + $V_{DROPOUT\_MAX}$, V_{OUT} = 1.175 V, I_{OUT} = 1 mA to 500 mA, t_R = t_F = 1 µs	-	21	29	mV
Turn-On Time	t_{ON}	Time from LDO Enable Command to 90 % of V_{OUT} = 1.175 V, I_{OUT} = 0 mA, C_{OUT} = 20 µF [8]	-	0.2	-	ms
Turn-Off Time	t_{OFF}	Time from LDO Enable Command to 10 % of V_{OUT} = 1.175 V, I_{OUT} = 0 mA, C_{OUT} = 20 µF, R_{PD_OFF} = 380 Ω	-	2	5 [9]	ms
AC Parameters						
Power Supply Rejection Ratio	PSRR 1kHz	f = 1 kHz, V_{IN} = V_{OUT} + $V_{DROPOUT\_MAX}$ + 200 mV, V_{OUT} = 1.175 V, I_{OUT} = 500 mA, C_{OUT} = 20 µF	-	70	-	dB
Power Supply Rejection Ratio	PSRR 100kHz	f = 100 kHz, V_{IN} = V_{OUT} + $V_{DROPOUT\_MAX}$ + 200 mV, V_{OUT} = 1.175 V, I_{OUT} = 500 mA, C_{OUT} = 20 µF	-	50	-	dB
Power Supply Rejection Ratio	PSRR 1MHz	f = 1 MHz, V_{IN} = V_{OUT} + $V_{DROPOUT\_MAX}$ + 200 mV, V_{OUT} = 1.175 V, I_{OUT} = 500 mA, C_{OUT} = 20 µF	-	40	-	dB
Output Noise	V_N	f = 10 Hz to 100 kHz, I_{OUT} = 500 mA	-	100	-	µV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current Sink						
Current Sink at Over-voltage	I_{OV_SINK}	$V_{OV} = V_{OUT}$ + 100 mV	10	-	-	mA
Quiescent Current Specifications						
Quiescent Current	$I_{Q\_ON\_0mA}$	I_{OUT} = 0 mA [10]	-	8	15	µA
Quiescent Current	$I_{Q\_ON\_1mA}$	I_{OUT} = 1 mA [10]	-	10	16	µA
Quiescent Current	$I_{Q\_ON\_IMAX}$	$I_{OUT} = I_{OUT\_MAX}$ [10]	-	0.42	1.5	mA

1. For currents less than 400 mA, a minimum of 1.2 µF (after derating) can be used.
2. $I_{OUT\_MAX} \geq$ 500 mA guaranteed for (V_{IN} - V_{OUT}) ≤ 300 mV.
3. For I_{OUT_MAX}, see $I_{MAX\_LDO\_LV}$ in Absolute Maximum Ratings table.
4. For programmable selections, refer to section 6 I2C Serial Command Register Map.
5. The output can be lowered to 0.4 V at reduced accuracy. Please contact Renesas Electronics Corporation for more information.
6. The overall accuracy can be calculated by summing V_{OUT_PP} + V_{OUT_TEMP} + $V_{OUT\_STATIC\_LD}$ + $V_{OUT\_STATIC\_LINE}$.
7. The dropout voltage is linear with the load current. If using lower I_{OUT_MAX} than specified, the dropout can be calculated using 10 mV per 100 mA of load.
8. For slew rate set at 100 mV/us, V_{OUT} = 1.175 V.
9. Max t_{OFF} of 20 ms achieved for C_{OUT} = 80 µF.
10. The internal regulator current flowing to ground.

3.5.7.2. Load Switch Mode Specifications

V_{DD} = 2.8 V to 5.0 V, C_{OUT3} = 10 µF, T_A = -40 °C to +85 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
Input Voltage	V_{IN}		0.5 [1]	-	1.4	V
Maximum Output Current	I_{OUT_MAX}		800	-	-	mA
Electrical Performance						
On Resistance	R_{ON}		-	40	-	mΩ
Quiescent Current in OFF Mode	I_{Q_OFF}	T_A = +25 °C	-	2	-	µA
Current Limit Accuracy [2]	I_{LIM_ACC}	SEL_FUNC_ILIM = 0x23 to 0x76	-30	-	40	%
Slew rate [2]	SR	SEL_BYP_SLEW_RATE = 0x3, V_{OUT} = 1.175 V	6.6	10	13.4	mV/us
Output Discharge (Pull-Down) Resistance [2]	R_{PD_OFF}	SEL_PULLDN = 0x7, VOUT = 0.5 V, LDO Disabled	22	37.5	70.3	Ω

1. The SEL_BYP_VGATE register bit must be set to 0 for V_{IN} between 0.5 V and 0.8 V, and is recommended to be set to 1 for V_{IN} between 0.8 V and 1.25 V.
2. For programmable selections, refer to section 6 I2C Serial Command Register Map.

3.5.8. V_{REF}, I_{REF}, Temperature Supervision Specifications

V_{DD} = 2.8 V to 5.0 V, T_A = -40 °C to +85 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference Voltage [1]	V_{REF}	Internal V_{REF}	-	1.2	-	V
Warning Temperature Threshold [1]	T_{WARN}	REFGEN_SEL_TEMP_WARN_THR = 0x0	-	90	-	°C
Electrical Performance						
Reference Voltage Accuracy	V_{REF_ACC}	Internal V_{REF}	-1	-	1	%
Thermal Shutdown Threshold	T_{OT}		125	140	155	°C
Warning Temperature Threshold Accuracy	T_{WARN_ACC}		-5	-	5	°C
1. For programmable selections, refer to section 6 I2C Serial Command Register Map.						

3.5.9. Internal Oscillator Specifications

V_{DD} = 2.8 V to 5.0 V, T_A = -40 °C to +85 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Clock Frequency	f_{CLK}		7.2	8	8.8	MHz

3.5.10. UVLO Specifications

V_{DD} = 2.8 V to 5.0 V, T_A = -40 °C to +85 °C, typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Undervoltage Lockout Threshold [1]	V_{DD_UVLO}	VMON_UVLO_SEL_THR = 0x1B	2.62	2.658	2.79	V
Electrical Performance						
Deep Discharge Lockout Upper Threshold	$V_{DD\_POR\_UPPER}$		-	2.1	2.2	V
Deep Discharge Lockout Lower Threshold	$V_{DD\_POR\_LWR}$		-	1.9	-	V
Undervoltage Lower Threshold Static Accuracy with Flip Gate Bandgap Reference	$V_{DD\_UVLO\_STAT\_ACC}$		-1.5	-	1.5	%
1. For programmable selections, refer to section 6 I2C Serial Command Register Map.						

4. Functional Description

4.1 Main Operating States

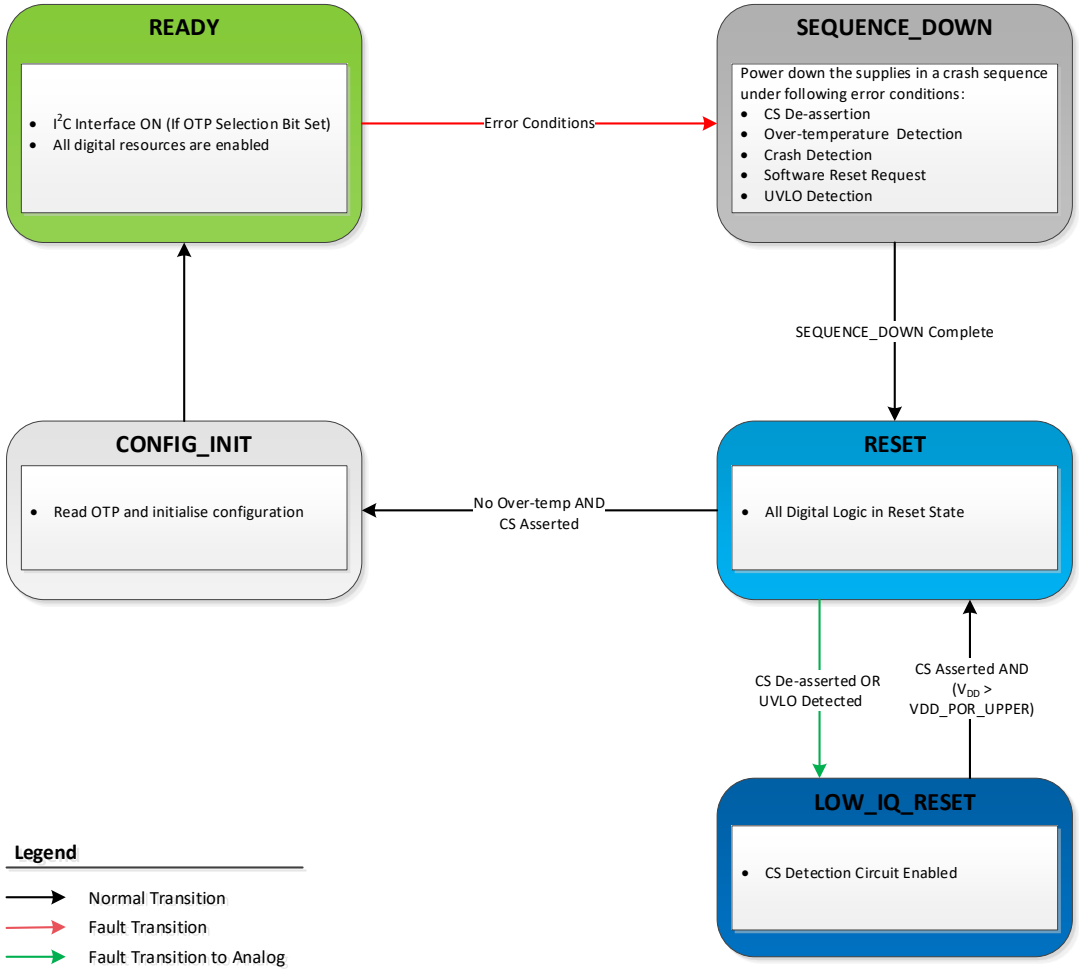


Figure 4. System State Machine Diagram

4.1.1. LOW_IQ_RESET

If the CS is de-asserted or UVLO is detected, the SLG51003 enters its lowest power state (LOW_IQ_RESET) and the device is disabled. It cannot leave LOW_IQ_RESET state while the CS is de-asserted.

4.1.2. RESET

RESET state can be entered from:

- SEQUENCE_DOWN: if there was an error due to over-temperature, crash detect event, UVLO detection, or a software reset was requested via I²C (if enabled), any enabled supplies will be disabled.
- LOW_IQ_RESET: following assertion of the CS and the V_{DD} > VDD_POR_UPPER.

By entering RESET state, all digital logics get reset. A timer of 1.25 ms is started and state transitions from this state cannot occur until the timer expires.

After the timer expires, transitions from this state are carried out as follows:

- If the CS is de-asserted or UVLO is detected, the SLG51003 transitions to LOW_IQ_RESET state.
- If no over-temperature condition is detected and the CS remains asserted, the SLG51003 transitions to CONFIG_INIT state.

4.1.3. CONFIG_INIT

By entering CONFIG_INIT state, the OTP is read and loaded into the associated registers to ensure safe settings. The OTP read is skipped if the OTP is not programmed. The SLG51003 then transitions to READY state.

4.1.4. READY

In READY state, the device operates in accordance with the design file implemented. All digital resources are enabled and can be controlled. It carries out power-up or power-down sequences as shown in Figure 5 and Figure 6.

If an error condition is detected in READY state, the SLG51003 transitions to SEQUENCE_DOWN state.

4.1.5. SEQUENCE_DOWN

The conditions that cause transition to SEQUENCE_DOWN state are:

- CS de-assertion
- Over-temperature detection
- Crash detection
- UVLO fault condition
- Software reset.

By entering SEQUENCE_DOWN state, the supply controller powers down the digital supplies that it controls.

After the supply controller powers down the digital supplies, the SLG51003 transitions to RESET state.

4.2 Timing Characteristics

4.2.1. Turn-On Timing

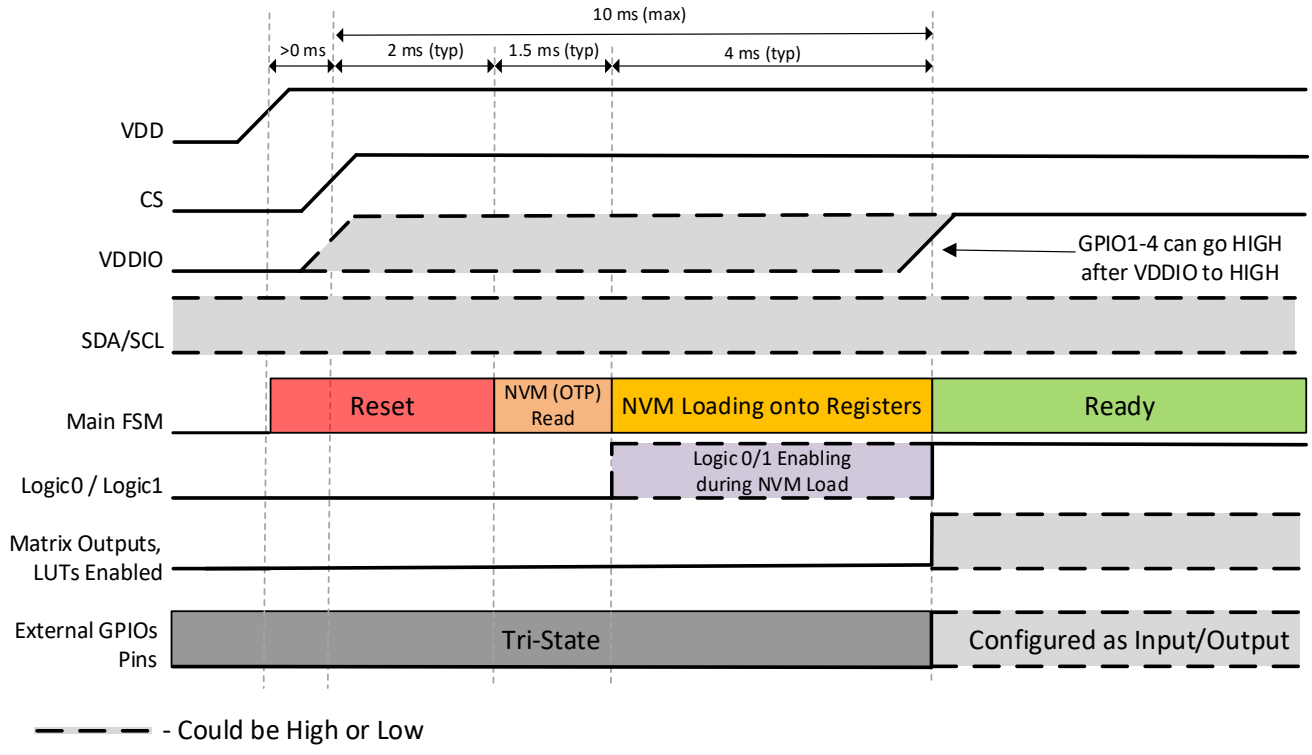


Figure 5. Turn-On Timing Diagram

4.2.2. Turn-Off Timing

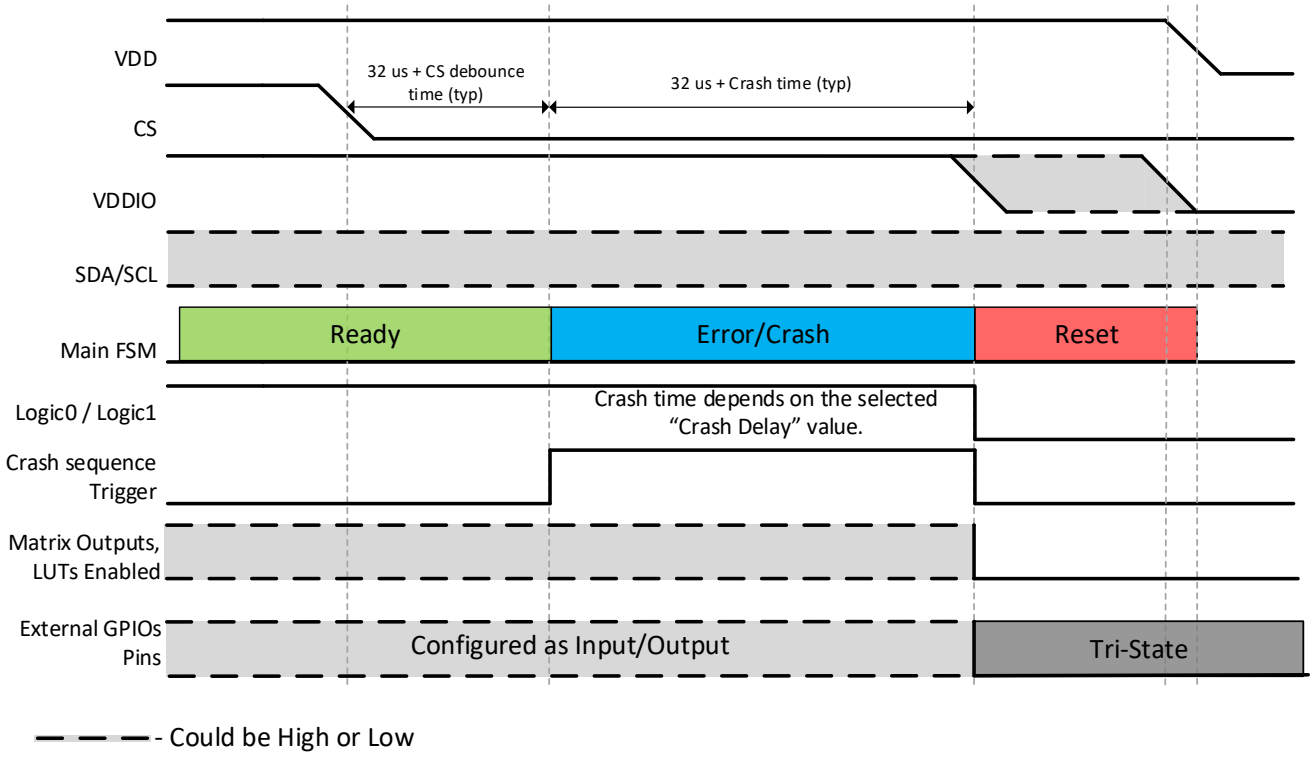


Figure 6. Turn-Off Timing Diagram

4.3 RESET Control

4.3.1. Power-On Reset Generator (nPOR_VDD)

To guarantee the correct start-up of the SLG51003, an internal power-on reset, nPOR_VDD (active low), monitors the V_{DD} supply. The nPOR_VDD is asserted when the voltage of V_{DD} pin is less than the $V_{DD\_POR\_UPPER}$ threshold.

4.3.2. UVLO

UVLO comparator is used to put the SLG51003 into LOW_IQ_RESET state when the V_{DD} supply drops below a predetermined programmable threshold. This comparator includes an internal hysteresis, meaning that the V_{DD} voltage during power-up must be at least 3 % higher than the UVLO threshold.

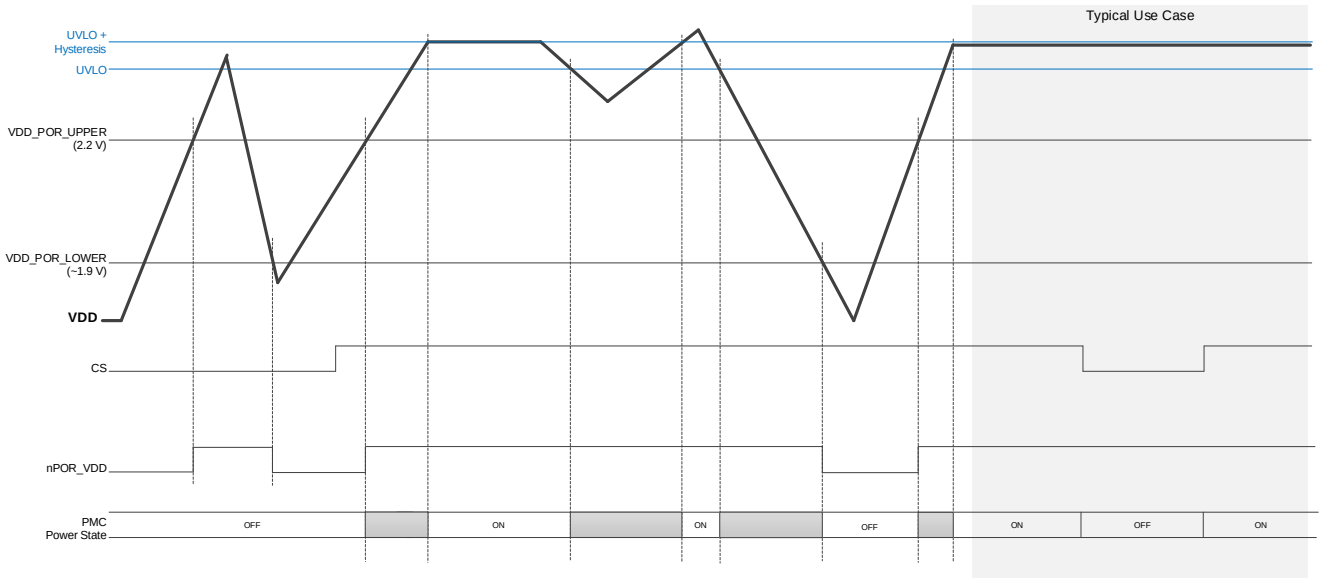


Figure 7. V_{DD} POR and UVLO Thresholds and System Behavior

4.4 General Purpose Supply Controller

The SLG51003 provides a flexible supply controller. The user configures the matrix interconnect logic, the GPIOs, and the macrocells of the SLG51003 to create a variety of functions and control logic for applications, such as power sequencing, fault signaling, input conditioning, and glue logic.

The supply controller supports flexible control of the following outputs:

- Three LDO enable signals
- Four GPIO output pins.

The supply controller also supports flexible control from the following inputs:

- Five GPIO input pins
- Three LDO OK signals
- Three LDO current limit signals
- One internal temperature warning signal
- Eight I^2C programmable signals.

The supply control can be done based on the input signals, delays, or by a combination of both. The controller provides a pool of seven combination function macrocells elements, that can serve as 3-bit look up tables (LUT) or as D flip-flops with Set/Reset Input, three delay blocks, and one multi-function block.

The supply controller is only enabled in READY and SEQUENCE_DOWN states. In all other states, the matrix interconnect, supply enables, and LUTs are disabled.

4.4.1. Matrix Interconnect

The matrix interconnect is a configurable switch that allows its output ports to be sourced from any of its input ports. Each output has a register bit to control its input port selection.

The matrix interconnect provides 42 outputs, which are mapped to supply controller signals, see Table 4. Each matrix interconnect output can be sourced from any of the input ports, see

Table 5.

Table 4. Matrix Interconnect Output Ports

Output Port	Destination
0	Matrix Event Register Input
1 to 4	GPIO Outputs 1 to 4
5 to 7	LDO Enable Inputs 1 to 3
8 to 10	LUT/DFF 1 Array 0 to 2
11 to 13	LUT/DFF 2 Array 0 to 2
	…
26 to 28	LUT/DFF 7 Array 0 to 2
29	DLY1 Enable
30 to 31	DLY1 Up, Down
32	DLY2 Enable
33 to 34	DLY2 Up, Down
35	DLY3 Enable
36 to 37	DLY3 Up, Down
38 to 40	MTFT 0 to 2
41	Crash Detect
42	Force Reset
43 to 63	No Connection

Table 5. Matrix Interconnect Input Ports

Input Port	Destination
0	Constant Logic '0'
1	Constant Logic '1'
2 to 9	Register Bit RESOURCE_CTRL (8-bit Value)
10	Temperature Warning Flag
11	Crash Event Flag
12 to 16	GPIO Inputs 1 to 5
17 to 19	LDO V_{OUT} OK Flags 1 to 3
20 to 22	LDO Current Limit Flags 1 to 3
23	Interrupt Request from Device’s Event Registers
24 to 30	LUT/DFF Outputs 0 to 6
31 to 33	DLY Outputs 0 to 2
34	MTFT LUT/DFF Output
35	MTFT CNT/DLY Output

4.5 Combination Function Macrocells

The SLG51003 has seven combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a 3-bit look up table (LUT) or as a D flip-flop (DFF)/LATCH with nRST/nSET Input.

The inputs and outputs of seven combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of configuration bits.

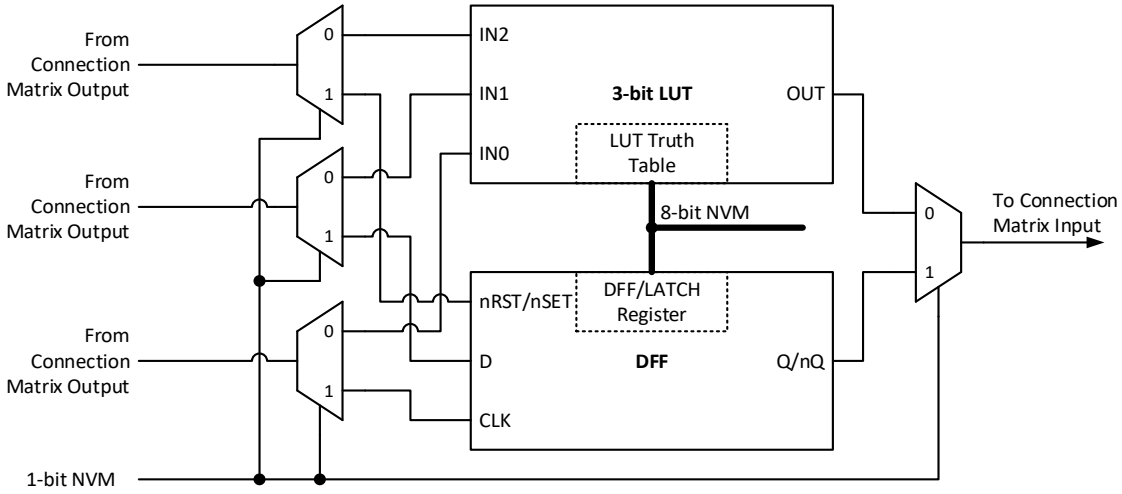


Figure 8. 3-bit LUT or DFF Block Diagram

When the macrocell is used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user-defined function, including the following standard digital logic blocks - AND, NAND, OR, NOR, XOR, or XNOR.

When it is used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

When it is used to implement DFF/LATCH function, the three input signals from the connection matrix go to the data (D), clock (CLK), and nRST/nSET inputs for the DFF/LATCH, with the output going back to the connection matrix. It is possible to select either nRST or nSET options.

The operation of the D flip-flop and LATCH will follow the functional descriptions below:

- DFF: CLK is rising edge triggered, then Q = D, otherwise, Q will not change.
- LATCH: when CLK is Low, then Q = D, otherwise, Q remains its previous value (input D has no effect on the output, when CLK is High).

4.6 Delay Macrocells

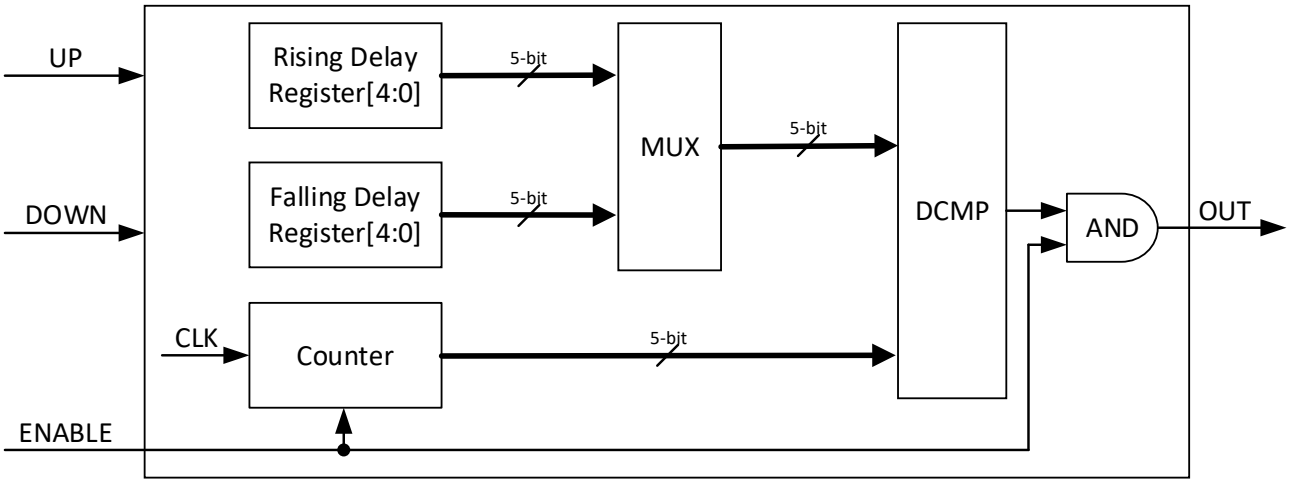


Figure 9. Delay Block Diagram

The SLG51003 contains three delay (DLY) macrocells. The DLY macrocell is a configurable delay. The users can choose rising delay time (rising delay counter data) and falling delay (falling delay counter data) time

independently, also can choose active (high or low) signal for UP and DOWN inputs independently. If either rising delay counter data or falling delay counter data are set to 0, the output of delay macrocell is LOW.

For flexibility, each of these delay cells have a large selection of internal clock sources (125 kHz, 31.25 kHz, 976,56 Hz, and 488,28 Hz), as well as the option to chain from the output of multi-functional macrocell, to implement longer delay time.

The DLY macrocell has three inputs. They are listed from lowest to highest priority: UP, DOWN, and ENABLE.

Also, DLY macrocell operates in two states:

1. DOWN_State is a default one. DLY macrocell OUT is in LOW level.
   Transition Trigger: DOWN signal active level is applied until falling delay time expires.
2. UP_State set DLY macrocell OUT is in HIGH level.
   Transition Trigger: UP signal active level is applied until rising delay time expires.

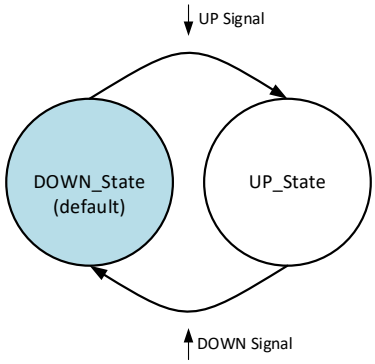


Figure 10. DLY Macrocell State Transitions

When UP input is tied to its active level, DOWN input is tied to its inactive level, and ENABLE signal is tied to HIGH, the counter starts counting. As soon as the rising delay time is expired, the OUT goes HIGH. The UP input should be tied to its active level and kept in its active level during rising delay time, otherwise, counter will be reset and OUT stays LOW.

When OUT becomes HIGH, in order to set OUT to LOW, DOWN input should be tied to its active level and kept in its active level during falling delay time. Because DOWN input has higher priority than UP input, it does not matter to which level UP input is tied when DOWN input is tied to its active level. ENABLE signal should be kept HIGH.

ENABLE signal and DCMP output are connected to the AND gate at the output of the macrocell. Therefore, ENABLE signal allows to enable or disable DLY macrocell. If this signal is tied to LOW, the OUT is LOW irrespective of UP and DOWN signals or macrocell states. ENABLE signal does not reset DLY macrocell state.

4.7 Multi-Function Macrocell

The SLG51003 has a multi-function macrocell that can be configured as a LUT/DFF with flexible settings, or as CNT/DLY with multiple modes, such as one shot, frequency detect, edge detect, and others. Also, the macrocell can combine the following functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF, see Figure 11.

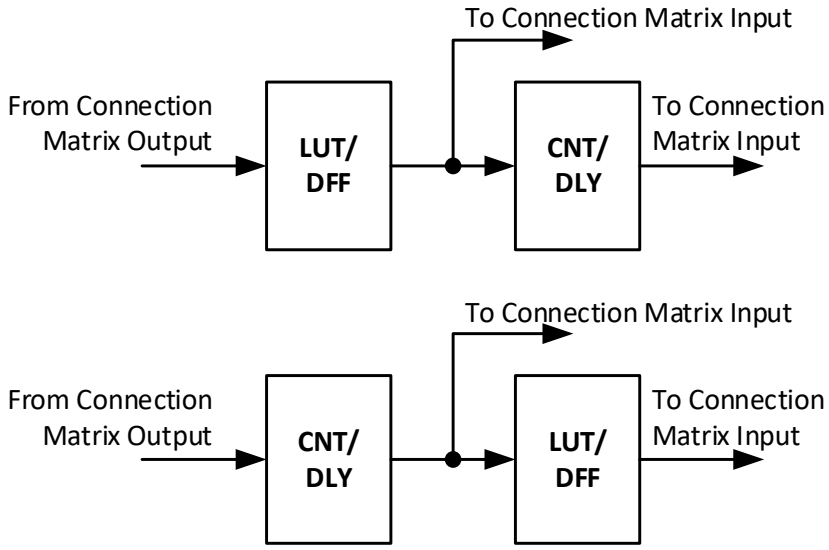


Figure 11. Possible Connections Inside Multi-Function Macrocell

Inputs/Outputs for the multi-function macrocell is configured from the connection matrix with specific logic functions being defined by the state of OTP bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user-defined function, including the following standard digital logic blocks - AND, NAND, OR, NOR, XOR, XNOR.

When the multi-function macrocell is used to implement a LUT function, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix or can be connected to CNT/DLY's input.

When it is used to implement a D flip-flop function, the three input signals from the connection matrix go to the data (D), clock (CLK), and Reset/Set (nRST/nSET) inputs of the flip-flop, with the output going back to the connection matrix or to the CNT/DLY's input.

When it is used to implement a CNT/DLY function, the macrocell has a dedicated matrix input connection. For flexibility, the macrocell has a large selection of internal and external clock sources. The macrocell can also operate in a one-shot mode, which will generate an output pulse of user-defined width or operate in a frequency detection or edge detection mode.

The CNT/DLY macrocell has an initial value, which defines its initial value after chip is powered up. It is possible to select initial LOW or initial HIGH, as well as the initial value defined by a DLY IN signal.

For example, in case the initial LOW option is used, the rising edge delay will start operation.

Note:

- After two DFFs: counters initialize with counter data = 0 after POR.
- Initial state = 1: counters initialize with counter data = 0 after POR.
- Initial state = 0 and after two DFFs is bypassed: counters initialize with counter data after POR.

The current counter value can be read via I^2C. Also, it is possible to change a counter data (value the counter starts operating from) using I^2C write commands. In this mode, it is possible to load count data immediately (after two DFFs) or after the counter ends counting.

For flexibility, CNT/DLY macrocell has a large selection of internal clock sources (125 kHz, 31.25 kHz, 976,56 Hz, 488,28 Hz).

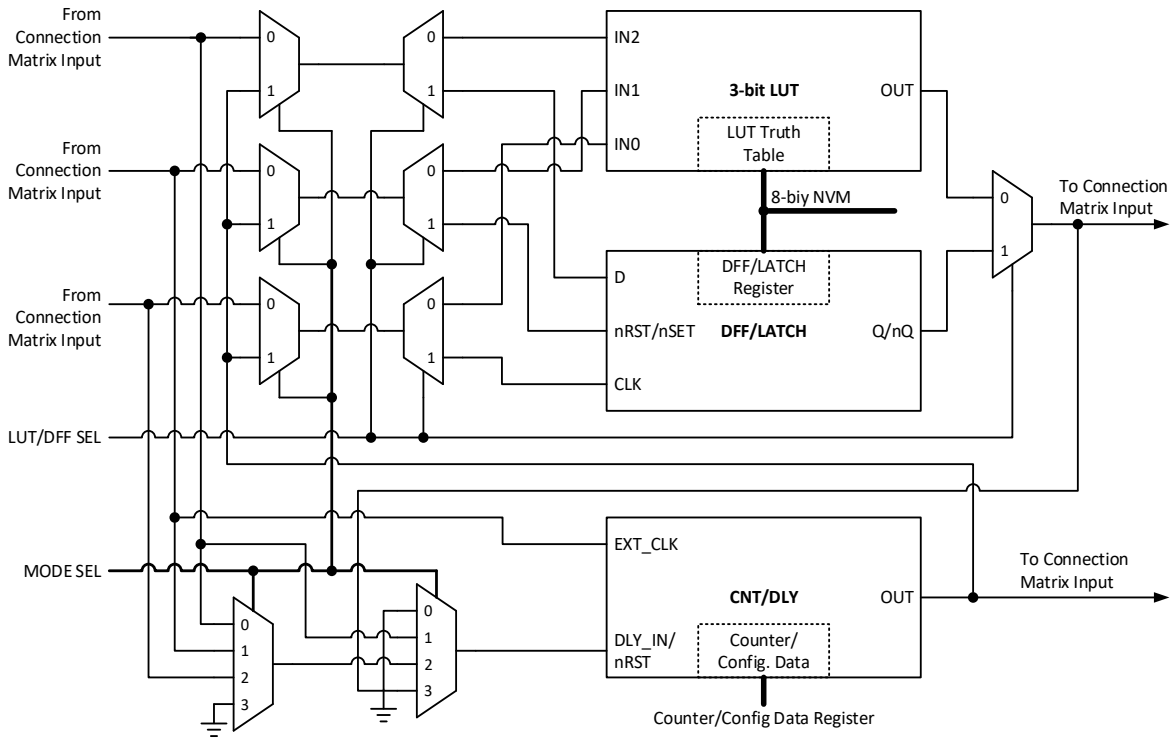


Figure 12. Multi-Function Macrocell Block Diagram

There is a possibility of using LUT/DFF and CNT/DLY simultaneously.

Note: It is not possible to use LUT and DFF at once, one of these macrocells must be selected.

- Case 1: LUT/DFF in front of CNT/DLY. Three input signals from the connection matrix go to previously selected LUT or DFF's inputs and produce a single output which goes to a CNT/DLY input. In its turn CNT/DLY's output goes back to the matrix.
- Case 2: CNT/DLY in front of LUT/DFF. Two input signals from the connection matrix go to CNT/DLY's inputs (IN and CLK). Its output signal can be connected to any input of previously selected LUT or DFF, after which the signal goes back to the matrix.
- Case 3: Single LUT/DFF or CNT/DLY. Also, it is possible to use standalone LUT/DFF or CNT/DLY. In this case, all inputs and output of the macrocell are connected to the matrix.

4.8 LDO Micro-Power Voltage Regulators

The SLG51003 includes three low noise, high performance, programmable LDO voltage regulators. The LDOs can be automatically enabled under the control of the power-on sequencer. They can also be controlled using I²C. For the enable signal and switch on statuses refer to section 6 I2C Serial Command Register Map. In case of output overvoltage, the LDOs enable an internal current sink to discharge the output back to its desired voltage.

The turn-on time for all LDOs depends on the programmed output voltage, the programmed startup current limit, the output load current, and the effective output capacitance, calculated by the following expression:

$$t_{ON} = \frac{V_{OUT}\, C_{OUT}}{I_{OUT\_STARTUP\_LIM} - I_{OUT}}$$

LDO2 and LDO3 have programmable slew rate features, see section below.

4.8.1. LDO Programmable Conditions

LDO1, LDO2, and LDO3 have a list of programmable features shown in Table 6. See section 6 I2C Serial Command Register Map for additional information.

Table 6. Programming Conditions

Parameter	Symbol	Bit Setting	Value	Unit
LDO_HP (LDO1)				
Selectable Output Voltage	V_{OUT}	VSEL = 0x28	2.4	V
		VSEL = 0x29	2.405	
		5 mV LSB of Programming DAC (8-bit Control)	…	
		VSEL = 0xDB	3.295	
		VSEL = 0xDC	3.3	
Selectable Minimal Output Voltage	V_{OUT_MIN}	VSEL_RANGE_MASK_MIN = 0x28	2.4	V
		VSEL_RANGE_MASK_MIN = 0x29	2.405	
		5 mV LSB of Programming DAC (8-bit Control)	…	
		VSEL_RANGE_MASK_MIN = 0xDB	3.295	
		VSEL_RANGE_MASK_MIN = 0xDC	3.3	
Selectable Maximum Output Voltage	V_{OUT_MAX}	VSEL_RANGE_MASK_MAX = 0x28	2.4	V
		VSEL_RANGE_MASK_ MAX = 0x29	2.405	
		5 mV LSB of Programming DAC (8-bit Control)	…	
		VSEL_RANGE_MASK_ MAX = 0xDB	3.295	
		VSEL_RANGE_MASK_ MAX = 0xDC	3.3	
Start-Up Current Limit	$I_{OUT\_STARTUP\_LIM}$	LDO1_SEL_ILIM = 0x1, At 90 % V_{OUT}	11	mA
		LDO1_SEL_ILIM = 0x2, At 90 % V_{OUT}	31	
		Programmable in approximately 20 mA steps	…	
		LDO1_SEL_ILIM = 0x7, At 90 % V_{OUT}	136	
		LDO1_SEL_ILIM = 0x0, At 90 % V_{OUT}	240	
LDO_HV (LDO2)				
Selectable Output Voltage	V_{OUT}	VSEL = 0x0	1.2	V
		VSEL = 0x1	1.21	
		10 mV LSB of Programming DAC (8-bit Control)	…	
		VSEL = 0xFE	3.74	
		VSEL = 0xFF	3.75	
Selectable Minimal Output Voltage	V_{OUT_MIN}	VSEL_RANGE_MASK_MIN = 0x0	1.2	V
		VSEL_RANGE_MASK_MIN = 0x1	1.21	
		10 mV LSB of Programming DAC (8-bit Control)	…	
		VSEL_RANGE_MASK_MIN = 0xFE	3.74	
		VSEL_RANGE_MASK_MIN = 0xFF	3.75	
Selectable Maximum Output Voltage	V_{OUT_MAX}	VSEL_RANGE_MASK_MAX = 0x0	1.2	V
		VSEL_RANGE_MASK_ MAX = 0x1	1.21	
		10 mV LSB of Programming DAC (8-bit Control)	…	
		VSEL_RANGE_MASK_ MAX = 0xFE	3.74	
		VSEL_RANGE_MASK_ MAX = 0xFF	3.75	

Parameter	Symbol	Bit Setting	Value	Unit
Slew Rate	SR	SEL_RAMP = 0x0, V_{OUT} = 3.3 V	1	mV/µs
		SEL_RAMP = 0x1, V_{OUT} = 3.3 V	2.5	
		Programmable, 9 selections	…	
		SEL_RAMP = 0x7, V_{OUT} = 3.3 V	50	
		SEL_RAMP = 0x8, V_{OUT} = 3.3 V	100	
Start-Up Current Limit	$I_{OUT\_STARTUP\_LIM}$	SEL_START_ILIM = 0x0, At 90 % V_{OUT}	30	mA
		SEL_START_ILIM = 0x1, At 90 % V_{OUT}	42	
		Programmable in 12 mA steps	…	
		SEL_START_ILIM = 0x29, At 90 % V_{OUT}	594	
		SEL_START_ILIM = 0x30, At 90 % V_{OUT}	606	
Functional Current Limit	$I_{OUT\_FUNC\_LIM}$	SEL_FUNC_ILIM = 0x0	30	mA
		SEL_FUNC_ILIM = 0x1	42	
		Programmable in 12 mA steps	…	
		SEL_FUNC_ILIM = 0x29	594	
		SEL_FUNC_ILIM = 0x30	606	
Output Discharge (Pull-Down) Resistance	R_{PD_OFF}	SEL_PULLDN = 0x7, V_{OUT} = 0.5 V, LDO Disabled	37.5	Ω
		SEL_PULLDN = 0x6, V_{OUT} = 0.5 V, LDO Disabled	42.9	
		Programmable, 8 selections	…	
		SEL_PULLDN = 0x1, V_{OUT} = 0.5 V, LDO Disabled	150	
		SEL_PULLDN = 0x0, V_{OUT} = 0.5 V, LDO Disabled	300	
LDO_LV (LDO3) in LDO Mode				
Selectable Output Voltage	V_{OUT}	VSEL = 0x14	0.5	V
		VSEL = 0x15	0.505	
		5 mV LSB of Programming DAC (8-bit Control)	…	
		VSEL = 0xC7	1.395	
		VSEL = 0xC8	1.4	
Selectable Minimal Output Voltage	V_{OUT_MIN}	VSEL_RANGE_MASK_MIN = 0x14	0.5	V
		VSEL_RANGE_MASK_MIN = 0x15	0.505	
		5 mV LSB of Programming DAC (8-bit Control)	…	
		VSEL_RANGE_MASK_MIN = 0xC7	1.395	
		VSEL_RANGE_MASK_MIN = 0xC8	1.4	
Selectable Maximum Output Voltage	V_{OUT_MAX}	VSEL_RANGE_MASK_MAX = 0x14	0.5	V
		VSEL_RANGE_MASK_ MAX = 0x15	0.505	
		5 mV LSB of Programming DAC (8-bit Control)	…	
		VSEL_RANGE_MASK_ MAX = 0xC7	1.395	
		VSEL_RANGE_MASK_ MAX = 0xC8	1.4	
Slew Rate	SR	SEL_RAMP = 0x0, V_{OUT} = 1.175 V	1	mV/µs
		SEL_RAMP = 0x1, V_{OUT} = 1.175 V	2.5	
		Programmable, 9 selections	…	
		SEL_RAMP = 0x7, V_{OUT} = 1.175 V	50	
		SEL_RAMP = 0x8, V_{OUT} = 1.175 V	100	

Parameter	Symbol	Bit Setting	Value	Unit
Start-Up Current Limit	$I_{OUT\_STARTUP\_LIM}$	SEL_START_ILIM = 0x0, At 90 % V_{OUT}	14.3	mA
		SEL_START_ILIM = 0x1, At 90 % V_{OUT}	28.6	
		Programmable in 14.3 mA steps	…	
		SEL_START_ILIM = 0x44, At 90 % V_{OUT}	986.7	
		SEL_START_ILIM = 0x45, At 90 % V_{OUT}	1001	
Functional Current Limit	$I_{OUT\_FUNC\_LIM}$	SEL_FUNC_ILIM = 0x0	14.3	mA
		SEL_FUNC_ILIM = 0x1	28.6	
		Programmable in 14.3 mA steps	…	
		SEL_FUNC_ILIM = 0x44	986.7	
		SEL_FUNC_ILIM = 0x45	1001	
Output Discharge (Pull-Down) Resistance	R_{PD_OFF}	SEL_PULLDN = 0x7, V_{OUT} = 0.5 V, LDO Disabled	37.5	Ω
		SEL_PULLDN = 0x6, V_{OUT} = 0.5 V, LDO Disabled	42.9	
		Programmable, 8 selections	…	
		SEL_PULLDN = 0x1, V_{OUT} = 0.5 V, LDO Disabled	150	
		SEL_PULLDN = 0x0, V_{OUT} = 0.5 V, LDO Disabled	300	
LDO_LV (LDO3) in Load Switch Mode				
Slew Rate	SR	SEL_BYP_SLEW_RATE = 0x0	4	mV/µs
		SEL_BYP_SLEW_RATE = 0x1	6	
		SEL_BYP_SLEW_RATE = 0x2	8	
		SEL_BYP_SLEW_RATE = 0x3	10	
Functional Current Limit	$I_{OUT\_FUNC\_LIM}$	SEL_FUNC_ILIM = 0x0	14.3	mA
		SEL_FUNC_ILIM = 0x1	28.6	
		Programmable in 12 mA steps	…	
		SEL_FUNC_ILIM = 0x44	986.7	
		SEL_FUNC_ILIM = 0x45	1001	
Output Discharge (Pull-Down) Resistance	R_{PD_OFF}	SEL_PULLDN = 0x7, V_{OUT} = 0.5 V, LDO Disabled	37.5	Ω
		SEL_PULLDN = 0x6, V_{OUT} = 0.5 V, LDO Disabled	42.9	
		Programmable, 8 selections	…	
		SEL_PULLDN = 0x1, V_{OUT} = 0.5 V, LDO Disabled	150	
		SEL_PULLDN = 0x0, V_{OUT} = 0.5 V, LDO Disabled	300	

4.8.2. LDO_HP in Remote Sense Mode

LDO_HP (LDO1) allows the user to apply remote sense mode in order to regulate voltage at load side. This allows to handle distant loads, such as one with flex cable applied.

In this mode, GPIO1 pin will be configured as an analog input to serve as remote sense pin. GPIO1 should be connected to the load side that is powered by LDO_HP. Because the GPIO1 depends on V_{DDIO}, the latter should be higher than the voltage at LDO_HP output.

LDO_HP in remote sense mode can affect electrical specification. Load regulation performance will depend on the parasitic parameters of the system.

4.9 Temperature Supervision

The SLG51003 includes a mechanism to protect the die from damage due to excessive temperature. An internal temperature measurement is performed and debounced for 384 ms (up to 392 ms). To indicate a thermal

overload, an OVER_TEMP condition is generated. This resets the device, recording the fault in the SYSCTL_FAULT_LOG register. Also, there is a lower temperature threshold, which indicates a thermal warning, which can be recorded in the SYSCTL_EVENT register.

4.10 Internal Oscillator

An internal oscillator provides a nominal 8 MHz clock used by the core.

4.11 Undervoltage Lockout (UVLO)

An internal UVLO monitor with a programmable threshold monitors the V_{DD} input voltage and shuts down the system if the voltage is below the threshold. The system behavior can be seen in Figure 7.

4.12 Crash Sequence (Watchdog)

A crash sequence digital block operates as a configurable watchdog that allows to perform soft power-down sequence. It can be triggered either from system state machine error conditions or from its inputs from the matrix interconnect. Both crash detect and force reset inputs are OTP configurable as an active-high or active-low input.

The crash detect input is one of the system state machine error conditions that can be routed by using matrix interconnect.

If the crash detect is triggered, this digital block allows to make transition into ERROR state for a preset amount of time. There are four watchdog timer options available - 10 ms, 50 ms, 100 ms, and 200 ms.

The force reset input allows force transition into RESET state right after it was triggered, allowing to decrease or skip set watchdog timer.

4.13 I²C Interface

The SLG51003 includes an I²C compatible interface based on the following signals:

- SCL: up to 400 kHz I²C bus serial clock generated by the host processor.
- SDA: up to 400 kHz I²C bus serial address/data input/output. Internally, it's an open-drain output.

The I²C bus is used to control the power supply modules of the SLG51003. The I²C serial interface uses two signals: data and clock input. A 3-byte serial protocol is used containing two bytes for address and one byte for data.

For cases where the I²C interface is not used, the following connections are recommended: SCL connected to ground, SDA connected to ground ensuring no external pull-up exists.

4.13.1. Details of the I²C Protocol

The standard frequency of the I²C bus in fast mode is 400 kHz. The I²C suppresses glitches in both SCL and SDA that are less than 50 ns wide. The input Schmitt trigger has a minimum hysteresis of 0.05 * V_{DDIO}. The I²C communication is only available in READY state, if configured. The leakage through the SCL and SDA pins is less than 10 µA when the I²C pads are powered.

The I²C lines are also fail-safe when the pads are not powered. The maximum leakage through the SCL and SDA pins does not exceed 1 µA even when the I²C lines are driven by other devices on the same bus.

The SLG51003 is compatible with the standard I²C protocol and operates as a slave. The SLG51003 has an I²C slave address with the default set to 0x75. The slave base address can be OTP programmed (I2C_ADD, register SYSCTL_SYS_CONF_A). For three LSBs of the slave address, each bit can be sourced independently from the OTP or by a value defined externally by GPIO3, GPIO2, and GPIO1. The LSB of the slave address is defined by the value of GPIO1.

The I²C bus is always monitored for a valid SLAVE address. An acknowledge bit is generated if the SLAVE address was true, see Figure 14.

- A START condition is initiated by a high to low transition on the SDA line while the SCL is in the high state.
- A STOP condition is indicated by a low to high transition on the SDA line while the SCL is in the high state.

- An ACKNOWLEDGE is indicated by the receiver pulling the SDA line low during the following clock cycle.

Figure 13. I²C Start and Stop Conditions

The sequences shown in Figure 14 occur when performing register read or write operations to the SLG51003.

If a new START or STOP condition occurs within a message, the bus returns to IDLE mode. Also, if the SCL clock frequency drops below 10 Hz during a message, the bus is reset to IDLE mode.

Data is transmitted with the MSB first, for both read and write operations.

Bit order definitions:

- Address[15:8] = 15:MSB and 8:LSB.
- Address[7:0] = 7:MSB and 0:LSB.
- Data[7:0] = 7:MSB and 0:LSB.

The MSB is sent first, for both the address word and the data word.

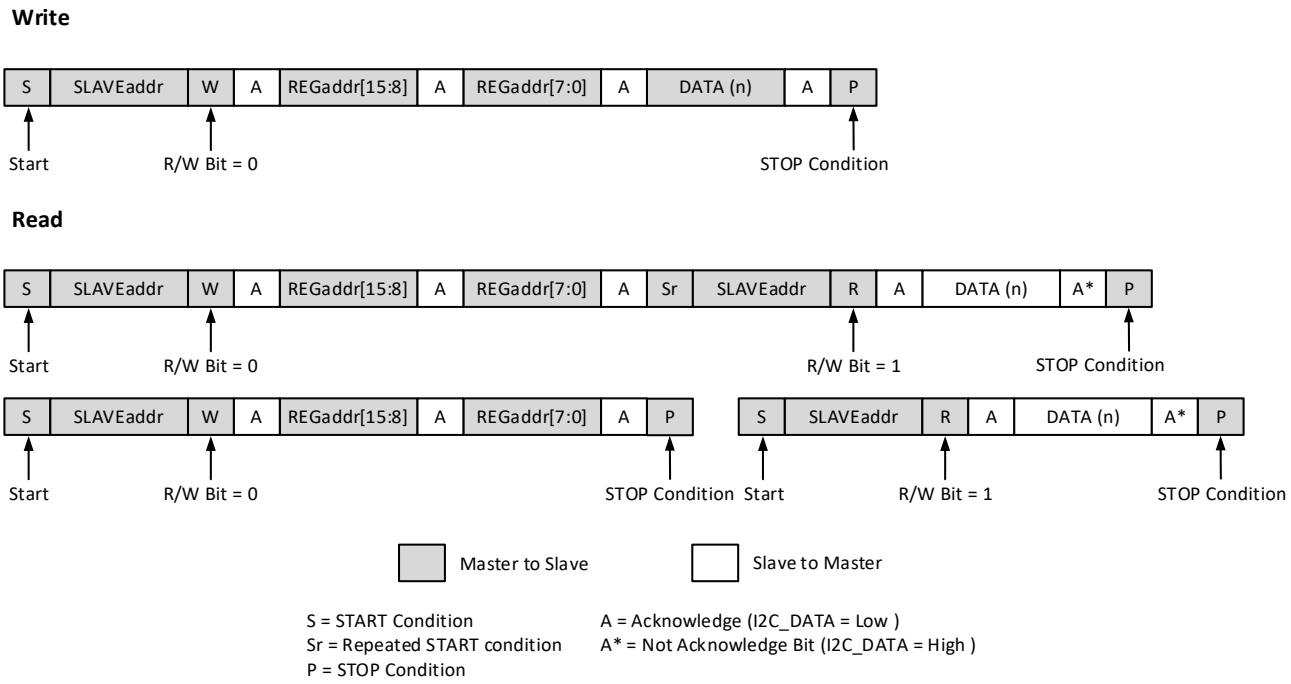


Figure 14. I²C Register Accesses

Consecutive (page) read out mode is initiated from the master by sending an ACK instead of a NACK after receiving the data word. The I²C control block then increments the address pointer to the next I²C address and sends the data to the master. This process repeats until the master sends the NACK after receiving the data. If a non-existent I²C address is read out, then the SLG51003 returns code zero.

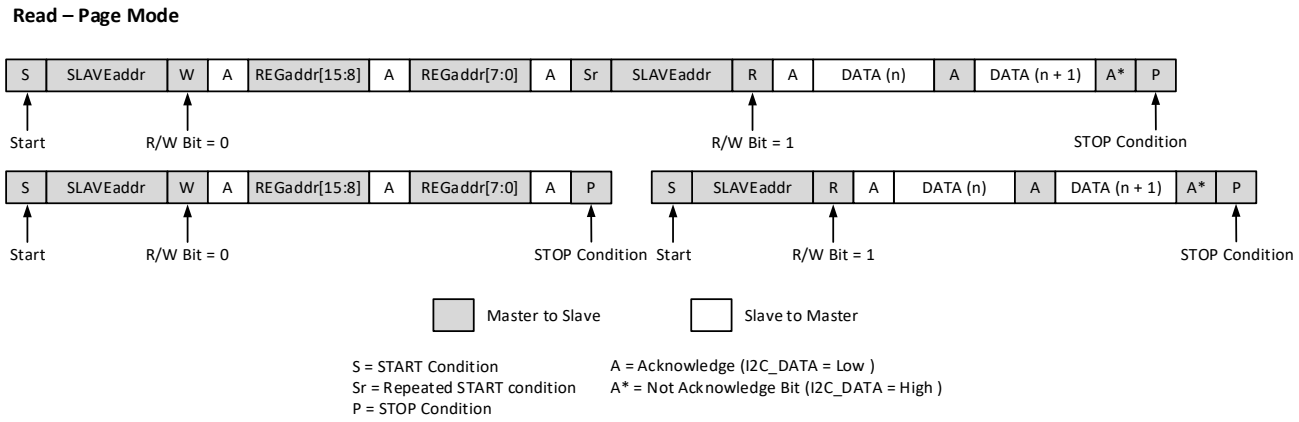


Figure 15. I²C Page Read Mode

4.14 Connection Matrix Virtual Inputs

The connection matrix inputs come from the outputs of various digital macrocells on the device. Eight of the connection matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I²C. This gives the users the ability to write data via the serial channel, and have this information translated into signals that can be driven into the connection matrix and from the connection matrix to the digital inputs of other macrocells on the device.

An I²C write command to these register bits will set the signal values going into the connection matrix to the desired state. A read command to these register bits will read either the original data values coming from the OTP memory bits (that were loaded during the initial device start-up), or the values from a previous write command (if that has happened).

4.15 Connection Matrix Virtual Outputs

Output state of digital blocks that are present in Table 5 are I²C accessible.

Digital blocks output state is stored in SYSCTL_MATRIX_VIRTUAL_OUTx registers. See section 6 I2C Serial Command Register Map for more information.

4.15.1. High Voltage GPIOs Structure (GPIO1 – GPIO3)

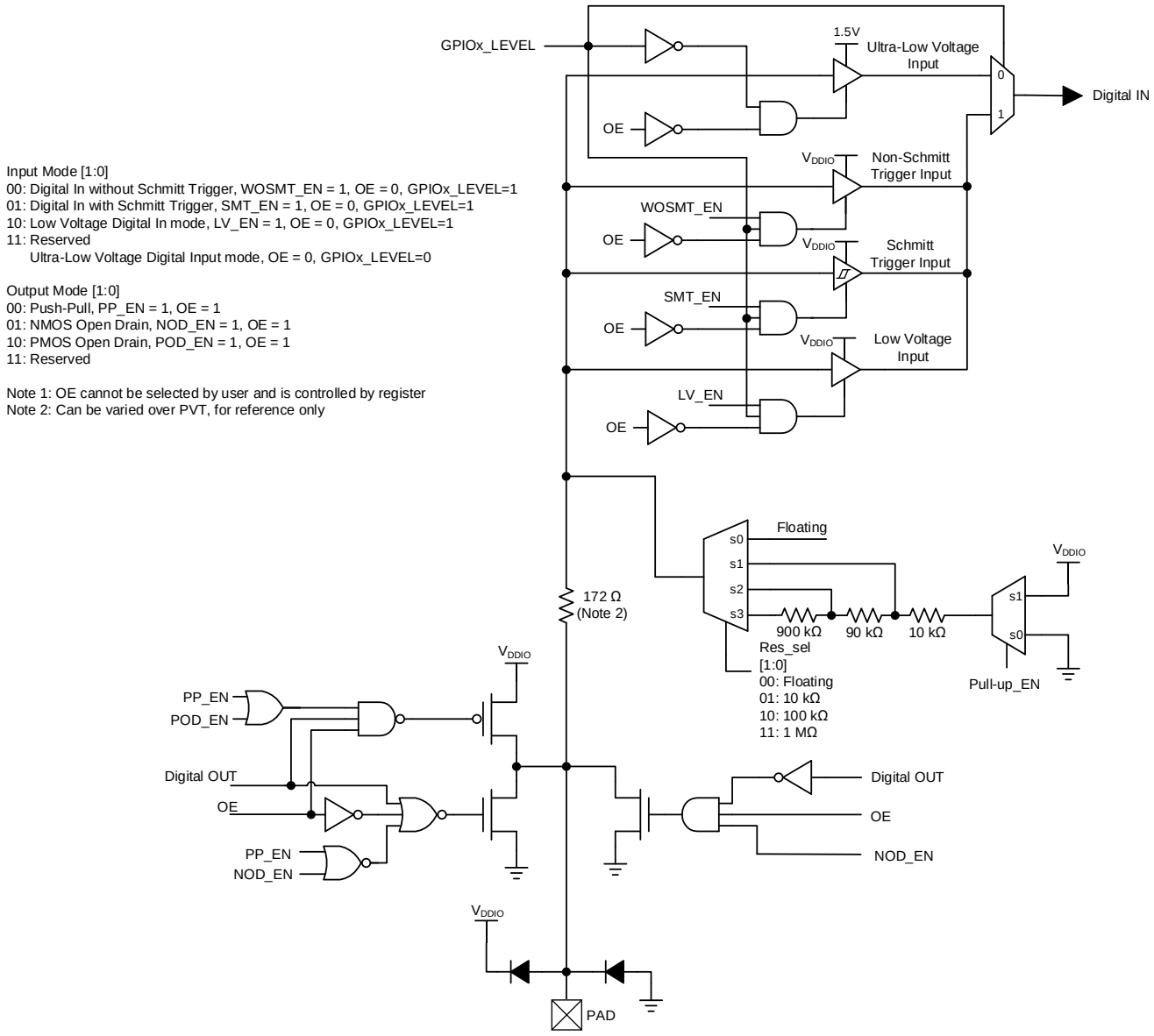


Figure 16. High Voltage GPIOs Structure

4.16 Event and Status Register

The SLG51003 offers I²C access to event and status registers of the system and LDOs.

Status registers offer a live representation of various aspects, such as temperature warning, configuration matrix, LDO start-up, and LDO current limit.

Event registers are a latched version of the status registers and can be used to raise a device interrupt request, which can be used by the configuration matrix to take further action or be routed externally via the GPIOs.

For the LDOs, EVT_VOUT_OK_FLAG events indicate that the LDO has started up. It is debounced on the positive edge, with debounce time controlled by OTP bit VOUT_OK_DEB for each LDO.

Event EVT_ILIM_FLAG can be used to detect a current limit detection in each LDO. This event is debounced on the falling edge only, allowing for any current limit detection to be captured, with debounce time controlled by OTP bit ILIM_FLAG_DEB in each LDO. Fast load transients can cause the event to be captured, even if the LDO load is less than I_{OUT_MAX}.

There are two possible methods for clearing the event registers controlled by OTP bit I2C_CLR_MODE (register SYSCTL_SYS_CONF_D).

- CLR_MODE (= 0): each event or fault log register bit is cleared either when it is read or by writing a 1 to each bit. In this mode, the ‘read’ clears the entire register. This is the default mode.
- CLR_MODE (= 1): each event or fault log register bit is only cleared by writing a 1 to each bit.

5. Typical Performance Charts

5.1 Load Transient Response

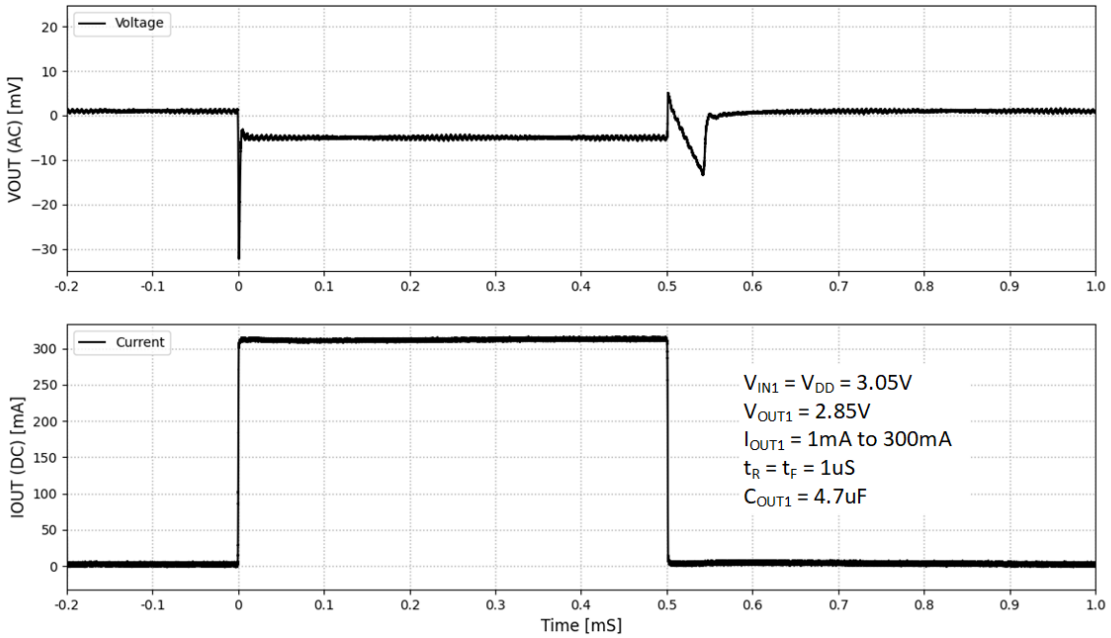


Figure 17. Load Transient for LDO1 at I_{OUT1} = 1 mA to 300 mA

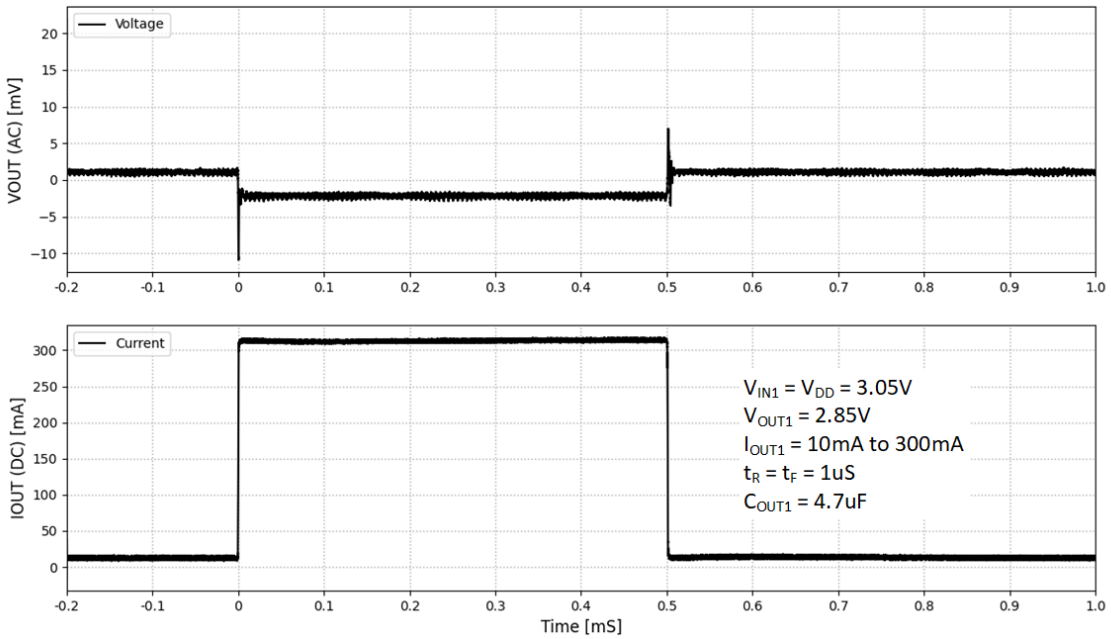


Figure 18. Load Transient for LDO1 at I_{OUT1} = 10 mA to 300 mA

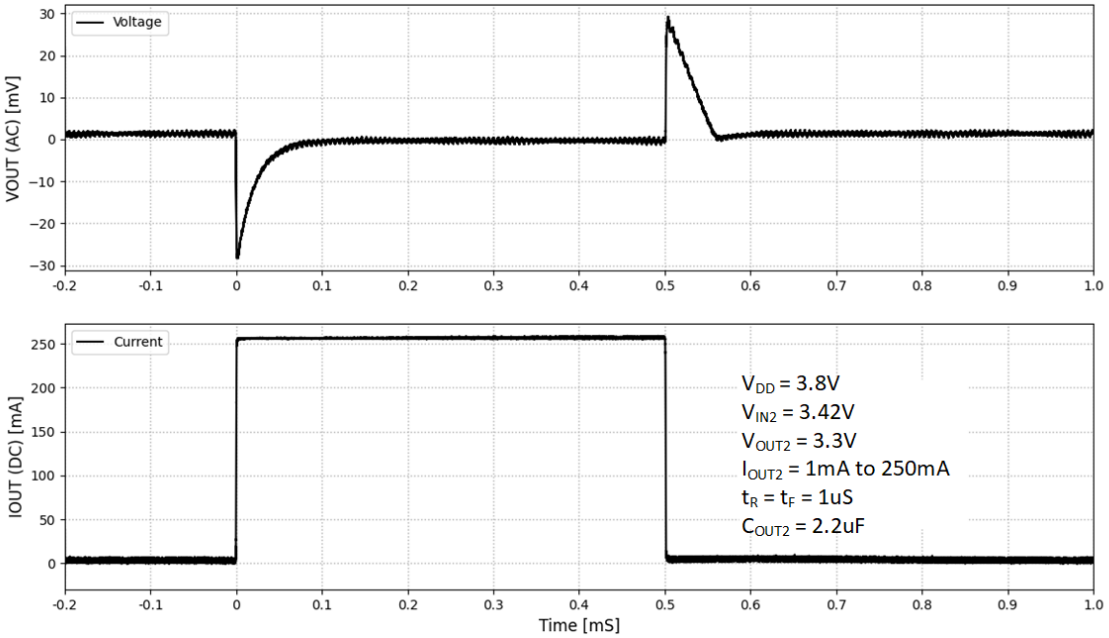


Figure 19. Load Transient for LDO2

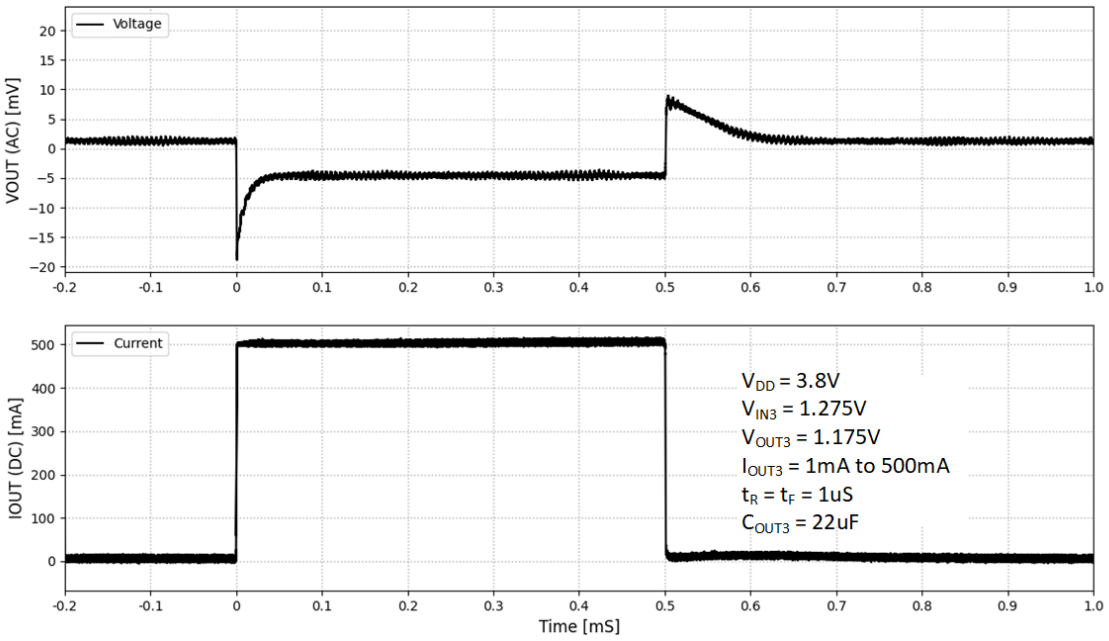


Figure 20. Load Transient for LDO3

6. I²C Serial Command Register Map

6.1 Register Map

6.1.1. SYSTEM CONTROL

Table 7. Chip Identification Registers

Address	Register Name	Bit	Type	Field Name	Description
0x1105	SYSCTL_PATTERN_ID_BYTE0	[7:0]	RWT OTP	PATTERN_ID_BYTE 0	Programming Code Number
0x1106	SYSCTL_PATTERN_ID_BYTE1	[7:0]	RWT OTP	PATTERN_ID_BYTE 1	Part Number Byte 0
0x1107	SYSCTL_PATTERN_ID_BYTE2	[7:0]	RWT OTP	PATTERN_ID_BYTE 2	Part Number Byte 1

Table 8. System Configuration Registers

Address	Register Name	Bit	Type	Field Name	Description
0x1109	SYSCTL_SYS_CONF_A	[6:0]	RW OTP	I2C_ADDRESS	Full I²C slave address
		[7]	RW OTP	I2C_DISABLE	I²C Disable (set high to disable I²C)
0x110C	SYSCTL_SYS_CONF_D	[5]	RWT OTP	I2C_CLR_MODE	Event and Faultlog register clear mode **Value Description** 0x0 Event/faultlog register read-to-clear mode 0x1 Event/faultlog register write-to-clear mode
		[7:6]	RWT OTP	CS_T_DEB	Chip select falling-edge debounce time **Value Description** 0x0 0.0 µs 0x1 64.0 µs 0x2 128.0 µs 0x3 256.0 µs
0x110D	SYSCTL_MATRIX_CTRL_CONF_A	[7:0]	RW OTP	RESOURCE_CTRL	Control byte into the matrix interconnect
0x110E	SYSCTL_MATRIX_CTRL_CONF_B	[2:0]	RW OTP	MATRIX_EVENT_SENSE	Controls the sensitivity of the EVT_MATRIX Field: EVT_MATRIX (Reg: SYSCTL_EVENT [0x111D]) to its connection from the matrix interconnect **Value Description** 0x0 Events Disabled 0x1 Pos.edge Event Sensitive 0x2 Neg.edge Event Sensitive 0x3 Both edges sensitive 0x4 Level sensitive event HIGH, stuck until sig rises 0x5 Level sensitive event LOW, stuck until sig falls 0x6 Events Disabled

Address	Register Name	Bit	Type	Field Name	Description
					0x7 Events Disabled
0x110F	SYSCTL_MATRIX_VIRTUAL_OUT0	[7:0]	RO	MARTIX_VIRTUAL_OUT0	Matrix Virtual Output[7:0]
0x1110	SYSCTL_MATRIX_VIRTUAL_OUT1	[7:0]	RO	MARTIX_VIRTUAL_OUT1	Matrix Virtual Output[15:8]
0x1111	SYSCTL_MATRIX_VIRTUAL_OUT2	[7:0]	RO	MARTIX_VIRTUAL_OUT2	Matrix Virtual Output[23:16]
0x1112	SYSCTL_MATRIX_VIRTUAL_OUT3	[7:0]	RO	MARTIX_VIRTUAL_OUT3	Matrix Virtual Output[31:24]
0x1113	SYSCTL_MATRIX_VIRTUAL_OUT4	[7:0]	RO	MARTIX_VIRTUAL_OUT4	Matrix Virtual Output[39:32]
0x1114	SYSCTL_MATRIX_VIRTUAL_OUT5	[7:0]	RO	MARTIX_VIRTUAL_OUT5	Matrix Virtual Output[47:40]
0x1117	SYSCTL_REFGEN_CONF_C	[1:0]	RWT OTP	REFGEN_SEL_TEMP_WARN_THR	Bandgap over-temperature threshold selection **Value Description** 0x0 120.0 °C 0x1 110.0 °C 0x2 100.0 °C 0x3 90.0 °C
		[3:2]	RWT OTP	REFGEN_SEL_TEMP_WARN_DEBOUNCE	Temperature Warning debounce selection (Implementation note: uncertainty is 1 ms resolution) **Value Description** 0x0 0.0 ms 0x1 8.0 ms 0x2 32.0 ms 0x3 128.0 ms
0x1118	SYSCTL_UVLO_CONF_A	[4:0]	RW OTP	VMON_UVLO_SEL_THR	Threshold used for PMU power fault, no dynamic threshold switching: Note: 2.2154 V is the recommended min value **Value Description** 0x0 1.994 V 0x1 to 0x1E 0.0246*VMON_UVLO_SEL_THR + 1.994 V 0x1F 2.756 V
0x111A	SYSCTL_CRH_CONF_A	[1:0]	RW OTP	CRH_DELAY_TIME	Delay time options of crash sequencer **Value Description** 0x0 10.0 ms 0x1 50.0 ms 0x2 100.0 ms 0x3 200.0 ms
		[2]	RW OTP	CRH_DETECT_SENSE	Detect sense controller of crash sequencer
		[3]	RW OTP	CRH_FORCE_RST_SENSE	Force reset controller of crash sequencer

Table 9. FaultLog, Events, Status and IRQ Control Registers

Address	Register Name	Bit	Type	Field Name	Description
0x111C	SYSCTL_FAULT_LOG1	[1]	FAULT LOG	FLT_OVER_TEMP	Over-temperature shutdown occurred
		[2]	FAULT LOG	FLT_CRASH_REQ	Crash sequencer requested shutdown occurred
		[4]	FAULT LOG	FLT_RST	System reset event occurred
		[5]	FAULT LOG	FLT_POR	Power-on reset event occurred
0x111D	SYSCTL_EVENT	[0]	EVENT	EVT_HIGH_TEMP_ WARNING	High temperature warning detected
		[1]	EVENT	EVT_MATRIX	Matrix input event detected
0x111E	SYSCTL_STATUS	[0]	RO	STA_HIGH_TEMP_ WARNING	High temperature warning status
		[1]	RO	STA_MATRIX	Matrix input status
0x111F	SYSCTL_IRQ_MASK	[0]	IRQ_M ASK	IRQ_HIGH_TEMP_ WARNING	Mask IRQ for the high temperature warning event
		[1]	IRQ_M ASK	IRQ_MATRIX	Mask IRQ for the matrix event
0x113C	SYSCTL_MEM_STATUS	[0]	RW OTP	MEM_STATUS	Memory Status bit **Value Description** 0x0 digital power cycling indication 0x1 digital power on

6.1.2. I/O

Table 10. GPIO Configuration Registers

Address	Register Name	Bit	Type	Field Name	Description
0x1500	IO_GPIO1_CONF	[0]	RW OTP	GPIO1_LEVEL	GPIO1 pad input voltage threshold level **Value Description** 0x0 Ultra-Low voltage digital input 0x1 Digital Input with/without Schmitt trigger, Low voltage digital input modes
		[2:1]	RW OTP	GPIO1_T_DEB	GPIO1 input debounce time **Value Description** 0x0 INPUT: 0 µs 0x1 INPUT: 5 ms 0x2 INPUT: 10 ms 0x3 INPUT: 50 ms
		[3]	RW OTP	GPIO1_BYP	GPIO1 output register bypass **Value Description** 0x0 Output data registered 0x1 Register bypassed
		[4]	RW OTP	GPIO1_INVERT	OUTPUT: Data to pad inversion control;

Address	Register Name	Bit	Type	Field Name	Description
					INPUT: Data from pad inversion control **Value Description** 0x0 OUTPUT: Data to pad non-inverted INPUT: Data to Matrix Interconnect non-inverted 0x1 OUTPUT: Data to pad inverted INPUT: Data to Matrix Interconnect inverted
		[6:5]	RW OTP	GPIO1_SENS	GPIO1 Input Debouncer Level-Sense **Value Description** 0x0 Rising-edge sensitive 0x1 Falling-edge sensitive 0x2 Sensitive on both edges 0x3 Sensitive on both edges
		[7]	RW OTP	GPIO1_DIR	GPIO1 Pad Direction **Value Description** 0x0 GPIO pad configured as INPUT 0x1 GPIO pad configured as OUTPUT
0x1501	IO_GPIO2_CONF	[0]	RW OTP	GPIO2_LEVEL	GPIO2 pad input voltage threshold level (see Field: GPIO1_LEVEL (Reg: IO_GPIO1_CONF [0x1500]) for details)
		[2:1]	RW OTP	GPIO2_T_DEB	GPIO2 input debounce time (see Field: GPIO1_T_DEB (Reg: IO_GPIO1_CONF [0x1500]) for details)
		[3]	RW OTP	GPIO2_BYP	GPIO2 output register bypass (see Field: GPIO1_BYP (Reg: IO_GPIO1_CONF [0x1500]) for details)
		[4]	RW OTP	GPIO2_INVERT	GPIO2 inversion (see Field: GPIO1_INVERT (Reg: IO_GPIO1_CONF [0x1500]) for details)
		[6:5]	RW OTP	GPIO2_SENS	GPIO2 input Debouncer sensitivity (see Field: GPIO1_SENS (Reg: IO_GPIO1_CONF [0x1500]) for details)
		[7]	RW OTP	GPIO2_DIR	GPIO2 direction (see Field: GPIO1_DIR (Reg: IO_GPIO1_CONF [0x1500]) for details)
0x1502	IO_GPIO3_CONF	[0]	RW OTP	GPIO3_LEVEL	GPIO3 pad input voltage threshold level (see Field: GPIO1_LEVEL (Reg: IO_GPIO1_CONF [0x1500]) for details)
		[2:1]	RW OTP	GPIO3_T_DEB	GPIO3 input debounce time (see Field: GPIO1_T_DEB (Reg: IO_GPIO1_CONF [0x1500]) for details)

Address	Register Name	Bit	Type	Field Name	Description
		[3]	RW OTP	GPIO3_BYP	GPIO3 output register bypass (see Field: GPIO1_BYP (Reg: IO_GPIO3_CONF [0x1500]) for details)
		[4]	RW OTP	GPIO3_INVERT	GPIO3 inversion (see Field: GPIO1_INVERT (Reg: IO_GPIO1_CONF [0x1500]) for details)
		[6:5]	RW OTP	GPIO3_SENS	GPIO3 input Debouncer sensitivity (see Field: GPIO1_SENS (Reg: IO_GPIO1_CONF [0x1500]) for details)
		[7]	RW OTP	GPIO3_DIR	GPIO3 direction (see Field: GPIO1_DIR (Reg: IO_GPIO1_CONF [0x1500]) for details)
0x1503	IO_GPIO4_CONF	[0]	RW OTP	GPIO4_LEVEL	GPIO4 pad input voltage threshold level **Value** **Description** 0x0 1.2 V 0x1 5.0 V
		[2:1]	RW OTP	GPIO4_T_DEB	GPIO4 input debounce time (see Field: GPIO1_T_DEB (Reg: IO_GPIO1_CONF [0x1500]) for details)
		[3]	RW OTP	GPIO4_BYP	GPIO4 output register bypass (see Field: GPIO1_BYP (Reg: IO_GPIO3_CONF [0x1500]) for details)
		[4]	RW OTP	GPIO4_INVERT	GPIO4 inversion (see Field: GPIO1_INVERT (Reg: IO_GPIO1_CONF [0x1500]) for details)
		[6:5]	RW OTP	GPIO4_SENS	GPIO4 input Debouncer sensitivity (see Field: GPIO1_SENS (Reg: IO_GPIO1_CONF [0x1500]) for details)
		[7]	RW OTP	GPIO4_DIR	GPIO4 direction (see Field: GPIO1_DIR (Reg: IO_GPIO1_CONF [0x1500]) for details)
0x1504	IO_GPIO5_CONF	[0]	RW OTP	GPIO5_LEVEL	GPI5 pad input voltage threshold level **Value** **Description** 0x0 1.2 V 0x1 5.0 V
		[2:1]	RW OTP	GPIO5_T_DEB	GPI5 input debounce time (see Field: GPIO1_T_DEB (Reg: IO_GPIO1_CONF [0x1500]) for details)
		[4]	RW OTP	GPIO5_INVERT	GPI5 inversion (see Field: GPIO1_INVERT (Reg: IO_GPIO1_CONF [0x1500]) for details)
		[6:5]	RW OTP	GPIO5_SENS	GPI5 input Debouncer sensitivity (see Field: GPIO1_SENS (Reg:

Address	Register Name	Bit	Type	Field Name	Description
					IO_GPIO1_CONF [0x1500]) for details)
0x1505	IO_GPIO_STATUS	[0]	ROT	GPIO1_STATUS	State of debounced GPIO1 if configured as input (includes the configurable inversion, see Field: GPIO1_INVERT (Reg: IO_GPIO1_CONF [0x1500]))
		[1]	ROT	GPIO2_STATUS	State of debounced GPIO2 if configured as input (includes the configurable inversion, see Field: GPIO2_INVERT (Reg: IO_GPIO1_CONF [0x1501]))
		[2]	ROT	GPIO3_STATUS	State of debounced GPIO3 if configured as input (includes the configurable inversion, see Field: GPIO3_INVERT (Reg: IO_GPIO1_CONF [0x1502]))
		[3]	ROT	GPIO4_STATUS	State of debounced GPIO4 if configured as input (includes the configurable inversion, see Field: GPIO4_INVERT (Reg: IO_GPIO1_CONF [0x1503]))
		[4]	ROT	GPIO5_STATUS	State of debounced GPIO5 if configured as input (includes the configurable inversion, see Field: GPIO5_INVERT (Reg: IO_GPIO1_CONF [0x1505]))
0x1506	IO_GPIO1_MODE	[1:0]	RW OTP	GPIO1_IN_MODE	Input selection **Value Description** 0x0 Digital Input w/o Schmitt trigger if GPIO1_LEVEL is 1. Ultra-Low voltage digital input if GPIO1_LEVEL is 0. 0x1 Digital Input w/ Schmitt trigger if GPIO1_LEVEL is 1. Ultra-Low voltage digital input if GPIO1_LEVEL is 0. 0x2 Low voltage digital input if GPIO1_LEVEL is 1. Ultra-Low voltage digital input if GPIO1_LEVEL is 0.
		[3:2]	RW OTP	GPIO1_OUT_MODE	Output mode selection **Value Description** 0x0 Push-pull 0x1 NMOS open-drain 0x2 PMOS open-drain
		[5:4]	RW OTP	GPIO1_RES_MODE	Resistor selection **Value Description** 0x0 Not using pull-up/down functionality 0x1 10 kΩ 0x2 100 kΩ 0x3 1.0 MΩ
		[6]	RW OTP	GPIO1_PULLUP	Pull-up/down selection **Value Description**

Address	Register Name	Bit	Type	Field Name	Description
					0x0 pull-down 0x1 pull-up
0x1507	IO_GPIO2_MODE	[1:0]	RW OTP	GPIO2_IN_MODE	Input selection **Value Description** 0x0 Digital Input w/o Schmitt trigger if GPIO2_LEVEL is 1. Ultra-Low voltage digital input if GPIO2_LEVEL is 0. 0x1 Digital Input w/ Schmitt trigger if GPIO2_LEVEL is 1. Ultra-Low voltage digital input if GPIO2_LEVEL is 0. 0x2 Low voltage digital input if GPIO2_LEVEL is 1. Ultra-Low voltage digital input if GPIO2_LEVEL is 0.
		[3:2]	RW OTP	GPIO2_OUT_MODE	Output mode selection **Value Description** 0x0 Push-pull 0x1 NMOS open-drain 0x2 PMOS open-drain
		[5:4]	RW OTP	GPIO2_RES_MODE	Resistor selection **Value Description** 0x0 Not using pull-up/down functionality 0x1 10 kΩ 0x2 100 kΩ 0x3 1.0 MΩ
		[6]	RW OTP	GPIO2_PULLUP	Pull-up/down selection **Value Description** 0x0 pull-down 0x1 pull-up
0x1508	IO_GPIO3_MODE	[1:0]	RW OTP	GPIO3_IN_MODE	Input selection **Value Description** 0x0 Digital Input w/o Schmitt trigger if GPIO3_LEVEL is 1. Ultra-Low voltage digital input if GPIO3_LEVEL is 0. 0x1 Digital Input w/ Schmitt trigger if GPIO3_LEVEL is 1. Ultra-Low voltage digital input if GPIO3_LEVEL is 0. 0x2 Low voltage digital input if GPIO3_LEVEL is 1. Ultra-Low voltage digital input if GPIO3_LEVEL is 0.
		[3:2]	RW OTP	GPIO3_OUT_MODE	Output mode selection **Value Description** 0x0 Push-pull 0x1 NMOS open-drain 0x2 PMOS open-drain
		[5:4]	RW OTP	GPIO3_RES_MODE	Resistor selection **Value Description**

Address	Register Name	Bit	Type	Field Name	Description
					0x0 Not using pull-up/down functionality 0x1 10 kΩ 0x2 100 kΩ 0x3 1.0 MΩ
		[6]	RW OTP	GPIO3_PULLUP	Pull-up/down selection **Value Description** 0x0 pull-down 0x1 pull-up
0x1509	IO_GPIO_QCHG	[2]	RW OTP	GPIO1_DISABLE_SYNC	GPIO1 disable synchronizer **Value Description** 0x0 Enable 0x1 Disable
		[3]	RW OTP	GPIO2_DISABLE_SYNC	GPIO2 disable synchronizer **Value Description** 0x0 Enable 0x1 Disable
		[4]	RW OTP	GPIO3_DISABLE_SYNC	GPIO3 disable synchronizer **Value Description** 0x0 Enable 0x1 Disable
		[5]	RW OTP	GPIO4_DISABLE_SYNC	GPIO4 disable synchronizer **Value Description** 0x0 Enable 0x1 Disable
		[6]	RW OTP	GPIO5_DISABLE_SYNC	GPI5 disable synchronizer **Value Description** 0x0 Enable 0x1 Disable

6.1.3. MUX ARRAY

Table 11. Matrix Interconnect Input Port Configuration Registers

Address	Register Name	Bit	Type	Field Name	Description
0x1700	MUXARRAY_INPUT_SEL_0	[5:0]	RW OTP	INPUT_SEL_0	Matrix interconnect input port selection for output port to Matrix Event. Input selection options: **Value Description** 0x0 Logic 0 constant 0x1 Logic 1 constant 0x2 I^2C Resource Control[0] 0x3 I^2C Resource Control[1] 0x4 I^2C Resource Control[2] 0x5 I^2C Resource Control[3] 0x6 I^2C Resource Control[4] 0x7 I^2C Resource Control[5] 0x8 I^2C Resource Control[6] 0x9 I^2C Resource Control[7] 0xA High Temperature Warning

Address	Register Name	Bit	Type	Field Name	Description
					0xB Crash Event Flag 0xC GPIO1 Input 0xD GPIO2 Input 0xE GPIO3 Input 0xF GPIO4 Input 0x10 GPIO5 Input 0x11 LDO1 Vout OK Flag 0x12 LDO2 Vout OK Flag 0x13 LDO3 Vout OK Flag 0x14 LDO1 Current Limit Flag 0x15 LDO2 Current Limit Flag 0x16 LDO3 Current Limit Flag 0x17 Device Interrupt Request 0x18 LUT/DFF 1 OUTPUT 0x19 LUT/DFF 2 OUTPUT 0x1A LUT/DFF 3 OUTPUT 0x1B LUT/DFF 4 OUTPUT 0x1C LUT/DFF 5 OUTPUT 0x1D LUT/DFF 6 OUTPUT 0x1E LUT/DFF 7 OUTPUT 0x1F DLY1 OUTPUT 0x20 DLY2 OUTPUT 0x21 DLY3 OUTPUT 0x22 MTFT LUT0/DFF0 OUTPUT 0x23 MTFT CNT0/DLY0 OUTPUT
0x1701	MUXARRAY_INPUT_SEL_1	[5:0]	RW OTP	INPUT_SEL_1	Matrix interconnect input port selection for output port to GPIO1 output. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1702	MUXARRAY_INPUT_SEL_2	[5:0]	RW OTP	INPUT_SEL_2	Matrix interconnect input port selection for output port to GPIO2 output. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1703	MUXARRAY_INPUT_SEL_3	[5:0]	RW OTP	INPUT_SEL_3	Matrix interconnect input port selection for output port to GPIO3 output. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1704	MUXARRAY_INPUT_SEL_4	[5:0]	RW OTP	INPUT_SEL_4	Matrix interconnect input port selection for output port to GPIO4 output. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1705	MUXARRAY_INPUT_SEL_5	[5:0]	RW OTP	INPUT_SEL_5	Matrix interconnect input port selection for output port to LDO1 Enable. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1706	MUXARRAY_INPUT_SEL_6	[5:0]	RW OTP	INPUT_SEL_6	Matrix interconnect input port selection for output port to LDO2

Address	Register Name	Bit	Type	Field Name	Description
					Enable. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1707	MUXARRAY_INPUT_SEL_7	[5:0]	RW OTP	INPUT_SEL_7	Matrix interconnect input port selection for output port to LD03 Enable. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1708	MUXARRAY_INPUT_SEL_8	[5:0]	RW OTP	INPUT_SEL_8	Matrix interconnect input port selection for output port to LUT1[IN0], DFF1[CLK]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1709	MUXARRAY_INPUT_SEL_9	[5:0]	RW OTP	INPUT_SEL_9	Matrix interconnect input port selection for output port to LUT1[IN1], DFF1[D]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x170A	MUXARRAY_INPUT_SEL_10	[5:0]	RW OTP	INPUT_SEL_10	Matrix interconnect input port selection for output port to LUT1[IN2], DFF1[nRST/nSET. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x170B	MUXARRAY_INPUT_SEL_11	[5:0]	RW OTP	INPUT_SEL_11	Matrix interconnect input port selection for output port to LUT2[IN0], DFF2[CLK]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x170C	MUXARRAY_INPUT_SEL_12	[5:0]	RW OTP	INPUT_SEL_12	Matrix interconnect input port selection for output port to LUT2[IN1], DFF2[D]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x170D	MUXARRAY_INPUT_SEL_13	[5:0]	RW OTP	INPUT_SEL_13	Matrix interconnect input port selection for output port to LUT2[IN2], DFF2[nRST/nSET]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x170E	MUXARRAY_INPUT_SEL_14	[5:0]	RW OTP	INPUT_SEL_14	Matrix interconnect input port selection for output port to LUT3[IN0], DFF3[CLK]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x170F	MUXARRAY_INPUT_SEL_15	[5:0]	RW OTP	INPUT_SEL_15	Matrix interconnect input port selection for output port to LUT3[IN1], DFF3[D]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1710	MUXARRAY_INPUT_SEL_16	[5:0]	RW OTP	INPUT_SEL_16	Matrix interconnect input port selection for output port to LUT3[IN2], DFF3[nRST/nSET]. See

Address	Register Name	Bit	Type	Field Name	Description
					Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1711	MUXARRAY_INPUT_SEL_17	[5:0]	RW OTP	INPUT_SEL_17	Matrix interconnect input port selection for output port to LUT4[IN0], DFF4[CLK]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1712	MUXARRAY_INPUT_SEL_18	[5:0]	RW OTP	INPUT_SEL_18	Matrix interconnect input port selection for output port to LUT4[IN1], DFF4[D]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1713	MUXARRAY_INPUT_SEL_19	[5:0]	RW OTP	INPUT_SEL_19	Matrix interconnect input port selection for output port to LUT4[IN2], DFF4[nRST/nSET]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1714	MUXARRAY_INPUT_SEL_20	[5:0]	RW OTP	INPUT_SEL_20	Matrix interconnect input port selection for output port to LUT5[IN0], DFF5[CLK]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1715	MUXARRAY_INPUT_SEL_21	[5:0]	RW OTP	INPUT_SEL_21	Matrix interconnect input port selection for output port to LUT5[IN1], DFF5[D]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1716	MUXARRAY_INPUT_SEL_22	[5:0]	RW OTP	INPUT_SEL_22	Matrix interconnect input port selection for output port to LUT5[IN2], DFF5[nRST/nSET]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1717	MUXARRAY_INPUT_SEL_23	[5:0]	RW OTP	INPUT_SEL_23	Matrix interconnect input port selection for output port to LUT6[IN0], DFF6[CLK]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1718	MUXARRAY_INPUT_SEL_24	[5:0]	RW OTP	INPUT_SEL_24	Matrix interconnect input port selection for output port to LUT6[IN1], DFF6[D]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1719	MUXARRAY_INPUT_SEL_25	[5:0]	RW OTP	INPUT_SEL_25	Matrix interconnect input port selection for output port to LUT6[IN2], DFF6[nRST/nSET]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x171A	MUXARRAY_INPUT_SEL_26	[5:0]	RW OTP	INPUT_SEL_26	Matrix interconnect input port selection for output port to

Address	Register Name	Bit	Type	Field Name	Description
					LUT7[IN0], DFF7[CLK]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x171B	MUXARRAY_INPUT_SEL_27	[5:0]	RW OTP	INPUT_SEL_27	Matrix interconnect input port selection for output port to LUT7[IN1], DFF7[D]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x171C	MUXARRAY_INPUT_SEL_28	[5:0]	RW OTP	INPUT_SEL_28	Matrix interconnect input port selection for output port to LUT7[IN2], DFF7[nRST/nSET]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x171D	MUXARRAY_INPUT_SEL_29	[5:0]	RW OTP	INPUT_SEL_29	Matrix interconnect input port selection for output port to DLY1[EN]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x171E	MUXARRAY_INPUT_SEL_30	[5:0]	RW OTP	INPUT_SEL_30	Matrix interconnect input port selection for output port to DLY1[UP]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x171F	MUXARRAY_INPUT_SEL_31	[5:0]	RW OTP	INPUT_SEL_31	Matrix interconnect input port selection for output port to DLY1[DOWN]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1720	MUXARRAY_INPUT_SEL_32	[5:0]	RW OTP	INPUT_SEL_32	Matrix interconnect input port selection for output port to DLY2[EN]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1721	MUXARRAY_INPUT_SEL_33	[5:0]	RW OTP	INPUT_SEL_33	Matrix interconnect input port selection for output port to DLY2[UP]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1722	MUXARRAY_INPUT_SEL_34	[5:0]	RW OTP	INPUT_SEL_34	Matrix interconnect input port selection for output port to DLY2[DOWN]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1723	MUXARRAY_INPUT_SEL_35	[5:0]	RW OTP	INPUT_SEL_35	Matrix interconnect input port selection for output port to DLY3[EN]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1724	MUXARRAY_INPUT_SEL_36	[5:0]	RW OTP	INPUT_SEL_36	Matrix interconnect input port selection for output port to DLY3[UP]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.

Address	Register Name	Bit	Type	Field Name	Description
0x1725	MUXARRAY_INPUT_SEL_37	[5:0]	RW OTP	INPUT_SEL_37	Matrix interconnect input port selection for output port to DLY3[DOWN]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1726	MUXARRAY_INPUT_SEL_38	[5:0]	RW OTP	INPUT_SEL_38	Matrix interconnect input port selection for output port to MTFT[0]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1727	MUXARRAY_INPUT_SEL_39	[5:0]	RW OTP	INPUT_SEL_39	Matrix interconnect input port selection for output port to MTFT[1]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1728	MUXARRAY_INPUT_SEL_40	[5:0]	RW OTP	INPUT_SEL_40	Matrix interconnect input port selection for output port to MTFT[2]. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x1729	MUXARRAY_INPUT_SEL_41	[5:0]	RW OTP	INPUT_SEL_41	Matrix interconnect input port selection for output port to Crash Detect of Crash Sequencer. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x172A	MUXARRAY_INPUT_SEL_42	[5:0]	RW OTP	INPUT_SEL_42	Matrix interconnect input port selection for output port to Force Reset of Crash Sequencer. See Field: INPUT_SEL_0 (Reg: MUXARRAY_INPUT_SEL_0 [0x1700]) for details.
0x172B	MUXARRAY_INPUT_SEL_43	[5:0]	RW OTP	INPUT_SEL_43	No Connection
0x172C	MUXARRAY_INPUT_SEL_44	[5:0]	RW OTP	INPUT_SEL_44	No Connection
0x172D	MUXARRAY_INPUT_SEL_45	[5:0]	RW OTP	INPUT_SEL_45	No Connection
0x172E	MUXARRAY_INPUT_SEL_46	[5:0]	RW OTP	INPUT_SEL_46	No Connection
0x172F	MUXARRAY_INPUT_SEL_47	[5:0]	RW OTP	INPUT_SEL_47	No Connection
0x1730	MUXARRAY_INPUT_SEL_48	[5:0]	RW OTP	INPUT_SEL_48	No Connection
0x1731	MUXARRAY_INPUT_SEL_49	[5:0]	RW OTP	INPUT_SEL_49	No Connection
0x1732	MUXARRAY_INPUT_SEL_50	[5:0]	RW OTP	INPUT_SEL_50	No Connection
0x1733	MUXARRAY_INPUT_SEL_51	[5:0]	RW OTP	INPUT_SEL_51	No Connection
0x1734	MUXARRAY_INPUT_SEL_52	[5:0]	RW OTP	INPUT_SEL_52	No Connection
0x1735	MUXARRAY_INPUT_SEL_53	[5:0]	RW OTP	INPUT_SEL_53	No Connection

Address	Register Name	Bit	Type	Field Name	Description
0x1736	MUXARRAY_INPUT_SEL_54	[5:0]	RW OTP	INPUT_SEL_54	No Connection
0x1737	MUXARRAY_INPUT_SEL_55	[5:0]	RW OTP	INPUT_SEL_55	No Connection
0x1738	MUXARRAY_INPUT_SEL_56	[5:0]	RW OTP	INPUT_SEL_56	No Connection
0x1739	MUXARRAY_INPUT_SEL_57	[5:0]	RW OTP	INPUT_SEL_57	No Connection
0x173A	MUXARRAY_INPUT_SEL_58	[5:0]	RW OTP	INPUT_SEL_58	No Connection
0x173B	MUXARRAY_INPUT_SEL_59	[5:0]	RW OTP	INPUT_SEL_59	No Connection
0x173C	MUXARRAY_INPUT_SEL_60	[5:0]	RW OTP	INPUT_SEL_60	No Connection
0x173D	MUXARRAY_INPUT_SEL_61	[5:0]	RW OTP	INPUT_SEL_61	No Connection
0x173E	MUXARRAY_INPUT_SEL_62	[5:0]	RW OTP	INPUT_SEL_62	No Connection
0x173F	MUXARRAY_INPUT_SEL_63	[5:0]	RW OTP	INPUT_SEL_63	No Connection

6.1.4. LDOs

Table 12. LDO_HP (LDO1) Registers

Address	Register Name	Bit	Type	Field Name	Description
0x2000	LDO1_VSEL	[7:0]	RW OTP	VSEL	This register is capped by Field: VSEL_RANGE_MASK_MAX (Reg: LDO1_VSEL_RANGE_MASK_MAX [0x2061]) and Field: VSEL_RANGE_MASK_MIN (Reg: LDO1_VSEL_RANGE_MASK_MIN [0x2060]). Field: VSEL_ACTUAL (Reg: LDO1_VSEL_ACTUAL [0x2065]) returns the LDO limited value. **Value** **Description** 0x0 2.2 V 0x1 to 0xFE 0.005*VSEL + 2.2 V 0xFF 3.475 V
0x2060	LDO1_VSEL_RANGE_MASK_MIN	[7:0]	RW OTP	VSEL_RANGE_MASK_MIN	Min output voltage setting for LDO (see Field: VSEL (Reg: LDO1_VSEL [0x2000]) for encodings). Locked by Register: LOCK_GLOBAL_LOCK_CTRL1 [0x8000]
0x2061	LDO1_VSEL_RANGE_MASK_MAX	[7:0]	RW OTP	VSEL_RANGE_MASK_MAX	Max output voltage setting for LDO (see Field: VSEL (Reg: LDO1_VSEL [0x2000]) for encodings). Locked by Register: LOCK_GLOBAL_LOCK_CTRL1 [0x8000]
0x2063	LDO1_TRIM2	[2:1]	RW OTP	VOUT_OK_DEB	Configures debounce duration of VOUT OK signal from analogue

Address	Register Name	Bit	Type	Field Name	Description
					Value **Description** 0x0 0.0 µs 0x1 64.0 µs 0x2 256.0 µs 0x3 512.0 µs
		[4:3]	RW OTP	ILIM_FLAG_DEB	Configures debounce duration of ILIM FLAG signal from analogue **Value** **Description** 0x0 0.0 µs 0x1 64.0 µs 0x2 256.0 µs 0x3 512.0 µs
0x2064	LDO1_MISC1	[0]	RWT OTP	SEL_VRANGE	**Value** **Description** 0x0 Low range for start-up okay 0x1 High range for start-up okay
0x2065	LDO1_VSEL_ACTUAL	[7:0]	RO	VSEL_ACTUAL	This register returns the actual Field: VSEL (Reg: LDO1_VSEL [0x2000]) capped by Field: VSEL_RANGE_MASK_MAX (Reg: LDO1_VSEL_RANGE_MASK_MAX [0x2061]) and Field: VSEL_RANGE_MASK_MIN (Reg: LDO1_VSEL_RANGE_MASK_MIN [0x2060]).
0x20C0	LDO1_EVENT	[0]	EVENT	EVT_ILIM_FLAG	Current Limit Flag Event Detected
		[1]	EVENT	EVT_VOUT_OK_FLAG	VOUT OK Flag Event Detected
0x20C1	LDO1_STATUS	[0]	RO	STA_ILIM_FLAG	Current Status of the Current Limit Flag
		[1]	RO	STA_VOUT_OK_FLAG	Current Status of the VOUT OK Flag
0x20C2	LDO1_IRQ_MASK	[0]	IRQ_MASK	IRQ_ILIM_FLAG	Mask IRQ for the Current Limit Flag
0x112C	SYSCTL_LDO_CTRL_A	[5]	RW OTP	LDO1_SNS_REMOTE	LDO1 remote sense mode
		[6]	RW OTP	LDO1_SNS_HBW	LDO1 loop lower bandwidth enable

Table 13. LDO_HV (LDO2) Registers

Address	Register Name	Bit	Type	Field Name	Description
0x2200	LDO2_VSEL	[7:0]	RW OTP	VSEL	This register is capped by Field: VSEL_RANGE_MASK_MAX (Reg: LDO2_VSEL_RANGE_MASK_MAX [0x2261]) and Field: VSEL_RANGE_MASK_MIN (Reg: LDO2_VSEL_RANGE_MASK_MIN [0x2260]). Field: VSEL_ACTUAL (Reg: LDO2_VSEL_ACTUAL [0x2265]) returns the LDO limited value. **Value** **Description** 0x0 1.2 V

Address	Register Name	Bit	Type	Field Name	Description
					0x1 to 0xFE 0.01*VSEL + 1.2 V 0xFF 3.75 V
0x2260	LDO2_VSEL_RANGE_MASK_MIN	[7:0]	RW OTP	VSEL_RANGE_MASK_MIN	Min output voltage setting for LDO (see Field: VSEL (Reg: LDO2_VSEL [0x2200]) for encodings). Locked by Register: LOCK_GLOBAL_LOCK_CTRL1 [0x8000]
0x2261	LDO2_VSEL_RANGE_MASK_MAX	[7:0]	RW OTP	VSEL_RANGE_MASK_MAX	Max output voltage setting for LDO (see Field: VSEL (Reg: LDO2_VSEL [0x2200]) for encodings). Locked by Register: LOCK_GLOBAL_LOCK_CTRL1 [0x8000]
0x2263	LDO2_TRIM2	[2:1]	RW OTP	VOUT_OK_DEB	Configures debounce duration of VOUT OK signal from analogue **Value Description** 0x0 0.0 µs 0x1 64.0 µs 0x2 256.0 µs 0x3 512.0 µs
		[4:3]	RW OTP	ILIM_FLAG_DEB	Configures debounce duration of ILIM FLAG signal from analogue **Value Description** 0x0 0.0 µs 0x1 64.0 µs 0x2 256.0 µs 0x3 512.0 µs
0x2264	LDO2_CONF1	[6:0]	RW OTP	SEL_START_ILIM	Startup Current Limit **Value Description** 0x0 30.0 mA 0x1 to 0x7E 12.0*SEL_START_ILIM + 30.0 mA 0x7F 1.554 A
0x2265	LDO2_CONF2	[6:0]	RW OTP	SEL_FUNC_ILIM	Functional Current Limit **Value Description** 0x0 30.0 mA 0x1 to 0x7E 12.0*SEL_FUNC_ILIM + 30.0 mA 0x7F 1.554 A
0x2066	LDO2_VSEL_ACTUAL	[7:0]	RO	VSEL_ACTUAL	This register returns the actual Field: VSEL (Reg: LDO2_VSEL [0x2200]) capped by Field: VSEL_RANGE_MASK_MAX (Reg: LDO2_VSEL_RANGE_MASK_MAX [0x2261]) and Field: VSEL_RANGE_MASK_MIN (Reg: LDO2_VSEL_RANGE_MASK_MIN [0x2260]).
0x2267	LDO2_CONF3	[2:0]	RW OTP	SEL_PULLDN	Pull-down resistors selection bits **Value Description** 0x0 300.0 Ω

Address	Register Name	Bit	Type	Field Name	Description
					0x1 150.0 Ω 0x2 100.0 Ω 0x3 75.0 Ω 0x4 60.0 Ω 0x5 50.0 Ω 0x6 42.9 Ω 0x7 37.5 Ω
		[6:3]	RW OTP	SEL_RAMP	Start-up slew rate control selection bits **Value Description** 0x0 1.0 mV/µs 0x1 2.5 mV/µs 0x2 5.0 mV/µs 0x3 7.5 mV/µs 0x4 10.0 mV/µs 0x5 12.5 mV/µs 0x6 25.0 mV/µs 0x7 50.0 mV/µs 0x8 100.0 mV/µs
0x22C0	LDO2_EVENT	[0]	EVENT	EVT_ILIM_FLAG	Current Limit Flag Event Detected
		[1]	EVENT	EVT_VOUT_OK_FLAG	VOUT OK Flag Event Detected
0x22C1	LDO2_STATUS	[0]	RO	STA_ILIM_FLAG	Current Status of the Current Limit Flag
		[1]	RO	STA_VOUT_OK_FLAG	Current Status of the VOUT OK Flag
0x22C2	LDO2_IRQ_MASK	[0]	IRQ_MASK	IRQ_ILIM_FLAG	Mask IRQ for the Current Limit Flag

Table 14. LDO_LV (LDO3) Registers

Address	Register Name	Bit	Type	Field Name	Description
0x2300	LDO3_VSEL	[7:0]	RW OTP	VSEL	This register is capped by Field: VSEL_RANGE_MASK_MAX (Reg: LDO3_VSEL_RANGE_MASK_MAX [0x2361]) and Field: VSEL_RANGE_MASK_MIN (Reg: LDO3_VSEL_RANGE_MASK_MIN [0x2360]). Field: VSEL_ACTUAL (Reg: LDO3_VSEL_ACTUAL [0x2365]) returns the LDO limited value. **Value Description** 0x0 0.4 V 0x1 to 0xFE 0.005*VSEL + 0.4 V 0xFF 1.675 V
0x2360	LDO3_VSEL_RANGE_MASK_MIN	[7:0]	RW OTP	VSEL_RANGE_MASK_MIN	Min output voltage setting for LDO (see Field: VSEL (Reg: LDO3_VSEL [0x2300]) for encodings). Locked by Register: LOCK_GLOBAL_LOCK_CTRL1 [0x8000]

Address	Register Name	Bit	Type	Field Name	Description
0x2361	LDO3_VSEL_RANGE_MASK_MAX	[7:0]	RW OTP	VSEL_RANGE_MASK_MAX	Max output voltage setting for LDO (see Field: VSEL (Reg: LDO3_VSEL [0x2300]) for encodings). Locked by Register: LOCK_GLOBAL_LOCK_CTRL1 [0x8000]
0x2363	LDO3_TRIM2	[0]	RW OTP	SEL_BYP_MODE	LDO/Bypass Mode configuration. This selection should be set before IP is enabled **Value** **Description** 0x0 Supply is in LDO Mode 0x1 Supply is in Bypass (Load Switch) mode
		[1]	RW OTP	SEL_BYP_VGATE	Voltage output setting for regulator that supplies the pass device gate voltage in Bypass Mode **Value** **Description** 0x0 Gate Voltage set to 2.0 V (to be used when V_{IN} is between 0.5 V to 0.8 V) 0x1 Gate Voltage set to 2.3 V (to be used when V_{IN} is between 0.8 V to 1.25 V)
		[3:2]	RW OTP	SEL_BYP_SLEW_RATE	Bypass Mode Slew Rate Setting during start-up **Value** **Description** 0x0 Slew Rate typically 4mV/µs 0x1 Slew Rate typically 6mV/µs 0x2 Slew Rate typically 8mV/µs 0x3 Slew Rate typically 10mV/us
0x2364	LDO3_TRIM3	[2:1]	RW OTP	VOUT_OK_DEB	Configures debounce duration of VOUT OK signal from analogue **Value** **Description** 0x0 0.0 µs 0x1 64.0 µs 0x2 256.0 µs 0x3 512.0 µs
		[4:3]	RW OTP	ILIM_FLAG_DEB	Configures debounce duration of ILIM FLAG signal from analogue **Value** **Description** 0x0 0.0 µs 0x1 64.0 µs 0x2 256.0 µs 0x3 512.0 µs
0x2365	LDO3_CONF1	[6:0]	RW OTP	SEL_START_ILIM	Startup Current Limit **Value** **Description** 0x0 14.3 mA 0x1 to 0x7E 14.3*SEL_START_ILIM + 14.3 mA 0x7F 1.83 A
0x2366	LDO3_CONF2	[6:0]	RW OTP	SEL_FUNC_ILIM	Functional Current Limit **Value** **Description**

Address	Register Name	Bit	Type	Field Name	Description
					0x0 14.3 mA 0x1 to 0x7E 14.3*SEL_FUNC_ILIM + 14.3 mA 0x7F 1.83 A
0x2367	LDO3_VSEL_ACTUAL	[7:0]	RO	VSEL_ACTUAL	This register returns the actual Field: VSEL (Reg: LDO3_VSEL [0x2300]) capped by Field: VSEL_RANGE_MASK_MAX (Reg: LDO3_VSEL_RANGE_MASK_MAX [0x2361]) and Field: VSEL_RANGE_MASK_MIN (Reg: LDO3_VSEL_RANGE_MASK_MIN [0x2360]).
0x2368	LDO3_CONF3	[2:0]	RW OTP	SEL_PULLDN	Pull-down resistors selection bits **Value Description** 0x0 300.0 Ω 0x1 150.0 Ω 0x2 100.0 Ω 0x3 75.0 Ω 0x4 60.0 Ω 0x5 50.0 Ω 0x6 42.9 Ω 0x7 37.5 Ω
		[6:3]	RW OTP	SEL_RAMP	Start-up slew rate control selection bits **Value Description** 0x0 1.0 mV/µs 0x1 2.5 mV/µs 0x2 5.0 mV/µs 0x3 7.5 mV/µs 0x4 10.0 mV/µs 0x5 12.5 mV/µs 0x6 25.0 mV/µs 0x7 50.0 mV/µs 0x8 100.0 mV/µs
0x23C0	LDO3_EVENT	[0]	EVENT	EVT_ILIM_FLAG	Current Limit Flag Event Detected
		[1]	EVENT	EVT_VOUT_OK_FLAG	V_{OUT} OK Flag Event Detected
0x23C1	LDO3_STATUS	[0]	RO	STA_ILIM_FLAG	Current Status of the Current Limit Flag
		[1]	RO	STA_VOUT_OK_FLAG	Current Status of the V_{OUT} OK Flag
0x23C2	LDO3_IRQ_MASK	[0]	IRQ_MASK	IRQ_ILIM_FLAG	Mask IRQ for the Current Limit Flag

6.1.5. GreenPAK

Table 15. Multi-Function Macrocell Registers

Address	Register Name	Bit	Type	Field Name	Description
0x3300	PAK_MULTI_MCELL_CONFIG_0	[7:0]	RW OTP	LUT3_0_DFF0_CNTDLY0_SETTING	LUT0 or DFF/LATCH configuration **Value Description**

Address	Register Name	Bit	Type	Field Name	Description
					0x0 LUT0[0] or DFF
0x3301	PAK_MULTI_MCELL_CONFIG_1	[3:0]	RW OTP	LUT3_0_DFF0_CNTDLY0_FUNC_SEL	Multi-function mode selection **Value Description** 0x0 Both edge Delay 0x1 Falling edge Delay 0x2 Rising edge Delay 0x3 Both edge One Shot 0x4 Falling edge One Shot 0x5 Rising edge One Shot 0x6 Both edge Frequency detect 0x7 Falling edge Frequency detect 0x8 Rising edge Frequency detect 0x9 Both edge detect 0xA Falling edge detect 0xB Rising edge detect 0xC Both edge reset CNT 0xD Falling edge reset CNT 0xE Rising edge reset CNT 0xF High level reset CNT
		[4]	RW OTP	LUT3_0_DFF0_CNTDLY0_LUT_DFF_SEL	LUT or DFF/LATCH function select **Value Description** 0x0 LUT0 0x1 DFF/LATCH
		[5]	RW OTP	LUT3_0_DFF0_CNTDLY0_CNT_OUT_POL_SEL	CNT/DLY output Polarity selection **Value Description** 0x0 Default Output 0x1 Inverted Output
		[6]	RW OTP	LUT3_0_DFF0_CNTDLY0_DLY_OUT_EGDT_EN	DLY mode edge detection selection **Value Description** 0x0 Normal 0x1 Enable DLY mode edge detection
		[7]	RW OTP	LUT3_0_DFF0_CNTDLY0_CNT_SYNC_EN	CNT mode synchronizer selection **Value Description** 0x0 bypass synchronizer 0x1 enable synchronizer (after two DFFs)
0x3302	PAK_MULTI_MCELL_CONFIG_2	[1:0]	RW OTP	LUT3_0_DFF0_CNTDLY0_MULTI_FUNC_SEL	Multi-function selection **Value Description** 0x0 Single LUT0 or DFF (DLY0 input is low) 0x1 Single CNT0/DLY0 (DLY0 ouput connect to LUT0/DFF) 0x2 CNT0/DLY0 connected to LUT0 or DFF 0x3 LUT0 or DFF connected to CNT0/DLY0

Address	Register Name	Bit	Type	Field Name	Description
		[3:2]	RW OTP	LUT3_0_DFF0_CNTDLY0_DLY2LUT_SEL	CNT0/DLY0 and LUT0 or DFF connection (only works when LUT3_0_DFF0_CNTDLY0_MULTI_FUNC_SEL is 2'b10) **Value Description** 0x0 Input 2 from matrix and connected to LUT's In2 or DFF's D 0x1 Input 1 from matrix and connected to LUT's In1 or DFF's nSET/nRST 0x2 Input 0 from matrix and connected to LUT's In0 or DFF's CLK 0x3 0
		[5:4]	RW OTP	LUT3_0_DFF0_CNTDLY0_CNT_DLY_INIT_SEL	CNT0/DLY0 initial value selection **Value Description** 0x0 Bypass the initial 0x1 Initial 0 0x2 Initial 1 0x3 Initial 1
		[6]	RW OTP	MTFT_EN_SYNC	enable synchronizer **Value Description** 0x0 disable synchronizer
0x3303	PAK_MULTI_MCELL_CONFIG_3	[3:0]	RW OTP	LUT3_0_DFF0_CNTDLY0_CLK_SEL	CNT0/DLY0 clock source selection **Value Description** 0x0 125 kHz selection 0x1 31.25 kHz selection 0x2 976.56 Hz selection 0x3 488.28 Hz selection 0x4 External clock selection 0x5 to 0xF not used
0x3304	PAK_MULTI_MCELL_CONFIG_4	[7:0]	RW OTP	LUT3_0_DFF0_CNTDLY0_CNT_DATA	CNT Data
0x3305	PAK_MULTI_MCELL_CONFIG_5	[7:0]	RO	LUT3_0_DFF0_CNTDLY0_CURRENT_CNT_VALUE	Current CNT Value

Table 16. LUT DFF Registers

Address	Register Name	Bit	Type	Field Name	Description
0x3306	PAK_LUT_MCELL_CONFIG_6	[0]	RW OTP	LUT3_1_DFF1_SETTING_0	DFF/LATCH configuration **Value Description** 0x0 LUT1[0] or DFF 0x1 LUT1[0] or LATCH
		[1]	RW OTP	LUT3_1_DFF1_SETTING_1	DFF/LATCH configuration **Value Description** 0x0 LUT1[1] or Q 0x1 LUT1[1] or QB
		[2]	RW OTP	LUT3_1_DFF1_SETTING_2	DFF/LATCH configuration **Value Description** 0x0 LUT1[2] or low initial polarity

Address	Register Name	Bit	Type	Field Name	Description
					0x1 LUT1[2] or high initial polarity
		[3]	RW OTP	LUT3_1_DFF1_SETTING_3	DFF/LATCH configuration **Value Description** 0x0 LUT1[3] or nRST 0x1 LUT1[3] or nSET
		[7:0]	RW OTP	LUT3_1_DFF1_SETTING_7	Alternative bit setting for 3-bit LUT configuration
0x3307	PAK_LUT_MCELL_CONFIG_7	[7:0]	RW OTP	LUT3_2_DFF2_SETTING	LUT2 or DFF/LATCH configuration (see Reg: PAK_LUT_MCELL_CONFIG_6 [0x3306])
0x3308	PAK_LUT_MCELL_CONFIG_8	[7:0]	RW OTP	LUT3_3_DFF3_SETTING	LUT3 or DFF/LATCH configuration (see Reg: PAK_LUT_MCELL_CONFIG_6 [0x3306])
0x3309	PAK_LUT_MCELL_CONFIG_9	[7:0]	RW OTP	LUT3_4_DFF3_SETTING	LUT4 or DFF/LATCH configuration (see Reg: PAK_LUT_MCELL_CONFIG_6 [0x3306])
0x330A	PAK_LUT_MCELL_CONFIG_10	[7:0]	RW OTP	LUT3_5_DFF3_SETTING	LUT5 or DFF/LATCH configuration (see Reg: PAK_LUT_MCELL_CONFIG_6 [0x3306])
0x330B	PAK_LUT_MCELL_CONFIG_11	[7:0]	RW OTP	LUT3_6_DFF3_SETTING	LUT6 or DFF/LATCH configuration (see Reg: PAK_LUT_MCELL_CONFIG_6 [0x3306])
0x330C	PAK_LUT_MCELL_CONFIG_12	[7:0]	RW OTP	LUT3_7_DFF3_SETTING	LUT7 or DFF/LATCH configuration (see Reg: PAK_LUT_MCELL_CONFIG_6 [0x3306])
0x330D	PAK_LUT_MCELL_CONFIG_13	[0]	RW OTP	LUT3_1_DFF1_LUT_DFF_SEL	LUT1 or DFF/LATCH function select **Value Description** 0x0 LUT1 0x1 DFF/LATCH
		[1]	RW OTP	LUT3_2_DFF2_LUT_DFF_SEL	LUT2 or DFF/LATCH function select **Value Description** 0x0 LUT2 0x1 DFF/LATCH
		[2]	RW OTP	LUT3_3_DFF3_LUT_DFF_SEL	LUT3 or DFF/LATCH function select **Value Description** 0x0 LUT3 0x1 DFF/LATCH
		[3]	RW OTP	LUT3_4_DFF4_LUT_DFF_SEL	LUT4 or DFF/LATCH function select **Value Description** 0x0 LUT4 0x1 DFF/LATCH
		[4]	RW OTP	LUT3_5_DFF5_LUT_DFF_SEL	LUT5 or DFF/LATCH function select **Value Description** 0x0 LUT5 0x1 DFF/LATCH

Address	Register Name	Bit	Type	Field Name	Description
		[5]	RW OTP	LUT3_6_DFF6_LUT_DFF_SEL	LUT6 or DFF/LATCH function select **Value** **Description** 0x0 LUT6 0x1 DFF/LATCH
		[6]	RW OTP	LUT3_7_DFF7_LUT_DFF_SEL	LUT7 or DFF/LATCH function select **Value** **Description** 0x0 LUT7 0x1 DFF/LATCH

Table 17. DLY Macrocell Registers

Address	Register Name	Bit	Type	Field Name	Description
0x330E	DLY_MCELL_CONFIG_14	[4:0]	RW OTP	DLY_1_RISING_DELAY_REGISTER	DLY 1 macrocell rising delay register
0x330F	DLY_MCELL_CONFIG_15	[4:0]	RW OTP	DLY_1_FALLING_DELAY_REGISTER	DLY 1 macrocell falling delay register
0x3310	DLY_MCELL_CONFIG_16	[7]	RW OTP	DLY_1_EN	DLY 1 enable
		[6:5]	RW OTP	DLY_1_POL_REGISTER	DLY 1 macrocell up/down polarity select **Value** **Description** 0x0 up active high, down active high 0x1 up active low, down active high 0x2 up active high, down active low 0x3 up active low, down active low
		[4:0]	RW OTP	DLY_1_DIVIDER_REGISTER	DLY 1 macrocell clock divider select **Value** **Description** 0x1 125 kHz 0x2 31.25 kHz 0x4 976.56 Hz 0x8 488.28 Hz 0x10 Multi-function CNT0/DLY0 output
0x3311	DLY_MCELL_CONFIG_17	[4:0]	RW OTP	DLY_2_RISING_DELAY_REGISTER	DLY 2 macrocell rising delay register
0x3312	DLY_MCELL_CONFIG_18	[4:0]	RW OTP	DLY_2_FALLING_DELAY_REGISTER	DLY 2 macrocell falling delay register
0x3313	DLY_MCELL_CONFIG_19	[7]	RW OTP	DLY_2_EN	DLY 2 enable
		[6:5]	RW OTP	DLY_2_POL_REGISTER	DLY 2 macrocell up/down polarity select **Value** **Description** 0x0 up active high, down active high 0x1 up active low, down active high 0x2 up active high, down active low

Address	Register Name	Bit	Type	Field Name	Description
					0x3 up active low, down active low
		[4:0]	RW OTP	DLY_1_DIVIDER_REGISTER	DLY 2 macrocell clock divider select **Value Description** 0x1 125 kHz 0x2 31.25 kHz 0x4 976.56 Hz 0x8 488.28 Hz 0x10 Multi-function CNT0/DLY0 output
0x3314	DLY_MCELL_CONFIG_20	[4:0]	RW OTP	DLY_3_RISING_DELAY_REGISTER	DLY 3 macrocell rising delay register
0x3315	DLY_MCELL_CONFIG_21	[4:0]	RW OTP	DLY_3_FALLING_DELAY_REGISTER	DLY 3 macrocell falling delay register
0x3316	DLY_MCELL_CONFIG_22	[7]	RW OTP	DLY_3_EN	DLY 3 enable
		[6:5]	RW OTP	DLY_3_POL_REGISTER	DLY 3 macrocell up/down polarity select **Value Description** 0x0 up active high, down active high 0x1 up active low, down active high 0x2 up active high, down active low 0x3 up active low, down active low
		[4:0]	RW OTP	DLY_1_DIVIDER_REGISTER	DLY 3 macrocell clock divider select **Value Description** 0x1 125 kHz 0x2 31.25 kHz 0x4 976.56 Hz 0x8 488.28 Hz 0x10 Multi-function CNT0/DLY0 output

6.1.6. LOCK CONTROL

Table 18. System Lock Control Registers

Address	Register Name	Bit	Type	Field Name	Description
0x8000	LOCK_GLOBAL_LOCK_CTRL1	[1]	RWL OTP	LDO1_LOCK	Write-once bit to lock generic LDO1 features.
		[2]	RWL OTP	LDO2_LOCK	Write-once bit to lock generic LDO2 features.
		[3]	RWL OTP	LDO3_LOCK	Write-once bit to lock generic LDO3 features.
0x8004	LOCK_GLOBAL_LOCK_CTRL	[0]	RWL OTP	GLOBAL_DFT_LOCK	Write-once bit to lock all DFT (RTWT type) registers. A power-on reset is required to clear the lock bit.

Address	Register Name	Bit	Type	Field Name	Description
		[1]	RWL OTP	GLOBAL_RWT_LOCK	Write-once bit to lock all RWT type registers. A power-on reset is required to clear the lock bit.
0x800F	LOCK_LOCK_CTRL	[0]	RWL OTP	FINAL_LOCK_DONE	Write-once bit to lock all RWL type registers globally.

6.2 Register Definitions

Table 19. Register Access Type Definitions

Register Access Type	Description
RO	Register is read-only.
RW	Register is readable and writeable.
RWT	Register is readable; it is writeable only if test register access is enabled.
RTWT	Register is readable and writeable only if test register access is enabled.
R*W* OTP	Register is OTP-programmable. Additionally, it can be read/written as described above.
EVENT	Special register type reserved for events.
LOG_MASK	RW only register. Write 1 to mask FAULT_L event.

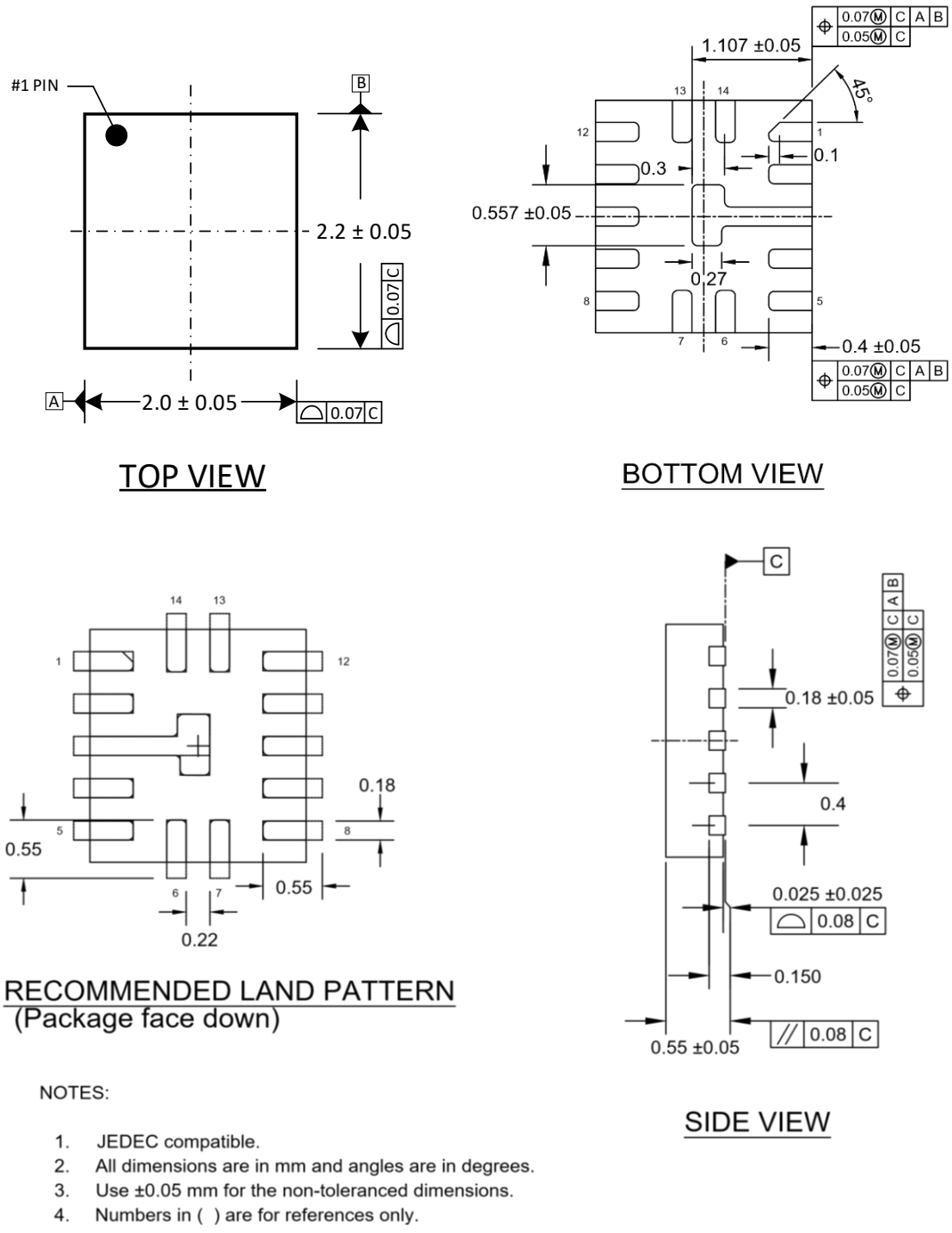
7. Package Information

7.1 Junction-to-Ambient Thermal Resistance (θ_{JA})

Table 20. Junction-to-Ambient Thermal Resistance

Package Option	Thermal Resistance (θ_{JA})
TQFN-14 (SLG51003)	55.4 °C/W

7.2 Package Outline Drawings



NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Figure 21. Package Outline Drawing

7.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 21.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The TQFN-14 package is qualified for MSL 1.

Table 21. MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

7.4 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

8. PCB Layout Guidelines

8.1 Layout Recommendation

To ensure stability and the best performance, please apply the following practices:

- Place input and output decoupling capacitors as close to their respective device pins as possible, on same side as the device, and connected via wide tracks and paralleled vias to reduce inductance.
- Use wide tracks where possible for high current carrying paths, such as V_{IN} and V_{OUT}.
- Do not allow V_{IN} and V_{OUT} routes to run alongside each other too closely for a long distance. This may cause crosstalk or coupling effects.

8.2 PCB Layers Recommended Layout

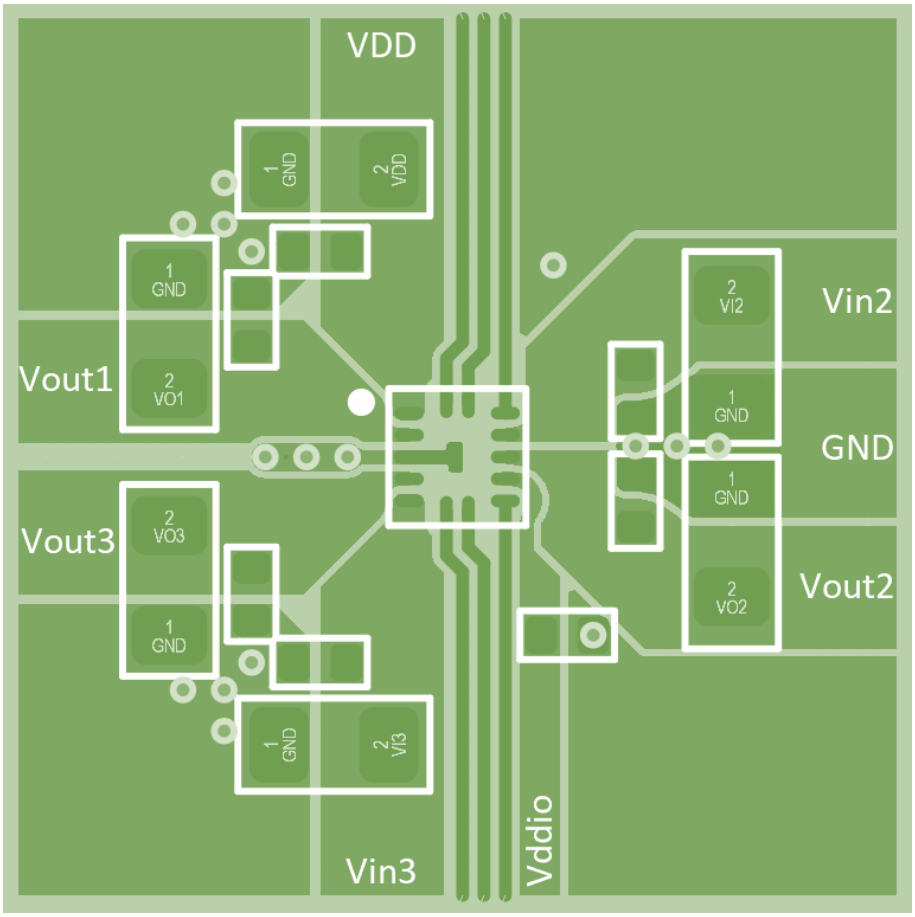


Figure 22. 2-Layer PCB Layout (Top View)

Legend:

– Top Layer (Signal Layer)

– Bottom Layer (Ground Plane)

– Via (Connection to Ground Plane)

9. Glossary

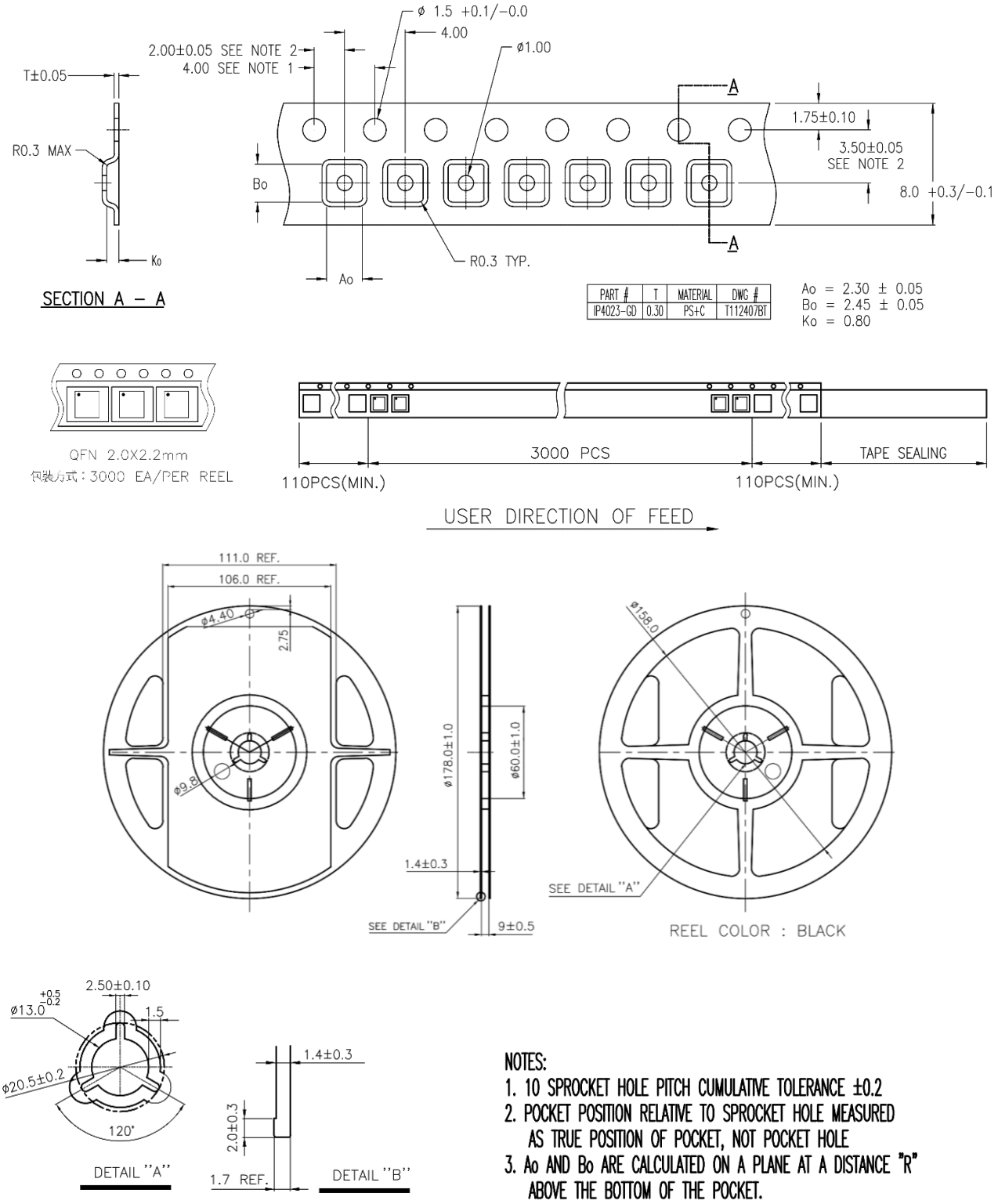
Table 22. Terms and Definitions

Term	Definition
CNT	Counter
CS	Chip Select
DC/DC	Direct Current to Direct Current Converter
DFF	D-Type Flip-Flop
DLY	Delay
EOS	Electrical Overstress
ESD	Electrostatic discharge
GND	Ground
GPIO	General-Purpose Input/Output
I^2C	Inter-Integrated Circuit (Protocol)
LDO	Low Dropout (Regulator)
LDO_HP	LDO High Performance
LDO_HV	LDO High Voltage
LDO_LV	LDO Low Voltage
LSB	Least Significant Bit
LUT	Look Up Table
MSB	Most Significant Bit
MUX	Multiplexor
OTP	One Time Programmable (Memory)
PCB	Printed Circuit Board
POR	Power-On Reset
PSRR	Power Supply Rejection Ratio
SCL	Serial Clock Line
SDA	Serial Data Line
TQFN	Thin Quad Flat No-Lead (Package)
UVLO	Undervoltage Lockout
V_{DD}	Positive Supply Voltage
V_{DDIO}	Positive Supply Voltage for Input/Output pins

10. Ordering Information

Part Number	Package Description	Carrier Type	Temperature Range
SLG51003	TQFN-14, 2.0 mm x 2.2 mm	Tape and Reel	-40 °C to +85 °C

10.1 Tape and Reel Specifications



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
3. Ao AND Bo ARE CALCULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

11. Revision History

Revision	Date	Description
1.00	Sep 12, 2024	Production release