# PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switch

## General Description

SLG51001 contains six compact and customizable low dropout regulators and is designed for high performance camera modules and other small multi-rail applications.

The LDO_HP is optimized to meet the requirements of high-performance analog circuits. It provides very low output voltage noise characteristics of 13 µV (rms) in addition to high PSRR of 81 dB at 1 MHz and tight output voltage accuracy of ±1 % over temperature.

The 1 A capable LDO_LV can be configured to operate as a load switch which is optimized to meet the requirements of low $R_{ON}$. By using efficient DC-DC switching regulators upstream in conjunction with SLG51001's linear regulators and load switch downstream, applications can leverage the best characteristics of each to simultaneously achieve low power, low noise, and low voltage dropout, respectively.

Built-in safety protection such as under-voltage lockout, over-temperature protection, and current limit ensures that the ICs are operating under nominal conditions. SLG51001 has an $I^2C$-compatible interface for flexible power control. SLG51001 is available in a small 16-pin WLCSP package with a wide ambient operating temperature range of -40 °C to 85 °C.

## Key Features

- Input voltage range:
  - 2.8 V to 5.0 V (1 x HP LDO)
  - 1.7 V to 5.0 V (4 x HV LDO)
  - 0.8 V to 1.5 V (1 x LV LDO)
  - 0.5 V to 1.25 V (1 x load switch)
- Separate input supply and enable pins for flexible power configurations
- Output voltage range:
  - 2.4 V to 3.3 V (1 x HP LDO)
  - 1.2 V to 3.75 V (4 x HV LDO)
  - 0.5 V to 1.2 V (1 x LV LDO)
- Output current levels:
  - Up to 475 mA (1 x HP LDO)
  - Up to 500 mA (4 x HV LDO)
  - Up to 1 A (1 x LV LDO)
  - Up to 1 A (1 x load switch)
- High PSRR of 102 dB at 1 kHz and 81 dB at 1 MHz (1 x HP LDO)
- Ultra-low output voltage noise of 13 µV (1 x HP LDO)
- Low dropout voltage (10 mV per 100 mA of load) for high current LDO supply rail (LV LDO)
- Ultra-low $R_{ON}$ load switch with low leakage and slew rate control for low $V_{IN}$ supplies
- Tight output voltage accuracy of ±1 % over-temperature
- Low shutdown current of 300 nA
- Low quiescent current of 14 µA
- User configurable settings via $I^2C$ interface and OTP
  - Including output voltage, power sequencing, soft-start timing, and current limit threshold
- Soft start and soft shutdown
- Under-voltage lockout (UVLO)
- Thermal shutdown
- Configurable temperature alerts
- Wide -40 °C to +85 °C operating temperature
- 16-pin WLCSP: 1.675 mm x 1.675 mm x 0.465 mm, 0.4 mm pitch

## Applications

- High End Camera Module Applications
- Smartphones
- Digital Cameras
- Smart Devices with Imaging

# Contents



# 1 Block Diagram

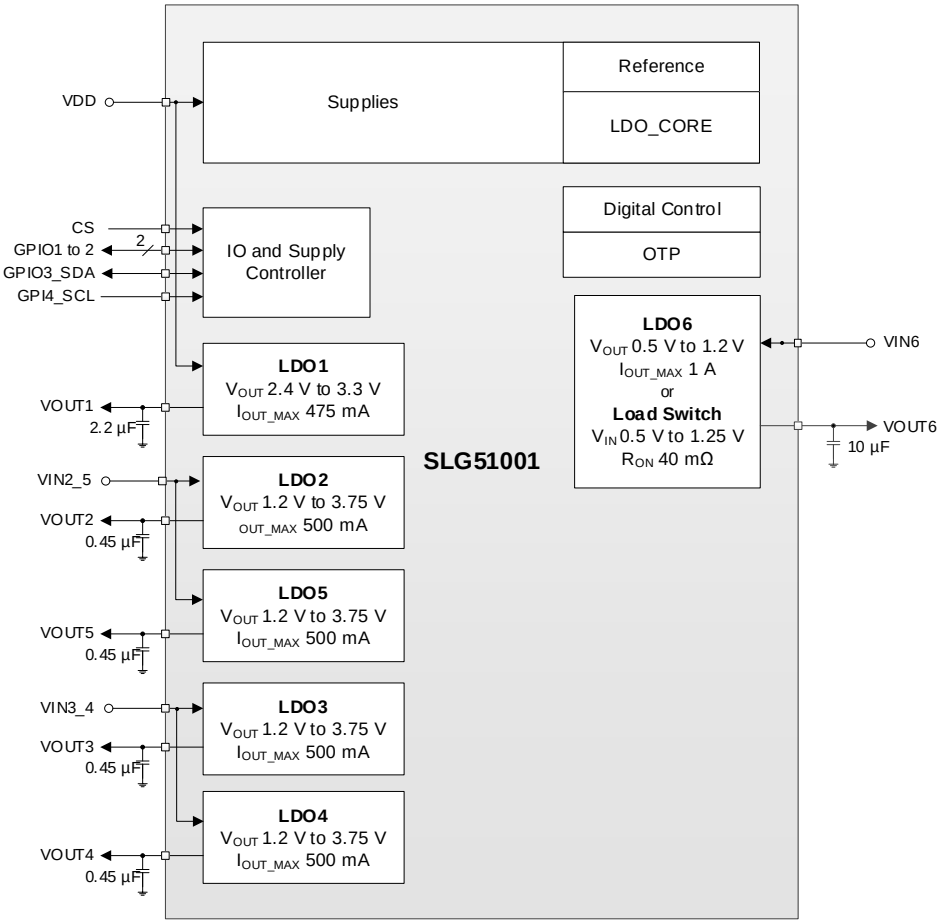
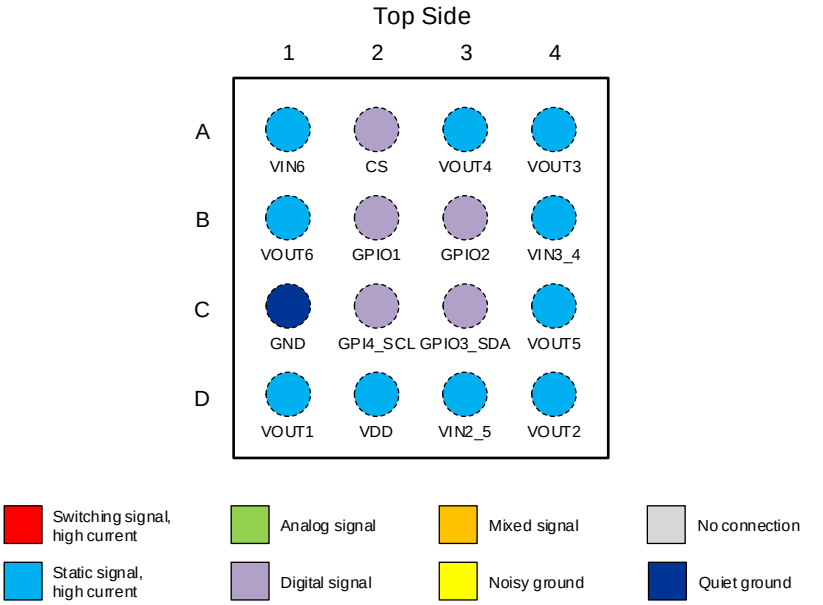



**Figure 1: Block Diagram**

# 2 Pinout



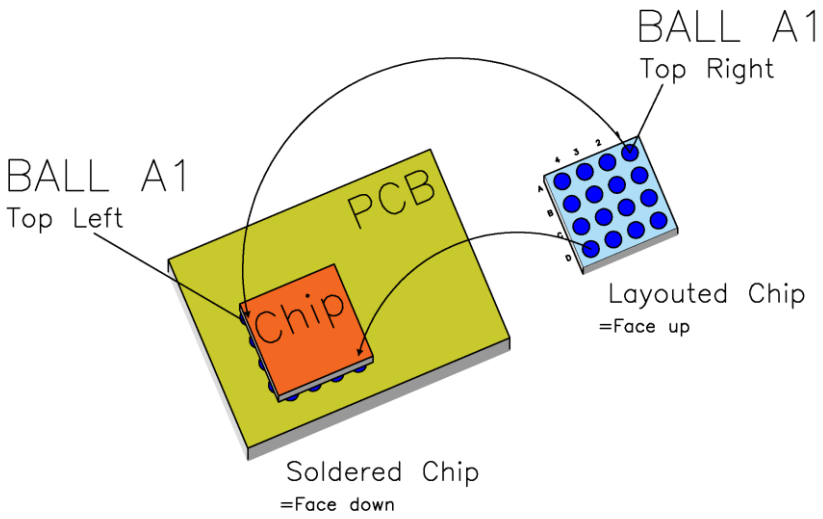




**Figure 2: Pinout Diagram (Top View, Face Down)**

**Table 1: Pin Description**

| Pin No. | Pin Name | Type (Table 2) | Drive (mA) | Reset State | Description |
|---|---|---|---|---|---|
| A2 | CS | DI/PWR | | | Chip select. Also used as the OTP programming power supply. |
| C1 | GND | GND | | | Ground. |
| C2 | GPI4_SCL | DI | | | 1.2 V/1.8 V input cell, or $I^2C$ Serial Clock Line (SCL). |
| B2 | GPIO1 | DIOD | | | 1.2 V/1.8 V input cell, open-drain output. |
| B3 | GPIO2 | DIOD | | | 1.2 V/1.8 V input cell, open-drain output. |
| C3 | GPIO3_SDA | DIOD | | | 1.2 V/1.8 V input cell, open-drain output, or $I^2C$ Serial Data Line (SDA). |
| D2 | VDD | PWR | | | Supply voltage for overall chip control. Controller and power FET supply voltage for low noise LDO (LDO1). |
| D3 | VIN2_5 | PWR | | | Controller and power FET supply voltage for LDO2 and LDO5. |
| B4 | VIN3_4 | PWR | | | Controller and power FET supply voltage for LDO3 and LDO4. |
| A1 | VIN6 | PWR | | | Controller and power FET supply voltage for LDO6. LDO6 can be configured as a load switch |
| D1 | VOUT1 | PWR | | | LDO1 power output. |
| D4 | VOUT2 | PWR | | | LDO2 power output. |
| A4 | VOUT3 | PWR | | | LDO3 power output. |
| A3 | VOUT4 | PWR | | | LDO4 power output. |
| C4 | VOUT5 | PWR | | | LDO5 power output. |
| B1 | VOUT6 | PWR | | | LDO6 power output. LDO6 can be configured as a load switch. |

**Table 2: Pin Type Definition**

| Pin Type | Description | Pin Type | Description |
|---|---|---|---|
| DI | Digital input | AI | Analog input |
| DO | Digital output | AO | Analog output |
| DIO | Digital input/output | AIO | Analog input/output |
| DIOD | Digital input/output open drain | BP | Back drive protection |
| PU | Pull-up resistor (fixed) | SPU | Switchable pull-up resistor |
| PD | Pull-down resistor (fixed) | SPD | Switchable pull-down resistor |
| PWR | Power | GND | Ground |

## 2.1 Input Pins

### 2.1.1 CS – Chip Select

This active-high pin is used to wake SLG51001 from a low-power reset state

To guarantee correct operation, CS must be de-asserted whenever the voltage at the VDD pin is out of the operating conditions boundary (that is VDD < 2.8 V, or VDD > 5.0 V). See Guidelines for Reliable Operation.

When de-asserting the CS pin, it can have a programmable shutdown debounce time (from 0 µs to 256 µs, register CS_T_DEB).

### 2.1.2 SCL – I²C Clock

The SCL signal is the I²C clock.

## 2.2 Bidirectional Pins

### 2.2.1 GPIO1 to GPIO3 and GPI4 – General Purpose Input/Output

The general-purpose input/output pins are configurable by dedicated registers (IO_GPIO<x>_CONF). GPIO1 to GPIO3 can be configured as an input or an open-drain output. GPI4 is always an input pin. In the LOW IQ RESET state, all GPIOs are configured as inputs with no pull-down.

The user-configurable input levels are 1.2 V and 1.8 V.

### 2.2.2 SDA – I²C Data

The SDA signal is the I²C data signal. It is an open-drain signal so that either side can pull it down to a logic low level.

# 3 Characteristics

## 3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Table 3: Absolute Maximum Ratings**

| Parameter | Description | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | Non operational | -40 | +150 | °C |
| $T_J$ | Junction temperature | | -25 | +125 | °C |
| $T_A$ | Ambient temperature | | -40 | +85 | °C |
| $V_{DD}$ | Power supply voltage on VDD pin | | -0.3 | +6.0 | V |
| | Power supply voltage on VIN2_5, VIN3_4 pins | | -0.3 | +6.0 | V |
| | Power supply voltage on VIN5_6 pin | | -0.3 | +1.8 | V |
| $V_{PIN\_LV}$ | Voltage on low-voltage pins | GPIO1 to GPIO3 and GPI4 | -0.3 | +1.98 | V |
| $V_{PIN\_HV}$ | Voltage on high-voltage pins | CS | -0.3 | $V_{DD}$ + 0.3 | V |
| ESD | ESD Protection (Human Body Model) | | 2000 | | V |
| | ESD Protection (Charged Device Model) | | 500 | | V |

### 3.1.1 Guidelines for Reliable Operation

- Low Voltage Pins: take care that the low voltage pins (GPIO1 to GPIO3, GPI4, and VIN6) do not exceed their Abs. Max. ratings, even briefly. Transients both positive (above max) and negative (below min) can cause EOS (Electrical Overstress) damage.
- Power sequencing: CS should not be asserted high before VDD is powered up. CS pin should be de-asserted before VDD falls out of operating range. VIN supplies for LDO_HV and LDO_LV channels (VIN2_5, VIN3_4, VIN6) can be safely biased even if VDD is not present. VIN supplies should be powered up before enabling their respective LDO channels. GPIO's configured as inputs are allowed to be forced high before VDD is powered up.

## 3.2 Recommended Operating Conditions

**Table 4: Recommended Operating Conditions**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient temperature | | -40 | | +85 | °C |
| $V_{DD}$ | Power supply voltage on VDD pin | | 2.8 | | 5.0 | V |
| | Power supply voltage on VIN2_5, VIN3_4 pins | | 1.7 | | 5.0 | V |
| | Power supply voltage on VIN6 pin | LDO Mode | 0.8 | | 1.5 | V |

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Power supply voltage on VIN6 pin | Load Switch Mode | 0.5 | | 1.25 | V |
| $V_{PIN\_LV}$ | Voltage on low-voltage pins | GPIO1 to GPIO3 and GPI4 | 0 | | 1.8 | V |
| $V_{PIN\_HV}$ | Voltage on high-voltage pins | CS | 0 | | VDD | V |

## 3.3 Thermal Characteristics

**Table 5: Package Ratings**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{\Theta\_JA}$ | Package thermal resistance | Junction to ambient JEDEC standard PCB | | 64.3 | | K/W |

## 3.4 Current Consumption

Note: Current consumption electrical characteristics apply over the full operating temperature range.

**Table 6: Current Consumption**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Electrical Performance** | | | | | | |
| IQ_SLEEP | Current consumption in SLEEP. IQ_SLEEP is the IQ in LOW IQ RESET State | VIN = 3.8 V<br>VIN6 = 0 V<br>All references disabled<br>I2C interface disabled<br>All rails disabled | | 0.15 | 0.65 | µA |
| IQ_READY_DIS | Current consumption in READY State | VIN = 3.8 V,<br>VIN6 = 0 V<br>All references enabled<br>I2C interface enabled<br>All rails disabled | | 14 | 24 | µA |
| IQ_READY_EN | Current consumption in READY State | VIN = 3.8 V<br>All references enabled<br>I2C interface enabled<br>All rails enabled, no load | | 390 | 630 | µA |
| IQ_OFF_25C | Quiescent current in OFF Mode | TA = 25 °C | | | 1 | µA |
| IQ_OFF | Quiescent current in OFF Mode | TA =-40 °C to 85 °C | | | 7.6 | µA |

## 3.5 Chip Select Digital I/O Characteristics

Digital I/O electrical characteristics apply over the full operating temperature range, see Section 3.1.1.

**Table 7: High-Voltage Digital I/O Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Electrical Performance** | | | | | | |
| VIH | CS input high voltage | | 0.9 | | VDD | V |
| VIL | CS input low voltage | | 0 | | 0.2 | V |
| ILKG | CS input leakage current | CS < 2V | | | 1 | µA |
| tON_READY | Turn-on time from CS HIGH to Ready State | | | | 10 | ms |

## 3.6 1.2 V/1.8 V Digital I/O Characteristics

1.2 V/1.8 V digital I/O electrical characteristics apply over the full operating temperature range, see Section 3.1.1. The voltage thresholds for all I/Os are referenced to VDDIO, where VDDIO can be 1.2 V or 1.8 V. The supply configuration options depend on the I/O, see Register Definition.

**Table 8: 1.2 V/1.8 V Digital I/O Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Electrical Performance** | | | | | | |
| **GPIO1 to GPIO2** | | | | | | |
| VTHR_POS | Positive going threshold voltage | | 0.4*VDDIO | | 0.7*VDDIO | V |
| VTHR_NEG | Negative going threshold voltage | | 0.3*VDDIO | | 0.6*VDDIO | V |
| VOL | Output low voltage | IOUT ≤ IOL | 0 | | 0.3 | V |
| IOL | Output current | VOL = 0.3 V | 2 | 13 | | mA |
| ILKG | Input leakage | | | | 500 | nA |
| **SCL, SDA, GPIO3 and GPI4** | | | | | | |
| VTHR_POS | Positive going threshold voltage | | 0.4*VDDIO | | 0.7*VDDIO | V |
| VTHR_NEG | Negative going threshold voltage | | 0.3*VDDIO | | 0.6*VDDIO | V |
| VHYS | Schmitt trigger hysteresis | | 0.1*VDDIO | | | V |
| VOL | Output low voltage SDA, GPIO5 | IOUT ≤ IOL | 0 | | 0.3 | V |
| IOL | Output current | VOL = 0.3 V | 20 | | | mA |
| ILKG | Input leakage | | | | 500 | nA |
| CIN | Pin capacitance | | | | 10 | pF |

## 3.7 LDO_HP Characteristics

**Table 9: LDO_HP (LDO1) Electrical Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **External Electrical Conditions** | | | | | | |
| $V_{IN}$ | Input voltage | | 2.8 | | 5 | V |
| $C_{OUT}$ | Output capacitance | Effective capacitance after derating | 2.2 | 4.7 | 10 | µF |
| $I_{OUT\_MAX}$ | Maximum output current | $V_{IN}$ = 3.3 V<br>$V_{OUT}$ drops 50 mV | 475 | | | mA |
| **Programmable Conditions** | | | | | | |
| $V_{OUT}$ | Selectable output voltage | | 2.4 | 2.85 | 3.3 | V |
| $V_{OUT\_LSB}$ | LSB of output voltage programming DAC (8-bit control) | | | 5 | | mV |
| $I_{OUT\_STARTUP\_LIM}$ | Start-up current limit, programmable range<br>Note 1 | At 90 % $V_{OUT}$ | 11 | 140 | 240 | mA |
| **Electrical Performance** | | | | | | |
| **Static Parameters** | | | | | | |
| $V_{OUT\_PP}$ | Part to part output voltage accuracy<br>Note 2 | $I_{OUT}$ = 1 mA<br>$T_A$ = 25 °C | -5 | | 5 | mV |
| $V_{OUT\_TEMP}$ | Temperature dependence of $V_{OUT}$<br>Note 2 | $I_{OUT}$ = 1 mA | -0.65 | | 0.65 | % |
| $V_{OUT\_STATIC\_LINE}$ | Static line regulation<br>Note 2 | $I_{OUT}$ = 1 mA<br>$V_{IN}$ = $V_{OUT}$ + $V_{DROPOUT}$ (Max) to $V_{IN}$ (Max) | -2 | | 2 | mV |
| $V_{OUT\_STATIC\_LD}$ | Static load regulation<br>Note 2 | 1 mA < $I_{OUT}$ < 300 mA | -7.5 | | 5.5 | mV |
| $V_{DROPOUT}$ | Dropout voltage | @ $V_{OUT}$ = $V_{OUT}$ ($V_{IN}$ (Max)) - 10 mV<br>$I_{OUT}$ = 300 mA | | | 200 | mV |
| **Dynamic Parameters** | | | | | | |
| $V_{OUT\_TR\_LINE}$ | Line transient response | $V_{IN}$ = $V_{OUT}$ + $V_{DROPOUT}$ (Max) + 100 mV to $V_{IN}$ = $V_{OUT}$ + $V_{DROPOUT}$ (Max)<br>$V_{OUT}$ = $V_{OUT}$ (Typ)<br>$I_{OUT}$ = 300 mA<br>$t_R$ = $t_F$ = 1 µs | | | 0.3 | mV |

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OUT\_TR\_LD\_1mA}$ | Load transient response | $V_{IN}$ = $V_{OUT}$ + $V_{DROPOUT}$ (Max)<br>$V_{OUT}$ = $V_{OUT}$ (Typ)<br>$I_{OUT}$ = 1 mA to 300 mA<br>$t_R$ = $t_F$ = 1 µs | | | 20 | mV |
| $t_{ON}$ | Turn-on time | Time to 90 % of $V_{OUT}$<br>$I_{OUT}$ = 0 mA | | 0.15 | | ms |
| $t_{OFF}$ | Turn-off time | Time to 10 % of $V_{OUT}$<br>$I_{OUT}$ = 0 mA | | | 2 | ms |
| **AC Parameters** | | | | | | |
| $PSRR_{1kHz}$ | Power supply rejection ratio | f = 1 kHz<br>$V_{IN}$ = 3.2 V<br>$V_{OUT}$ = $V_{OUT}$ (Typ)<br>$I_{OUT}$ = 150 mA<br>$C_{OUT}$ = 4.7 µF<br>Note 3 | | 102 | | dB |
| $PSRR_{100kHz}$ | Power supply rejection ratio | f = 100 kHz<br>$V_{IN}$ = 3.2 V<br>$V_{OUT}$ = $V_{OUT}$ (Typ)<br>$I_{OUT}$ = 150 mA<br>$C_{OUT}$ = 4.7 µF<br>Note 3 | | 87 | | dB |
| $PSRR_{1MHz}$ | Power supply rejection ratio | f = 1 MHz<br>$V_{IN}$ = 3.2 V<br>$V_{OUT}$ = $V_{OUT}$ (Typ)<br>$I_{OUT}$ = 150 mA<br>$C_{OUT}$ = 4.7 µF<br>Note 3 | | 81 | | dB |
| $V_{N\_100kHz}$ | Output noise | f = 10 Hz to 100 kHz<br>$V_{IN}$ = 3.2 V<br>$V_{OUT}$ = $V_{OUT}$ (Typ)<br>$I_{OUT}$ > 30 mA | | 13 | | µV |
| $V_{N\_1MHz}$ | Output noise | f = 10 Hz to 1 MHz<br>$V_{IN}$ = 3.2 V<br>$V_{OUT}$ = $V_{OUT}$ (Typ)<br>$I_{OUT}$ > 10 mA | | 21 | | µV |
| **Current Limit Accuracy** | | | | | | |
| $I_{OUT\_FUNC\_LIM}$ | Functional current limit | | 500 | | | mA |
| $I_{OUT\_STARTUP\_LIM\_ACC}$ | Start-up current limit accuracy | $I_{OUT\_STARTUP\_LIM}$ > 11 mA | -50 | | 50 | % |
| $I_{OUT\_STARTUP\_LIM\_ACC\_11}$ | Start-up current limit accuracy | $I_{OUT\_STARTUP\_LIM}$ = 11 mA | -75 | | 75 | % |

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Quiescent Current Specifications** | | | | | | |
| $I_{Q\_ON\_0mA}$ | Quiescent current | $I_{OUT}$ = 0 mA | | 380 | 600 | µA |
| $I_{Q\_ON\_1mA}$ | Quiescent current | $I_{OUT}$ = 1 mA | | 400 | 600 | µA |
| $I_{Q\_ON\_300mA}$ | Quiescent current | $I_{OUT}$ = 300 mA | | 2.8 | 3.2 | mA |
| $R_{PD\_OFF}$ | Output pull down resistance | $V_{OUT}$ = 0.5 V<br>LDO disabled | | | 40 | Ω |

**Note 1** For programmable selections, refer to Section 4.4.1

**Note 2** The overall accuracy can be calculated by summing $V_{OUT\_PP}$ + $V_{OUT\_TEMP}$ + $V_{OUT\_STATIC\_LD}$ + $V_{OUT\_STATIC\_LINE}$

**Note 3** For $V_{IN}$ - $V_{OUT}$ < 350 mV, PSRR will be degraded.

## 3.8 LDO_HV Characteristics

In the LDO_HV electrical characteristics table, unless otherwise specified, all specifications are guaranteed for VDD above 2.5 V and below 5 V, for $V_{IN}$ as defined in the table, and apply over the full operating temperature range, see Section 3.1.1.

**Table 10: LDO_HV (LDO2, 3, 4, and 5) Electrical Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **External Electrical Conditions** | | | | | | |
| VIN | Input voltage | | 1.7<br>Note 1 | 3.8 | 5 | V |
| COUT | Output capacitance | Effective capacitance after derating | 0.45 | 2.2 | 20 | µF |
| IOUT_MAX | Maximum output current | VOUT drops 50 mV<br>Note 2 | 500 | | | mA |
| **Programmable Conditions** | | | | | | |
| VOUT | Selectable output voltage | | 1.2 | 3.3 | 3.75 | V |
| VOUT_LSB | LSB of output voltage programming DAC (8-bit control) | | | 10 | | mV |
| IOUT_STARTUP_LIM | Start-up current limit, programmable in 12 mA steps<br>Note 3 | At 90 % VOUT | 30 | 150 | 606 | mA |
| IOUT_FUNC_LIM | Functional current limit, programmable in 12 mA steps<br>Note 3 | | 30 | 550 | 606 | mA |

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Electrical Performance** | | | | | | |
| **Static Parameters** | | | | | | |
| VOUT_PP | Part to part output voltage accuracy<br>Note 4 | IOUT = 1 mA<br>TA = 25 °C | -10<br>Note 5 | | 10<br>Note 5 | mV |
| VOUT_TEMP | Temperature dependence of VOUT<br>Note 4 | IOUT = 1 mA<br>Note 6 | -0.65 | | 0.65 | % |
| VOUT_STATIC_LINE | Static line regulation<br>Note 4 | IOUT = 1 mA<br>VIN = VOUT + VDROPOUT (Max) to VIN (Max) | -2 | | 2 | mV |
| VOUT_STATIC_LD | Static load regulation<br>Note 4 | 1 mA < IOUT < IOUT_MAX | -7 | | 2 | mV |
| VDROPOUT | Dropout voltage | @ VOUT = VOUT (VIN (Max)) - 10 mV<br>IOUT = 250mA<br>Note 7 | | | 200<br>Note 8 | mV |
| RON | On resistance | @ VIN = VOUT (VIN (Max)) - 50 mV<br>IOUT = IOUT_MAX<br>Note 7 | | | 800 | mΩ |
| **Dynamic Parameters** | | | | | | |
| VOUT_TR_LINE | Line transient response | VIN = VOUT + VDROPOUT (Max) + 0.6 V to VIN = VOUT + VDROPOUT (Max)<br>VOUT = VOUT (Typ)<br>IOUT = IOUT_MAX<br>tR = tF = 100 mV/µs | | 2 | 5<br>Note 9 | mV |
| VOUT_TR_LD_1mA | Load transient response | VIN = VOUT + VDROPOUT (Max)<br>VOUT = VOUT (Typ)<br>IOUT = 1 mA to IOUT_MAX/2<br>tR = tF = 1 µs | | 28 | 37 | mV |
| tON | Turn-on time | Time to 90 % of VOUT<br>IOUT = 0 mA | | 0.2 | | ms |
| tOFF | Turn-off time | Time to 10 % of VOUT<br>IOUT = 0 mA | | 0.2 | 10 | ms |

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **AC Parameters** | | | | | | |
| PSRR1kHz | Power supply rejection ratio | f = 1 kHz<br>VIN = VOUT + 500 mV<br>VOUT = VOUT (Typ)<br>IOUT = IOUT_MAX/2<br>$C_{OUT}$ = 4.7 µF | | 80 | | dB |
| PSRR100kHz | Power supply rejection ratio | f = 100 kHz<br>VIN = VOUT + 500 mV<br>VOUT = VOUT (Typ)<br>IOUT = IOUT_MAX/2<br>$C_{OUT}$ = 4.7 µF | | 54 | | dB |
| PSRR1MHz | Power supply rejection ratio | f = 1 MHz<br>VIN = VOUT + 500 mV<br>VOUT = VOUT (Typ)<br>IOUT = IOUT_MAX/2<br>$C_{OUT}$ = 4.7 µF | | 47 | | dB |
| VN | Output noise | f = 10 Hz to 100 kHz<br>IOUT = IOUT_MAX/2 | | 152 | | µV |
| **Current Limit Accuracy** | | | | | | |
| IOV_SINK | Current sink at over-voltage | VOV = VOUT + 100 mV<br>Note 10 | 10 | 77 | | mA |
| **Quiescent Current Specifications** | | | | | | |
| IQ_ON_0mA | Quiescent current | IOUT = 0 mA<br>Note 11 | | 13 | 19 | µA |
| IQ_ON_1mA | Quiescent current | IOUT = 1 mA<br>Note 11 | | 36 | 48 | µA |
| IQ_ON_IMAX | Quiescent current | IOUT = IOUT_MAX<br>Note 11 | | 2.25 | 3.5 | mA |
| RPD_OFF | Output pull down resistance | VOUT = 0.5 V<br>LDO disabled | | 30 | 100 | Ω |

**Note 1** IOUT_MAX below 2.1 V is limited to 200 mA. For VIN above 2.1 V, IOUT_MAX of 500 mA is guaranteed.

**Note 2** Guaranteed for VIN > 2.1 V, between 1.7 V and 2.1 V the IOUT_MAX guaranteed is 200 mA.

**Note 3** Accuracy ±30 %

**Note 4** The overall accuracy can be calculated by summing VOUT_PP + VOUT_TEMP + VOUT_STATIC_LD + VOUT_STATIC_LINE.

**Note 5** +10 mV / -10 mV accuracy applies to factory-trimmed VOUT values targeted between 1.23 V to 3.72 V. VOUT targets from 1.20 V to 1.22 V can be trimmed to +24 mV/ -10 mV accuracy. VOUT targets from 3.73 V to 3.75 V can be trimmed to +10 mV / -30 mV accuracy

**Note 6** Guaranteed for VIN ≥ 2.5 V.

**Note 7** Guaranteed for VIN > 1.8 V.

**Note 8** Dropout voltage is linear with the load current. If using a lower IOUT_MAX than specified, the dropout can be calculated using 80 mV per 100 mA of load.

**Note 9** Guaranteed for VIN > 2.1 V. Otherwise, maximum line transient is 20 mV.

**Note 10** Guaranteed for VIN > 2.35 V.

**Note 11** Internal regulator current flowing to ground.

## 3.9 LDO_LV Characteristics

In the LDO_LV electrical characteristics table, unless otherwise specified, all specifications are guaranteed for VDD above 2.5 V and below 4.9 V, for $V_{IN}$ as defined in the table, and apply over the full operating temperature range, see Section 3.1.1.

The characteristics for the LDOs in Load Switch Mode are given in Section 3.9.1.

**Table 11: LDO_LV (LDO6) Electrical Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **External Electrical Conditions** | | | | | | |
| VIN | Input supply (pass device + part of controller) | | 0.8 | 1.25 | 1.5 | V |
| VDD_CTRL | Supply for controller (VDD) | | 2.3 | 3.8 | 5 | V |
| COUT | Output capacitance | Effective capacitance after derating | 10 Note 1 | 20 | 80 | µF |
| ESLCOUT | Output capacitor series inductance | f > 100 kHz | | | 1 | nH |
| IOUT_MAX | Maximum output current | VOUT drops 50 mV | 1000 | | | mA |
| **Programmable Conditions** | | | | | | |
| VOUT | Selectable output voltage | | 0.5 Note 2 | 1.175 | 1.2 | V |
| VOUT_LSB | LSB of output voltage programming DAC (8-bit control) | | | 5 | | mV |
| IOUT_STARTUP_LIM | Start-up current limit, programmable in 13 mA steps Note 3 | At 90 % VOUT | 15 | 150 | 1434 | mA |
| IOUT_FUNC_LIM | Functional current limit, programmable in 13 mA steps Note 3 | | 15 | 1250 | 1434 | mA |
| **Electrical Performance** | | | | | | |
| **Static Parameters** | | | | | | |
| VOUT_PP | Part to part output voltage accuracy Note 4 | IOUT = 1 mA TA = 25 °C | -5 | | 5 | mV |
| VOUT_TEMP | Temperature dependence of VOUT Note 4 | IOUT = 1 mA Note 5 | -0.65 | | 0.65 | % |
| VOUT_STATIC_LINE | Static line regulation Note 4 | IOUT = 1 mA VIN = VOUT + VDROPOUT (Max) to VIN (Max) | -2 | | 2 | mV |

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VOUT_STATIC_LD | Static load regulation<br>Note 4 | 1 mA < IOUT < IOUT_MAX | -8 | | 2 | mV |
| VDROPOUT | Dropout voltage | @ VOUT = VOUT (VIN (Max)) - 10 mV<br>IOUT = IOUT_MAX<br>Note 5 | | | 100<br>Note 6 | mV |
| **Dynamic Parameters** | | | | | | |
| VOUT_TR_LINE | Line transient response | VIN = VOUT + VDROPOUT (Max) + 100 mV to VIN = VOUT + VDROPOUT (Max)<br>VOUT = VOUT (Typ)<br>IOUT = IOUT_MAX<br>tR = tF = 100 mV/µs | | 2 | 5 | mV |
| VOUT_TR_LD_1mA | Load transient response | VIN = VOUT + VDROPOUT (Max)<br>VOUT = VOUT (Typ)<br>IOUT = 1 mA to IOUT_MAX/2<br>tR = tF = 1 µs | | 21 | 29 | mV |
| tON | Turn-on time | Time to 90 % of VOUT<br>IOUT = 0 mA<br>COUT = 20 µF | | 0.15 | | ms |
| tOFF | Turn-off time | Time to 10 % of VOUT<br>IOUT = 0 mA<br>COUT = 20 µF | | 2 | 5<br>Note 7 | ms |
| **AC Parameters** | | | | | | |
| PSRR1kHz | Power supply rejection ratio | f = 1 kHz<br>VIN = VOUT + VDROPOUT (Max) + 200 mV<br>VOUT = VOUT (Typ)<br>IOUT = IOUT_MAX/2<br>$C_{OUT}$ = 20 µF | | 76 | | dB |
| PSRR100kHz | Power supply rejection ratio | f = 100 kHz<br>VIN = VOUT + VDROPOUT (Max) + 200 mV<br>VOUT = VOUT (Typ)<br>IOUT = IOUT_MAX/2<br>$C_{OUT}$ = 20 µF | | 54 | | dB |
| VN | Output noise | f = 10 Hz to 100 kHz<br>IOUT = IOUT_MAX/2 | | 100 | | µV |

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Current Limit Accuracy** | | | | | | |
| IOV_SINK | Current sink at over-voltage | VOV = VOUT + 100 mV | 10 | | | mA |
| **Quiescent Current Specifications** | | | | | | |
| IQ_ON_0mA | Quiescent current, no load | IOUT = 0 mA<br>Note 8 | | 8 | 15 | µA |
| IQ_ON_1mA | Quiescent current, low load | IOUT = 1 mA<br>Note 8 | | 10 | 16 | µA |
| IQ_ON_IMAX | Quiescent current, IOUT_MAX | IOUT = IOUT_MAX<br>Note 8 | | 0.35 | 1.5 | mA |
| RPD_OFF | Output pull down resistance | VOUT = 0.5 V<br>LDO disabled | | 35 | 100 | Ω |

**Note 1** For currents less than 400 mA, a minimum of 1.2 µF (after derating) can be used.

**Note 2** Output is capable down to 0.4 V at reduced accuracy. Please contact Renesas for more information

**Note 3** Accuracy ±30 %

**Note 4** The overall accuracy can be calculated by summing VOUT_PP + VOUT_TEMP + VOUT_STATIC_LD + VOUT_STATIC_LINE.

**Note 5** Spec guaranteed for VDD_CTRL ≥ 2.8 V.

**Note 6** Dropout voltage is linear with the load current. If using a lower IOUT_MAX than specified, the dropout can be calculated using 10 mV per 100 mA of load.

**Note 7** Max tOFF of 20 ms achieved for COUT = 80 µF.

**Note 8** Internal regulator current flowing to ground.

### 3.9.1 Load Switch Mode Characteristics

**Table 12: Load Switch Mode Electrical Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **External Electrical Conditions** | | | | | | |
| VIN | Input voltage | | 0.5<br>Note 1<br>Note 2 | | 1.25 | V |
| IOUT_MAX | Maximum output current | | 1000 | | | mA |
| **Programmable Conditions** | | | | | | |
| SR | Slew rate, programmable to (4, 6, 8, 10) mV/µs | | 4 | | 10 | mV/µs |
| ILIM | Current limit, programmable from 15 mA to 1.434 A in 13 mA steps<br>Note 3 | | 15 | | 1434 | mA |

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Electrical Performance** | | | | | | |
| RON | On resistance | | | 40 | | mΩ |
| SRACC | Slew rate accuracy | | -35 | | 35 | % |
| ILIM_ACC | Current limit accuracy | | -35 | | 35 | % |
| IQ_OFF | Quiescent current in off mode | TA = 25 °C | | | 2 | µA |

**Note 1** Input is capable down to 0.4 V. Please contact Renesas for more information

**Note 2** Register bit SEL_BYP_VGATE must be set to 0 for VIN between 0.5 V and 0.8 V, and is recommended to be set to 1 for VIN between 0.8 V and 1.25 V.

**Note 3** Current limit is guaranteed for VIN > 0.7 V. Below 0.7 V, a functional current limit is not guaranteed.

## 3.10 VREF, IREF, Temperature Supervision Characteristics

**Table 13: VREF, IREF, Temperature Supervision Electrical Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Programmable Conditions** | | | | | | |
| VREF | Reference voltage | Internal VREF | | 1.2 | | V |
| TWARN | Warning temperature threshold, programmable to (90, 100, 110, 120) °C | | 90 | | 120 | °C |
| TWARN_HYS | Warning temperature hysteresis, programmable to (0, 14) °C | | | 14 | | °C |
| **Electrical Performance** | | | | | | |
| VREF_ACC | Reference voltage accuracy | Internal VREF | -1 | | 1 | % |
| TOT | Thermal shutdown over-temperature | | 125 | 140 | 155 | °C |
| TWARN_ACC | Warning temperature threshold accuracy | | -5 | | 5 | °C |

## 3.11 Internal Oscillator Characteristics

**Table 14: Internal Oscillator Electrical Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Electrical Performance** | | | | | | |
| fCLK | Internal clock frequency | | 7.2 | 8 | 8.8 | MHz |

## 3.12 UVLO Characteristics

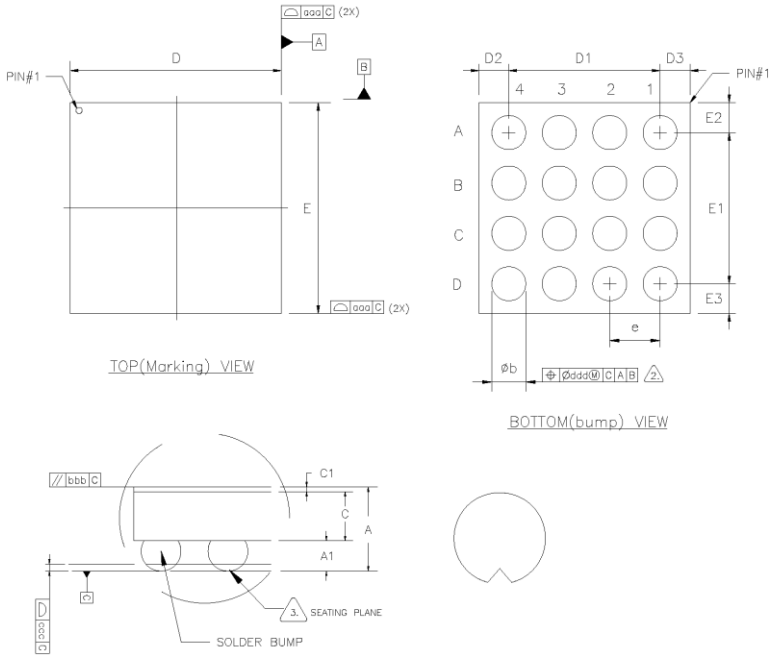
**Table 15: UVLO Electrical Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Programmable Conditions** | | | | | | |
| VDD_UVLO_LWR | Under-voltage lower threshold (falling edge) Note 1 | | 2.215 | | 2.658 | V |
| VDD_UVLO_UPPER | Under-voltage upper threshold (rising edge) | | | VDD_UVLO_LWR + 3 % | | V |
| **Electrical Performance** | | | | | | |
| VDD_POR_UPPER | Deep discharge lockout upper threshold | | | 2.1 | 2.2 | V |
| VDD_POR_LWR | Deep discharge lockout lower threshold | | | 1.9 | | V |
| VDD_UVLO_STAT_ACC | Under-voltage lower threshold static accuracy with flip gate bandgap reference | | -1.5 | | 1.5 | % |

**Note 1** This voltage is programmed from OTP.

# 4 Package Information

## 4.1 Package Outlines




| Symbol | Dimensions in mm | | | Dimensions in inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.4350 | 0.4650 | 0.4950 | 0.0171 | 0.0183 | 0.0195 |
| A1 | 0.1750 | 0.1900 | 0.2050 | 0.0069 | 0.0075 | 0.0081 |
| c | 0.2250 | 0.2500 | 0.2750 | 0.0089 | 0.0098 | 0.0108 |
| c1 | 0.0220 | 0.0250 | 0.0280 | 0.0009 | 0.0010 | 0.0011 |
| D | 1.6500 | 1.6750 | 1.7000 | 0.0650 | 0.0659 | 0.0669 |
| E | 1.6500 | 1.6750 | 1.7000 | 0.0650 | 0.0659 | 0.0669 |
| b | 0.2400 | 0.2700 | 0.3000 | 0.0094 | 0.0106 | 0.0118 |
| D1 | --- | 1.2000 | --- | --- | 0.0472 | --- |
| D2 | --- | 0.2375 | --- | --- | 0.0094 | --- |
| D3 | --- | 0.2375 | --- | --- | 0.0094 | --- |
| E1 | --- | 1.2000 | --- | --- | 0.0472 | --- |
| E2 | --- | 0.2375 | --- | --- | 0.0094 | --- |
| E3 | --- | 0.2375 | --- | --- | 0.0094 | --- |
| e | --- | 0.4000 | --- | --- | 0.0157 | --- |
| aaa | --- | 0.0250 | --- | --- | 0.0010 | --- |
| bbb | --- | 0.0600 | --- | --- | 0.0024 | --- |
| ccc | --- | 0.0300 | --- | --- | 0.0012 | --- |
| ddd | --- | 0.0150 | --- | --- | 0.0006 | --- |

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.

2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

**Figure 3: Package Outline Drawing**

## 4.2 PCB Landing Pattern

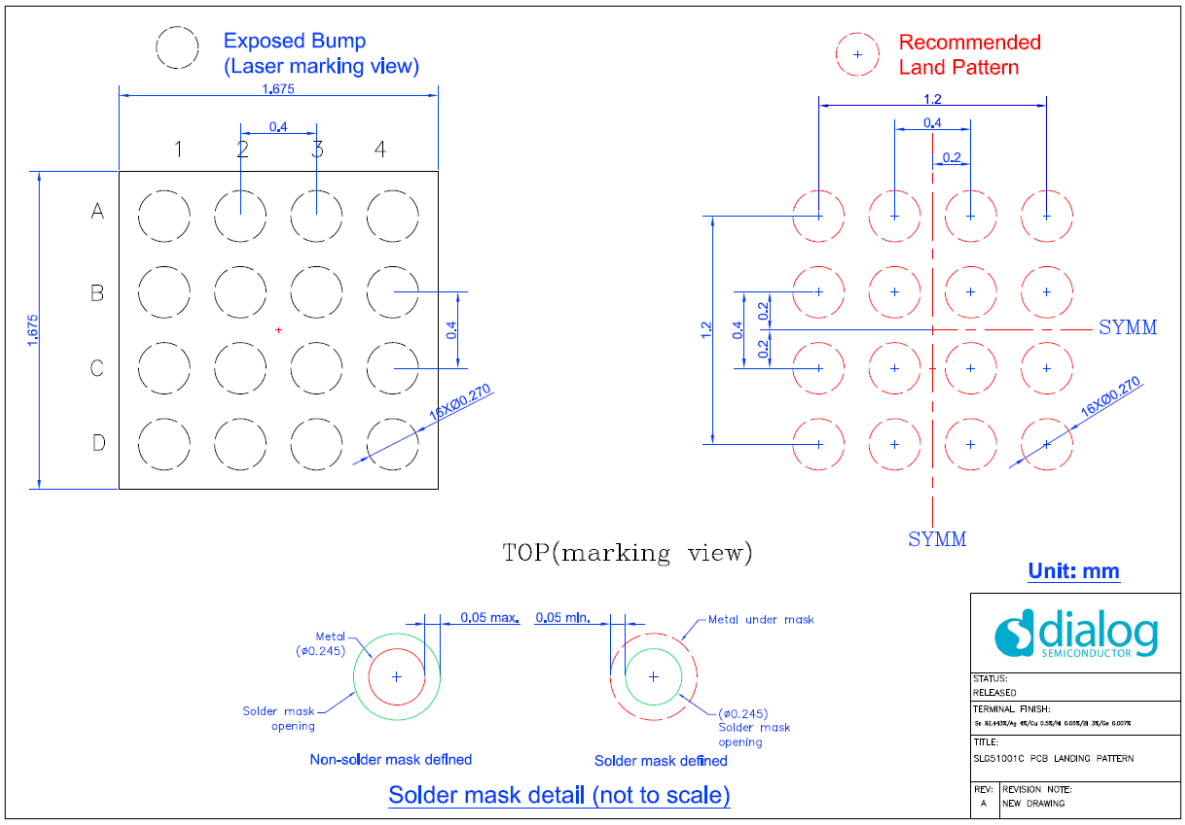



**Figure 4: PCB Landing Pattern**

## 4.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in

Table 16.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

MSL rating does not apply to this device as it is not plastic encapsulated.

**Table 16: MSL Classification**

| MSL Level | Floor Lifetime | Conditions |
|---|---|---|
| MSL 4 | 72 hours | 30 °C / 60 % RH |
| MSL 3 | 168 hours | 30 °C / 60 % RH |
| MSL 2A | 4 weeks | 30 °C / 60 % RH |
| MSL 2 | 1 year | 30 °C / 60 % RH |
| MSL 1 | Unlimited | 30 °C / 85 % RH |

## 4.4 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLCSP package will cause damage to the solder balls. Therefore a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

## 4.5 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

# 5 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Renesas customer support portal or your local sales representative.

**Table 17: Ordering Information**

| Part Number | Package | Size (mm) | Shipment Form | Pack Quantity |
|---|---|---|---|---|
| SLG51001CTR | WLCSP-16 | 1.675 x 1.675 | T & R | 3,000 |