SLG47004

GreenPAK Programmable Mixed-Signal Matrix with In-System Programmability and Advanced Analog Features

General Description

The SLG47004 provides a small, low power component for commonly used analog signal processing and mixed-signal functions. Individual, tunable, analog components used in conjunction with configurable logic provide a way to solve a wide variety of tasks with minimal costs. The user creates their circuit design by programming the multiple time Non-Volatile Memory (NVM) to configure the interconnect logic, the analog and digital macrocell, and the IO Pins of the SLG47004.

Key Features

- Two Programmable Bandwidth Op Amps
  - 3-Op Amp Instrumentation Amplifier Function (including Additional Internal Op Amp)
  - Rail to Rail Input
  - Low Quiescent Current
  - Low Offset Voltage
  - Analog Comparator Mode
  - Optional Vref Voltage Connection for Input Pins
- Two 1024 Position Digital Rheostats
  - User Defined Auto-Trim Option
  - Manual Control Option
  - I^2C Control Option
  - Potentiometer Mode
- Two Single-Pole/Single-Throw Analog Switches
  - Voltage or Current Source/Sink Mode
- One Low Offset Chopper Comparator
- Two Low Power General Purpose ACMPs
  - ACMP Sampling Mode
  - Hysteresis with Independently-Selectable Thresholds
- Three Voltage References
  - Two ACMP Vref Output Buffers
  - One High Drive Buffer
- Thirteen Combination Function Macrocells
  - Three Selectable DFF/LATCH or 2-bit LUTs
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Seven Selectable DFF/LATCH or 3-bit LUTs
  - One Selectable Pipe Delay or Ripple Counter or 3-bit LUT
  - One Selectable DFF/LATCH or 4-bit LUT
- Seven Multi-Function Macrocells
  - Six Selectable DFF/LATCH or 3-bit LUTs + 8-bit Delay/Counters
  - One Selectable DFF/LATCH or 4-bit LUT + 16-bit Delay/Counter
- Serial Communications
  - I^2C Protocol Interface
- 2-kbit (256 x 8) I^2C-Compatible (2-Wire) Serial EEPROM Emulation with Software Write Protection
- Programmable Delay with Edge Detector Output
- Deglitch Filter or Edge Detector
- Three Oscillators
  - 2.048 kHz Oscillator
  - 2.048 MHz Oscillator
  - 25 MHz Oscillator
- Analog Temperature Sensor
- Power-On Reset
- In-System Programmability
- Multiple Time Programmable Memory
- Wide Range Power Supply
  - 2.5 V (±4 %) to 5 V (±10 %) V_{DD}
- Operating Temperature Range: -40 °C to +85 °C
- RoHS Compliant/Halogen-Free
- Package Available
  - 24-pin STQFN: 3 mm x 3 mm x 0.55 mm, 0.4 mm pitch

Applications

- Adjust Precision Threshold
- Sensor Offset Trimming/Calibration
- Tunable Analog Filters
- Operational Amplifier Adjustable Gain and Offset
- Adjustable Voltage-to-Current Conversions
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics
- Smartphones and Fitness Bands
- Notebook and Tablet PCs

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1 Block Diagram

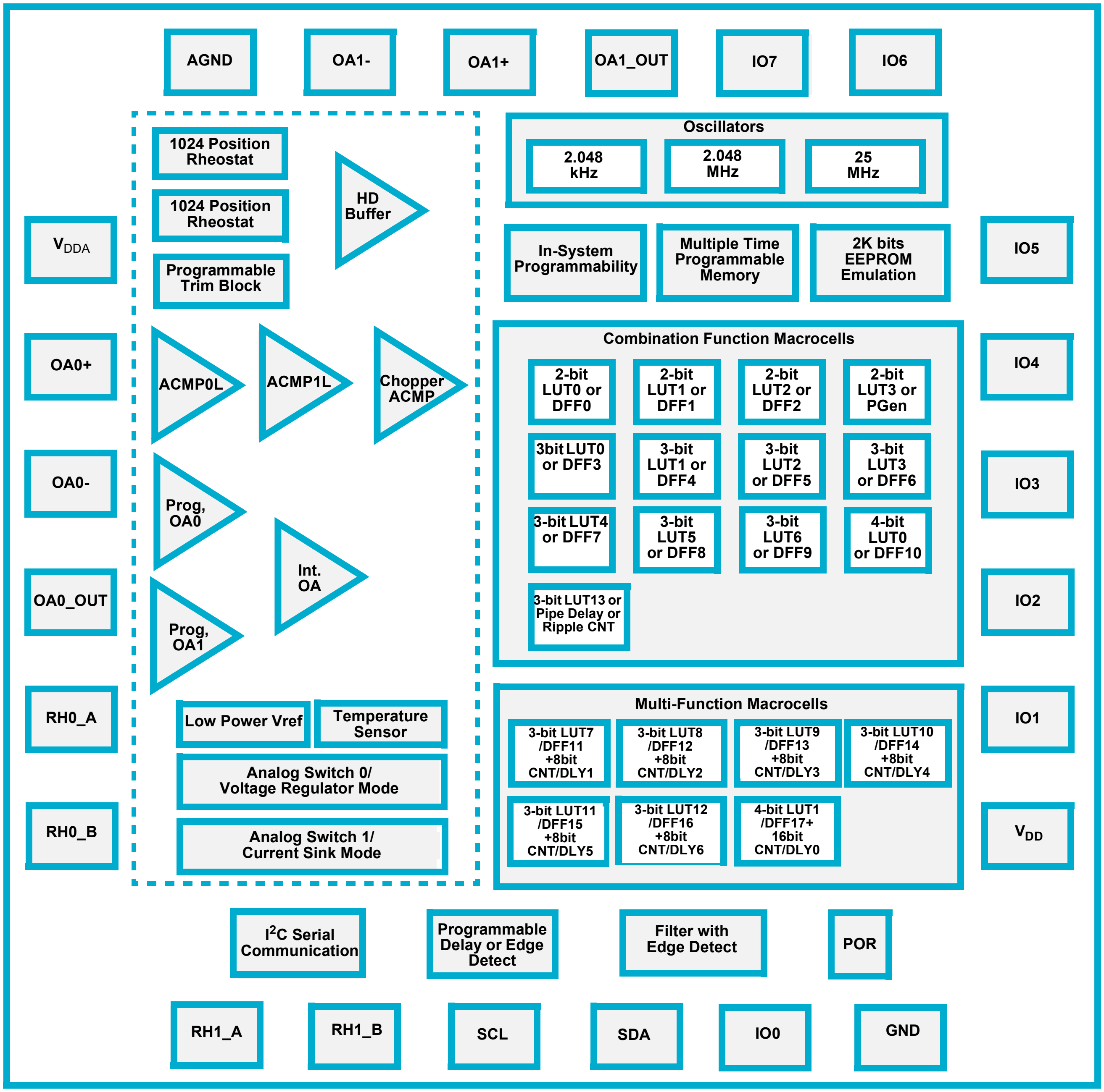
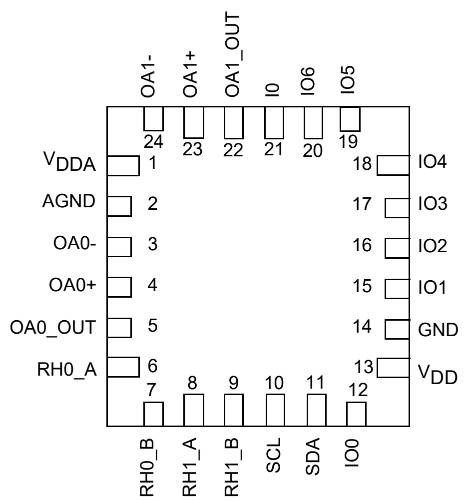


Figure 1: Block Diagram

2 Pinout

2.1 PIN CONFIGURATION - STQFN-24L



STQFN-24
(Top View)

Pin #	Signal Name	Pin Functions
1	V_{DDA}	Analog Power Supply
2	AGND	Analog Ground
3	OA0-	Op Amp0 Inverting Input
4	OA0+	Op Amp0 Non-Inverting Input
5	OA0_OUT	Op Amp0_OUT/ACMP0L+ /
6	RH0_A	Digital Rheostat 0 Terminal A
7	RH0_B	Digital Rheostat 0 Terminal B
8	RH1_A	Digital Rheostat 1 Terminal A
9	RH1_B	Digital Rheostat 1 Terminal B
10	SCL	I^2C_SCL
11	SDA	I^2C_SDA
12	IO0	GPIO, ACMP0L-, ACMP1L-, EXT_OSC0_IN, Vref0_Out or Temp_Sens_Out
13	V_{DD}	Digital Power Supply
14	GND	Digital Ground
15	IO1	GPIO, Chop_ACMP+, Vref1_OUT or Temp_Sens_Out, EXT_OSC1_IN or SLA_0
16	IO2	GPIO, ACMP0L+, EXT_OSC2_IN, SLA_1
17	IO3	GPIO, AS_1_A, ACMP1L+ or SLA_2
18	IO4	GPIO, AS_1_B, Chop_ACMP-or SLA_3
19	IO5	GPIO, AS_0_B
20	IO6	GPIO, AS_0_A, HD_Buff_Out, In Amp_Vref
21	I0	GPI, In Amp_OUT
22	OA1_OUT	Op Amp1_OUT, ACMP1L+
23	OA1+	Op Amp1 Non-inverting Input
24	OA1-	Op Amp1 Inverting Input

Legend:

ACMPx+: ACMPx Positive Input
ACMPx-: ACMPx Negative Input
SCL: I^2C Clock Input
SDA: I^2C Data Input/Output
Vrefx: Voltage Reference Output
SLA: Slave Address

Table 1: Functional Pin Description

Pin No. STQFN 24L	Pin Name	Signal Name	Function	Input Options	Output Options
1	V_{DDA}	V_{DDA}	Analog Power Supply	--	--
2	AGND	AGND	Analog Ground	--	--
3	OA0-	OA0-	Op Amp0 Inverting Input	Analog	--
4	OA0+	OA0+	Op Amp0 Non-Inverting Input	Analog	--
5	OA0_OUT	OA0_OUT	Op Amp0 Output	--	Analog
		ACMP0L+	Analog Comparator 0 Positive Input	Analog	--
6	RH0_A	RH0_A	Digital Rheostat 0 Terminal A	--	--

Table 1: Functional Pin Description(Continued)

Pin No. STQFN 24L	Pin Name	Signal Name	Function	Input Options	Output Options
7	RH0_B	RH0_B	Digital Rheostat 0 Terminal B	--	--
8	RH1_A	RH1_A	Digital Rheostat 1 Terminal A	--	--
9	RH1_B	RH1_B	Digital Rheostat 1 Terminal B	--	--
10	SCL	SCL	I^2C Serial Clock	--	--
11	SDA	SDA	I^2C Serial Data	--	--
12	IO0	IO0	General Purpose IO	--	--
		ACMP0L-	Analog Comparator 0 Negative Input	Analog	--
		ACMP1L-	Analog Comparator 1 Negative Input	Analog	--
		EXT_OSC0_IN	External Clock Connection	--	--
		Vref0_Out	Voltage Reference 0 Output	--	Analog
13	V_{DD}	V_{DD}	Digital Power Supply	--	--
14	GND	GND	Digital Ground	--	--
15	IO1	IO1	General Purpose IO	--	--
		CHOP_ACMP+	Chopper ACMP Positive Input	Analog	--
		Temp_Sens_Out	Temperature Sensor Output	--	Analog
		EXT_OSC1_IN	External Clock Connection	--	--
		SLA_0	Slave Address 0	--	--
16	IO2	IO2	General Purpose IO	--	--
		ACMP0L+	Analog Comparator 0 Positive Input	Analog	--
		EXT_OSC2_IN	External Clock Connection	--	--
		SLA_1	Slave Address 1	--	--
17	IO3	IO3	General Purpose IO	--	--
		AS_1_A	Analog Switch 1Input A	Analog	Analog
		ACMP1L+	Analog Comparator 1 Positive Input	--	--
		SLA_2	Slave Address 2	--	--
18	IO4	IO4	General Purpose IO	--	--
		AS_1_B	Analog Switch 1 Input B	Analog	Analog
			Chopper ACMP Negative Input	Analog	--
		SLA_3	Slave Address 3	--	--

Table 1: Functional Pin Description(Continued)

Pin No. STQFN 24L	Pin Name	Signal Name	Function	Input Options	Output Options
19	IO5	IO5	General Purpose IO	--	--
		AS_0_B	Analog Switch 0 Input B	Analog	Analog
20	IO6	IO6	General Purpose IO	--	--
		AS_0_A	Analog Switch 0 Input A	Analog	Analog
		HD_Buffer_Out	High Drive Buffer Out put	--	Analog
		In Amp_Vref	Instrumentation Amplifier Voltage Reference	Analog	--
21	I0	I0	General Purpose Input	--	--
		In Amp Out	Instrumentation Amplifier Output	Analog	--
22	OA1_OUT	OA1_OUT	Op Amp1 Output	--	Analog
		ACMP1L+	Analog Comparator 1 Positive Input	Analog	--
23	OA1+	OA1+	Op Amp1 Non-inverting Input	Analog	--
24	OA1-	OA1-	Op Amp1 Inverting Input	Analog	--

Table 2: Pin Type Definitions

Pin Type	Description
V_{DDA}	Analog Power Supply
AGND	Analog Ground
OA-	Op Amp Inverting Input
OA+	Op Amp Non-Inverting Input
OA_OUT	Op Amp Output
RH_A	Digital Rheostat Terminal A
RH_B	Digital Rheostat Terminal B
SCL	I^2C Serial Clock
SDA	I^2C Serial Data
IO	General Purpose Input/Output
V_{DD}	Digital Power Supply
GND	Digital Ground
I	General Purpose Input

3 Characteristics

3.1 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Analog and digital grounds must be connected together on the PCB board. The place of connection depends on users schematic. For application cases with low digital current of SLG47004, both AGND and GND should be connected to analog ground plane.

Table 3: Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{DD} to GND, V_{DDA} to AGND **(Note 1)**		-0.3	7	V
Maximum Slew Rate of V_{DDA}		--	2	V/µs
Voltage at Input Pin		GND-0.3	V_{DD}+0.3	V
Current at Input Pin		-1.0	1.0	mA
Maximum Average or DC Current through V_{DDA} or AGND Pin (Per chip side)	T_J = 85 °C	--	110	mA
	T_J = 110°C	--	50	mA
Maximum Average or DC Current through V_{DD} or GND Pin (Per chip side)	T_J = 85 °C	--	100	mA
	T_J = 110°C	--	50	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
Thermal Resistance **(Note 2)**		--	132	°C/W
Moisture Sensitivity Level		1		

Note 1 V_{DDA} must be equal to V_{DD}
Note 2 Measurements based on Analog Switches

3.2 ELECTROSTATIC DISCHARGE RATINGS

Table 4: Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V

3.3 RECOMMENDED OPERATING CONDITIONS

Table 5: Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DDA})		2.4	5.5	V
	During NVM Write and Erase commands	2.5	5.5	V
Operating Temperature		-40	85	°C
Capacitor Value at V_{DD}		0.1	--	µF
Analog Input Common Mode Range	Allowable Input Voltage at Analog Pins	-0.2	V_{DDA}+0.2	V

3.4 ELECTRICAL CHARACTERISTICS

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IH}	HIGH-Level Input Voltage	Logic Input **(Note 1)**	0.7x V_{DD}	--	V_{DD}+ 0.3	V
		Logic Input with Schmitt Trigger	0.8x V_{DD}	--	V_{DD}+ 0.3	V
		Low-Level Logic Input **(Note 1)**	1.25	--	V_{DD}+ 0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input **(Note 1)**	GND-0.3	--	0.3x V_{DD}	V
		Logic Input with Schmitt Trigger	GND-0.3	--	0.2x V_{DD}	V
		Low-Level Logic Input **(Note 1)**	GND-0.3	--	0.5	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	V_{DD} = 2.5 V +/- 8 %	0.30	0.43	0.58	V
		V_{DD} = 3.3 V +/- 10 %	0.34	0.46	0.60	V
		V_{DD} = 5 V +/- 10 %	0.45	0.58	0.77	V
V_O	Maximal Voltage Applied to any PIN in High Impedance State		--	--	V_{DD}+ 0.3	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull, 1x Drive, I_{OH} = 1 mA, V_{DD} = 2.4 V **(Note 1)**	2.282	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 1 mA, V_{DD} = 2.5 V **(Note 1)**	2.387	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 1 mA, V_{DD} = 2.7 V **(Note 1)**	2.597	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.0 V **(Note 1)**	2.709	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V **(Note 1)**	3.037	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V **(Note 1)**	3.359	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = 4.5 V **(Note 1)**	4.161	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = 5.0 V **(Note 1)**	4.687	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = 5.5 V **(Note 1)**	5.213	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 1 mA, V_{DD} = 2.4 V **(Note 1)**	2.342	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 1 mA, V_{DD} = 2.5 V **(Note 1)**	2.445	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 1 mA, V_{DD} = 2.7 V **(Note 1)**	2.649	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.0 V **(Note 1)**	2.859	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V **(Note 1)**	3.171	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V **(Note 1)**	3.481	--	--	V

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OH}	HIGH-Level Output Voltage	Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = 4.5 V **(Note 1)**	4.333	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = 5.0 V **(Note 1)**	4.845	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = 5.5 V **(Note 1)**	5.356	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, 1x Drive, I_{OL}= 1 mA, V_{DD} = 2.4 V **(Note 1)**	--	--	0.085	V
		Push-Pull, 1x Drive, I_{OL}= 1 mA, V_{DD} = 2.5 V **(Note 1)**	--	--	0.082	V
		Push-Pull, 1x Drive, I_{OL}= 1 mA, V_{DD} = 2.7 V **(Note 1)**	--	--	0.077	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.0 V **(Note 1)**	--	--	0.218	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V **(Note 1)**	--	--	0.202	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V **(Note 1)**	--	--	0.190	V
		Push-Pull, 1x Drive, I_{OL}= 5 mA, V_{DD} = 4.5 V **(Note 1)**	--	--	0.277	V
		Push-Pull, 1x Drive, I_{OL}= 5 mA, V_{DD} = 5.0 V **(Note 1)**	--	--	0.260	V
		Push-Pull, 1x Drive, I_{OL}= 5 mA, V_{DD} = 5.5 V **(Note 1)**	--	--	0.245	V
		Push-Pull, 2x Drive, I_{OL}= 1 mA, V_{DD} = 2.4 V **(Note 1)**	--	--	0.043	V
		Push-Pull, 2x Drive, I_{OL} = 1 mA, V_{DD} = 2.5 V **(Note 1)**	--	--	0.042	V
		Push-Pull, 2x Drive, I_{OL} = 1 mA, V_{DD} = 2.7 V **(Note 1)**	--	--	0.039	V
		Push-Pull, 2x Drive, I_{OL}= 3 mA, V_{DD} = 3.0 V **(Note 1)**	--	--	0.109	V
		Push-Pull, 2x Drive, I_{OL}= 3 mA, V_{DD} = 3.3 V **(Note 1)**	--	--	0.102	V
		Push-Pull, 2x Drive, I_{OL}= 3 mA, V_{DD} = 3.6 V **(Note 1)**	--	--	0.096	V
		Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = 4.5 V **(Note 1)**	--	--	0.143	V
		Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = 5.0 V **(Note 1)**	--	--	0.136	V
		Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = 5.5 V **(Note 1)**	--	--	0.127	V
		NMOS OD, 1x Drive, I_{OL}= 1 mA, V_{DD} = 2.4 V **(Note 1)**	--	--	0.035	V
		NMOS OD, 1x Drive, I_{OL} = 1 mA, V_{DD} = 2.5 V **(Note 1)**	--	--	0.034	V
		NMOS OD, 1x Drive, I_{OL} = 1 mA, V_{DD} = 2.7 V **(Note 1)**	--	--	0.032	V
		NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.0 V **(Note 1)**	--	--	0.088	V

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OL}	LOW-Level Output Voltage	NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V **(Note 1)**	--	--	0.082	V
		NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V **(Note 1)**	--	--	0.078	V
		NMOS OD, 1x Drive, I_{OL} = 5 mA, V_{DD} = 4.5 V **(Note 1)**	--	--	0.114	V
		NMOS OD, 1x Drive, I_{OL} = 5 mA, V_{DD} = 5.0 V **(Note 1)**	--	--	0.108	V
		NMOS OD, 1x Drive, I_{OL} = 5 mA, V_{DD} = 5.5 V **(Note 1)**	--	--	0.103	V
		NMOS OD, 2x Drive, I_{OL}= 1 mA, V_{DD} = 2.4 V **(Note 1)**	--	--	0.019	V
		NMOS OD, 2x Drive, I_{OL} = 1 mA, V_{DD} = 2.5 V **(Note 1)**	--	--	0.019	V
		NMOS OD, 2x Drive, I_{OL} = 1 mA, V_{DD} = 2.7 V **(Note 1)**	--	--	0.018	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.0 V **(Note 1)**	--	--	0.047	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V **(Note 1)**	--	--	0.044	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V **(Note 1)**	--	--	0.042	V
		NMOS OD, 2x Drive, I_{OL} = 5 mA, V_{DD} = 4.5 V **(Note 1)**	--	--	0.063	V
		NMOS OD, 2x Drive, I_{OL} = 5 mA, V_{DD} = 5.0 V **(Note 1)**	--	--	0.060	V
		NMOS OD, 2x Drive, I_{OL} = 5 mA, V_{DD} = 5.5 V **(Note 1)**	--	--	0.057	V
I_{OH}	HIGH-Level Output Current **(Note 2)**	Push-Pull, 1x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.4 V **(Note 1)**	1.63	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.5 V **(Note 1)**	1.72	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.7 V **(Note 1)**	1.88	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.0 V **(Note 1)**	5.48	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V **(Note 1)**	8.31	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V **(Note 1)**	11.11	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 4.5 V **(Note 1)**	19.61	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 5.0 V **(Note 1)**	24.00	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 5.5 V **(Note 1)**	29.24	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.4 V **(Note 1)**	3.25	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.5 V **(Note 1)**	3.42	--	--	mA

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OH}	HIGH-Level Output Current **(Note 2)**	Push-Pull, 2x Drive, $V_{OH} = V_{DD}$ - 0.2 V_{DD} = 2.7 V **(Note 1)**	3.73	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.0 V **(Note 1)**	10.84	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V **(Note 1)**	16.34	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V **(Note 1)**	21.83	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 4.5 V **(Note 1)**	38.34	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 5.0 V **(Note 1)**	47.07	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 5.5 V **(Note 1)**	56.68	--	--	mA
I_{OL}	LOW-Level Output Current **(Note 2)**	Push-Pull, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.4 V **(Note 1)**	1.67	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.5 V **(Note 1)**	1.74	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.7 V **(Note 1)**	1.85	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.0 V **(Note 1)**	5.07	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.3 V **(Note 1)**	5.48	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.6 V **(Note 1)**	5.85	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 4.5 V **(Note 1)**	6.81	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 5.0 V **(Note 1)**	7.27	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 5.5 V **(Note 1)**	7.72	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.4 V **(Note 1)**	3.27	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.5 V **(Note 1)**	3.39	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.7 V **(Note 1)**	3.61	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.0 **(Note 1)**	9.85	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.3 **(Note 1)**	10.63	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.6 **(Note 1)**	11.33	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 4.5 **(Note 1)**	13.06	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 5.0 **(Note 1)**	13.79	--	--	mA

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 5.5 **(Note 1)**	14.80	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.4 V **(Note 1)**	4.07	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.5 V **(Note 1)**	4.22	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.7 V **(Note 1)**	4.49	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.0 V **(Note 1)**	12.24	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.3 V **(Note 1)**	13.20	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.6 V **(Note 1)**	14.04	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 4.5 V **(Note 1)**	16.24	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 5.0 V **(Note 1)**	17.24	--	--	mA
I_{OL}	LOW-Level Output Current **(Note 2)**	NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 5.5 V **(Note 1)**	18.24	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.4 V **(Note 1)**	7.71	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.5 V **(Note 1)**	7.97	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.7 V **(Note 1)**	8.46	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.0 V **(Note 1)**	22.96	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.3 V **(Note 1)**	24.63	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.6 V **(Note 1)**	26.10	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 4.5 V **(Note 1)**	29.82	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 5.0 V **(Note 1)**	31.42	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 5.5 V **(Note 1)**	33.25	--	--	mA
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	1.9	2.7	ms
T_{WR}	NVM Page Write Time	V_{DD} = 2.5 V to 5.5 V	--	--	20	ms
T_{ER}	NVM Page Erase Time	V_{DD} = 2.5 V to 5.5 V	--	--	20	ms
PON_{THR}	Power-On Threshold	V_{DD} Level Required to Start Up the Chip	1.63	--	2.04	V
$POFF_{THR}$	Power-Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.96	--	1.54	V

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
R_{PULL}	Pull-up or Pull-down Resistance	1 M for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD} **(Note 1)**	--	1	--	MΩ
		100 k for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD} **(Note 1)**	--	100	--	kΩ
		10 k For Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD} **(Note 1)**	--	9.3	--	kΩ
C_{IN}	Input Capacitance	PINs 10, 11	--	2.9	--	pF
		PIN 12	--	3.6	--	pF
		PINs 15, 16	--	3.8	--	pF
		PINs 17, 18, 19	--	10.2	--	pF
		PIN 20	--	27.8	--	pF
		PIN 21	--	5.7	--	pF
Note 1 No hysteresis.						
Note 2 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

3.5 I^2C PINS CHARACTERISTICS

Table 7: EC of the I^2C Pins for DI at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
V_{IL}	LOW-level Input Voltage		-0.5	$0.3xV_{DD}$	-0.5	$0.3xV_{DD}$	V
V_{IH}	HIGH-level Input Voltage		$0.7xV_{DD}$	5.5	$0.7xV_{DD}$	5.5	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		$0.05xV_{DD}$	--	$0.05xV_{DD}$	--	V
V_{OL1}	LOW-Level Output Voltage 1	(Open-Drain) at 3 mA sink current V_{DD} > 2 V	0	0.4	0	0.4	V
V_{OL2}	LOW-Level Output Voltage 2	(Open-Drain) at 2 mA sink current $V_{DD} \leq 2$ V	0	$0.2xV_{DD}$	0	$0.2xV_{DD}$	V
I_{OL}	LOW-Level Output Current **(Note 1)**	V_{OL} = 0.4 V, V_{DD} = 2.4 V	3	--	16.75	--	mA
		V_{OL} = 0.4 V, V_{DD} = 3.0 V	3	--	20	--	mA
		V_{OL} = 0.4 V, V_{DD} = 4.5 V	3	--	20	--	mA
		V_{OL}= 0.6 V	6	--	--	--	mA
t_{OF}	Output Fall Time from V_{IHmin} to V_{ILmax} **(Note 1)**		14x (V_{DD}/5.5 V)	250	10x (V_{DD}/5.5 V)	120	ns
t_{SP}	Pulse Width of Spikes that must be suppressed by the Input Filter		0	50	0	50	ns
I_i	Input Current (each IO Pin)	$0.1xV_{DD} < V_I < 0.9xV_{DDmax}$	-10	+10	-10	+10	µA
C_i	Capacitance (each IO Pin)		--	10	--	10	pF

Table 7: EC of the I²C Pins for DI at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
Note 1 Does not meet standard I²C specifications: t_{OF} = 20x(V_{DD}/5.5 V) (min); For Fast-mode Plus I_{OL} = 20 mA (min) at V_{OL} = 0.4 V. **Note 2** For Fast-mode Plus SDA pin must be configured as NMOS 2x Open-Drain, see register [1155] in Section 21.							

Table 8: EC of the I²C Pins for DILV at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Unit
			Min	Max	
V_{IL}	LOW-level Input Voltage		-0.5	0.3xV_{DD}	V
V_{IH}	HIGH-level Input Voltage		0.7xV_{DD}	5.5	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		0.05xV_{DD}	--	V
V_{OL1}	LOW-Level Output Voltage 1	(Open-Drain) at 3 mA sink current V_{DD} > 2 V	0	0.4	V
V_{OL2}	LOW-Level Output Voltage 2	(Open-Drain) at 2 mA sink current V_{DD} ≤ 2 V	0	0.2xV_{DD}	V
I_{OL}	LOW-Level Output Current **(Note 1)**	V_{OL} = 0.4 V, V_{DD} = 2.4 V	3	--	mA
		V_{OL} = 0.4 V, V_{DD} = 3.0 V	3	--	mA
		V_{OL} = 0.4 V, V_{DD} = 4.5 V	3	--	mA
		V_{OL}= 0.6 V	6	--	mA
t_{OF}	Output Fall Time from V_{IHmin} to V_{ILmax} **(Note 1)**		14x (V_{DD}/5.5 V)	250	ns
t_{SP}	Pulse Width of Spikes that must be suppressed by the Input Filter		0	50	ns
I_i	Input Current (each IO Pin)	0.1xV_{DD} < V_I < 0.9xV_{DDmax}	-10	+10	µA
C_i	Capacitance (each IO Pin)		--	10	pF
Note 1 Does not meet standard I²C specifications: t_{OF} = 20x(V_{DD}/5.5 V) (min); For Fast-mode Plus I_{OL} = 20 mA (min) at V_{OL} = 0.4 V. **Note 2** For Fast-mode Plus SDA pin must be configured as NMOS 2x Open-Drain, see register [1155] in Section 21.					

Table 9: I²C Pins Timing Characteristics at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		--	400	--	1000	kHz
t_{LOW}	SCL Clock, Low Period		1300	--	500	--	ns
t_{HIGH}	SCL Clock, High Period		600	--	260	--	ns
t_{VD_DAT}	Data Valid Time		--	900	--	450	ns
t_{VD_ACK}	Data Valid Acknowledge Time		--	900	--	450	ns
t_{BUF}	Bus Free Time between STOP and START Conditions		1300	--	500	--	ns

Table 9: I²C Pins Timing Characteristics at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
t_{HD_STA}	Hold Time for Repeated START Condition		600	--	260	--	ns
t_{SU_STA}	Set-Up Time for STOP Condition		600	--	260	--	ns
t_{HD_DAT}	Data Hold Time		0	--	0	--	ns
		Low-voltage Logic Input Mode **(Note 1)**	185	--	N/A	N/A	ns
t_{SU_DAT}	Data Set-up Time		100	--	50	--	ns
		Low-voltage Logic Input Mode **(Note 1)**	335	--	N/A	N/A	ns
t_R	SCL, SDA Rise Time		--	300	--	120	ns
t_F	SCL, SDA Fall Time		--	300	--	120	ns
t_{SU_STD}	Set-up Time for STOP Condition		600	--	260	--	ns

Note 1 Does not meet standard I²C specifications.
Note 2 Timing diagram can be found in Figure 237.

3.6 MACROCELLS CURRENT CONSUMPTION

Table 10: Typical Current Estimated for Each Macrocell at T = 25°C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I	Current	Chip Quiescent, BG disabled	0.06	0.08	0.13	µA
		Chip Quiescent, BG enabled	0.36	0.39	0.47	µA
		OSC2 25 MHz, pre-divider = 1	40.78	49.64	70.54	µA
		OSC2 25 MHz, pre-divider = 4	31.75	37.46	51.41	µA
		OSC2 25 MHz, pre-divider = 8	29.96	35.06	47.62	µA
		OSC1 2.048 MHz, pre-divider = 1	19.19	19.98	21.73	µA
		OSC1 2.048 MHz, pre-divider = 4	18.50	19.05	20.26	µA
		OSC1 2.048 MHz, pre-divider = 8	18.36	18.87	19.97	µA
		OS00 2.048 kHz, pre-divider = 1	0.33	0.36	0.44	µA
		OSC0 2.048 kHz, pre-divider = 4	0.33	0.36	0.44	µA
		OSC0 2.048 kHz, pre-divider = 8	0.33	0.36	0.44	µA
		Push-Pull 1x + 4 pF @ 2.048 kHz	0.38	0.44	0.55	µA
		Push-Pull 1x + 4 pF @ 2.048 MHz	66.8	82.6	116.0	µA
		Temperature Sensor, range 1	10.9	10.9	11.2	µA
		Temperature Sensor, range 2	11.0	11.1	11.4	µA
		One ACMPx_L (includes internal Vref)	6.1	6.2	6.4	µA
		Two ACMPx_L (includes internal Vref)	8.4	8.5	8.8	µA
		Op AmpX Quiescent Current (128 kHz bandwidth)	32.2	32.8	33.8	µA
		Op AmpX Quiescent Current (8.192 MHz bandwidth)	607	611	613	µA
		In Amp Quiescent Current (three Op Amps are ON, Rf1 = Rf2 = 50 kΩ, Rg =1 kΩ, 128 kHz bandwidth, Charge Pump - Disabled)	98	101	104	µA

Table 10: Typical Current Estimated for Each Macrocell at T = 25°C(Continued)

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
		In Amp Quiescent Current (three Op Amps are ON, Rf1 = Rf2 = 50 kΩ, Rg =1 kΩ, 128 kHz bandwidth, Charge Pump - Enabled)	75.2	77.5	80.8	µA
		In Amp Quiescent Current (three Op Amps are ON, Rf1 = Rf2 = 50 kΩ, Rg =1 kΩ, 8.192 MHz bandwidth, Charge Pump - Disabled)	1819	1834	1844	µA
		In Amp Quiescent Current (three Op Amps are ON, Rf1 = Rf2 = 50 kΩ, Rg =1 kΩ, 8.192 MHz bandwidth, Charge Pump - Enabled)	1225	1235	1245	µA
		Chopper ACMP (with 2.048 kHz clock)	31.4	33.6	38.4	µA

3.7 TIMING CHARACTERISTICS

Table 11: Typical Delay Estimated for Each Macrocell at T = 25 °C

Parameter	Description	Conditions	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Digital Input to PP 1x	26	27	18	20	13	15	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1x	27	28	19	21	15	15	ns
tpd	Delay	Digital Input to PP 2x	24	25	17	18	12	14	ns
tpd	Delay	Low Voltage Digital input to PP 1x	28	246	20	163	15	95	ns
tpd	Delay	Digital input to NMOS output	--	24	--	18	--	13	ns
tpd	Delay	Output enable from Pin, OE Hi-Z to 1	26	--	19	--	13	--	ns
tpd	Delay	Output enable from Pin, OE Hi-Z to 0	--	26	--	19	--	14	ns
tpd	Delay	Digital input to 1x3-State (Z to 1)	26	--	19	--	13	--	ns
tpd	Delay	Digital input to x3-State (Z to 0)	--	26	--	17	--	14	ns
tpd	Delay	Digital input to 2x3-State (Z to 1)	24	--	17	--	13	--	ns
tpd	Delay	Digital input to 2x3-State (Z to 0)	--	24	--	19	--	12	ns
tpd	Delay	2-bit LUT	17	17	12	12	8	8	ns
tpd	Delay	3-bit LUT	19	20	13	14	9	10	ns
tpd	Delay	4-bit LUT	20	21	15	14	9	10	ns
tpd	Delay	LATCH	25	25	17	18	12	12	ns
tpd	Delay	DFF	24	25	16	18	11	12	ns
tpd	Delay	CNT/DLY	107	107	77	74	48	70	ns
tw	Width	Edge detect	206	205	161	160	116	116	ns
tpd	Delay	Edge detect	19	20	13	13	8	8	ns
tpd	Delay	Edge detect Delayed	241	241	175	175	125	125	ns
tpd	Delay	Ripple Counter	45	60	32	44	22	31	ns

Table 11: Typical Delay Estimated for Each Macrocell at T = 25 °C(Continued)

Parameter	Description	Conditions	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	PGen	20	20	14	14	9	10	ns
tpd	Delay	Filter	177	177	121	121	77	78	ns
tpd	Delay	Inverter Filter	115	115	83	83	57	57	ns
tpd	Delay	Pipe Delay	36	37	25	26	17	18	ns

Table 12: Programmable Delay Expected Typical Delays and Widths at T = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
tw	Pulse Width, 1 cell	mode: (any) edge detect, edge detect output	223	163	118	ns
tw	Pulse Width, 2 cell	mode: (any) edge detect, edge detect output	444	324	233	ns
tw	Pulse Width, 3 cell	mode: (any) edge detect, edge detect output	663	484	347	ns
tw	Pulse Width, 4 cell	mode: (any) edge detect, edge detect output	882	643	461	ns
time1	Delay, 1 cell	mode: (any) edge detect, edge detect output	18	12	8	ns
time1	Delay, 2 cell	mode: (any) edge detect, edge detect output	18	12	8	ns
time1	Delay, 3 cell	mode: (any) edge detect, edge detect output	18	12	8	ns
time1	Delay, 4 cell	mode: (any) edge detect, edge detect output	18	12	8	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	243	176	126	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	464	337	241	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	683	497	356	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	902	655	470	ns

Table 13: Typical Filter Rejection Pulse Width at T = 25 °C

Parameter	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered Pulse Width	< 131	< 89	< 59	ns

Table 14: Typical Counter/Delay Offset Measurements at T = 25 °C

Parameter	OSC Freq	OSC Power	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Power-On time	25 MHz	auto	0.046	0.032	0.022	μs
Power-On time	2.048 MHz	auto	0.511	0.458	0.414	μs
Power-On time	2.048 kHz	auto	657	563	477	μs
frequency settling time	25 MHz	auto	0.314	0.378	0.455	μs
frequency settling time	2.048 MHz	auto	1.344	1.597	2.063	μs
frequency settling time	2.048 kHz	auto	657	1066	476	μs
variable (CLK period)	25 MHz	forced	0.039 - 0.042	0.040 - 0.041	0.038 - 0.042	μs
variable (CLK period)	2.048 MHz	forced	0.480 - 0.500	0.490 - 0.491	0.480 - 0.495	μs
variable (CLK period)	2.048 kHz	forced	477 - 500	478 - 499	478 - 498	μs
tpd (non-delayed edge)	25 MHz/ 2.048 kHz	either	35	14	10	ns

3.8 OSCILLATOR CHARACTERISTICS

Table 15: Oscillators Frequency Limits, V_{DD} = 2.4 V to 5.5 V

OSC	Temperature Range					
	+25 °C			-40 °C to +85 °C		
	Minimum Value, kHz	Maximum Value, kHz	Error, %	Minimum Value, kHz	Maximum Value, kHz	Error, %
2.048 kHz OSC0	2.029	2.065	+0.83	1.935	2.075	+1.32
			-0.93			-5.52
2.048 MHz OSC1	2023	2071	+1.12	2007	2073	+1.22
			-1.22			-2.00
25 MHz OSC2	24676	25323	+1.29	24144	25323	+1.29
			-1.30			-3.42

3.8.1 OSC Power-On Delay

Table 16: Oscillators Power-On Delay at T = 25 °C, OSC Power Setting: "Auto Power-On"

Power Supply Range (V_{DD}), V	OSC0 2.048 kHz		OSC1 2.048 MHz		OSC2 25 MHz		OSC2 25 MHz Start with Delay	
	Typical Value, μs	Maximum Value, μs	Typical Value, ns	Maximum Value, ns	Typical Value, ns	Maximum Value, ns	Typical Value, ns	Maximum Value, ns
2.50	492	559	491	500	46	53	145	153
3.30	490	525	489	501	32	37	140	148
4.00	489	509	489	509	26	31	139	146
5.00	488	495	488	530	22	26	138	146
5.50	488	499	487	532	20	24	138	145

3.9 ACMP CHARACTERISTICS

Table 17: ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Conditions	Note	Min	Typ	Max	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input		0	--	V_{DD}	V
		Negative Input		0	--	V_{DD}	V
V_{offset}	ACMP Input Offset	ACMPxL, Vhys = 0 mV, Gain = 1, Vref = 32 mV to 2048 mV	T = -40 °C to +85 °C	-6.27	--	3.67	mV
			T = 25 °C	-5.76	-0.98	3.39	mV
	Chopper ACMP Input Offset		T = -40 °C to +85 °C	-0.24	--	0.49	mV
			T = 25 °C	-0.12	0.11	0.39	mV
t_{start}	ACMP Startup Time when BG ON	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxL	T = -40 °C to +85 °C	--	51.0	99.6	μs
	ACMP Startup Time when BG OFF			--	1729	2822	μs
R_{sin}	Series Input Resistance	Gain = 1x		--	10	--	GΩ
		Gain = 0.5x		--	1.6	--	MΩ
		Gain = 0.33x		--	1.6	--	MΩ
		Gain = 0.25x		--	1.6	--	MΩ

Table 17: ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Conditions	Note	Min	Typ	Max	Unit
PROP	Propagation Delay, Response Time	ACMPxL, Vref =1.024 V, Gain = 1, Overdrive = 100 mV	Low to High	--	2.59	3.66	µs
			High to Low	--	2.80	5.21	µs
		ACMPxL, Vref = 32 mV to 2048 mV, Gain = 1, Overdrive = 100 mV	Low to High	--	2.83	5.16	µs
			High to Low	--	2.96	7.63	µs
		ACMPxL, Vref =1.024 V, Gain = 1, Overdrive = 10 mV	Low to High	--	8.18	12.57	µs
			High to Low	--	9.14	18.54	µs
		ACMPxL, Vref = 32 mV to 2048 mV, Gain = 1, Overdrive = 10 mV	Low to High	--	9.16	21.41	µs
			High to Low	--	10.01	32.37	µs
G	Gain Error	G = 1		1	1	1	
		G = 0.5		0.496	0.5	0.504	
		G = 0.33		0.331	0.330	0.336	
		G = 0.25		0.248	0.250	0.253	

3.10 INTERNAL VREF CHARACTERISTICS

Table 18: Internal Vref Characteristics at V_{DD} = 2.4 V to 5.5 V

Parameter	Description	Conditions	Note	Min	Typ	Max	Unit
Vref Accuracy and Loading	Internal Vref Accuracy at Vref > 1216 mV	No loading	T = 25 °C	-0.30	--	0.18	%
			T = -40 °C to +85 °C	-0.73	--	0.19	%
$Vref_{ACCURACY}$	Vref Divider Accuracy	Vref from (16/64) to (64/64)	T = -40 °C to +85 °C	-0.38	0.04	0.37	%
		Vref from (1/64) to (64/64)	T = -40 °C to +85 °C	-1.94	0.02	1.31	%
$Vref_{OFFSET}$	Vref Divider Offset	Vref from (16/64) to (64/64)	T = -40 °C to +85 °C	-5.58	0.83	7.84	mV
		Vref from (1/64) to (64/64)	T = -40 °C to +85 °C	-5.58	0.62	7.84	mV

3.11 OUTPUT BUFFERS CHARACTERISTICS

Table 19: HD Buffer Electrical Characteristics at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
Offset						
V_{OFFSET}	Input Offset Voltage	V_{DDA} = 5 V, V_{OUT} = 0.5 V to 4 V, T = 25 °C	--	0.25	8.0	mV
		V_{DDA} = 5 V, V_{OUT} = 0.5 V to 4 V	--	--	9.0	mV
dV_{OFFSET}/dt	Offset Drift with Temperature	$V_{OUT} = V_{DDA}/2$	--	0.75	13.5	µV/C
Output						

Table 19: HD Buffer Electrical Characteristics at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
$\Delta V_{OUT}(I)$	Load Regulation	V_{DDA} = 5 V, V_{OUT} = 2.048 V, I_{LOAD} = 0.5 mA to 2 mA, T = 25 °C	--	0.2	1.2	mV
		V_{DDA} = 5 V, V_{OUT} = 2.048 V, I_{LOAD} = 0.5 mA to 5 mA, T = 25 °C		0.4	1.9	mV
$\Delta V_{OUT}(U)$	Line Regulation	V_{DDA} = 2.5 V to 5 V, V_{OUT} = 2.048 V, T = 25 °C	--	0.9	5.0	mV
I_{SC}	Short Circuit Current	V_{DDA} = 2.4 V to 5.5 V	--	67.8	--	mA
Shutdown Characteristics						
t_{on}	Buffer Turn-On Time	R_{LOAD} = 5 kΩ, T = 25 °C,	--	--	50	μs
t_{off}	Buffer Turn-Off Time	R_{LOAD} = 5 kΩ, T = 25 °C	--	0.071	--	μs

Table 20: Vref Output Buffer at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Conditions	Note	Min	Typ	Max	Unit
$\Delta V_{OUT}(I)$	Load Regulation	V_{DDA} = 5 V, V_{OUT} = 2.048 V, I_{LOAD} = 0.5 mA to 2 mA, T = 25 °C	--	-0.99	--	1.21	mV
		V_{DDA} = 5 V, V_{OUT} = 2.048 V, I_{LOAD} = 0.5 mA to 5 mA, T = 25 °C	--	-0.99	--	1.39	mV
$\Delta V_{OUT}(U)$	Line Regulation	V_{DDA} = 2.5 V to 5 V, V_{OUT} = 2.048 V, T = 25 °C	--	-2.97	--	5.13	mV
Vref Buffer Accuracy and Loading	Vref Output Buffer Offset	Vref < 1024 mV, V_{DDA} = 2.4 V to 5.5V, No Loading	T = 25 °C	-11.2	--	10.0	mV
				-12.2	--	10.6	mV
		Vref =1024 mV to 1600 mV, V_{DDA} = 2.4 V to 5.5V, No Loading	T = 25 °C	-6.8	--	6.2	mV
				-7.3	--	6.9	mV
		Vref >1600 mV, V_{DDA} = 2.4 V to 5.5V, No Loading	T = 25 °C	-11.1	--	11.6	mV
				-12.0	--	12.9	mV
		Vref =1024 mV to 2048 mV, V_{DDA} = 3.3 V, No Loading	T = 25 °C	-6.8	--	5.8	mV
				-7.2	--	6.4	mV
	Vref0 Buffer Output Capacitance Loading		Load Resistance = 1 MΩ	--	--	5	pF
			Load Resistance = 560 kΩ	--	--	10	pF
			Load Resistance = 100 kΩ	--	--	40	pF
			Load Resistance = 10 kΩ	--	--	80	pF
			Load Resistance = 2 kΩ	--	--	120	pF
			Load Resistance = 1 kΩ, Vref = 32 mV to 1024 mV	--	--	150	pF

3.12 ANALOG TEMPERATURE SENSOR CHARACTERISTICS

Table 21: TS Output vs Temperature (Output Range 1)

T, °C	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V	
	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %
-40	991	±0.41	989	±0.38	989	±0.33
-30	968	±0.35	967	±0.32	966	±0.33
-20	945	±0.33	944	±0.31	943	±0.34
-10	922	±0.37	921	±0.35	920	±0.38
0	899	±0.39	898	±0.38	897	±0.42
10	876	±0.41	875	±0.39	874	±0.43
20	853	±0.41	852	±0.39	851	±0.44
30	830	±0.45	828	±0.44	828	±0.48
40	806	±0.52	805	±0.51	804	±0.55
50	782	±0.56	781	±0.55	780	±0.60
60	758	±0.62	756	±0.61	756	±0.65
70	733	±0.70	732	±0.69	731	±0.73
80	709	±0.77	707	±0.76	707	±0.80
85	696	±0.81	695	±0.80	694	±0.84

Table 22: TS Output vs Temperature (Output Range 2)

T, °C	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V	
	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %
-40	1195	±0.39	1194	±0.34	1193	±0.34
-30	1168	±0.37	1166	±0.35	1165	±0.36
-20	1141	±0.37	1139	±0.35	1138	±0.36
-10	1113	±0.40	1111	±0.39	1110	±0.41
0	1085	±0.43	1084	±0.42	1083	±0.44
10	1057	±0.44	1056	±0.43	1055	±0.45
20	1029	±0.45	1028	±0.44	1027	±0.45
30	1001	±0.48	999	±0.47	999	±0.50
40	972	±0.54	971	±0.53	970	±0.56
50	943	±0.58	942	±0.57	941	±0.60
60	914	±0.64	913	±0.63	912	±0.66
70	885	±0.72	883	±0.71	882	±0.74
80	855	±0.79	854	±0.77	853	±0.81
85	840	±0.83	839	±0.81	838	±0.84

3.13 PROGRAMMABLE OPERATIONAL AMPLIFIER CHARACTERISTICS

Table 23: EC of OA, V_{DDA} = 2.4 V to 5.5 V, V_{CM} = V_{DDA}/2, V_{OUT} ≈ V_{DDA}/2, R_L = 100 kΩ to V_{DDA}/2, C_L = 50 pF, T = 25 °C

Parameter	Description	Conditions (Note 1)	Min	Typ	Max	Unit
Input Voltage Offset (without Customers Trimming, Included Factory Block Offset Trim)						
V_{OFFSET}	Input Offset Voltage	BW = 128 kHz	--	69	500	µV
		BW = 128 kHz, T = -40 °C to +85 °C	--	69	930	µV
		BW = 512kHz	--	56	500	µV
		BW = 512 kHz, T = -40 °C to +85 °C	--	56	1230	µV
		BW = 2 MHz	--	47	500	µV
		BW = 2 MHz, T = -40 °C to +85 °C	--	47	1030	µV
		BW = 8 MHz	--	35	243	µV
		BW = 8 MHz, T = -40 °C to +85 °C	--	35	643	µV
dV_{OFFSET}/dt	Offset Drift with Temperature	$V_{CM} = V_{DD}/2$, T = -40 °C to +85 °C	--	0.6	13.0	µV/°C
		V_{CM} = GND, T = -40 °C to +85 °C	--	0.5	12.6	µV/°C
dV_{OFFSET}/ Time	Long-Term Offset Voltage Drift	$V_{CM} = V_{DD}/2$	0	--	985	µV
Trimmed Input Offset (Customer Perspective after Using Digital Rheostats with Gain = 200x) (Note 2)						
V_{OFFSET}	Input Offset Voltage	$V_{CM} = V_{DD}/2$	--	--	5	µV
Input Voltage Range						
V_{CMR}	Input Common-Mode Voltage Range	T = -40 °C to +85 °C	-0.2	--	V_{DD} + 0.2	V
CMRR	Common-Mode Rejection Ratio	All Op Amps, GND + 0.8 V < V_{CM} < V_{DD} - 0.8 V, T = -40 °C to +85 °C	73.5	102	--	dB
		All Op Amps, GND < V_{CM}< GND+ 0.8 V or V_{DD} - 0.8 V < V_{CM} < V_{DD}	69.7	101	--	dB
		Op Amp0 and Op Amp1, GND + 0.8 V < V_{CM} < V_{DD} - 0.8 V, T = -40 °C to +85 °C	73.5	103	--	dB
		Op Amp0 and Op Amp1, GND < V_{CM}< GND+ 0.8 V or V_{DD} - 0.8 V < V_{CM} < V_{DD}	69.7	102	--	dB
		Internal Op Amp, GND + 0.8 V < V_{CM} < V_{DD} - 0.8 V, T = -40 °C to +85 °C	77.6	100	--	dB
		Internal Op Amp, GND < V_{CM}< GND+ 0.8 V or V_{DD} - 0.8 V < V_{CM} < V_{DD}	69.7	100	--	dB
PSRR	Power Supply Rejection Ratio	$V_{CM} = V_{DD}/2$, T = -40 °C to +85 °C	80	101	--	dB
		V_{CM} = GND, T = -40 °C to +85 °C	83	102	--	dB

Table 23: EC of OA, V_{DDA} = 2.4 V to 5.5 V, V_{CM} = V_{DDA}/2, V_{OUT} ≈ V_{DDA}/2, R_L = 100 kΩ to V_{DDA}/2, C_L = 50 pF, T = 25 °C

Parameter	Description	Conditions (Note 1)	Min	Typ	Max	Unit
CS	Channel Separation	V_{DD} = 5 V, f = 10 Hz	--	119	--	dB
		V_{DD} = 5 V, f = 1 kHz	--	112	--	dB
Input Current and Impedance						
I_B	Input Bias Current		--	1.9	±9	pA
		T = -40 °C to +85 °C	--	1.9	±258	pA
I_{OFFSET}	Input Offset Current		--	--	3.2	pA
		T = +85 °C	--		210	pA
R_{CM}	Common-Mode Input Resistance		--	$3*10^{12}$	--	Ω
R_{DIFF}	Differential Input Resistance		--	10^{13}	--	Ω
C_{CM}	Input Capacitance Common-Mode		--	5	7	pF
C_{DIFF}	Input Capacitance Differential		--	1.98	2.27	pF
Open-Loop Gain						
A_{OL}	DC Open Loop Gain	R_{LOAD} = 1 MΩ, GND + 0.1 V < V_{OUT} < V_{DD} - 0.1 V, T = -40 °C to +85 °C	103.3	125	--	dB
		R_{LOAD} = 50 kΩ, GND + 0.5 V < V_{OUT} < V_{DD} - 0.5 V T = -40 °C to +85 °C	103.4	125	--	dB
Output						
V_{OH}	Maximum Voltage Swing	R_{LOAD} = 50 kΩ, T = -40 °C to +85 °C	V_{DD} - 5.73	--	--	mV
		BW = 8.192 MHz, R_{LOAD} = 600 Ω, T = -40 °C to +85 °C	V_{DD} - 135	--	--	mV
V_{OL}		R_{LOAD} = 50 kΩ, T = -40 °C to +85 °C	--	--	GND + 3.122	mV
		BW = 8.192 MHz, R_{LOAD} = 600 Ω, T = -40 °C to +85 °C	--	--	GND + 101	mV
V_{OSR}	Linear Output Swing Range	V_{OVR} from Rail R_{LOAD} = 1 MΩ	GND + 100	--	V_{DD} - 100	mV

Table 23: EC of OA, V_{DDA} = 2.4 V to 5.5 V, V_{CM} = V_{DDA}/2, V_{OUT} ≈ V_{DDA}/2, R_L = 100 kΩ to V_{DDA}/2, C_L = 50 pF, T = 25 °C

Parameter	Description	Conditions (Note 1)		Min	Typ	Max	Unit
I_{SC}	Short Circuit Current	I_{SC} to GND	BW = 128 kHz, T = -40 °C to +85 °C	--	10.8	--	mA
			BW = 512 kHz, T = -40 °C to +85 °C	--	14.4	--	mA
			BW = 2.048 MHz, T = -40 °C to +85 °C	--	22.5	--	mA
			BW = 8.192 MHz, T = -40 °C to +85 °C	--	52.0	--	mA
		I_{SC} to V_{DD}	BW = 128 kHz, T = -40 °C to +85 °C		20.6	--	mA
			BW = 512 kHz, T = -40 °C to +85 °C		27.0	--	mA
			BW = 2.048 MHz, T = -40 °C to +85 °C		41.1	--	mA
			BW = 8.192 MHz, T = -40 °C to +85 °C		92.1	--	mA
C_{LOAD}	Capacitive Load Drive			**See Section 10.3 (Small Signal Overshoot vs. Capacitive Load plots)**			
Power Supply							
V_{DD}	Supply Voltage	Guaranteed by PSRR Test		2.4	--	5.5	V
I_Q (including charge pump current consumption)	Quiescent Current per Amplifier, BW = 128 kHz	T = 25 °C, V_{DDA} = 2.5 V to 5.5 V		--	33.3	47	µA
		T = -40 °C to +85 °C, V_{DDA} = 2.5 V to 5.5 V		--	34.1	59	µA
	Quiescent Current per Amplifier, BW = 512 kHz	T = 25 °C, V_{DDA} = 2.5 V to 5.5 V		--	89.8	101	µA
		T = -40 °C to +85 °C, V_{DDA} = 2.5 V to 5.5 V		--	91.1	124	µA
	Quiescent Current per Amplifier, BW = 2.048 MHz	T = 25 °C, V_{DDA} = 2.5 V to 5.5 V		--	238.7	255	µA
		T = -40 °C to +85 °C, V_{DDA} = 2.5 V to 5.5 V		--	238.9	274	µA
	Quiescent Current per Amplifier, BW = 8.192 MHz	T = 25 °C, V_{DDA} = 2.5 V to 5.5 V		--	611.5	652	µA
		T = -40 °C to +85 °C, V_{DDA} = 2.5 V to 5.5 V		--	611.6	701	µA
I_Q (including charge pump current consumption)	Full Shutdown	T = 25 °C		--	105.8	--	nA
	Partial Shutdown **(Note 3)**, BW = 128 kHz	T = 25 °C		--	7.3	--	µA
	Partial Shutdown **(Note 3)**, BW = 8.192 MHz	T = 25 °C		--	21.3	--	µA
Frequency Response							

Table 23: EC of OA, V_{DDA} = 2.4 V to 5.5 V, V_{CM} = V_{DDA}/2, $V_{OUT} \approx V_{DDA}$/2, R_L = 100 kΩ to V_{DDA}/2, C_L = 50 pF, T = 25 °C

Parameter	Description	Conditions (Note 1)		Min	Typ	Max	Unit
GBW	Gain Bandwidth Product	R_{LOAD} = 10 kΩ, C_{LOAD} = 20 pF, G = +1 V/V, T = -40 °C to +85 °C	BW = 128 kHz	--	124	--	kHz
			BW = 512 kHz	--	542	--	kHz
			BW = 2.048 MHz	--	2569	--	kHz
			BW = 8.192 MHz	--	9594	--	kHz
PM	Phase Margin	G = +1 V/V, BW = 128 kHz → 8.192 MHz; R_{LOAD} = 10 kΩ, C_{LOAD} = 20 pF, T = -40 °C to +85 °C		43	71	--	degree
SR	Slew Rate	R_{LOAD} = 50 kΩ, C_{LOAD} = 85 pF	BW = 128 kHz, T = -40 °C to +85 °C	--	0.09	--	V/µs
			BW = 512 kHz, T = -40 °C to +85 °C	--	0.38	--	V/µs
			BW = 2.048 MHz, T = -40 °C to +85 °C	--	1.85	--	V/µs
			BW = 8.192 MHz, T = -40 °C to +85 °C	--	6.48	--	V/µs
t_{OR}	Overload Recovery Time	T = -40 °C to +85 °C R_{LOAD} = 50 kΩ		--	12.68	--	µs
Noise							
THD	Total Harmonic Distortion	AV = 1, R_{LOAD} = 50 kΩ, $V_{OUT(PP)}$ = V_{DD}/2	f = 1 kHz, BW = 128 kHz	--	0.171	--	%
			f = 1 kHz, BW = 512 kHz	--	0.073	--	%
			f = 1 kHz, BW = 2.048 MHz	--	0.033	--	%
			f = 1 kHz, BW = 8.192 MHz	--	0.02	--	%
e_n	Input Voltage Noise	f = 0.1 to 10 Hz		--	24.78	--	µVpp
Vn	Input Voltage Noise Density	f = 1 kHz	BW = 128 kHz	--	92	--	nV/√Hz
			BW = 512 kHz	--	86	--	
			BW = 2.048 MHz	--	74	--	
			BW = 8.192 MHz	--	51	--	
In	Input Current Noise Density	f = 1 kHz		--	1	--	fA/√Hz
Shutdown Characteristics							
t_{on}	Amplifier Turn-On Time	BW = 8.192 MHz, T = -40 °C to +85 °C	V_{CM} = V_{DDA}/2, R_L = 50 kΩ	--	2.143	6.095	µs
			V_{DDA} > V_{CM} > (V_{DDA} - 1.3)	--	2.166	6.070	µs
		BW = 128 kHz, T = -40 °C to +85 °C	V_{CM} = V_{DDA}/2, R_L = 50 kΩ	--	25.177	43.158	µs
			V_{DDA} > V_{CM} > (V_{DDA} - 1.3)	--	34.769	70.602	µs
t_{off}	Amplifier Turn-Off Time	--		--	0.653	1.015	µs

Table 23: EC of OA, V_{DDA} = 2.4 V to 5.5 V, V_{CM} = V_{DDA}/2, V_{OUT} ≈ V_{DDA}/2, R_L = 100 kΩ to V_{DDA}/2, C_L = 50 pF, T = 25 °C

Parameter	Description	Conditions (Note 1)		Min	Typ	Max	Unit
Comparator Mode							
t_{PHL}	Propagation Delay Output High to Low	Vref = 2.048 mV, Overdrive = 100 mV, Charge Pump is always On	BW = 128 kHz	--	23.6	39.4	µs
			BW = 512 kHz	--	10.8	17.9	µs
			BW = 2.048 MHz	--	6.8	11.5	µs
			BW = 8.192 MHz	--	5.6	10.0	µs
t_{PLH}	Propagation Delay Output Low to High		BW = 128 kHz	--	24.6	40.1	µs
			BW = 512 kHz	--	10.6	17.2	µs
			BW = 2.048 MHz	--	6.5	10.8	µs
			BW = 8.192 MHz	--	5.4	9.0	µs

Note 1 AGND = GND, unless otherwise noted
Note 2 Equivalent offset voltage of the amplifier after user's trim using digital rheostat. Gain of the amplifier is G=200 and the zero output voltage level V_{zero} = V_{DD}/2 (See Section 10.2.1)
Note 3 Op amps analog supporting blocks are always turned on.

3.14 100K DIGITAL RHEOSTAT CHARACTERISTICS

Table 24: 100K Digital Rheostat EC at V_A=V_{DD}, V_B=GND, T=-40°C to +85°C, V_{DD}=2.4V to 5.5V Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DR}	Rheostat Pin Voltage Range	Voltage between any (A or B) pins and AGND	AGND	--	V_{DDA}	V
R_{DR}	Digital Rheostat Resistance	Full resistance with all switches open (Note 1)	94.426	101.582	113.741	kΩ
R_{DR_MIN}	Minimal Rheostat Resistance	Code = 0x00	43.679	--	84.779	Ω
R_{MATCH}	Mismatch between rheostats	Code = 0x3FF, T = 25 °C	--	0.084	--	%
Number of taps					1024	
$BWDT_{DR}$	Digital Rheostat Bandwidth	Frequency applied on one side of resistor chain and -3 dB frequency measured at the other side with full 100 KΩ, assume no additional load	--	50	--	kHz
R_S	Step Resistance	V_{DD} = (2.4 V; 3.3 V; 5.5 V) V_{DDA} = (1 V; -1 V) T= (-40 °C; 25 °C; 85 °C)	--	99.236	--	Ω
I_{DR_MAX}	Max current through Rheostat	T = 25 °C+	--	--	2	mA
E_{SW_N}	Resistor Noise Voltage	R_{AB} = 25 kΩ, f = 1 kHz	--	30	--	nV/√Hz
f_{ChACMP}	Chopper Comparator Switching Frequency		--	--	30	kHz
V_{Ch_offset}	Chopper comparator offset when Auto-Trim process is active		--	100	300	µV
f_{DR_CLK}	Counter Frequency independent from the Rheostat	The counter frequency is determined by user selection	0	--	25	MHz

Table 24: 100K Digital Rheostat EC at V_A=V_{DD}, V_B=GND, T=-40°C to +85°C, V_{DD}=2.4V to 5.5V Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{DR_SWCH}	Rheostat Switch Speed **(Note 2)**	V_A = 5 V, V_B = 0 V, ±1 LSB error band, Auto-Trim or Fast mode	--	--	100	kHz
		V_A = 5 V, V_B = 0 V, ±1 LSB error band, regular mode	--	--	1	kHz
T_{settle}	Settling Time	Fast mode, I^2C code change from 0 to 1023	--	--	50	µs
		Fast mode, Rheostat 1 bit code change	--	--	10	µs
C_{DR}	Maximum Capacitance of A, B pins Measured to AGND	All switches are ON, f = 200 kHz	--	33.152	--	pF
I_{LKG}	Leakage Current	Including active charge pump current consumption	--	--	1000	nA
Error ZScale	Zero-Scale Error	Code = 0x00	--	--	0.776	LSB
INL	Integral Non-linearity		--	--	±2	LSB
DNL	Differential Non-linearity		--	--	±1	LSB
$BWDT_{CAP}$	Bandwidth -3 dB (Load = 30 pF)	$R_{RHEOSTAT}$ < 12.5 kΩ	--	240	--	kHz
		$R_{RHEOSTAT}$ = 12.5 kΩ to 25 kΩ	--	120	--	kHz
		$R_{RHEOSTAT}$ = 25 kΩ to 50 kΩ	--	60	--	kHz
		$R_{RHEOSTAT}$ = 50 kΩ to 100 kΩ	--	30	--	kHz
αR(T)	Resistance Temperature Coefficient	V_{AB} = const,	-119.69	0	163.84	ppm/°C

Note 1 User can calculate actual Digital Rheostat value using calibration data from NVM (see Section 12.2).
Note 2 Includes internal timing. External circuit should be counted separately.

3.15 ANALOG SWITCHES CHARACTERISTICS

Table 25: Analog Switch0/Voltage Regulator EC at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{AS}	Maximum Voltage At Pins	Voltage between any Analog Switch pin to AGND	0	--	V_{DD} + 0.3	V
f_{MAX}	Maximum Switching Frequency	Pull Up	2.5	--	--	MHz
		Pull Up, V_{DD} = 2.4 V	3.9	--	--	MHz
		Pull Down	363	--	--	kHz
		Pull Down, V_{DD} = 2.4 V	363	--	--	kHz
R_{ON}	ON Resistance	V_{DD} = 3.3 V, V_{IN} < 1.2 V, N-ch FET, T = 25 °C	--	30	53	Ω
		V_{DD} = 3.3 V, V_{IN} > V_{DD} - 1.2, P-ch FET, T = 25 °C	--	2	3	Ω
I_{PWROFF}	OFF Leakage Current	Switch OFF; from IN to OUT V_A = V_{DD} or V_B = V_{DD}	--	--	17	nA

Table 25: Analog Switch0/Voltage Regulator EC at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{SW_MAX}	Maximum ON-state Switch Current	$V_A = V_{DD}$, load connected to ground, V_{AB}= 0.4 V	--	--	300	mA
I_{SW_PULSE}	Maximum Pulse Current Through Switch	Pulse duration = 1 ms, Duty cycle < 5 %	--	--	500	mA

Table 26: Analog Switch1/Current Sink EC at T = -40 °C to +85 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{AS}	Maximum Voltage At Pins	Voltage between any Analog Switch pin to AGND	0	--	V_{DD} + 0.3	V
f_{MAX}	Maximum Switching Frequency	Pull Up	1.6	--	--	MHz
		Pull Up, V_{DD} = 2.4 V	1.6	--	--	MHz
		Pull Down	5	--	--	MHz
		Pull Down, V_{DD} = 2.4 V	5	--	--	MHz
R_{ON}	ON Resistance	V_{DD} = 3.3 V, V_{IN} < 1.2 V, N-ch FET, T = 25 °C	--	0.8	1.5	Ω
		V_{DD} = 3.3 V, $V_{IN} > V_{DD}$ - 1.2, P-ch FET, T = 25 °C	--	53.4	204	Ω
I_{PWROFF}	OFF Leakage Current	Switch OFF; from IN to OUT, $V_A = V_{DD}$ or $V_B = V_{DD}$	--	--	34	nA
I_{SW_MAX}	Maximum ON-state Switch Current	$V_A = V_{DD}$, load connected to ground, V_{AB}= 0.4 V	--	--	300	mA
I_{SW_PULSE}	Maximum Pulse Current Through Switch	Pulse duration = 1 ms, Duty cycle < 5 %	--	--	500	mA

4 User Programmability

The SLG47004 is a user programmable device with Multiple-Time-Programmable (MTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.aap file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

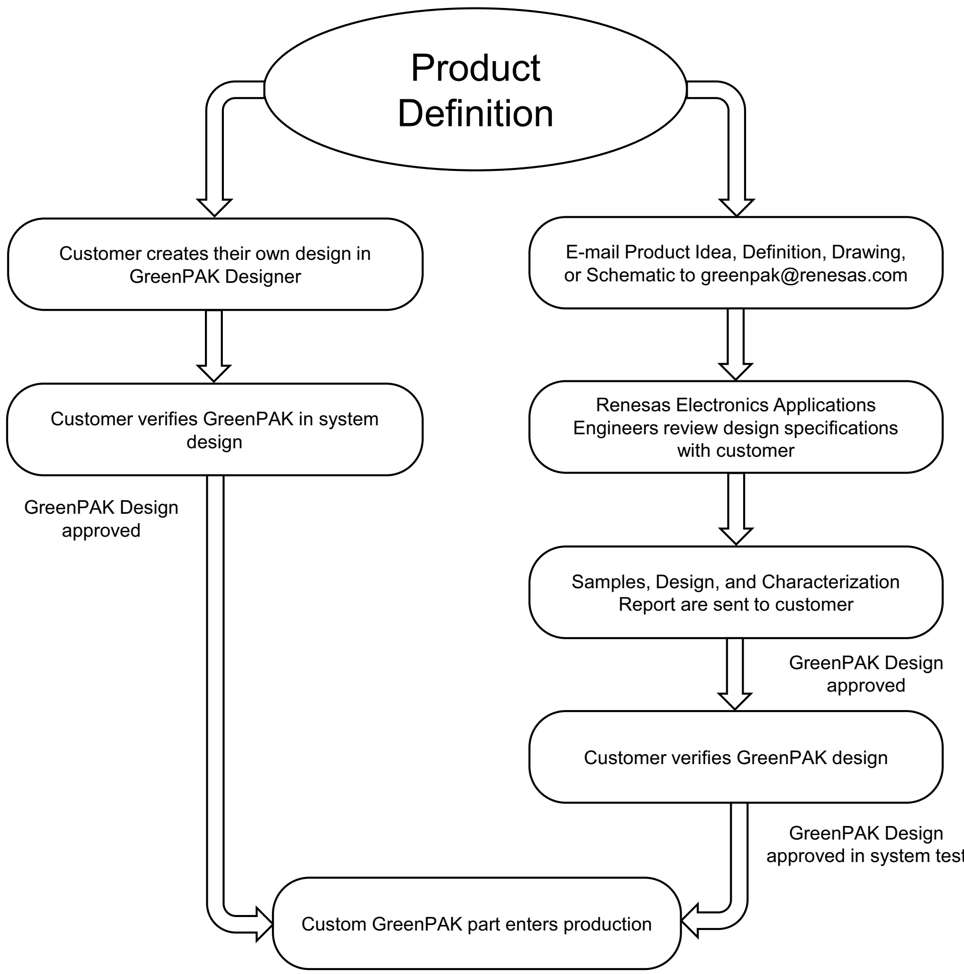


Figure 2: Steps to Create a Custom GreenPAK Device

5 IO Pins

The SLG47004 has a total of 7 GPIO Pins which can function as either a user-defined Input or Output, as well as serve as a special function (such as outputting the voltage reference) and 1 GPI Pin.

5.1 GPIO PINS

IO0, IO1, IO2, IO3, IO4, IO5, and IO6 serve as General Purpose IO Pins.

5.2 GPI PINS

I0 serves as General Purpose Input Pin. It is strongly recommended to connect I0 (Pin21) to the ground if it is not used in the project.

5.3 PULL-UP/DOWN RESISTORS

All IO Pins have the option of user-selectable resistors that can be connected to the pin structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. The internal resistors can be configured as either Pull-up or Pull-downs.

5.4 FAST PULL-UP/DOWN DURING POWER-UP

During power-up, IO Pull-up/down resistance will switch to 2.6 kΩ initially and then it will switch to normal setting value. This function is enabled by register [1207].

5.5 I²C MODE IO STRUCTURE

5.5.1 I²C Mode Structure (for SCL and SDA)

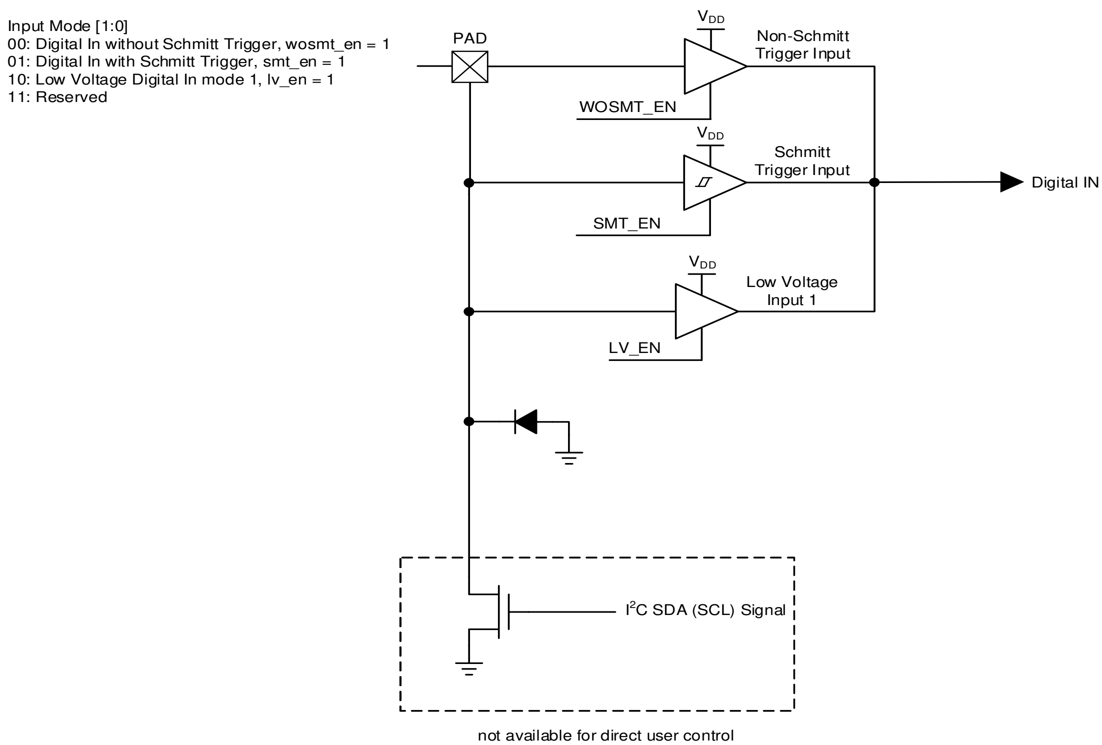


Figure 3: IO with I²C Mode IO Structure Diagram

5.6 MATRIX OE IO STRUCTURE

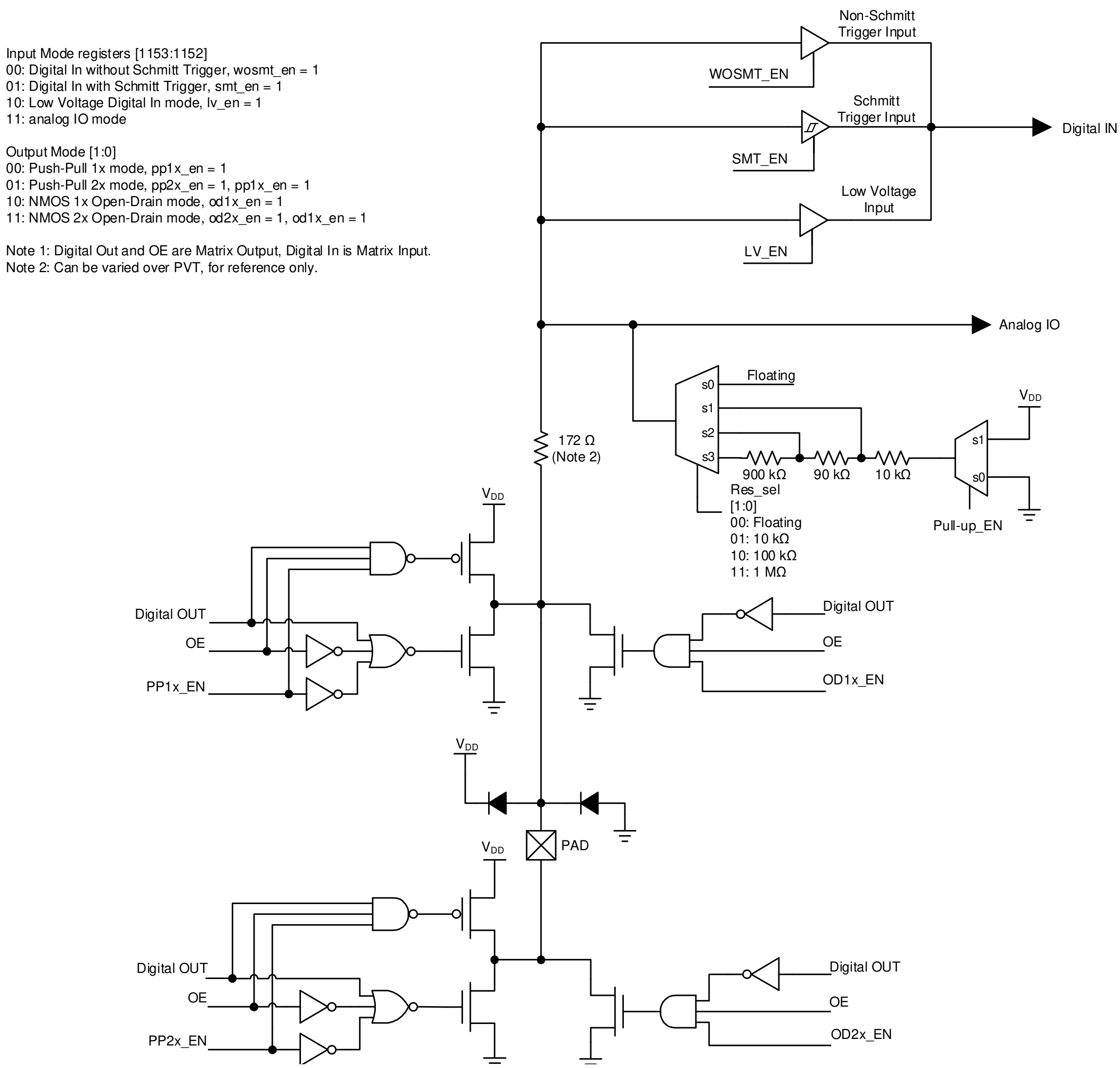


Figure 4: Matrix OE IO Structure Diagram

5.7 GPI STRUCTURE

5.7.1 GPI Structure (for I0)

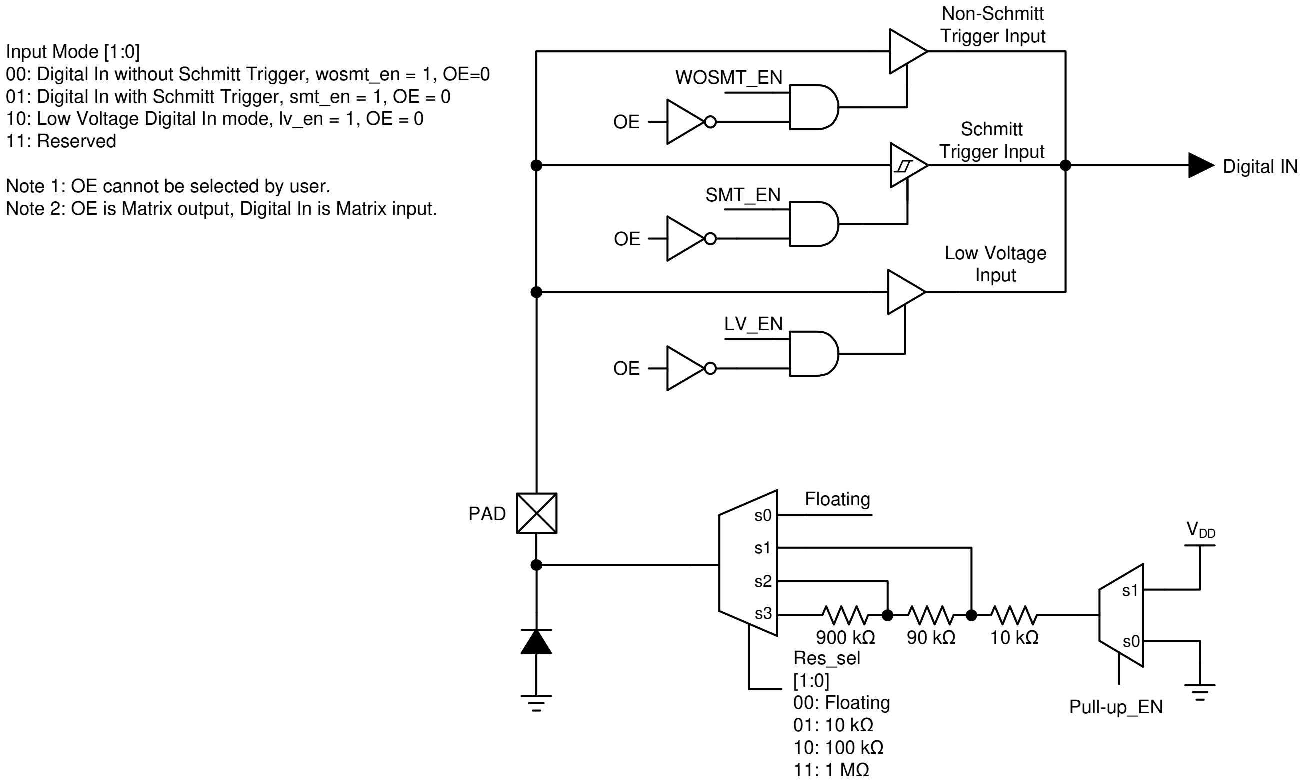


Figure 5: IO0 GPI Structure Diagram

5.8 IO PINS TYPICAL PERFORMANCE

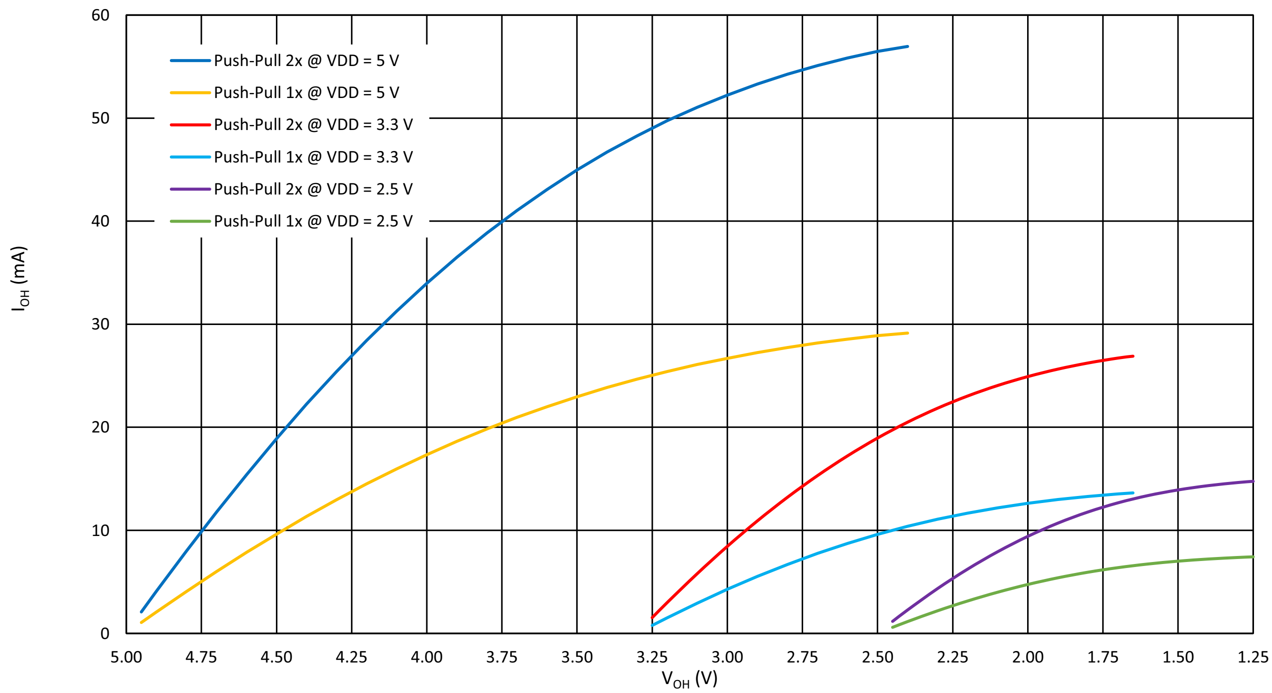


Figure 6: Typical High Level Output Current vs. High Level Output Voltage at T = 25 °C

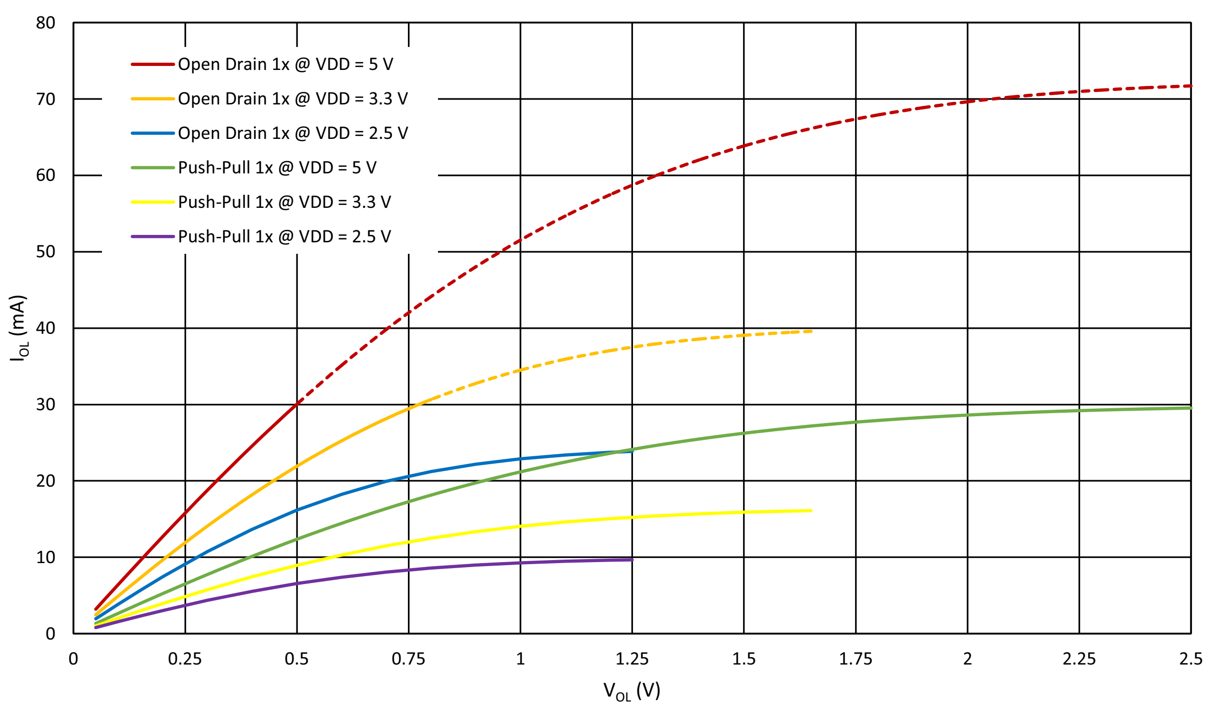


Figure 7: Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T = 25 °C, Full Range

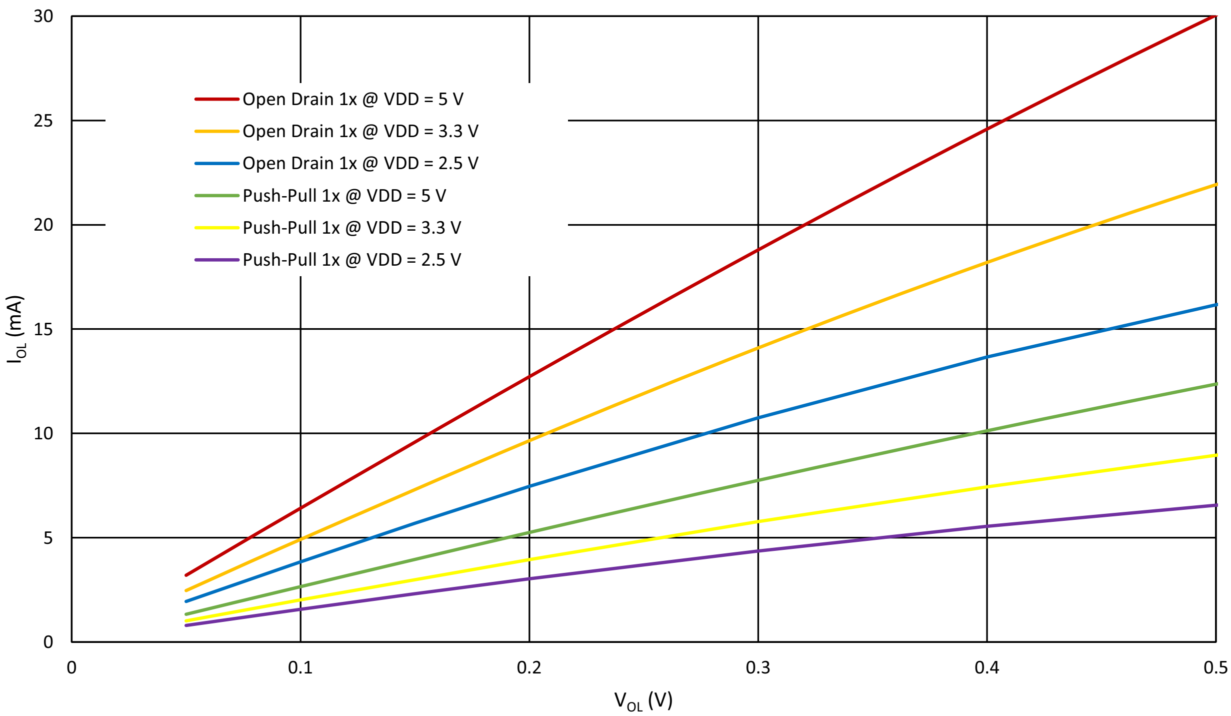


Figure 8: Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T = 25 °C

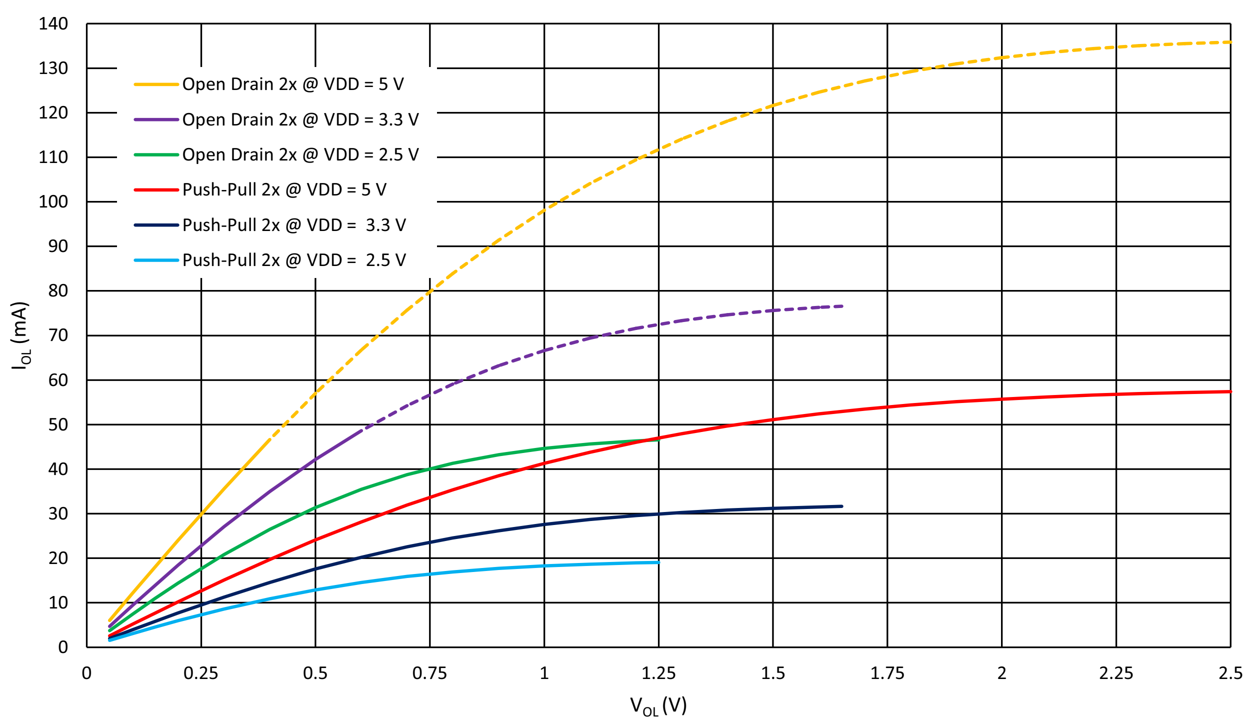


Figure 9: Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T = 25 °C, Full Range

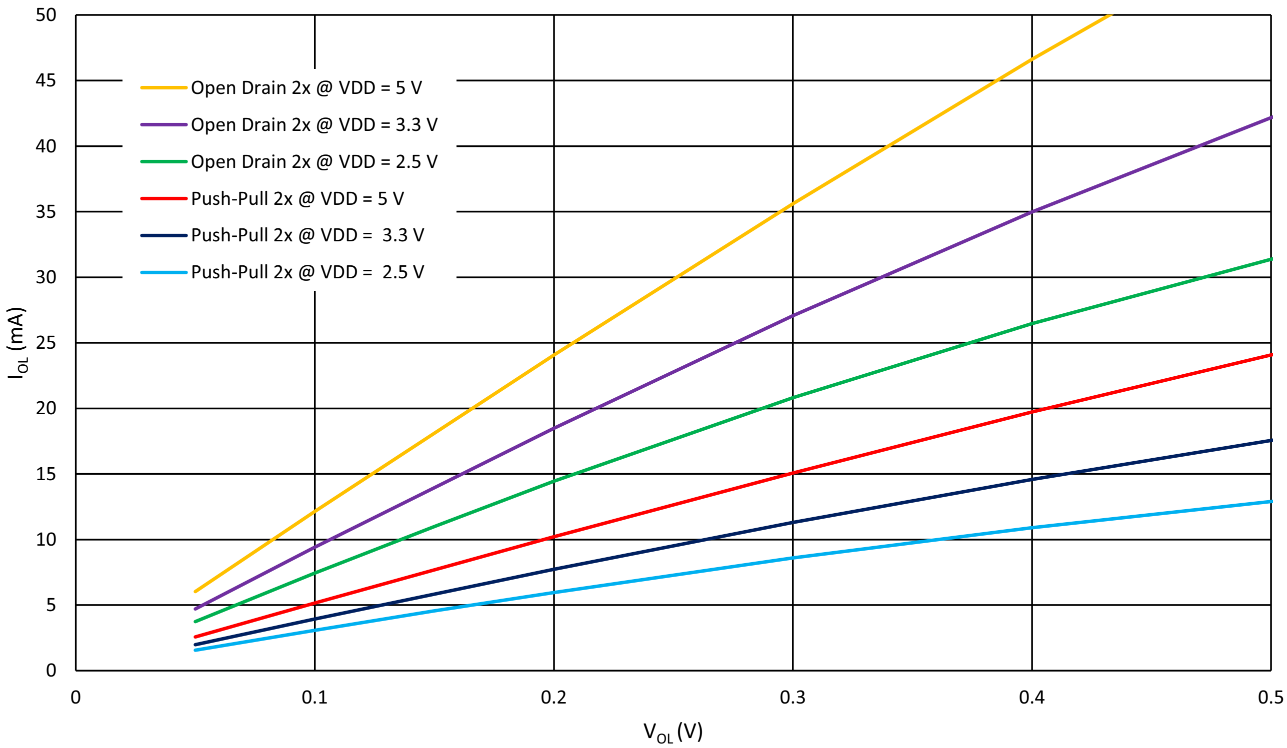


Figure 10: Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T = 25 °C

6 Connection Matrix

The Connection Matrix in the SLG47004 is used to create an internal routing for internal functional macrocells of the device once it is programmed. The output of each functional macrocell within the SLG47004 has a specific digital bit code assigned to it, that is either set to active "High" or inactive "Low", based on the design that is created. Once the 2048 register bits within the SLG47004 are programmed, a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 99 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IOs, LUTs, analog comparators, other digital resources, such as V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG47004's register table, see Section 21.

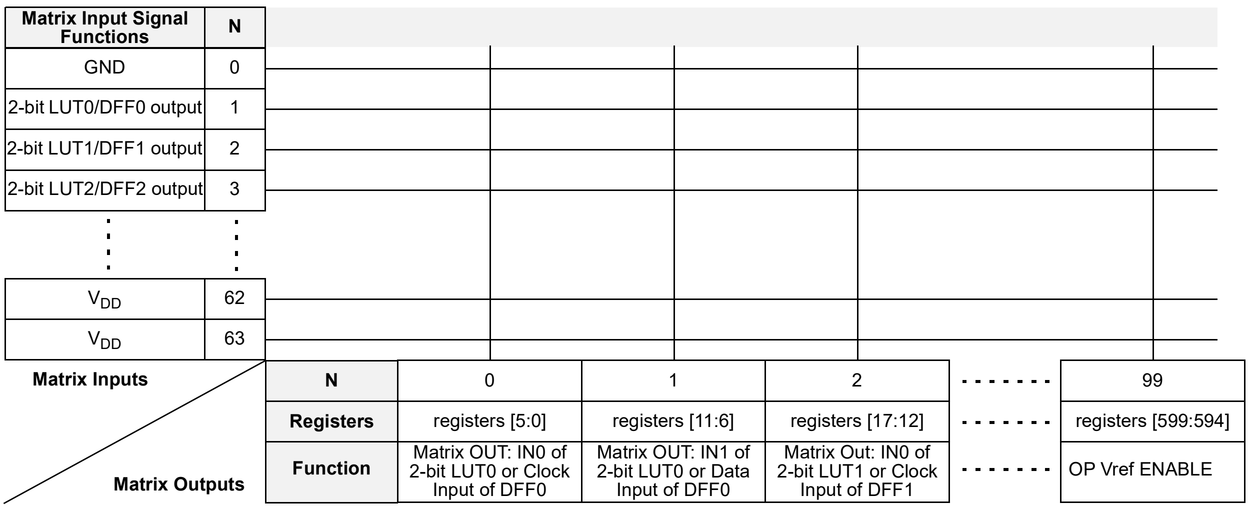


Figure 11: Connection Matrix

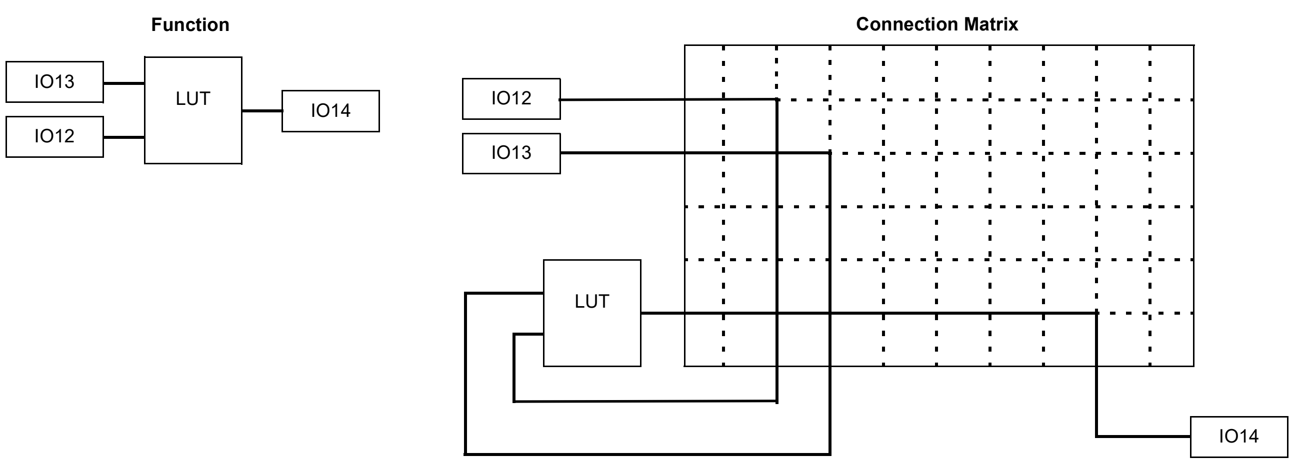


Figure 12: Connection Matrix Example

6.1 MATRIX INPUT TABLE

Table 27: Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	2-bit LUT0/DFF0 output	0	0	0	0	0	1
2	2-bit LUT1/DFF1 output	0	0	0	0	1	0
3	2-bit LUT2/DFF2 output	0	0	0	0	1	1
4	2-bit LUT3/PGen output	0	0	0	1	0	0
5	3-bit LUT0/DFF3 output	0	0	0	1	0	1
6	3-bit LUT1/DFF4 output	0	0	0	1	1	0
7	3-bit LUT2/DFF5 output	0	0	0	1	1	1
8	3-bit LUT3/DFF6 output	0	0	1	0	0	0
9	3-bit LUT4/DFF7 output	0	0	1	0	0	1
10	3-bit LUT5/DFF8 output	0	0	1	0	1	0
11	3-bit LUT6/DFF9 output	0	0	1	0	1	1
12	CNT_DLY0 output	0	0	1	1	0	0
13	MLT0 4-bit LUT1/DFF17_OUT	0	0	1	1	0	1
14	CNT_DLY1 output	0	0	1	1	1	0
15	MLT1 3-bit LUT7/DFF11_OUT	0	0	1	1	1	1
16	CNT_DLY2 output	0	1	0	0	0	0
17	MLT2 3-bit LUT8/DFF12_OUT	0	1	0	0	0	1
18	CNT_DLY3 output	0	1	0	0	1	0
19	MLT3 3-bit LUT9/DFF13_OUT	0	1	0	0	1	1
20	CNT_DLY4 output	0	1	0	1	0	0
21	MLT4 3-bit LUT10/DFF14_OUT	0	1	0	1	0	1
22	CNT_DLY5 output	0	1	0	1	1	0
23	MLT5 3-bit LUT11/DFF15_OUT	0	1	0	1	1	1
24	CNT_DLY6 output	0	1	1	0	0	0
25	MLT6 3-bit LUT12/DFF16_OUT	0	1	1	0	0	1
26	3-bit LUT13/Pipe Delay/RippleCNT_out0	0	1	1	0	1	0
27	Pipe Delay/RippleCNT_out1	0	1	1	0	1	1
28	Pipe Delay/RippleCNT_out2	0	1	1	1	0	0
29	4-bit LUT0/DFF10 output	0	1	1	1	0	1
30	Programmable Delay Edge Detect Output	0	1	1	1	1	0
31	Edge Detect Filter Output	0	1	1	1	1	1
32	I^2C_virtual_0 Input	1	0	0	0	0	0
33	I^2C_virtual_1 Input	1	0	0	0	0	1
34	I^2C_virtual_2 Input	1	0	0	0	1	0
35	I^2C_virtual_3 Input	1	0	0	0	1	1
36	I^2C_virtual_4 Input	1	0	0	1	0	0
37	I^2C_virtual_5 Input	1	0	0	1	0	1

Table 27: Matrix Input Table(Continued)

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
38	I^2C_virtual_6 Input	1	0	0	1	1	0
39	I^2C_virtual_7 Input	1	0	0	1	1	1
40	RH0 Idle/Active	1	0	1	0	0	0
41	RH1 Idle/Active	1	0	1	0	0	1
42	Output of Op Amp0 in ACMP mode	1	0	1	0	1	0
43	Output of Op Amp1 in ACMP mode	1	0	1	0	1	1
44	IO0 Digital Input	1	0	1	1	0	0
45	IO1 Digital Input	1	0	1	1	0	1
46	IO2 Digital Input	1	0	1	1	1	0
47	IO3 Digital Input	1	0	1	1	1	1
48	IO4 Digital Input	1	1	0	0	0	0
49	IO5 Digital Input	1	1	0	0	0	1
50	IO6 Digital Input	1	1	0	0	1	0
51	I0 Digital Input	1	1	0	0	1	1
52	Oscillator0 output 0	1	1	0	1	0	0
53	Oscillator1 output 0	1	1	0	1	0	1
54	Oscillator2 output	1	1	0	1	1	0
55	Chopper ACMP Out	1	1	0	1	1	1
56	ACMP0 Output (low speed)	1	1	1	0	0	0
57	ACMP1 Output (low speed)	1	1	1	0	0	1
58	Oscillator0 output 1	1	1	1	0	1	0
59	Oscillator1 output 1	1	1	1	0	1	1
60	POR OUT	1	1	1	1	0	0
61	V_{DD}	1	1	1	1	0	1
62	V_{DD}	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

6.2 MATRIX OUTPUT TABLE

Table 28: Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[5:0]	IN0 of 2-bit LUT0 or Clock Input of DFF0	0
[11:6]	IN1 of 2-bit LUT0 or Data Input of DFF0	1
[17:12]	IN0 of 2-bit LUT1 or Clock Input of DFF1	2
[23:18]	IN1 of 2-bit LUT1 or Data Input of DFF1	3
[29:24]	IN0 of 2-bit LUT2 or Clock Input of DFF2	4
[35:30]	IN1 of 2-bit LUT2 or Data Input of DFF2	5
[41:36]	IN0 of 2-bit LUT3 or Clock Input of PGen	6
[47:42]	IN1 of 2-bit LUT3 or nRST of PGen	7
[53:48]	IN0 of 3-bit LUT0 or CLK Input of DFF3	8

Table 28: Matrix Output Table(Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[59:54]	IN1 of 3-bit LUT0 or Data of DFF3	9
[65:60]	IN2 of 3-bit LUT0 or nRST (nSET) of DFF3	10
[71:66]	IN0 of 3-bit LUT1 or CLK Input of DFF4	11
[77:72]	IN1 of 3-bit LUT1 or Data of DFF4	12
[83:78]	IN2 of 3-bit LUT1 or nRST (nSET) of DFF4	13
[89:84]	IN0 of 3-bit LUT2 or CLK Input of DFF5	14
[95:90]	IN1 of 3-bit LUT2 or Data of DFF5	15
[101:96]	IN2 of 3-bit LUT2 or nRST(nSET) of DFF5	16
[107:102]	IN0 of 3-bit LUT3 or CLK Input of DFF6	17
[113:108]	IN1 of 3-bit LUT3 or Data of DFF6	18
[119:114]	IN2 of 3-bit LUT3 or nRST (nSET) of DFF6	19
[125:120]	IN0 of 3-bit LUT4 or CLK Input of DFF7	20
[131:126]	IN1 of 3-bit LUT4 or Data of DFF7	21
[137:132]	IN2 of 3-bit LUT4 or nRST (nSET) of DFF7	22
[143:138]	IN0 of 3-bit LUT5 or CLK Input of DFF8	23
[149:144]	IN1 of 3-bit LUT5 or Data of DFF8	24
[155:150]	IN2 of 3-bit LUT5 or nRST (nSET) of DFF8	25
[161:156]	IN0 of 3-bit LUT6 or CLK Input of DFF9	26
[167:162]	IN1 of 3-bit LUT6 or CLK Input of DFF9	27
[173:168]	IN2 of 3-bit LUT6 or nRST (nSET) of DFF9	28
[179:174]	IN0 of 3-bit LUT7 or CLK Input of DFF11 Delay1 Input (or Counter1 nRST Input)	29
[185:180]	IN1 of 3-bit LUT7 or nRST (nSET) of DFF11 Delay1 Input (or Counter1 nRST Input)	30
[191:186]	IN2 of 3-bit LUT7 or Data of DFF11 Delay1 Input (or Counter1 nRST Input)	31
[197:192]	IN0 of 3-bit LUT8 or CLK Input of DFF12 Delay2 Input (or Counter2 nRST Input)	32
[203:198]	IN1 of 3-bit LUT8 or nRST (nSET) of DFF12 Delay2 Input (or Counter2 nRST Input)	33
[209:204]	IN2 of 3-bit LUT8 or Data of DFF12 Delay2 Input (or Counter2 nRST Input)	34
[215:210]	IN0 of 3-bit LUT9 or CLK Input of DFF13 Delay3 Input (or Counter3 nRST Input)	35
[221:216]	IN1 of 3-bit LUT9 or nRST (nSET) of DFF13 Delay3 Input (or Counter3 nRST Input)	36
[227:222]	IN2 of 3-bit LUT9 or Data of DFF13 Delay3 Input (or Counter3 nRST Input)	37
[233:228]	IN0 of 3-bit LUT10 or CLK Input of DFF14 Delay4 Input (or Counter4 nRST Input)	38
[239:234]	IN1 of 3-bit LUT10 or nRST (nSET) of DFF14 Delay4 Input (or Counter4 nRST Input)	39

Table 28: Matrix Output Table(Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[245:240]	IN2 of 3-bit LUT10 or Data of DFF14 Delay4 Input (or Counter4 nRST Input)	40
[251:246]	IN0 of 3-bit LUT11 or CLK Input of DFF15 Delay5 Input (or Counter5 nRST Input)	41
[257:252]	IN1 of 3-bit LUT11 or nRST (nSET) of DFF15 Delay5 Input (or Counter5 nRST Input)	42
[263:258]	IN2 of 3-bit LUT11 or nRST (nSET) of DFF15 Delay5 Input (or Counter5 nRST Input)	43
[269:264]	IN0 of 3-bit LUT12 or CLK Input of DFF16 Delay6 Input (or Counter6 nRST Input)	44
[275:270]	IN1 of 3-bit LUT12 or nRST (nSET) of DFF16 Delay6 Input (or Counter6 nRST Input)	45
[281:276]	IN2 of 3-bit LUT12 or Data of DFF16 Delay6 Input (or Counter6 nRST Input)	46
[287:282]	IN0 of 3-bit LUT13 or Input of Pipe Delay or UP signal of RIPP CNT	47
[293:288]	IN1 of 3-bit LUT13 or nRST of Pipe Delay or nSet of RIPP CNT	48
[299:294]	IN2 of 3-bit LUT13 or CLK of Pipe Delay_RIPP CNT	49
[305:300]	IN0 of 4-bit LUT0 or CLK of DFF10	50
[311:306]	IN1 of 4-bit LUT0 or Data of DFF10	51
[317:312]	IN2 of 4-bit LUT0 or nRST (nSET) of DFF10	52
[323:318]	IN3 of 4-bit LUT0	53
[329:324]	IN0 of 4-bit LUT1 or CLK Input of DFF17 Delay0 Input (or Counter0 nRST Input)	54
[335:330]	IN1 of 4-bit LUT1 or nRST of DFF17 Delay0 Input (or Counter0 nRST Input) Delay/Counter0 External CLK source	55
[341:336]	IN2 of 4-bit LUT1 or nSet of DFF17 Delay0 Input (or Counter0 nRST Input) Delay/Counter0 External CLK source KEEP Input of FSM0	56
[347:342]	IN3 of 4-bit LUT1 or Data of DFF17 Delay0 Input (or Counter0 nRST Input) UP Input of FSM0	57
[353:348]	Programmable delay/edge detect input	58
[359:354]	Filter/Edge detect input	59
[365:360]	IO0 DOUT	60
[371:366]	IO0 DOUT OE	61
[377:372]	IO1 DOUT	62
[383:378]	IO1 DOUT OE	63
[389:384]	IO2 DOUT	64
[395:390]	IO2 DOUT OE	65
[401:396]	IO3 DOUT	66
[407:402]	IO3 DOUT OE	67
[413:408]	IO4 DOUT	68

Table 28: Matrix Output Table(Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[419:414]	IO4 DOUT OE	69
[425:420]	IO5 DOUT	70
[431:426]	IO5 DOUT OE	71
[437:432]	IO6 DOUT	72
[443:438]	IO6 DOUT OE	73
[449:444]	Set of PT0 block	74
[455:450]	Clock of PT0 block	75
[461:456]	Reload of PT0 block	76
[467:462]	Program of PT0 block	77
[473:468]	Up/Down of PT0 block	78
[479:474]	Set of PT1 block	79
[485:480]	Clock of PT1 block	80
[491:486]	Reload of PT1 block	81
[497:492]	Program of PT1 block	82
[503:498]	Up/Down of PT1 block	83
[509:504]	FIFO Reset of PT blocks	84
[515:510]	Power Up of Chopper ACMP	85
[521:516]	Rheostats Charge Pump Enable	86
[527:522]	ASW0 enable/Half bridge Enable	87
[533:528]	ASW1 enable/Half bridge data	88
[539:534]	ACMP0 Power Up	89
[545:540]	ACMP1 Power Up	90
[551:546]	Oscillator0 Enable	91
[557:552]	Oscillator1 Enable	92
[563:558]	Oscillator2 Enable	93
[569:564]	VrefO, Temp sensor, VrefO Power Up	94
[575:570]	HDBUF Enable	95
[581:576]	Op Amp0 Power Up	96
[587:582]	Op Amp1 Power Up	97
[593:588]	Op Amp2 Power Up	98
[599:594]	Op amps Vref Enable	99
Note 1 For each Address, the two most significant bits are unused.		

6.3 CONNECTION MATRIX VIRTUAL INPUTS

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at 0x7C (124).

An I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

See Table 29.

Table 29: Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
32	I^2C_virtual_0 Input	[992]
33	I^2C_virtual_1 Input	[993]
34	I^2C_virtual_2 Input	[994]
35	I^2C_virtual_3 Input	[995]
36	I^2C_virtual_4 Input	[996]
37	I^2C_virtual_5 Input	[997]
38	I^2C_virtual_6 Input	[998]
39	I^2C_virtual_7 Input	[999]

6.4 CONNECTION MATRIX VIRTUAL OUTPUTS

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via I^2C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I^2C addresses for reading these register values are bytes 0xC4 (196) to 0xCA (202). Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at byte 0x7C (124)).

7 Combination Function Macrocells

The SLG47004 has 13 combination function macrocells that can serve as more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells:

- Three macrocells that can serve as either 2-bit LUT or as D Flip-Flop
- Seven macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay/Ripple Counter
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGen)
- One macrocell that can serve as either 4-bit LUT or as D Flip-Flop with Set/Reset Input

Inputs/Outputs for the 13 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of configuration bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user-defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

7.1 2-BIT LUT OR D FLIP-FLOP MACROCELLS

There is one macrocell that can serve as either 2-bit LUT or as D Flip-Flop. When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.

LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

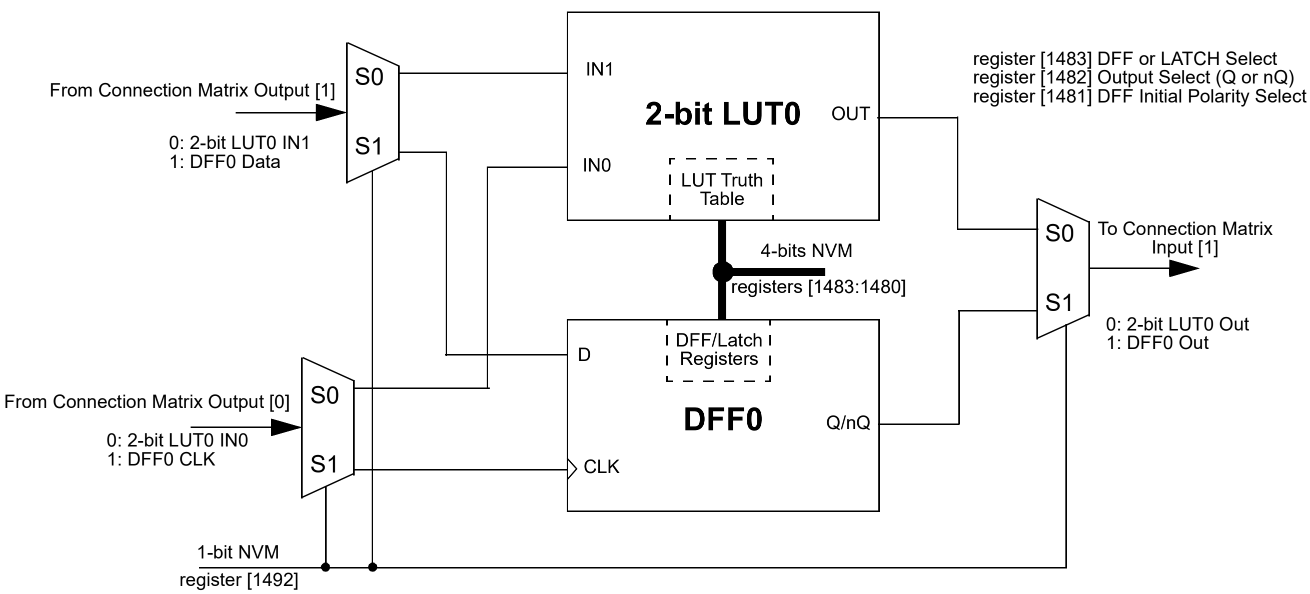


Figure 13: 2-bit LUT0 or DFF0

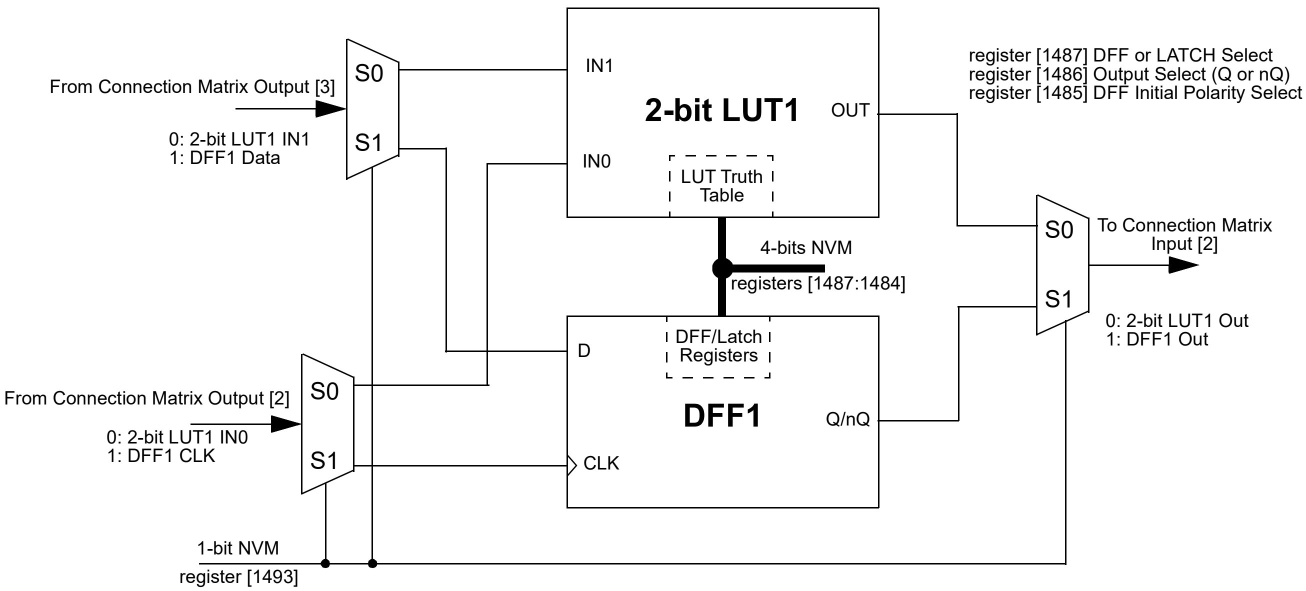


Figure 14: 2-bit LUT1 or DFF1

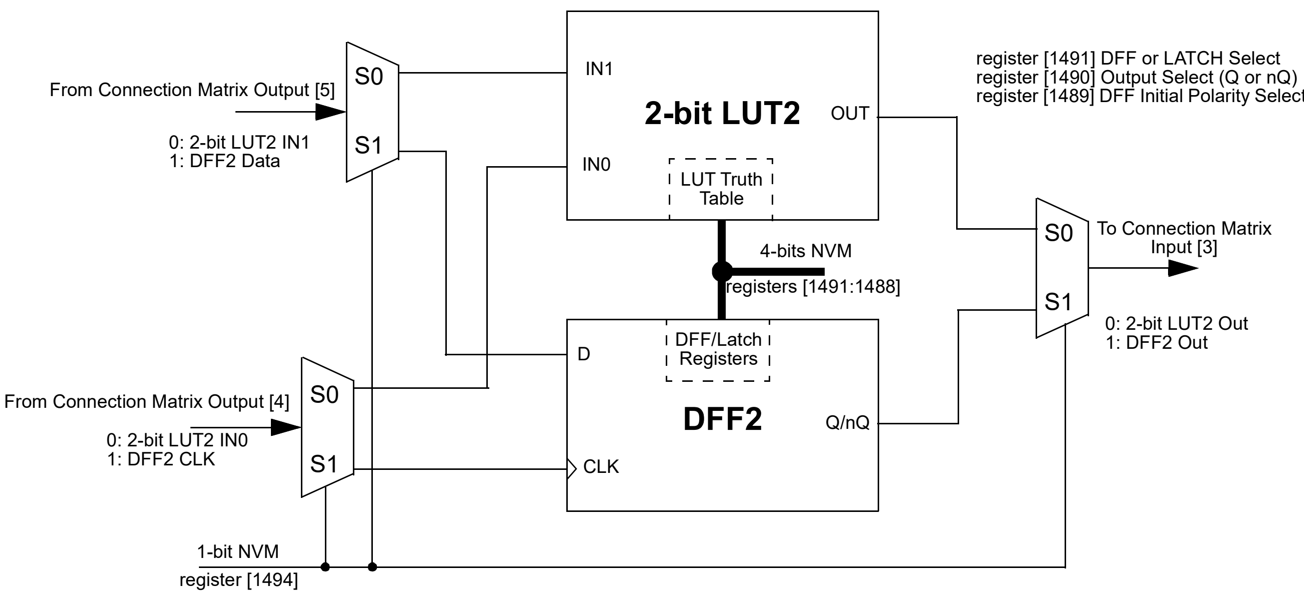


Figure 15: 2-bit LUT2 or DFF2

7.1.1 2-Bit LUT or D Flip-Flop Macrocell Used as 2-Bit LUT

Table 30: 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	register [1480]	LSB
0	1	register [1481]	
1	0	register [1482]	
1	1	register [1483]	MSB

Table 31: 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1484]	LSB
0	1	register [1485]	
1	0	register [1486]	
1	1	register [1487]	MSB

Table 32: 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	register [1488]	LSB
0	1	register [1489]	
1	0	register [1490]	
1	1	register [1491]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by registers [1483:1480]

2-Bit LUT1 is defined by registers [1487:1484]

2-Bit LUT2 is defined by registers [1491:1488]

Table 33 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 33: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.1.2 Initial Polarity Operations

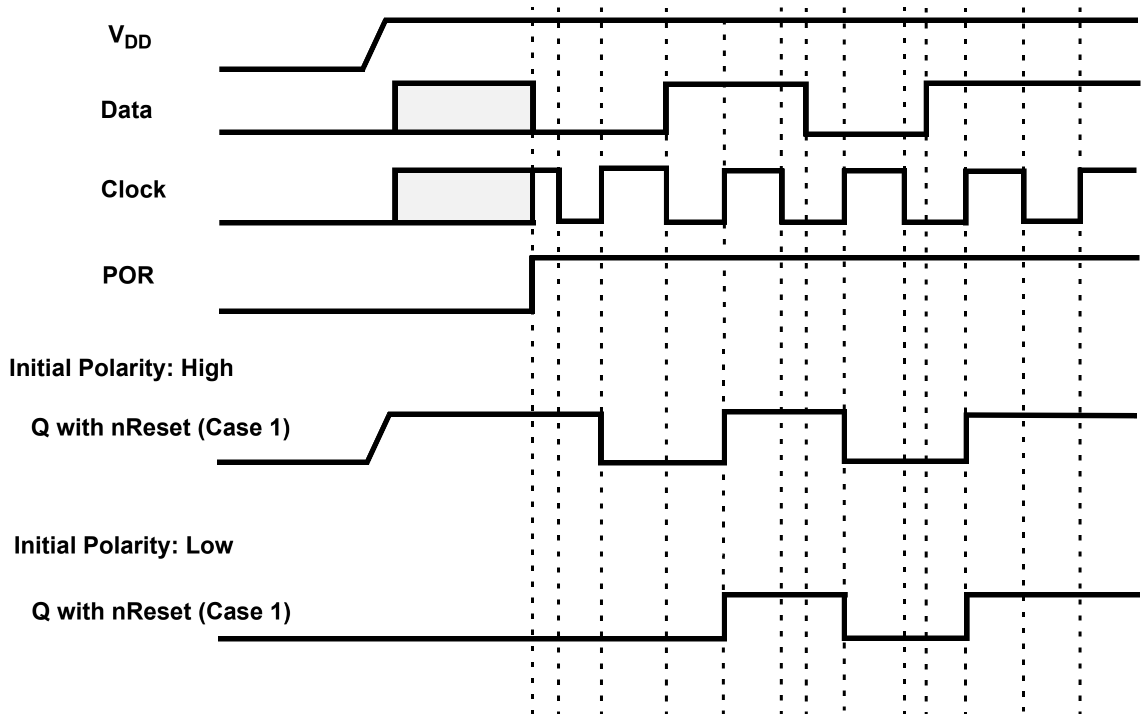


Figure 16: DFF Polarity Operations

7.2 2-BIT LUT OR PROGRAMMABLE PATTERN GENERATOR

The SLG47004 has one combination function macrocell that can serve as a logic or a timing function. This macrocell can serve as a Look Up Table (LUT), or a Programmable Pattern Generator (PGen).

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUT can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

It is possible to define the RST level for the PGen macrocell. There are both high level reset (RST) and a low level reset (nRST) options available, which are selected by register [1517]. When operating as the Programmable Pattern Generator, the output of the macrocell will clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.

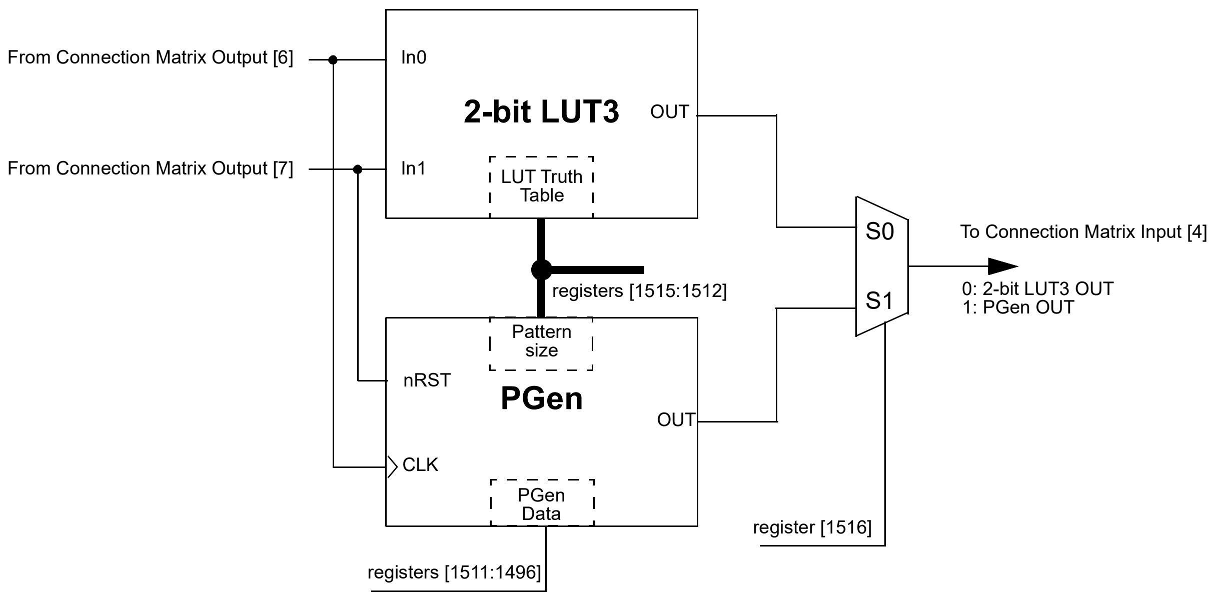


Figure 17: 2-bit LUT3 or PGen

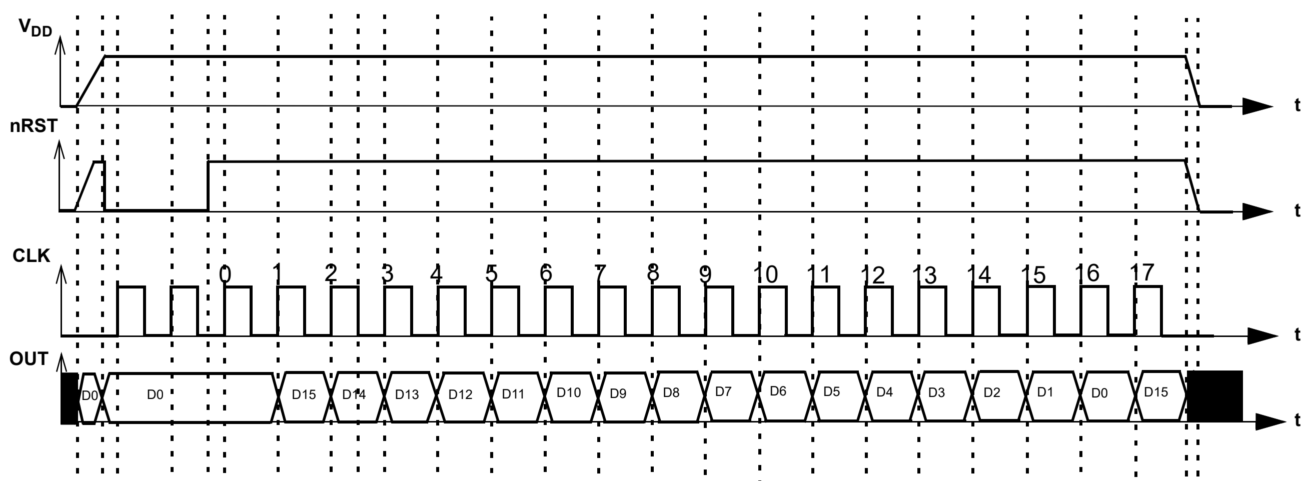


Figure 18: PGen Timing Diagram

7.2.1 2-Bit LUT or PGen Macrocell Used as 2-Bit LUT

Table 34: 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1512]	LSB
0	1	register [1513]	
1	0	register [1514]	
1	1	register [1515]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

*2-Bit LUT3 is defined by [*1515:1512*]*

Table 35 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 35: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.3 3-BIT LUT OR D FLIP-FLOP WITH SET/RESET MACROCELLS

There are seven macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix. It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active high level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available, which are selected by register [1523].

The DFF3 operation will flow the functional description:

- If register [1522] = 0, and the CLK is rising edge triggered, then Q = D, otherwise Q will not change.
- If register [1522] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

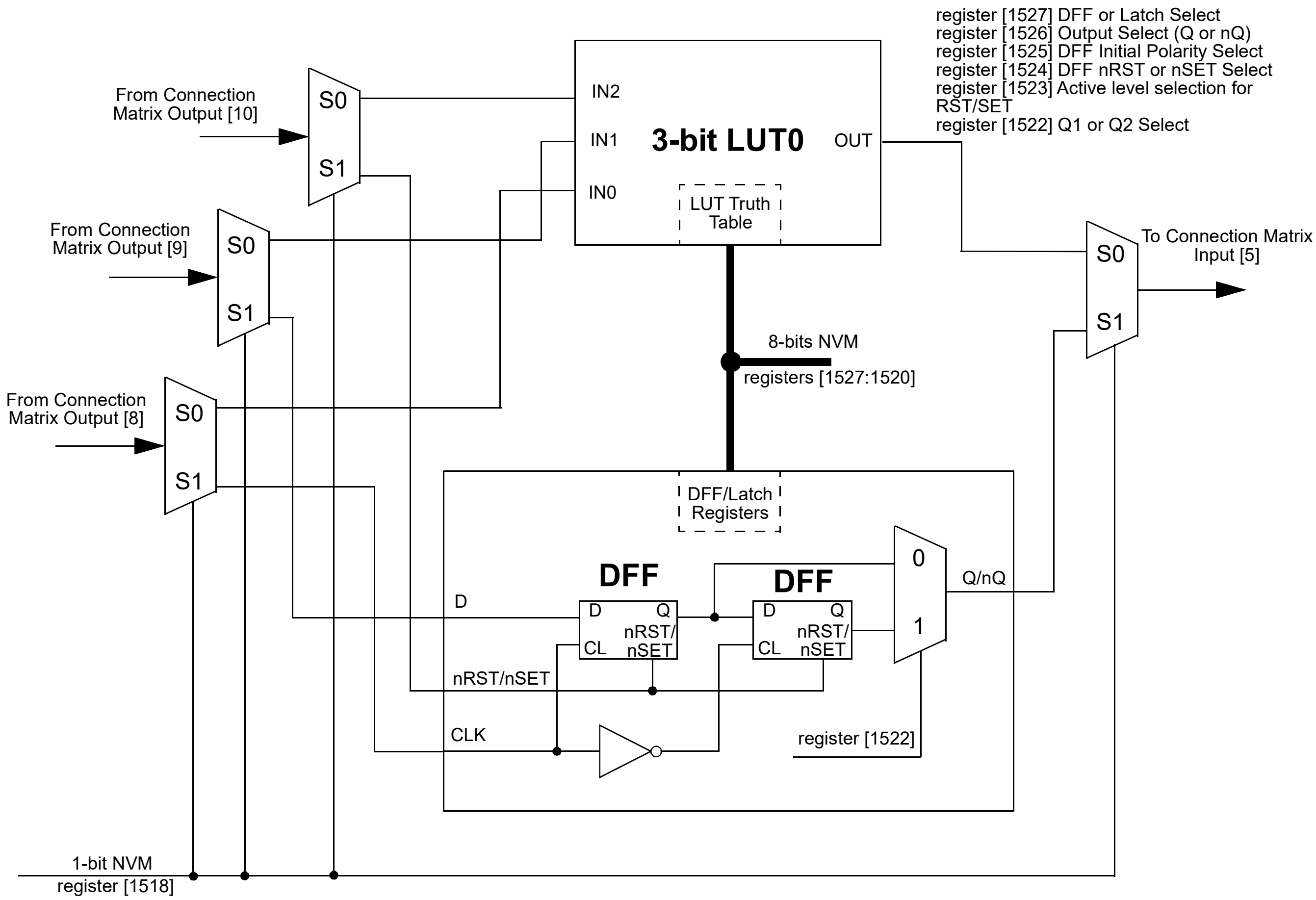


Figure 19: 3-bit LUT0 or DFF3

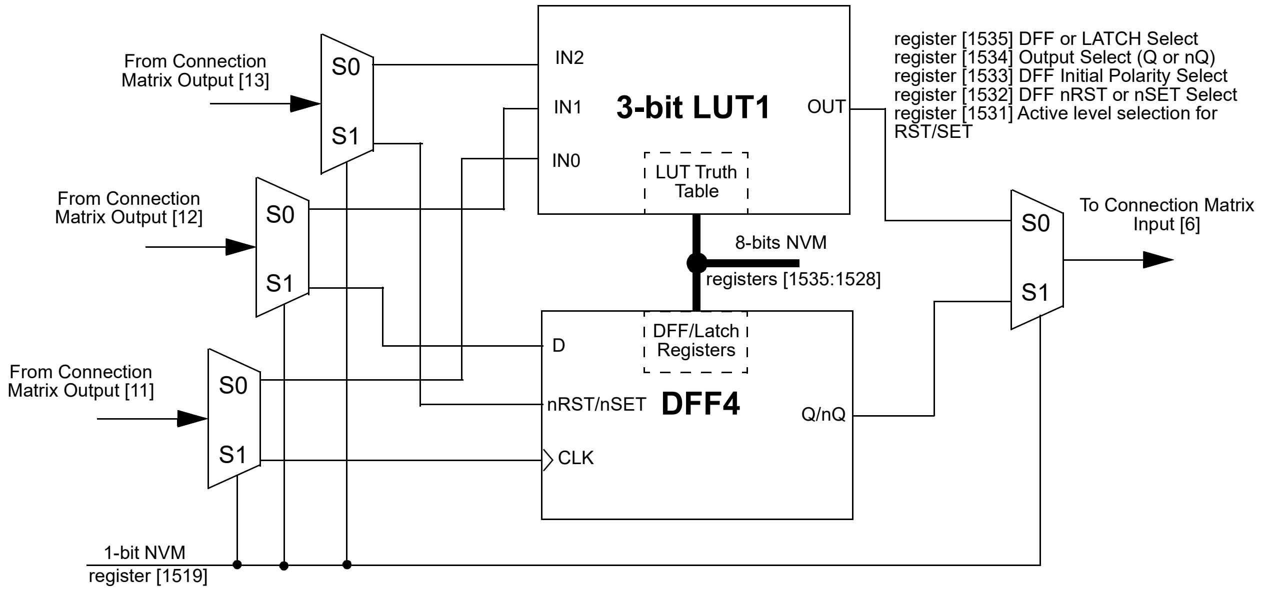


Figure 20: 3-bit LUT1 or DFF4

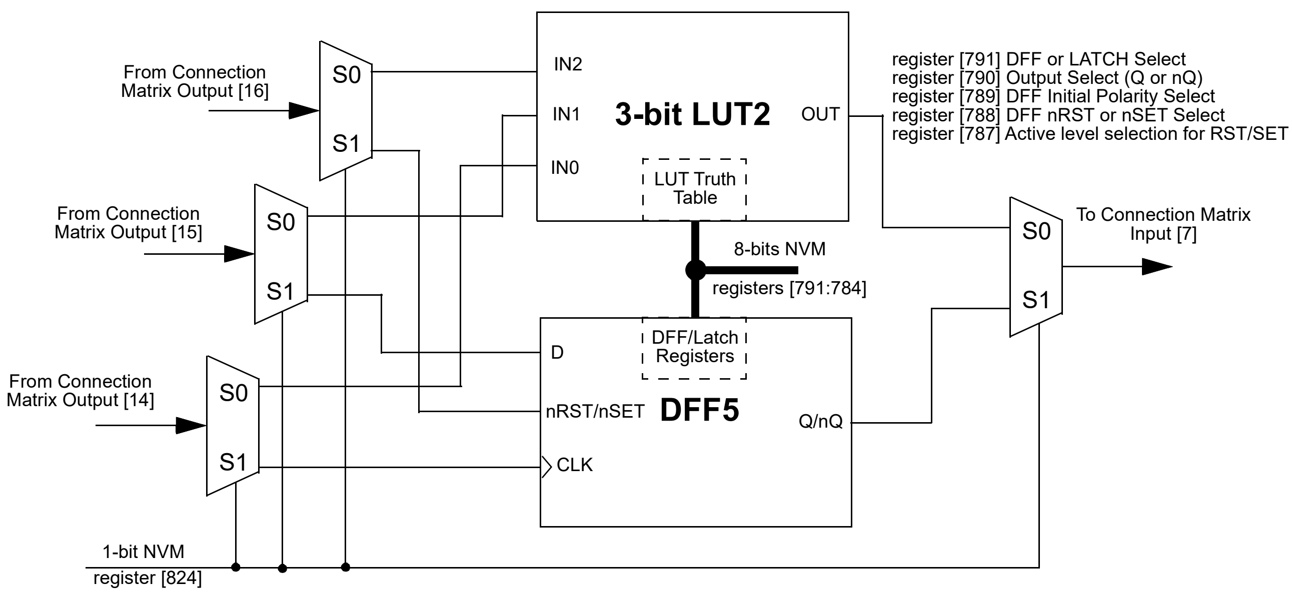


Figure 21: 3-bit LUT2 or DFF5

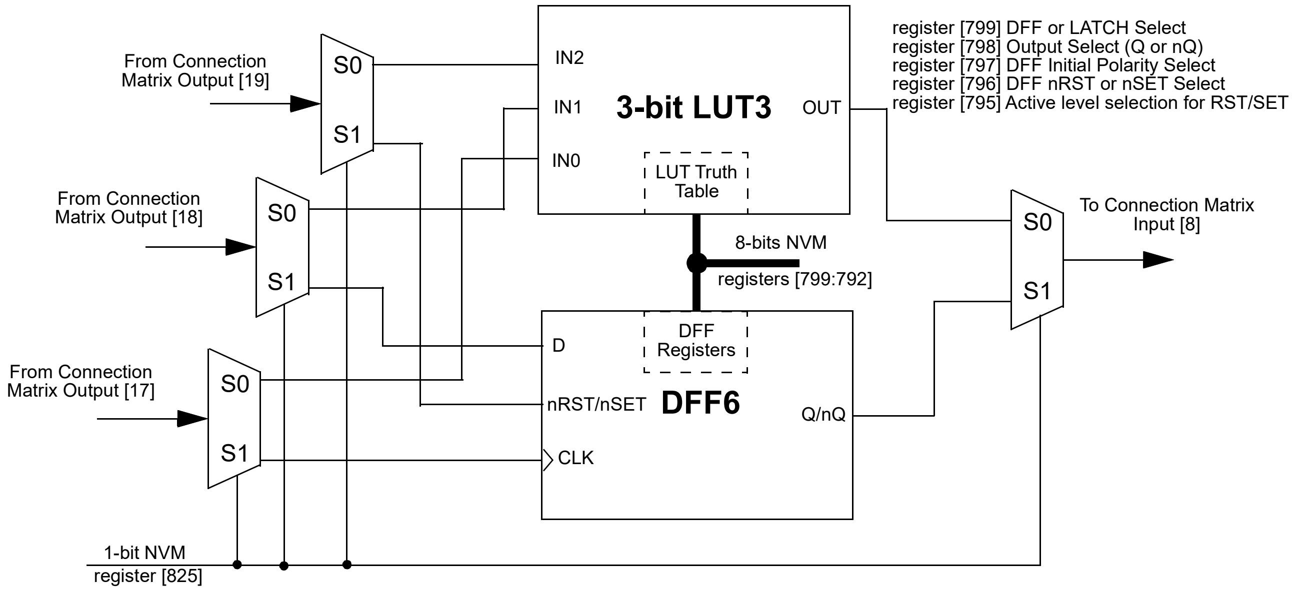


Figure 22: 3-bit LUT3 or DFF6

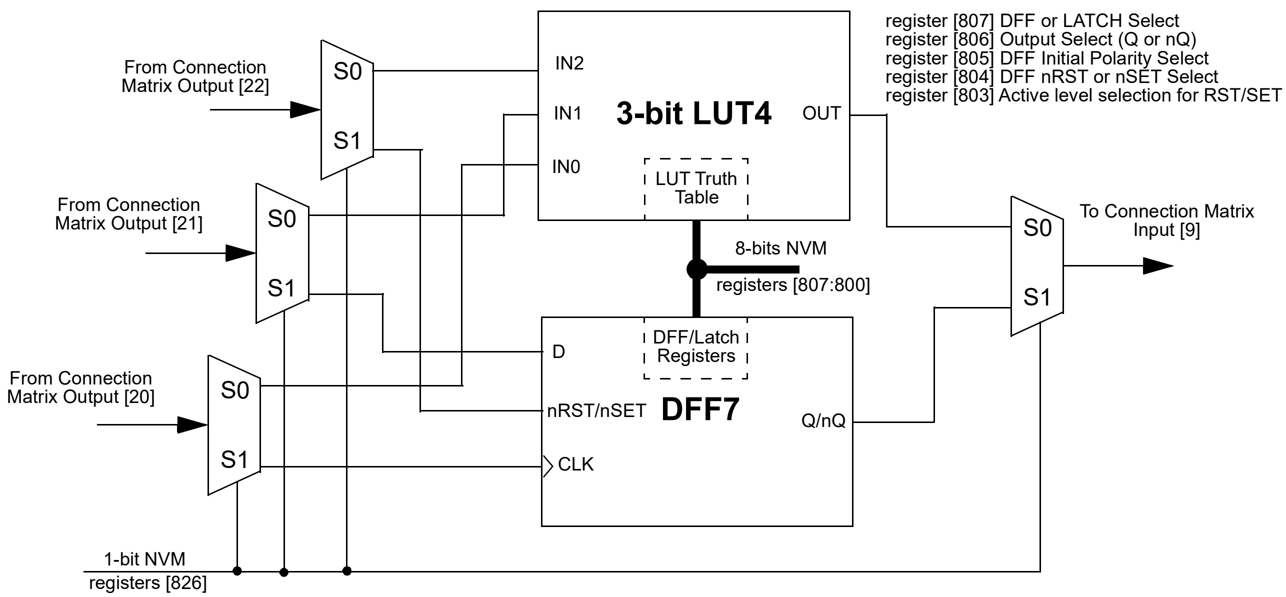


Figure 23: 3-bit LUT4 or DFF7

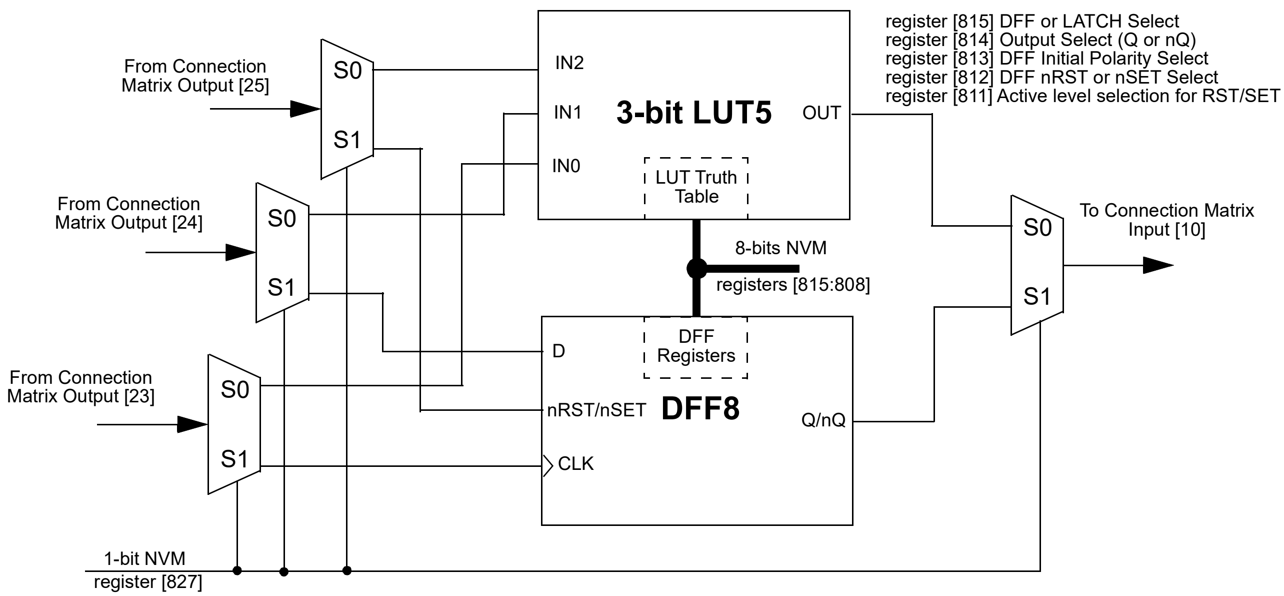


Figure 24: 3-bit LUT5 or DFF8

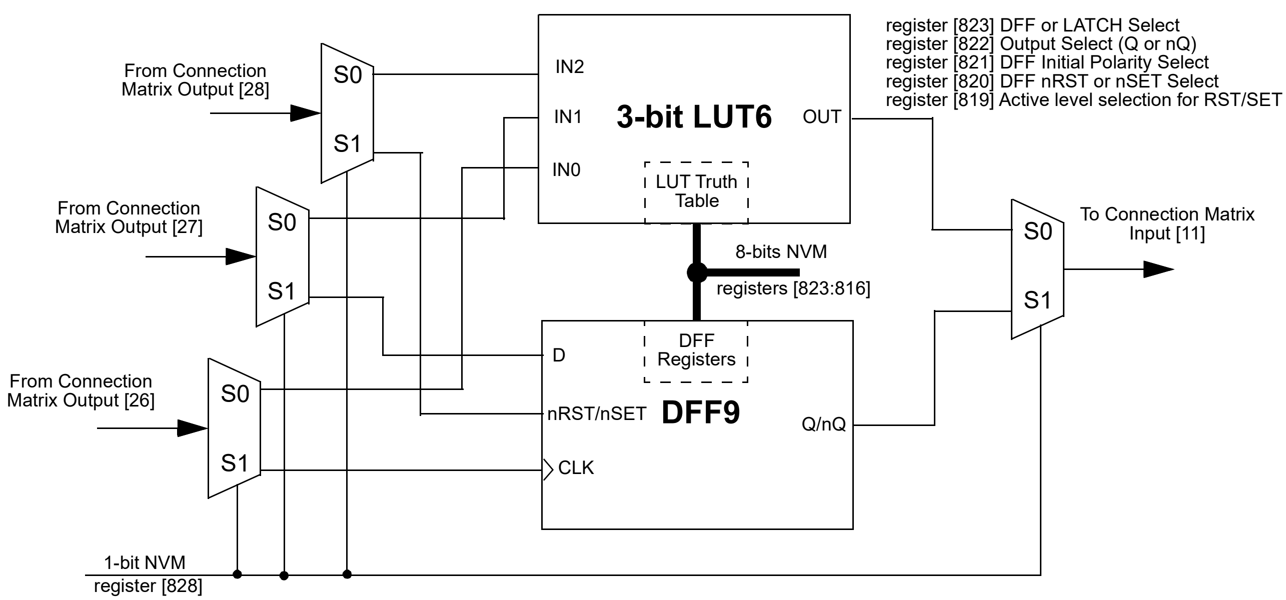


Figure 25: 3-bit LUT6 or DFF9

7.3.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Table 36: 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1520]	LSB
0	0	1	register [1521]	
0	1	0	register [1522]	
0	1	1	register [1523]	
1	0	0	register [1524]	
1	0	1	register [1525]	
1	1	0	register [1526]	
1	1	1	register [1527]	MSB

Table 37: 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1528]	LSB
0	0	1	register [1529]	
0	1	0	register [1530]	
0	1	1	register [1531]	
1	0	0	register [1532]	
1	0	1	register [1533]	
1	1	0	register [1534]	
1	1	1	register [1535]	MSB

Table 38: 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [784]	LSB
0	0	1	register [785]	
0	1	0	register [786]	
0	1	1	register [787]	
1	0	0	register [788]	
1	0	1	register [789]	
1	1	0	register [790]	
1	1	1	register [791]	MSB

Table 39: 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [792]	LSB
0	0	1	register [793]	
0	1	0	register [794]	
0	1	1	register [795]	
1	0	0	register [796]	
1	0	1	register [797]	
1	1	0	register [798]	
1	1	1	register [799]	MSB

Table 40: 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [800]	LSB
0	0	1	register [801]	
0	1	0	register [802]	
0	1	1	register [803]	
1	0	0	register [804]	
1	0	1	register [805]	
1	1	0	register [806]	
1	1	1	register [807]	MSB

Table 41: 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [808]	LSB
0	0	1	register [809]	
0	1	0	register [810]	
0	1	1	register [811]	
1	0	0	register [812]	
1	0	1	register [813]	
1	1	0	register [814]	
1	1	1	register [815]	MSB

Table 42: 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [816]	LSB
0	0	1	register [817]	
0	1	0	register [818]	
0	1	1	register [819]	
1	0	0	register [820]	
1	0	1	register [821]	
1	1	0	register [822]	
1	1	1	register [823]	MSB

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

3-Bit LUT0 is defined by registers [1527:1520]

3-Bit LUT1 is defined by registers [1535:1528]

3-Bit LUT2 is defined by registers [791:784]

3-Bit LUT3 is defined by registers [799:792]

3-Bit LUT4 is defined by registers [807:800]

3-Bit LUT5 is defined by registers [815:808]

3-Bit LUT6 is defined by registers [823:816]

Table 43 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 43: 3-bit LUT Standard Digital Functions

Function	MSB						LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.3.2 Initial Polarity Operations

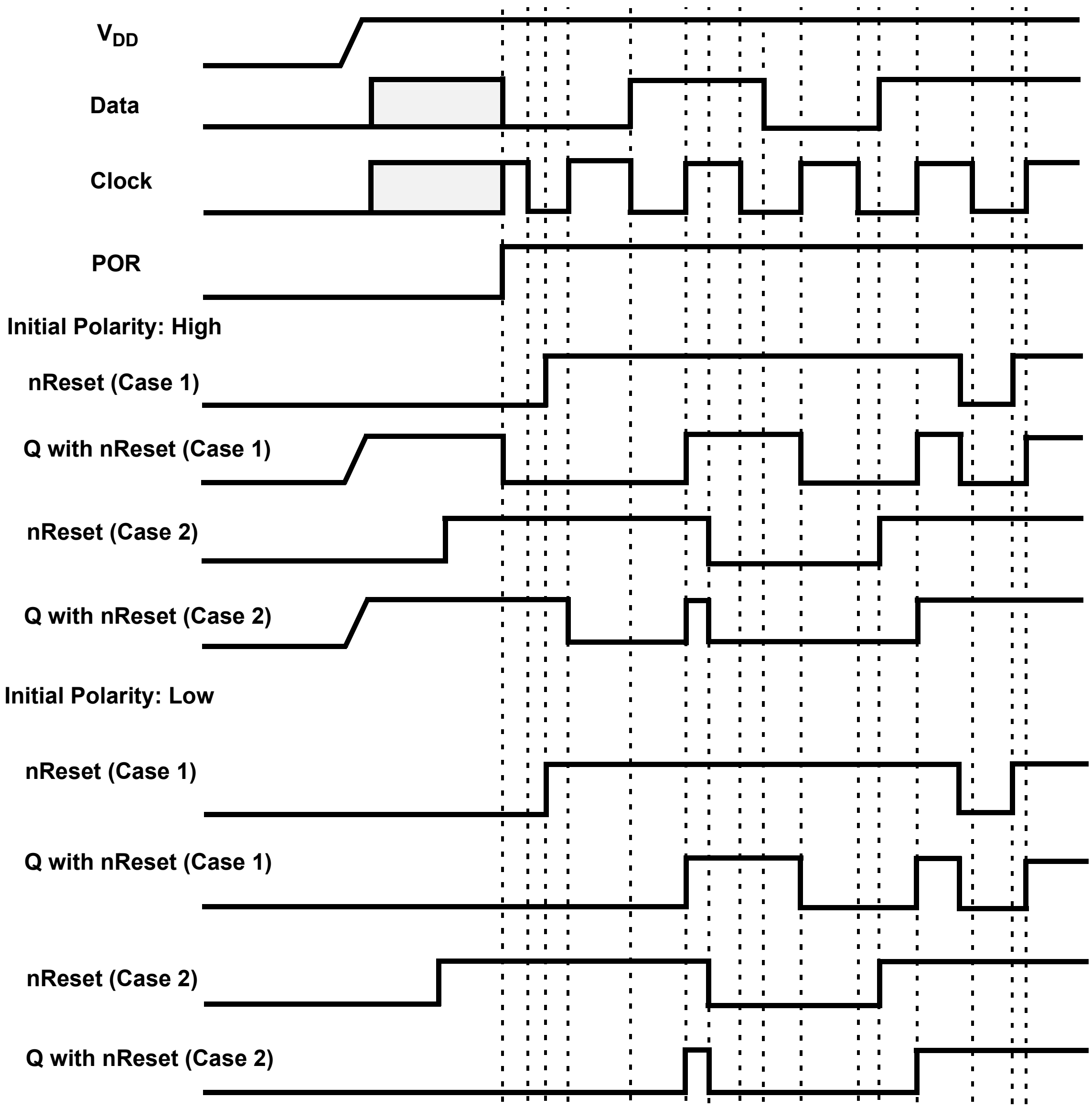


Figure 26: DFF Polarity Operations with nReset

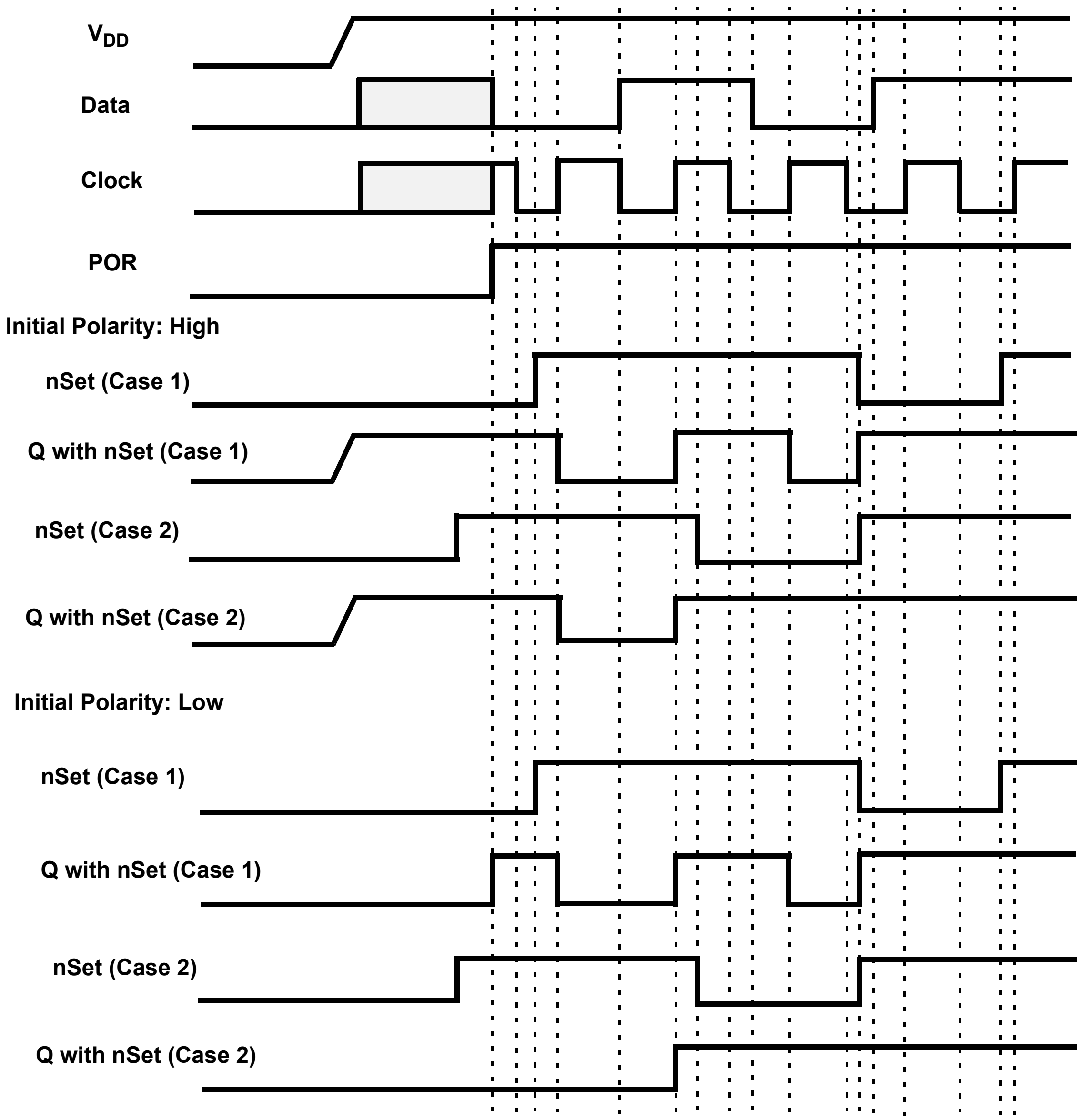


Figure 27: DFF Polarity Operations with nSet

7.4 4-BIT LUT OR D FLIP-FLOP WITH SET/RESET MACROCELL

There is one macrocell that can serve as either a 4-bit LUT or as a D Flip-Flop with Set/Reset inputs. When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix.

If register [842] = 0, and the CLK is rising edge triggered, then Q = D, otherwise Q will not change.

If register [842] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK. It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active high level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available, which are selected by register [843].

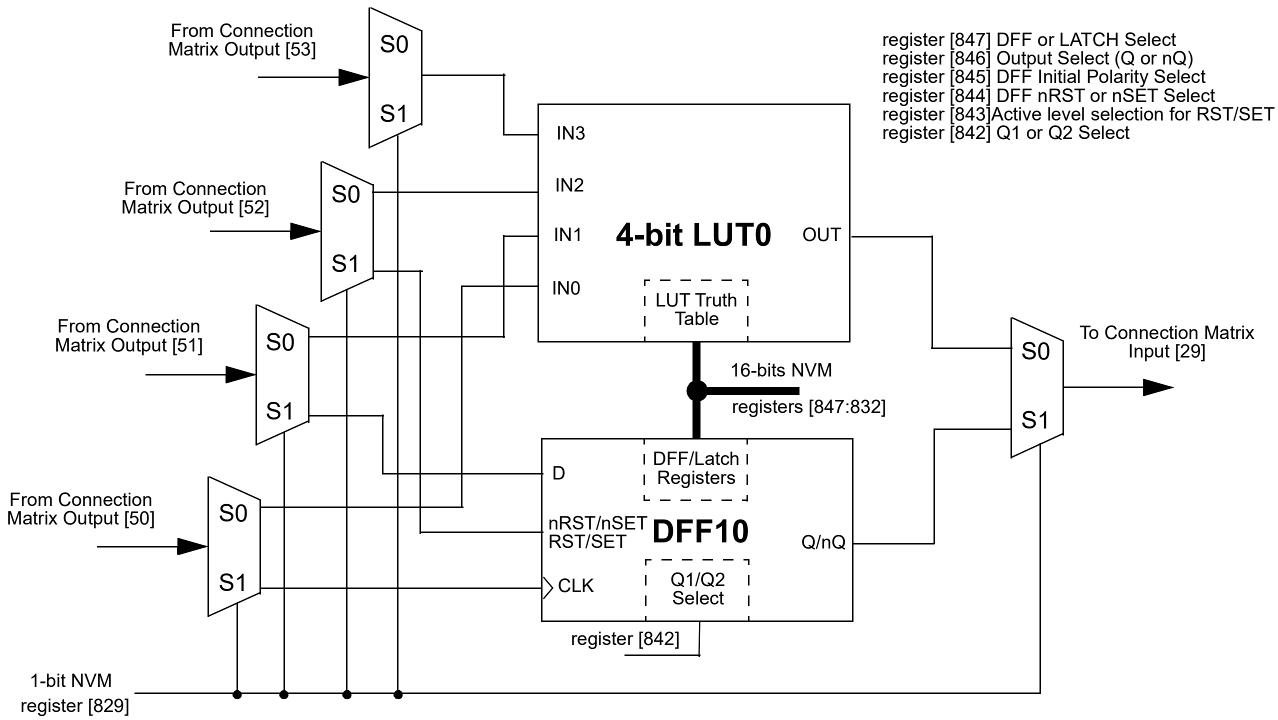


Figure 28: 4-bit LUT0 or DFF10

7.4.1 4-Bit LUT Macrocell Used as 4-Bit LUT

Table 44: 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [832]	LSB
0	0	0	1	register [833]	
0	0	1	0	register [834]	
0	0	1	1	register [835]	
0	1	0	0	register [836]	
0	1	0	1	register [837]	
0	1	1	0	register [838]	
0	1	1	1	register [839]	
1	0	0	0	register [840]	
1	0	0	1	register [841]	
1	0	1	0	register [842]	
1	0	1	1	register [843]	
1	1	0	0	register [844]	
1	1	0	1	register [845]	
1	1	1	0	register [846]	
1	1	1	1	register [847]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT0 is defined by registers [847:832]

Table 45: 4-bit LUT Standard Digital Functions

Function	MSB														LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

7.5 3-BIT LUT OR PIPE DELAY/RIPPLE COUNTER MACROCELL

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay/Ripple Counter.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a Pipe Delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK), and Reset (nRST). The Pipe Delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell input (IN). Both of the two outputs (OUT0 and OUT1) provide user selectable options for 1 to 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by registers [851:848] for OUT0 and registers [855:852] for OUT1. The 4-input MUX is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG47004 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the internal Oscillator within the SLG47004). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell. OUT1 Output can be inverted (as selected by register [859]).

In the Ripple Counter mode, there are 3 options for setting, which use 7 bits. There are 3 bits to set **nSET value (SV)** in range from 0 to 7. It is a value, which will be set into the Ripple Counter outputs when nSET input goes LOW. **End value (EV)** will use 3 bits for setting outputs code, which will be last code in the cycle. After reaching the EV, the Ripple Counter goes to the first code by the rising edge on CLK input. The **Functionality mode** option uses 1 bit. This setting defines how exactly Ripple Counter will operate.

The user can select one of the functionality modes by register: RANGE or FULL. If the RANGE option is selected, the count starts from SV. If UP input is LOW the count goes down: SV→EV→EV-1 to SV+1→SV, and others (if SV is smaller than EV), or SV→SV-1 to EV+1→EV→SV (if SV is bigger than EV). If UP input is HIGH, count starts from SV up to EV, and others.

In the FULL range configuration the Ripple Counter functions as follows. If UP input is LOW, the count starts from SV and goes down to 0. Then current counter value jumps to EV and goes down to 0, and others.

If UP input is HIGH, count goes up starting from SV. Then current counter value jumps to 0 and counts up to EV, and others. See Ripple Counter functionality example in Figure 30.

Every step is executed by the rising edge on CLK input.

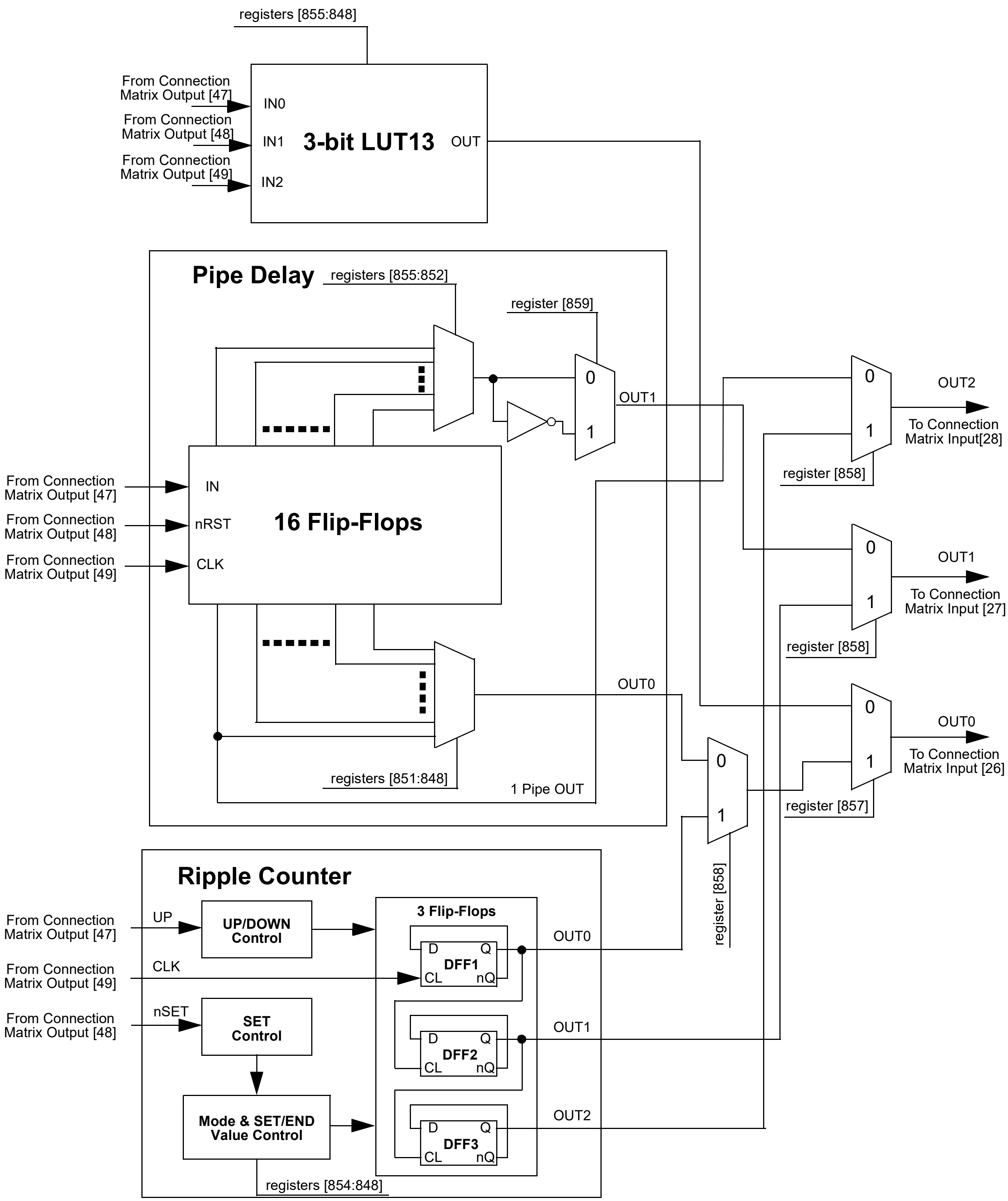


Figure 29: 3-bit LUT13/Pipe Delay/Ripple Counter

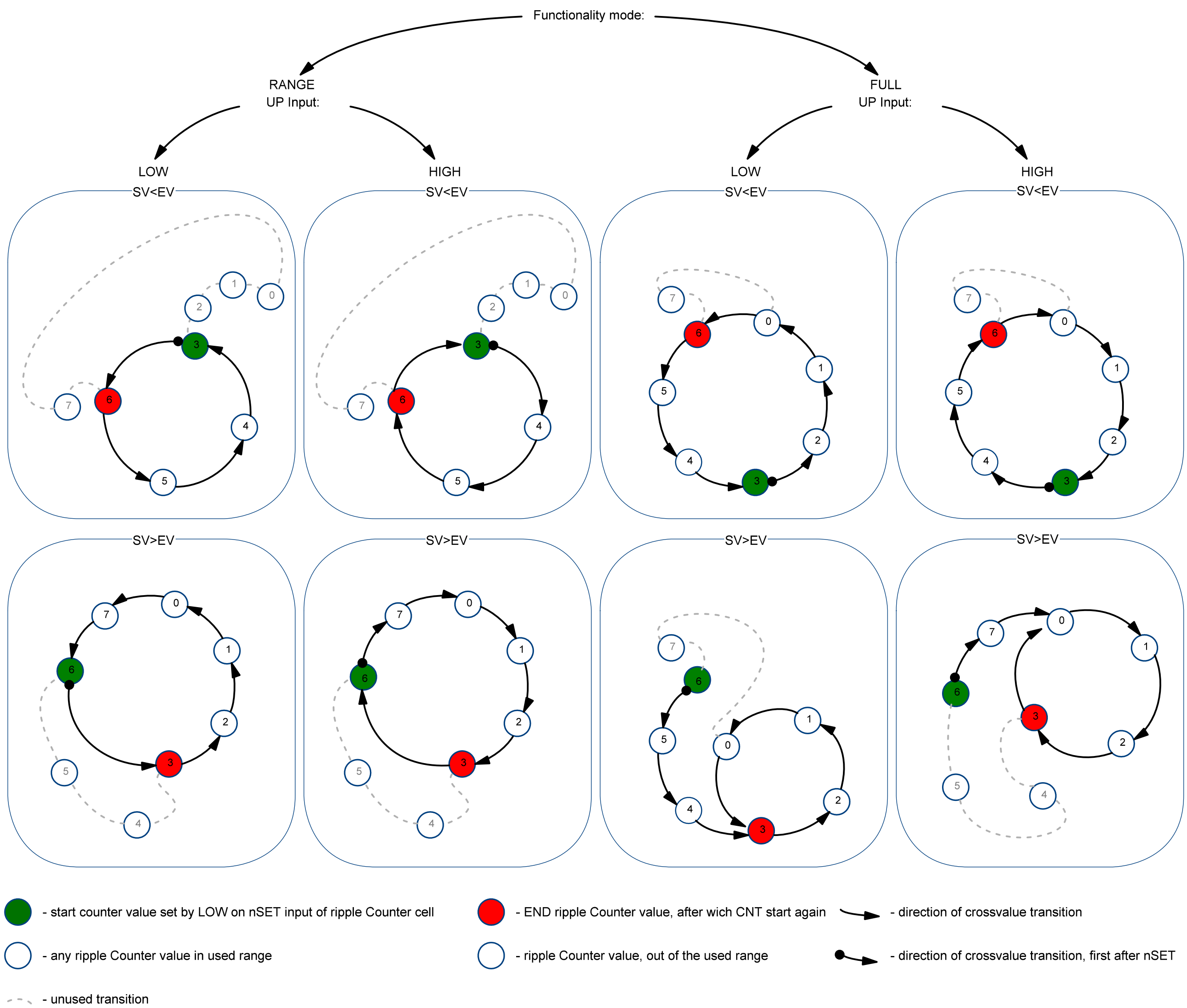


Figure 30: Example: Ripple Counter Functionality

7.5.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUT

Table 46: 3-bit LUT13 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [848]
0	0	1	register [849]
0	1	0	register [850]
0	1	1	register [851]
1	0	0	register [852]
1	0	1	register [853]
1	1	0	register [854]
1	1	1	register [855]

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

3-Bit LUT13 is defined by registers [855:848]

8 Multi-Function Macrocells

The SLG47004 has seven Multi-Function macrocells that can serve as more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes such as One Shot, Frequency Detect, Edge Detect, and others. Also, the macrocell is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF, see Figure 31.

See the list below for the functions that can be implemented in these macrocells:

- Six macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays
- One macrocell that can serve as a 4-bit LUT/D Flip-Flop and as 16-Bit Counter/Delay/FSM

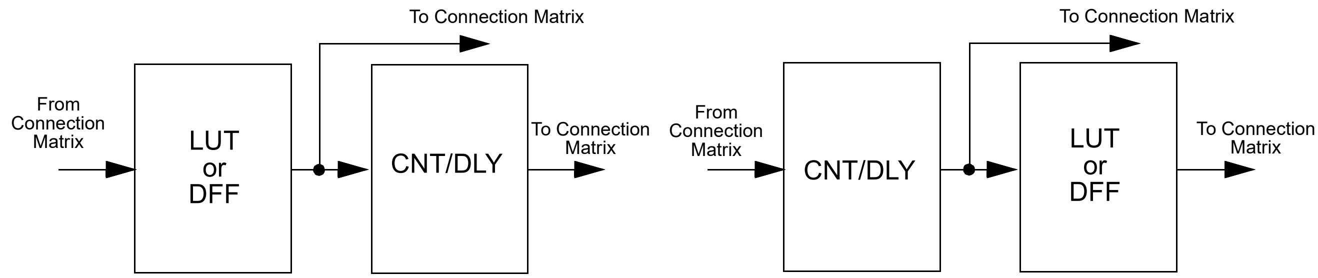


Figure 31: Possible Connections Inside Multi-Function Macrocell

Inputs/Outputs for the seven Multi-Function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

8.1 3-BIT LUT OR DFF/LATCH WITH 8-BIT COUNTER/DELAY MACROCELLS

There are six macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays.

When used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix or can be connected to CNT/DLY's input.

When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D), clock (CLK), and Reset/Set (nRST/nSET) inputs of the Flip-Flop, with the output going back to the connection matrix or to the CNT/DLY's input.

When used to implement Counter/Delays, each macrocell has a dedicated matrix input connection. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count/delay circuits. These macrocells can also operate in a One-Shot mode, which will generate an output pulse of user-defined width. They can also operate in a Frequency Detection or Edge Detection mode.

Counter/Delay macrocell has an initial value, which defines its initial value after SLG47004 is powered up. It is possible to select initial Low or initial High, as well as initial value defined by a Delay In signal.

For example, in case initial LOW option is used, the rising edge delay will start operation.

For timing diagrams refer to Section 8.3.

Note: After two DFF – counters initialize with counter data = 0 after POR.
Initial state = 1 – counters initialize with counter data = 0 after POR.
Initial state = 0 And After two DFF is bypass – counters initialize with counter data after POR.

CNT5 and CNT6 current count value can be read via I²C. However, it is possible to change the counter data (value counter starts operating from) for any macrocell using I²C write commands. In this mode, it is possible to load count data immediately (after two DFF) or after counter ends counting. See Section 18.7.1 for further details.

8.1.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

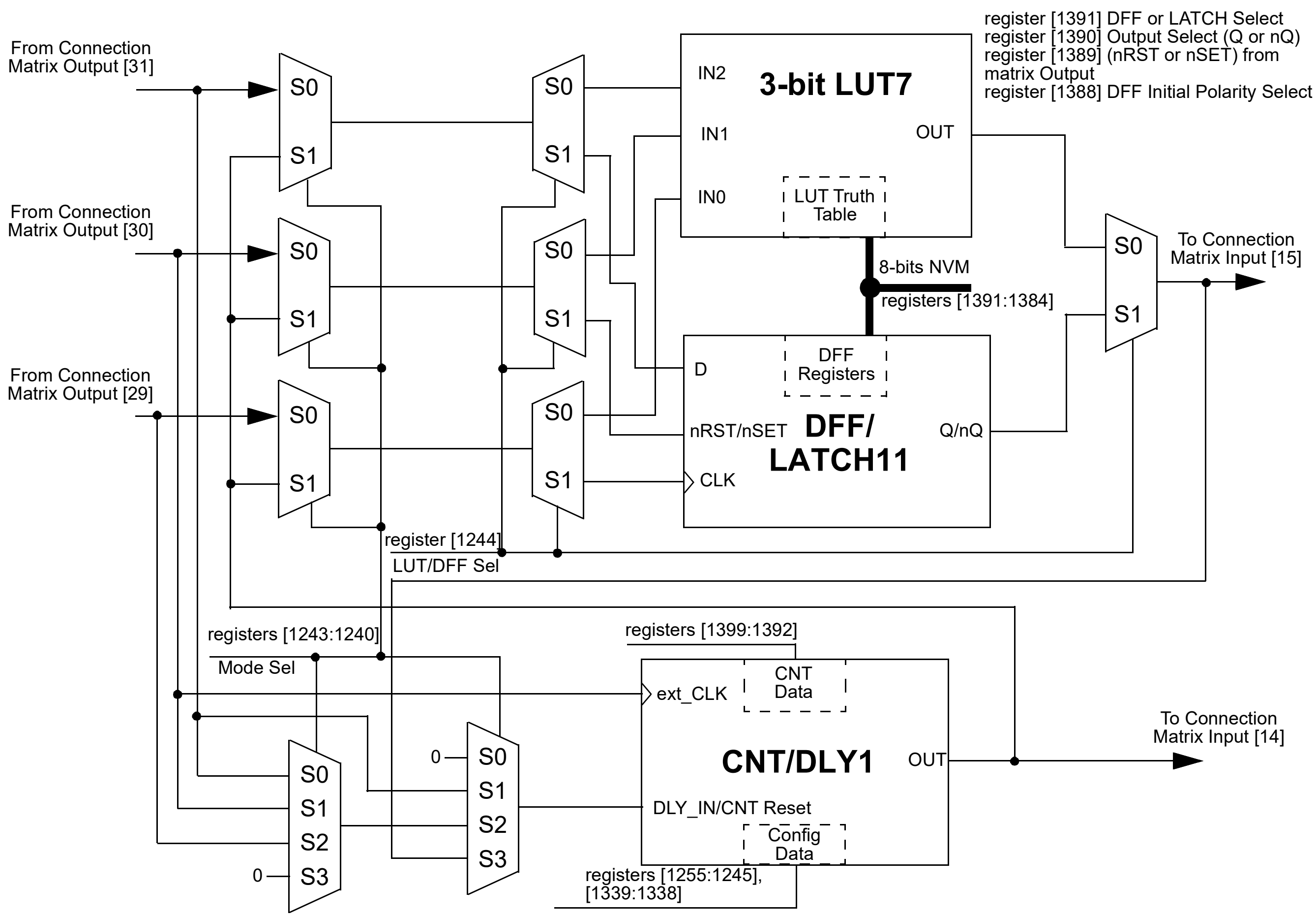


Figure 32: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT7/DFF11, CNT/DLY1)

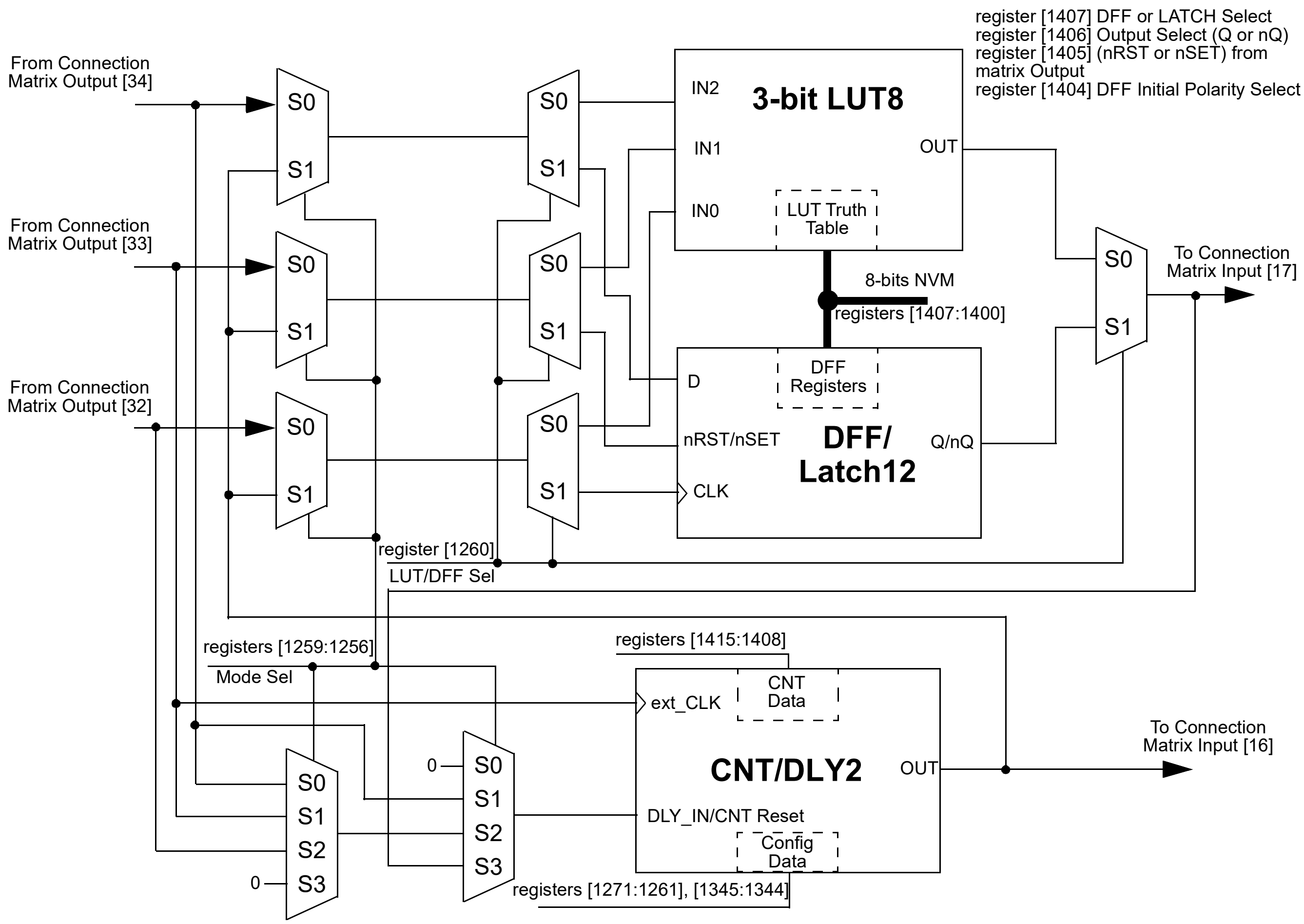


Figure 33: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT8/DFF12, CNT/DLY2)

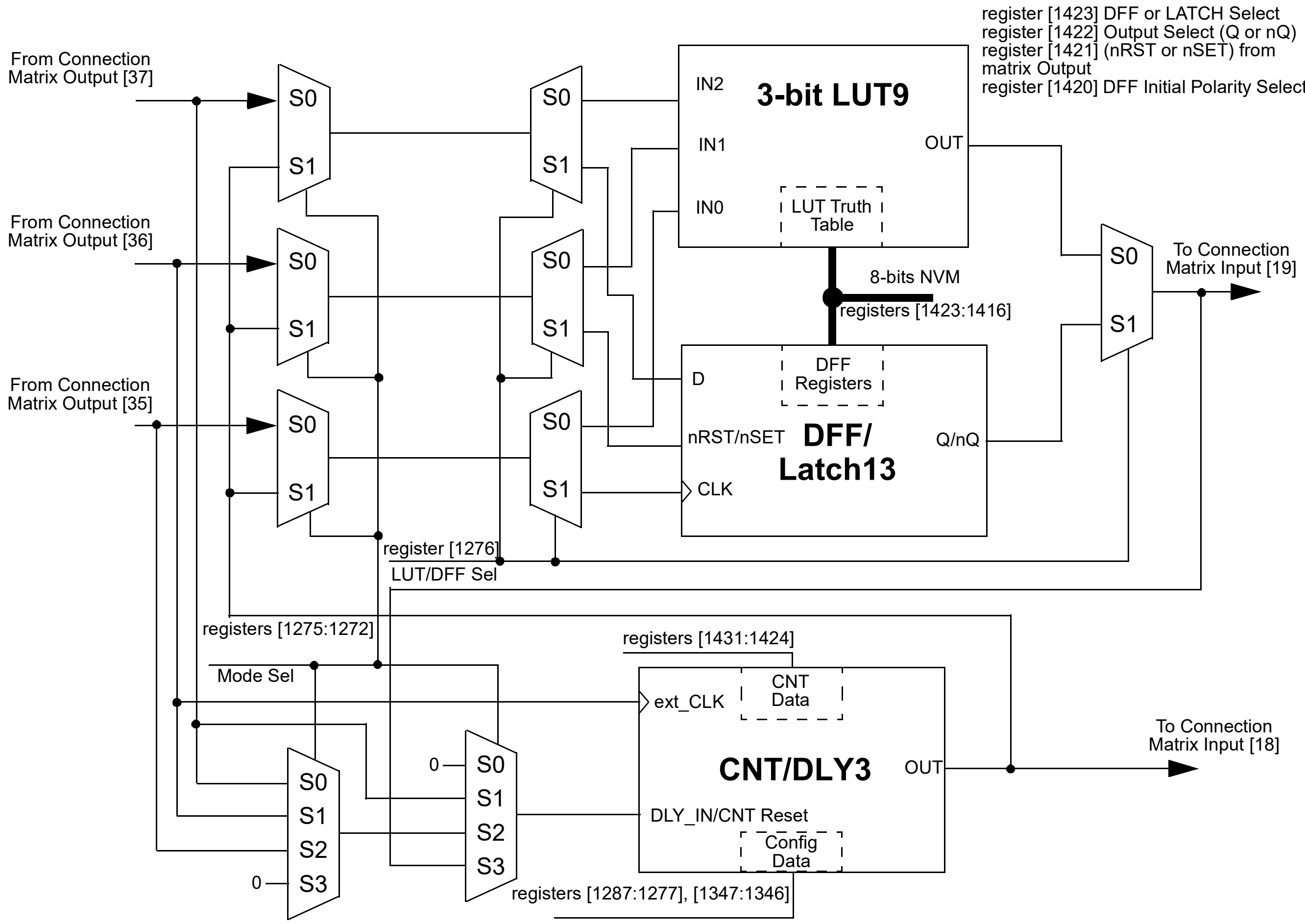


Figure 34: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT9/DFF13, CNT/DLY3)

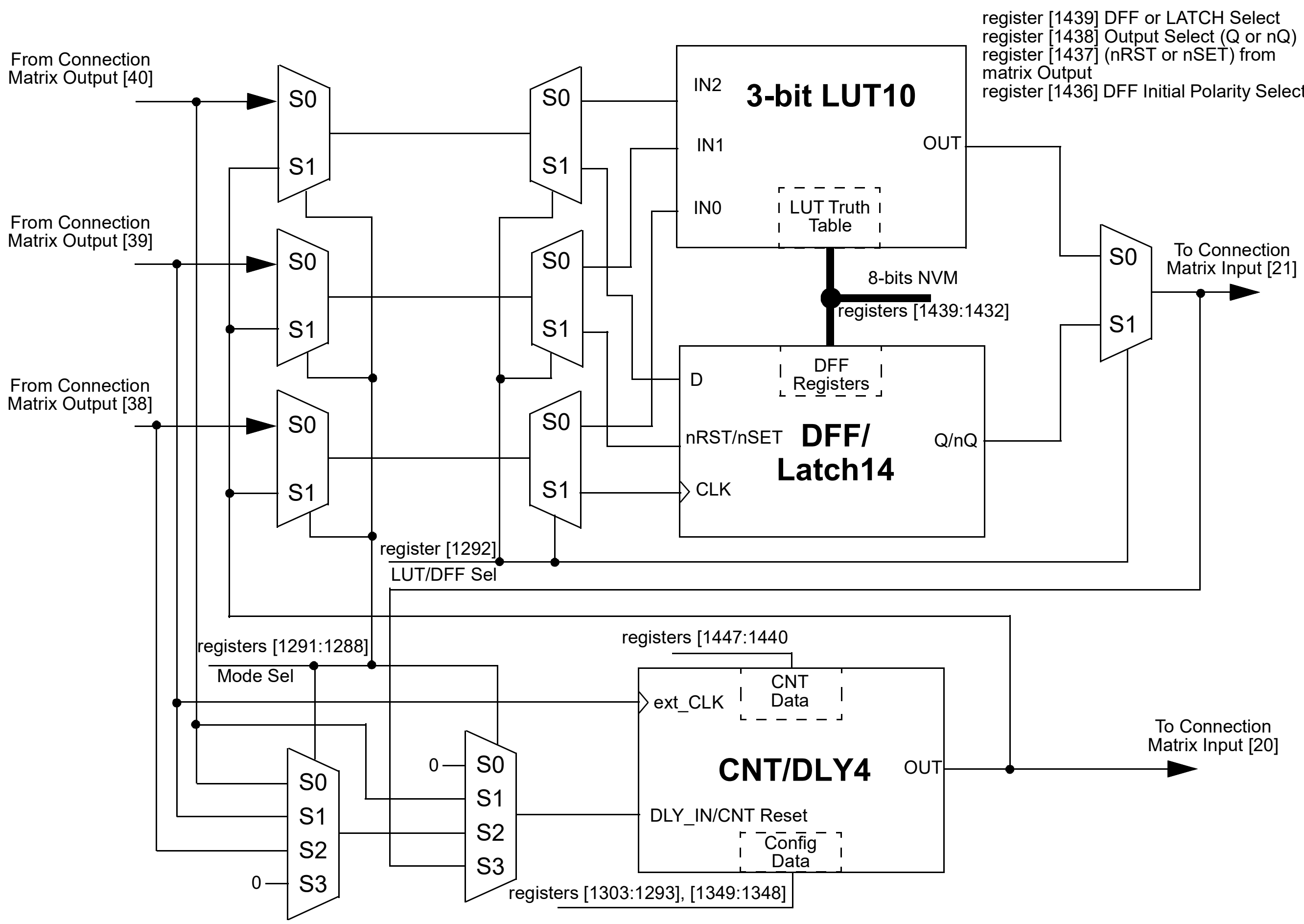


Figure 35: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT10/DFF14, CNT/DLY4)

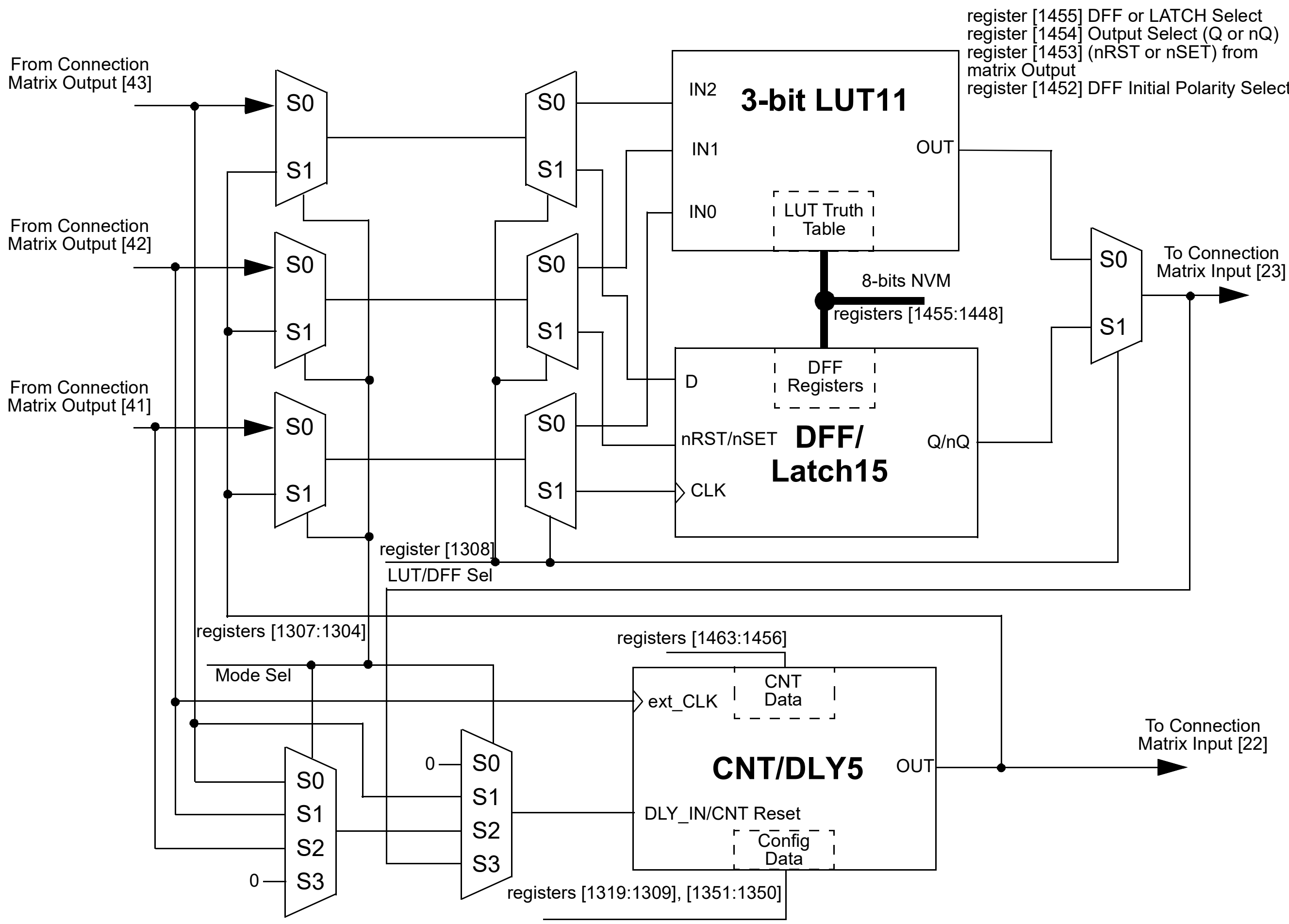


Figure 36: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT11/DFF15, CNT/DLY5)

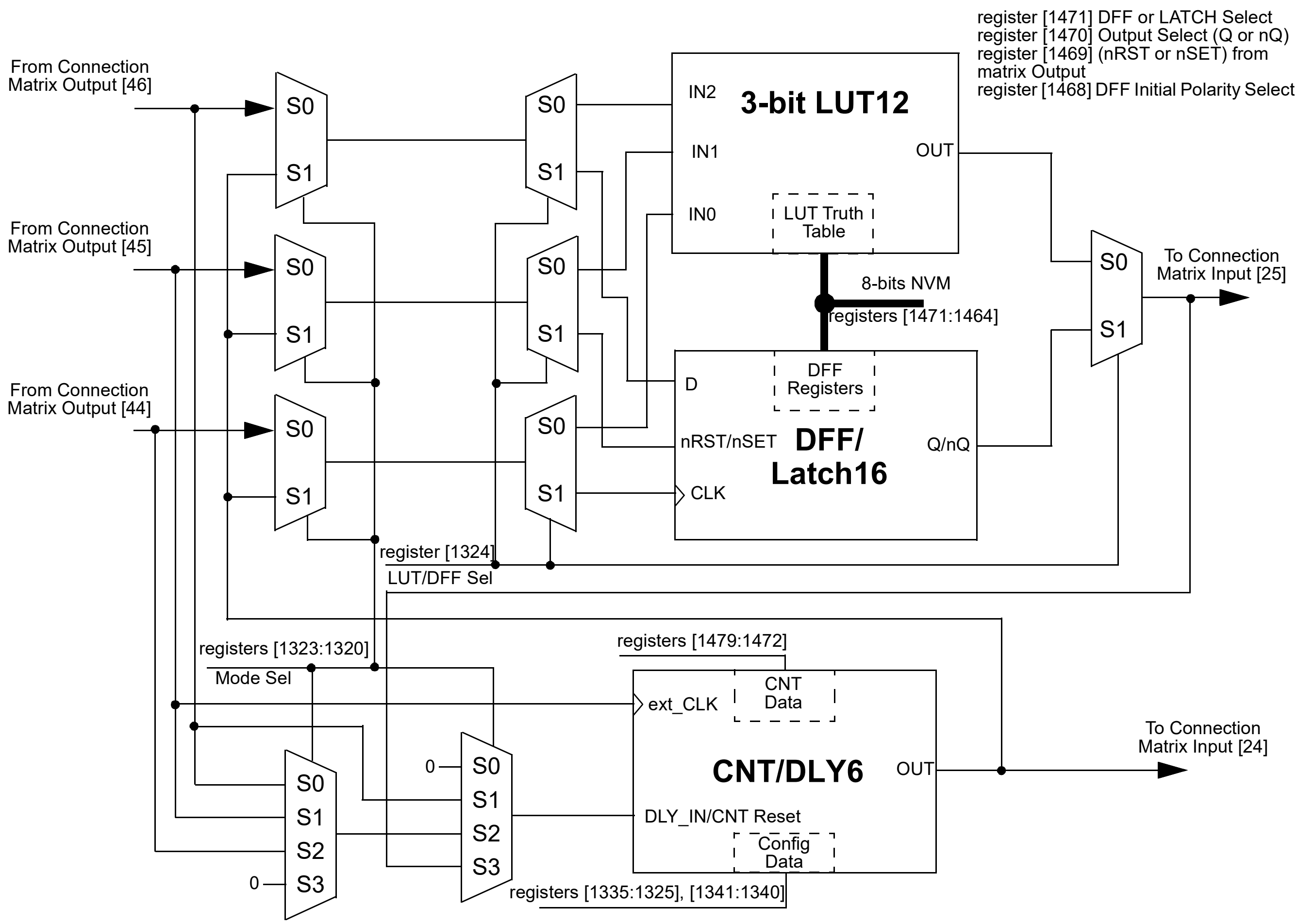


Figure 37: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT12/DFF16, CNT/DLY6)

As shown in Figure 32 to Figure 37 there is a possibility to use LUT/DFF and CNT/DLY simultaneously.

Note: It is not possible to use LUT and DFF at once, one of these macrocells must be selected.

- Case 1. LUT/DFF in front of CNT/DLY. Three input signals from the connection matrix go to previously selected LUT or DFF's inputs and produce a single output which goes to a CND/DLY input. In its turn Counter/Delay's output goes back to the matrix.
- Case 2. CNT/DLY in front of LUT/DFF. Two input signals from the connection matrix go to CND/DLY's inputs (IN and CLK). Its output signal can be connected to any input of previously selected LUT or DFF, after which the signal goes back to the matrix.
- Case 3. Single LUT/DFF or CNT/DLY. Also, it is possible to use a standalone LUT/DFF or CNT/DLY. In this case, all inputs and output of the macrocell are connected to the matrix.

8.1.2 3-Bit LUT or CNT/DLYs Used as 3-Bit LUTs

Table 47: 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1384]	LSB
0	0	1	register [1385]	
0	1	0	register [1386]	
0	1	1	register [1387]	
1	0	0	register [1388]	
1	0	1	register [1389]	
1	1	0	register [1390]	
1	1	1	register [1391]	MSB

Table 48: 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1400]	LSB
0	0	1	register [1401]	
0	1	0	register [1402]	
0	1	1	register [1403]	
1	0	0	register [1404]	
1	0	1	register [1405]	
1	1	0	register [1406]	
1	1	1	register [1407]	MSB

Table 49: 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1416]	LSB
0	0	1	register [1417]	
0	1	0	register [1418]	
0	1	1	register [1419]	
1	0	0	register [1420]	
1	0	1	register [1421]	
1	1	0	register [1422]	
1	1	1	register [1423]	MSB

Table 50: 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1432]	LSB
0	0	1	register [1433]	
0	1	0	register [1434]	
0	1	1	register [1435]	
1	0	0	register [1436]	
1	0	1	register [1437]	
1	1	0	register [1438]	
1	1	1	register [1439]	MSB

Table 51: 3-bit LUT11 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1448]	LSB
0	0	1	register [1449]	
0	1	0	register [1450]	
0	1	1	register [1451]	
1	0	0	register [1452]	
1	0	1	register [1453]	
1	1	0	register [1454]	
1	1	1	register [1455]	MSB

Table 52: 3-bit LUT12 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1464]	LSB
0	0	1	register [1465]	
0	1	0	register [1466]	
0	1	1	register [1467]	
1	0	0	register [1468]	
1	0	1	register [1469]	
1	1	0	register [1470]	
1	1	1	register [1471]	MSB

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

3-Bit LUT7 is defined by registers [1391:1384]

3-Bit LUT8 is defined by registers [1407:1400]

3-Bit LUT9 is defined by registers [1423:1416]

3-Bit LUT10 is defined by registers [1439:1432]

3-Bit LUT11 is defined by registers [1455:1448]

3-Bit LUT12 is defined by registers [1471:1464]

8.2 4-BIT LUT OR DFF/LATCH WITH 16-BIT COUNTER/DELAY MACROCELL

There is one macrocell that can serve as either 4-bit LUT/D Flip-Flops or as 16-bit Counter/Delay.

When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix.

When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

When used to implement 16-Bit Counter/Delay function, two of the four input signals from the connection matrix go to the external clock (EXT_CLK) and reset (DLY_IN/CNT Reset) for the Counter/Delay, with the output going back to the connection matrix.

This macrocell has an optional Finite State Machine (FSM) function. There are two additional matrix inputs for Up and Keep to support FSM functionality

This macrocell can also operate in a one-shot mode, which will generate an output pulse of user-defined width. This macrocell can also operate in a frequency detection or edge detection mode. This macrocell can have its active count value read via I^2C. See Section 18.7.1 for further details.

Note: After two DFF – counters initialize with counter data = 0 after POR.
Initial state = 1 – counters initialize with counter data = 0 after POR.
Initial state = 0 And After two DFF is bypass – counters initialize with counter data after POR.

8.2.1 4-Bit LUT or DFF/LATCH with 16-Bit CNT/DLY Block Diagram

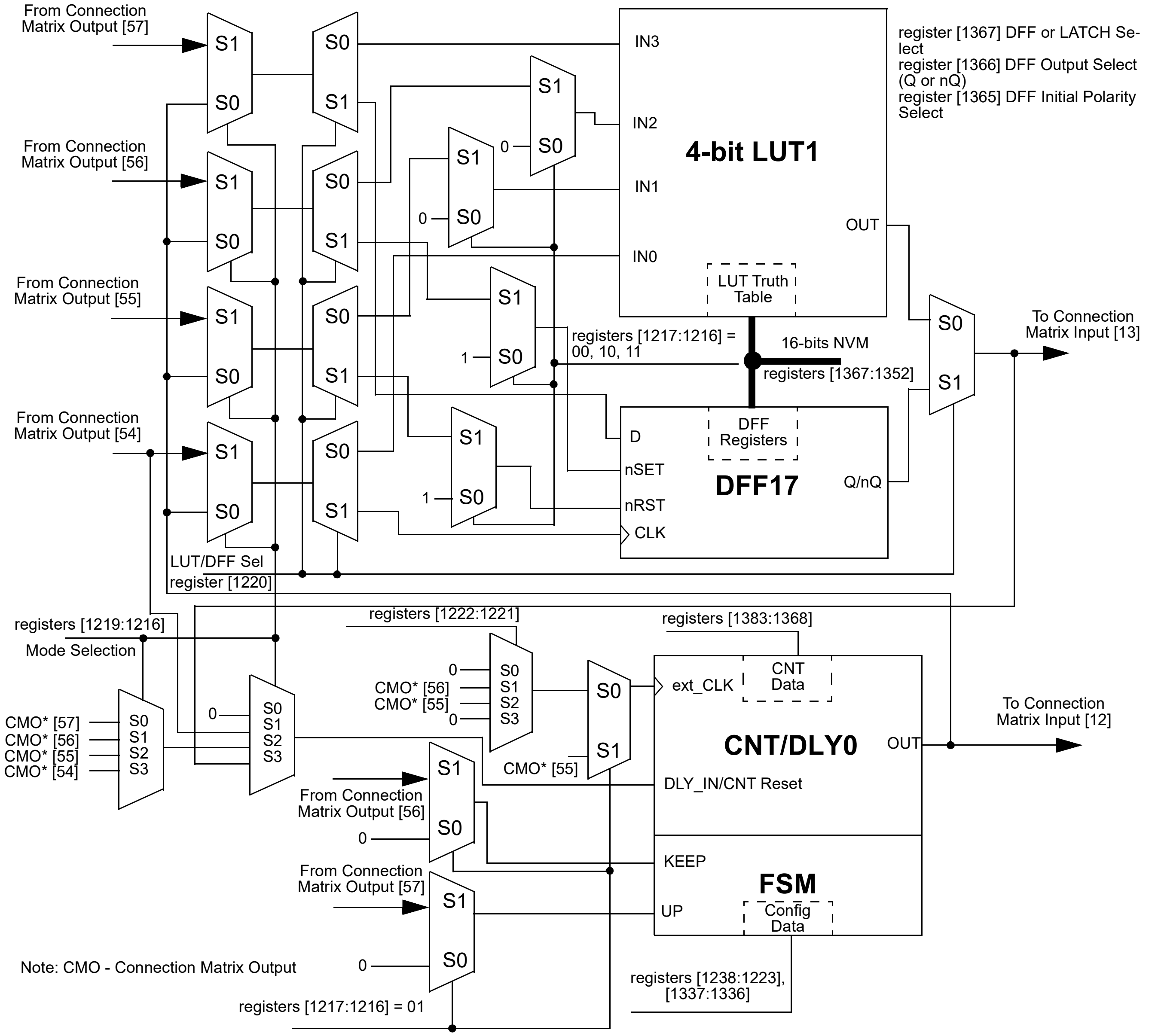


Figure 38: 4-bit LUT1 or CNT/DLY0

8.2.2 4-Bit LUT or 16-Bit Counter/Delay Macrocells Used as 4-Bit LUTs

Table 53: 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1352]	LSB
0	0	0	1	register [1353]	
0	0	1	0	register [1354]	
0	0	1	1	register [1355]	
0	1	0	0	register [1356]	
0	1	0	1	register [1357]	
0	1	1	0	register [1358]	
0	1	1	1	register [1359]	
1	0	0	0	register [1360]	
1	0	0	1	register [1361]	
1	0	1	0	register [1362]	
1	0	1	1	register [1363]	
1	1	0	0	register [1364]	
1	1	0	1	register [1365]	
1	1	1	0	register [1366]	
1	1	1	1	register [1367]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT1 is defined by registers [1367:1352]

Table 54: 4-bit LUT Standard Digital Functions

Function	MSB														LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	1

8.3 CNT/DLY/FSM TIMING DIAGRAMS

8.3.1 Delay Mode CNT/DLY0 to CNT/DLY6

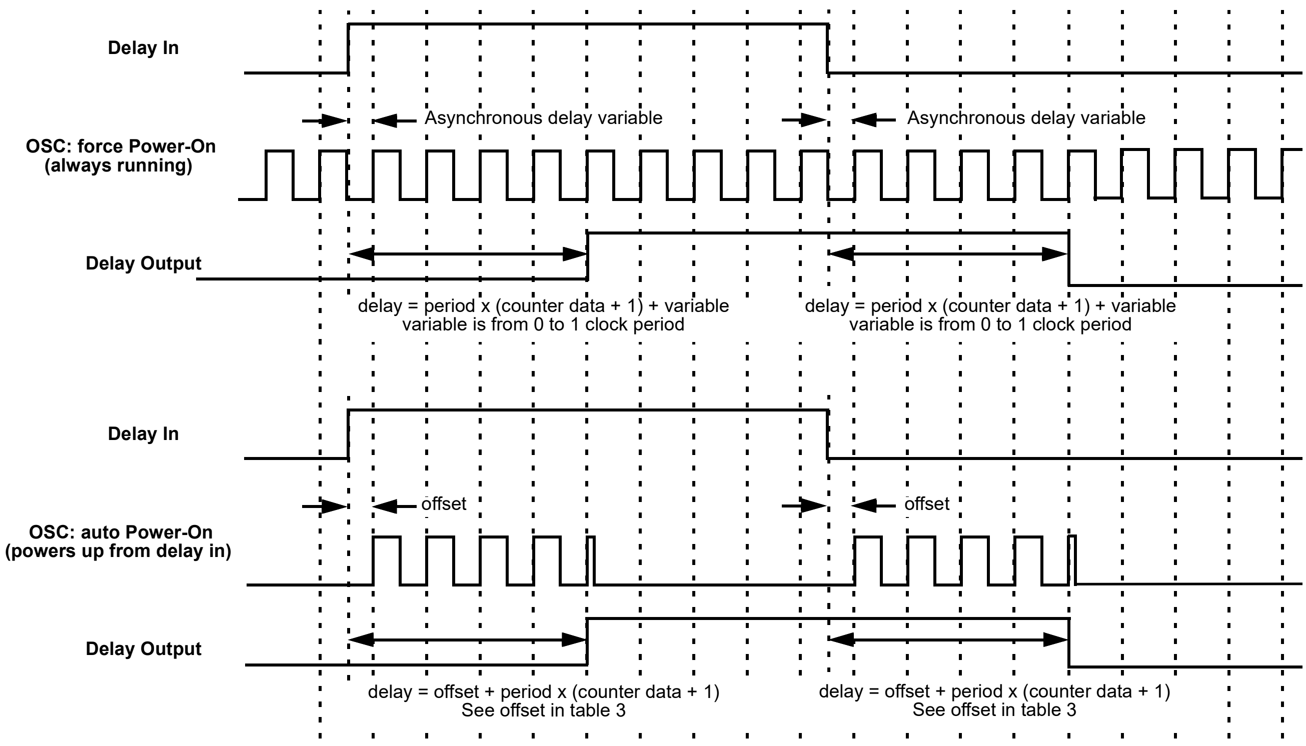


Figure 39: Delay Mode Timing Diagram, Edge Select: Both, Counter Data: 3

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

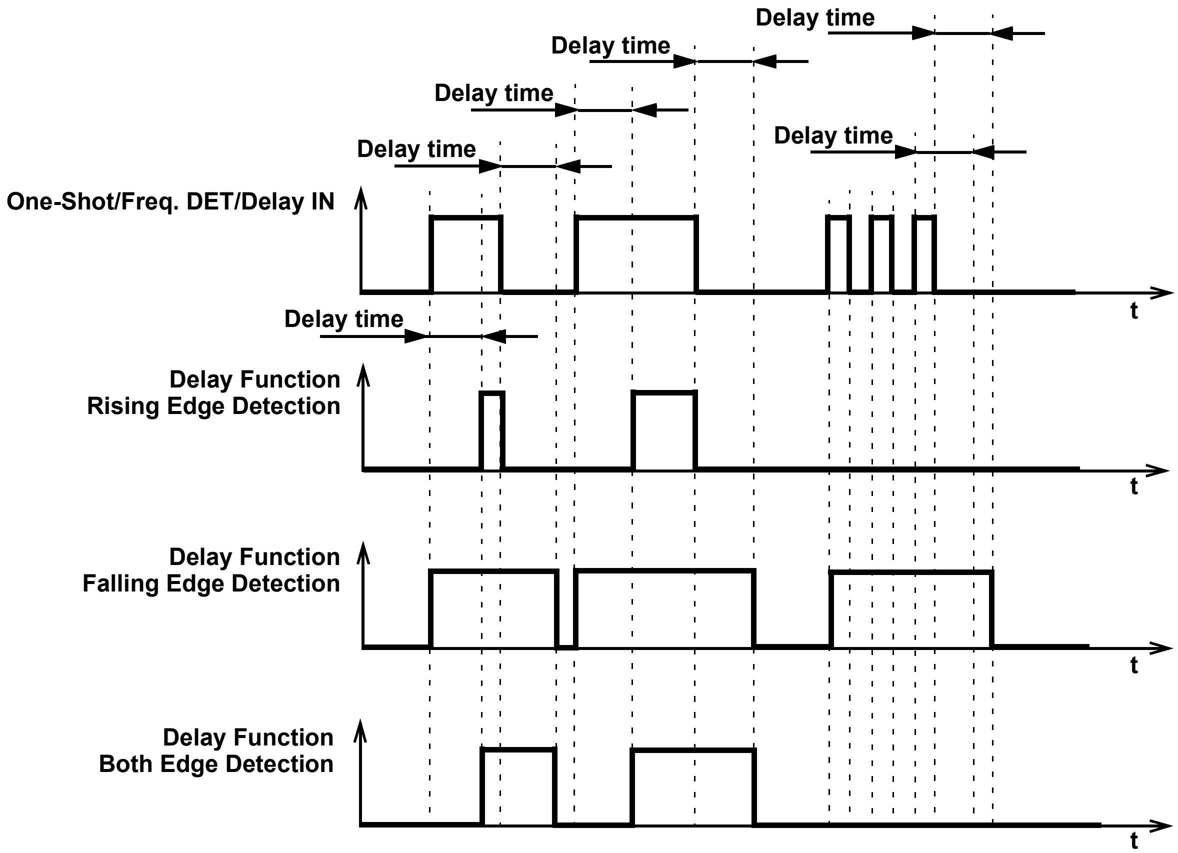


Figure 40: Delay Mode Timing Diagram for Different Edge Select Modes

8.3.2 Count Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY0 to CNT/DLY6

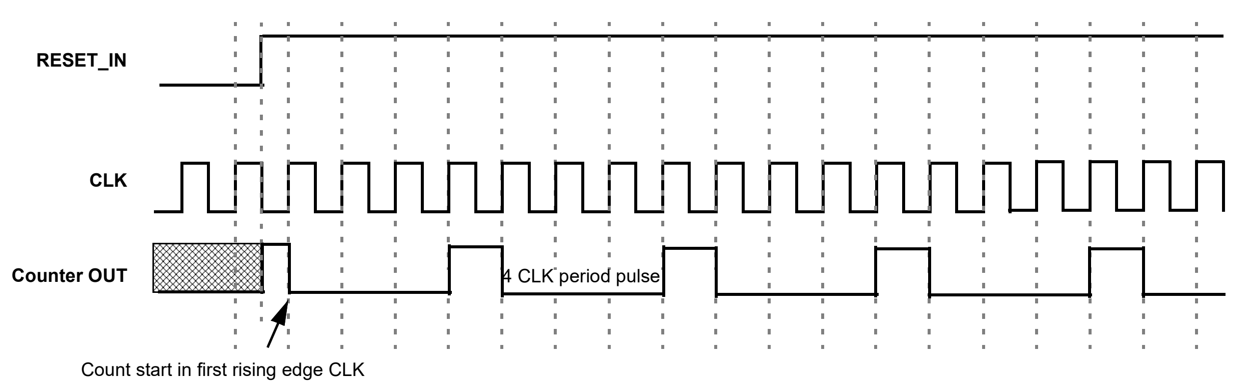


Figure 41: Counter Mode Timing Diagram without Two DFFs Synced Up

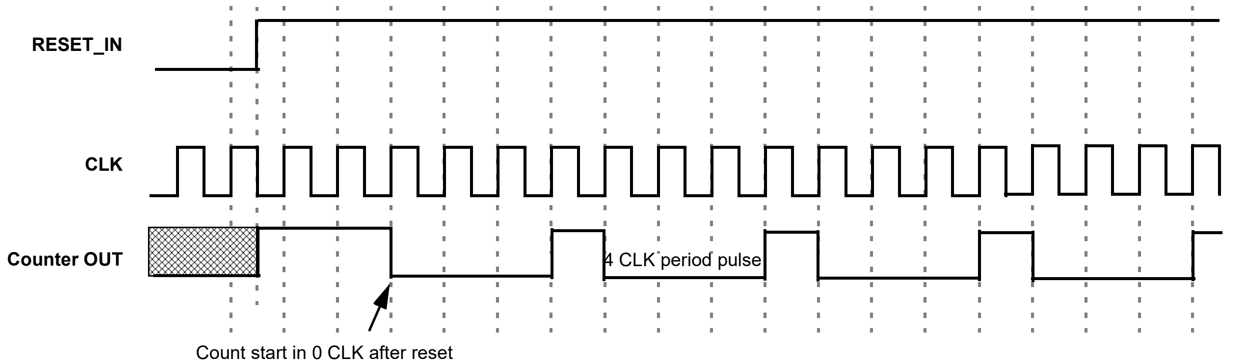


Figure 42: Counter Mode Timing Diagram with Two DFFs Synced Up

8.3.3 One-Shot Mode CNT/DLY0 to CNT/DLY6

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width is determined by counter data and clock selection properties.

The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

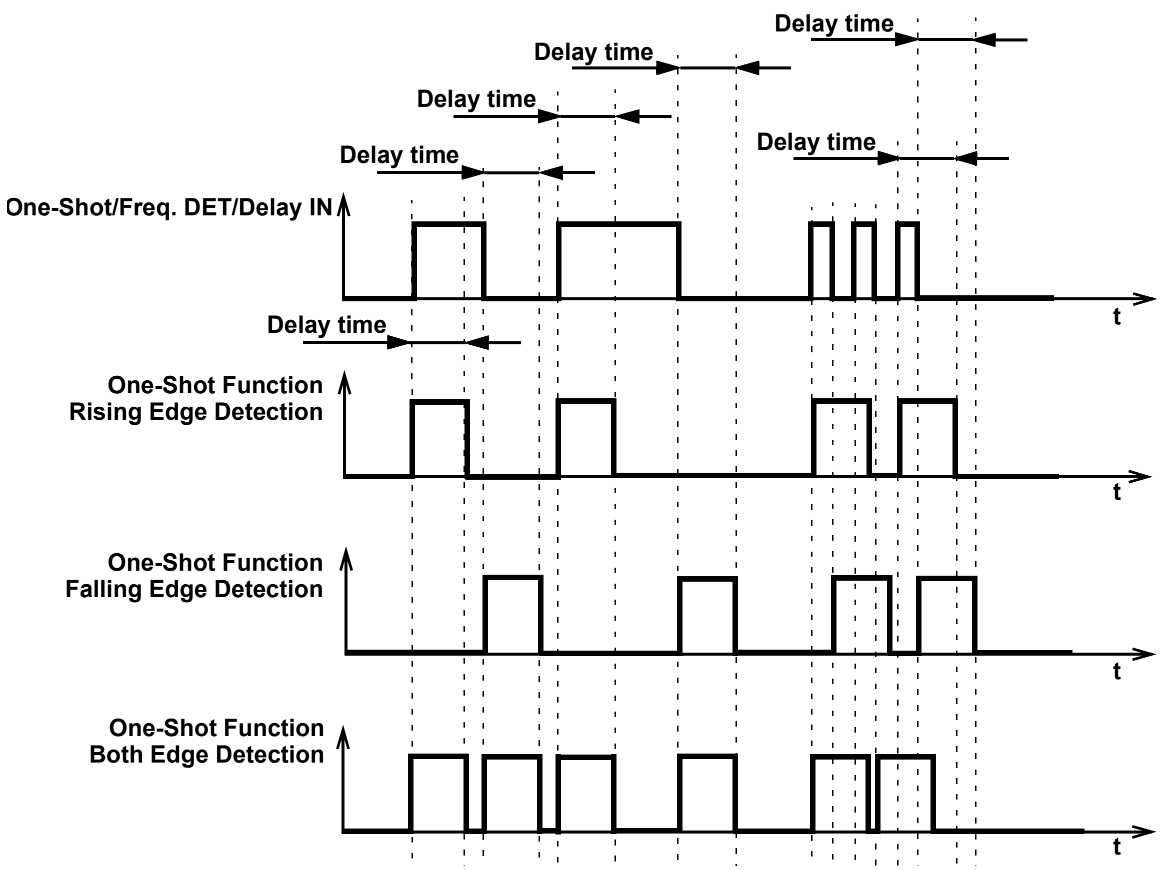


Figure 43: One-Shot Function Timing Diagram

This macrocell generates a high level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is high.

8.3.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY6

Rising Edge: The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

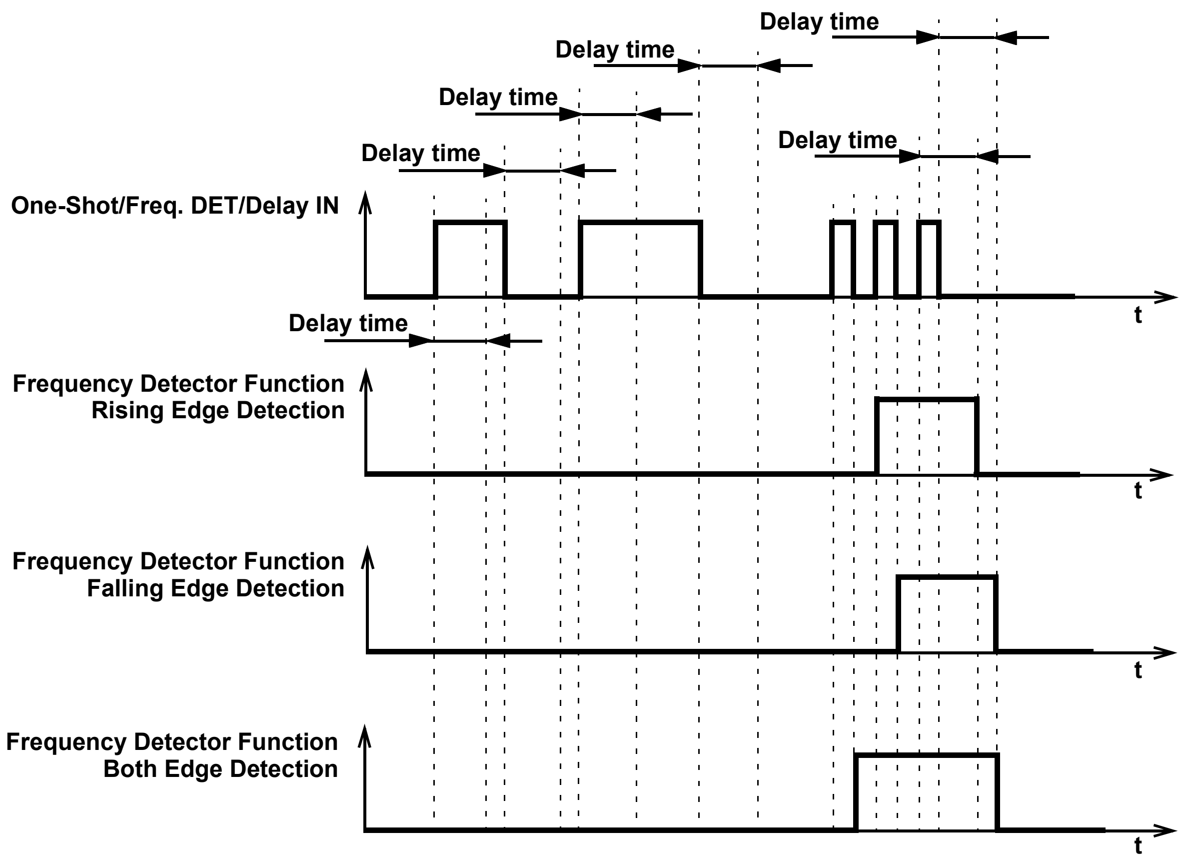


Figure 44: Frequency Detection Mode Timing Diagram

8.3.5 Edge Detection Mode CNT/DLY1 to CNT/DLY6

The macrocell generates high level short pulse when detecting the respective edge. See Table 11.

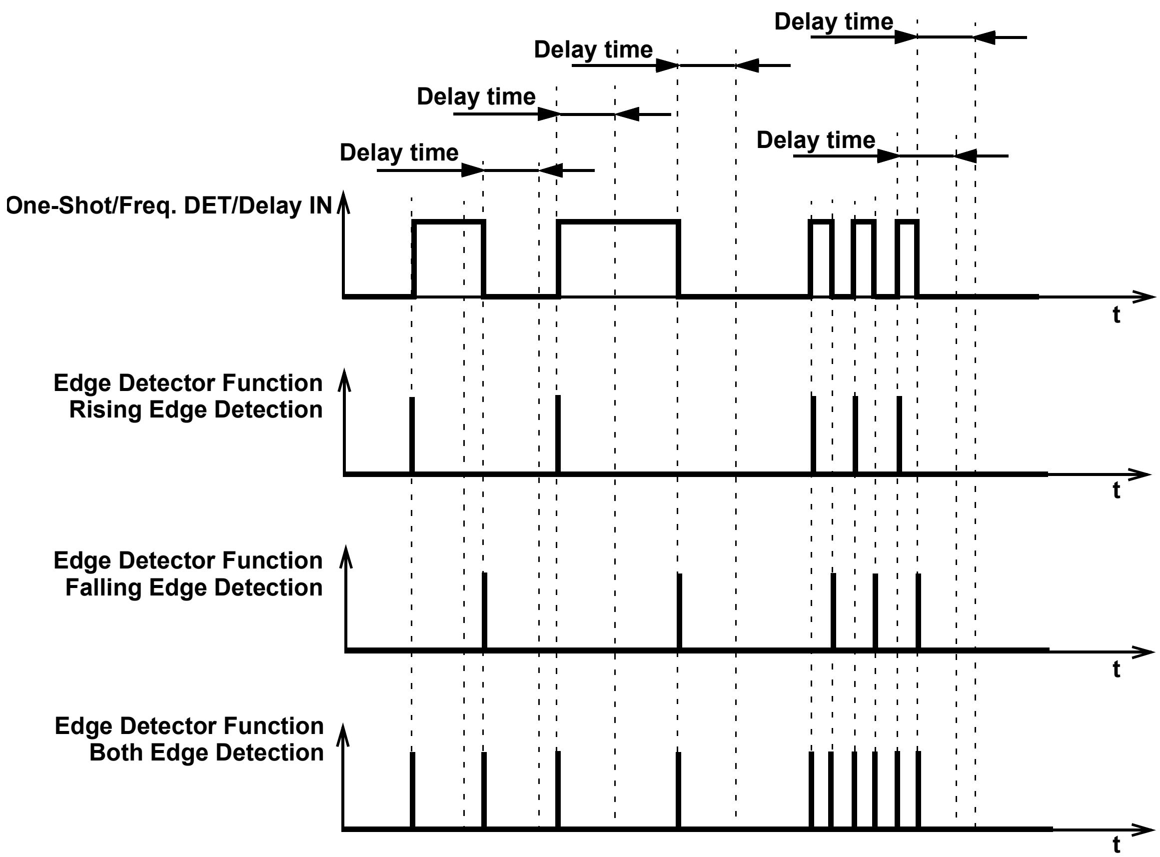


Figure 45: Edge Detection Mode Timing Diagram

8.3.6 Delayed Edge Detection Mode CNT/DLY0 to CNT/DLY6

In Delayed Edge Detection Mode, High-level short pulses are generated on the macrocell output after the configured delay time, if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated.

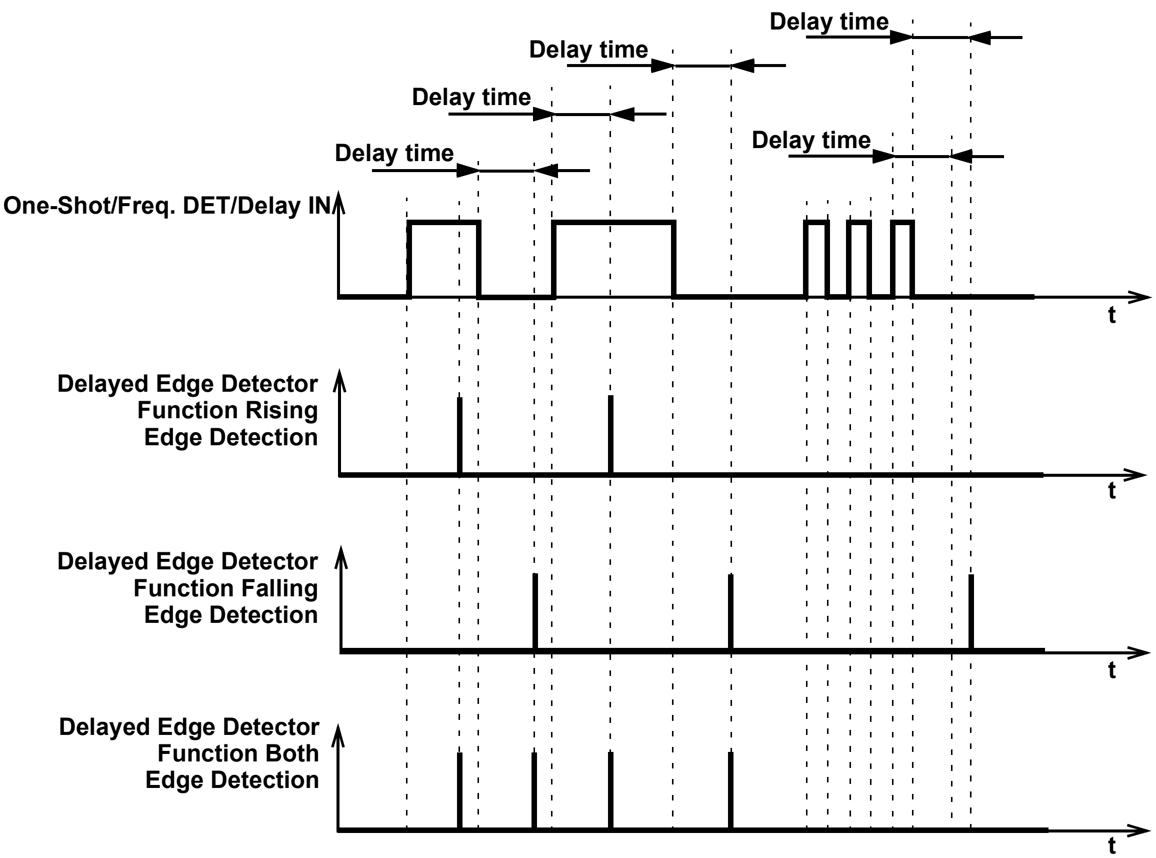


Figure 46: Delayed Edge Detection Mode Timing Diagram

8.3.7 CNT/FSM Mode CNT/DLY0

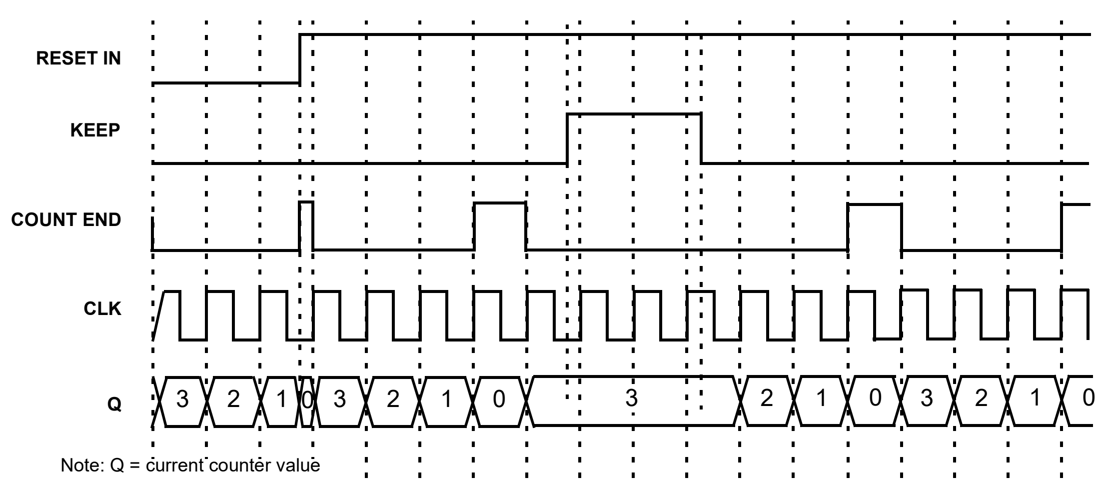


Figure 47: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

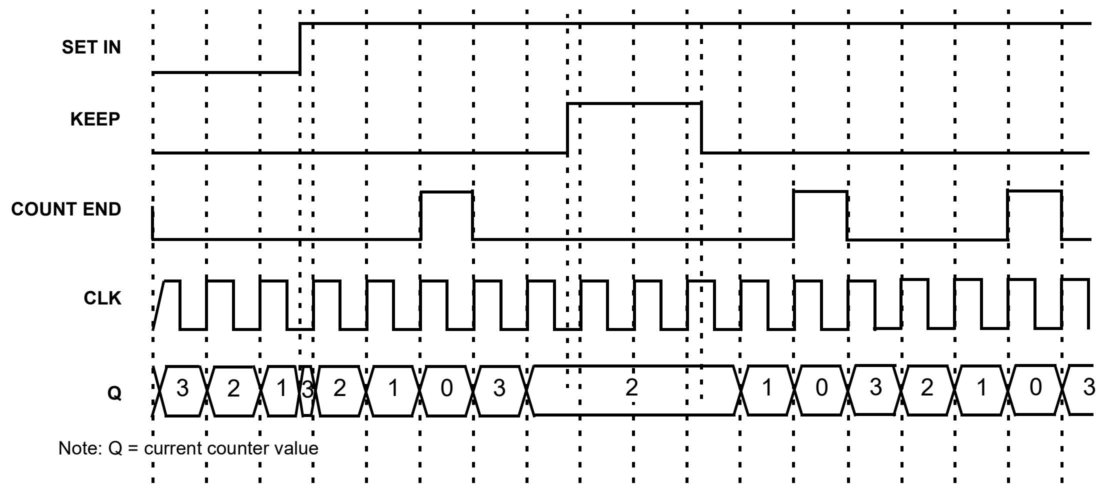


Figure 48: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

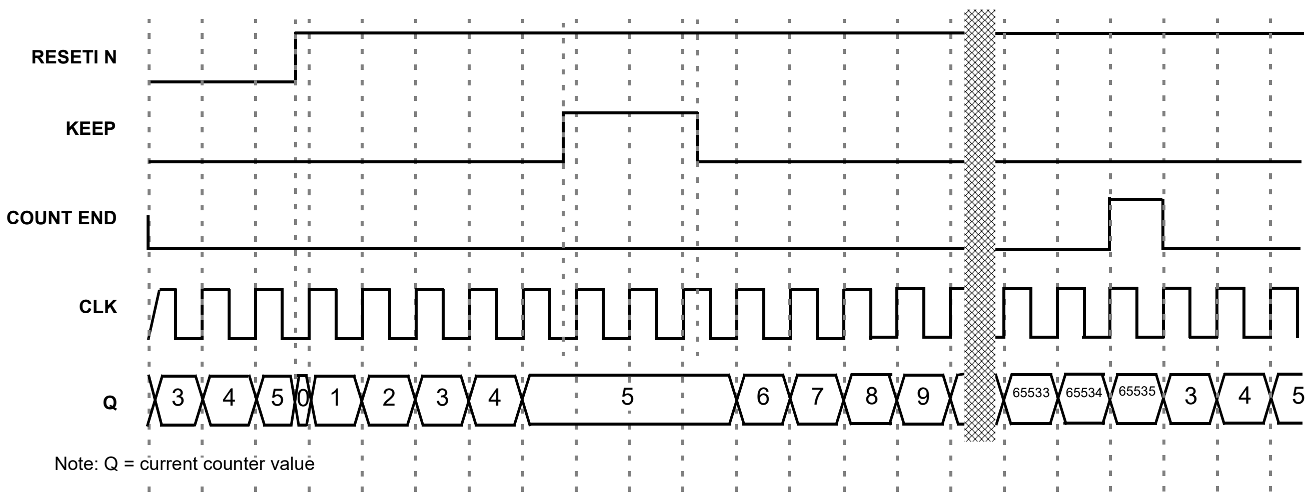


Figure 49: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3

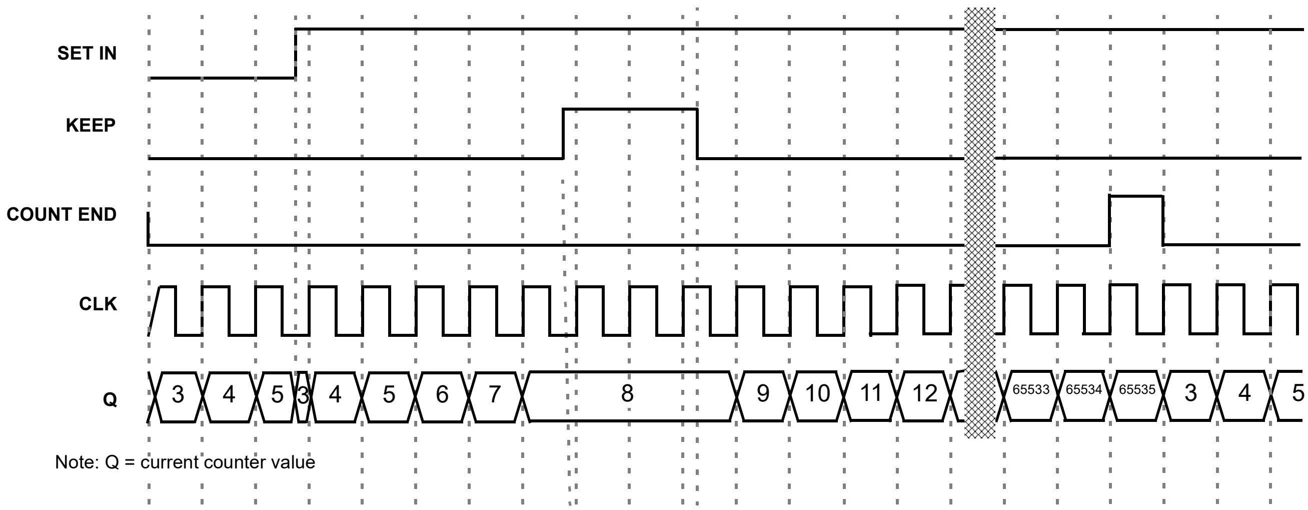


Figure 50: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3

8.3.8 Difference in Counter Value for Counter, Delay, One-Shot, and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. Compared to Counter mode, in Delay/One-Shot/Frequency Detect modes the counter value is shifted for two rising edges of the clock signal. See Figure 51.

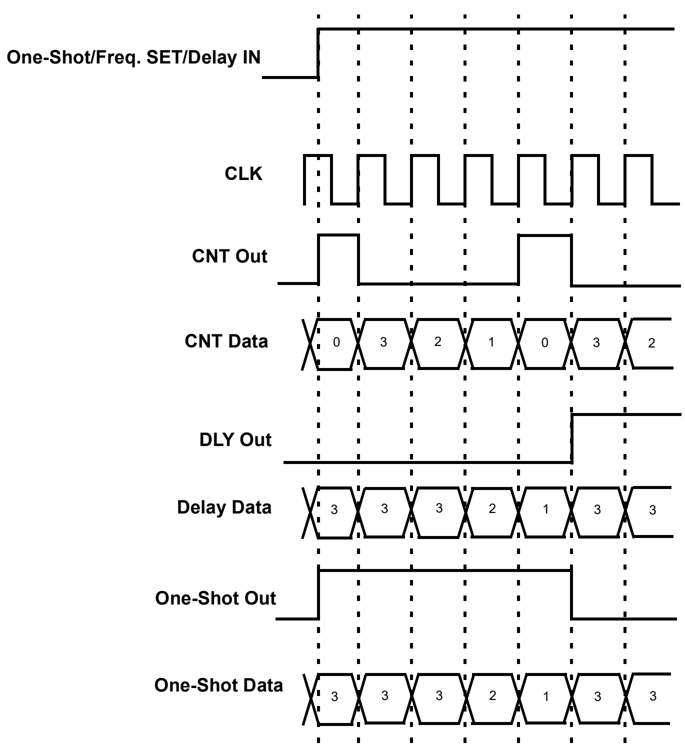


Figure 51: Counter Value, Counter Data = 3

8.4 WAKE AND SLEEP CONTROLLER

The SLG47004 has a Wake and Sleep (WS) function for ACMP. The macrocell CNT/DLY0 can be reconfigured for this purpose registers [1224:1223] = 11 and register [1232] = 1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 16-bit counter.

Note 1: BG/Analog_Good time is long and should be considered in the wake and sleep timing in case it dynamically powers on/off.

Note 2: Wake time should be long enough to make sure ACMP and Vref have enough time to get a sample before going to sleep.

Note 3: ACMPs power up must be connected to POR.

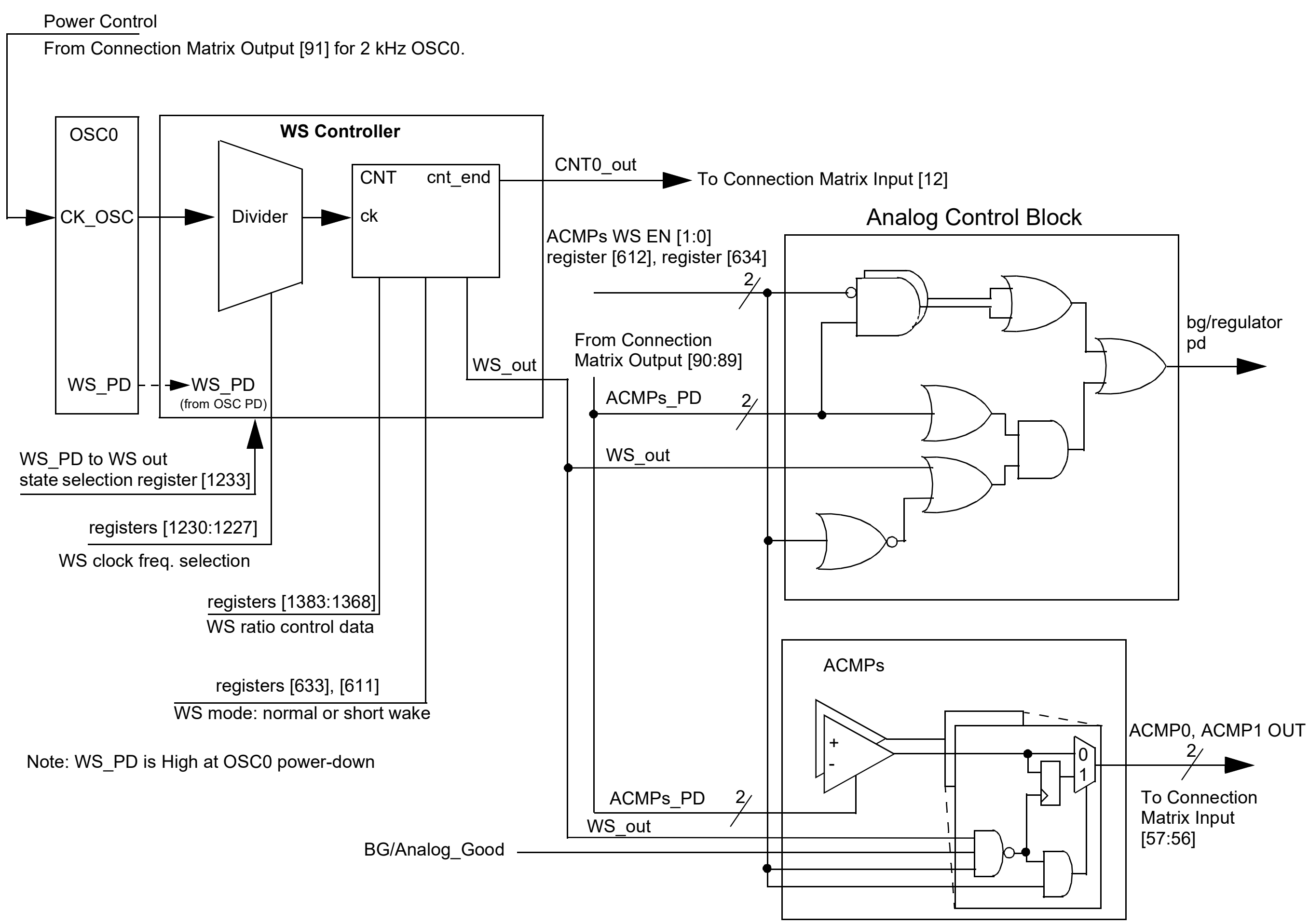


Figure 52: Wake and Sleep Controller

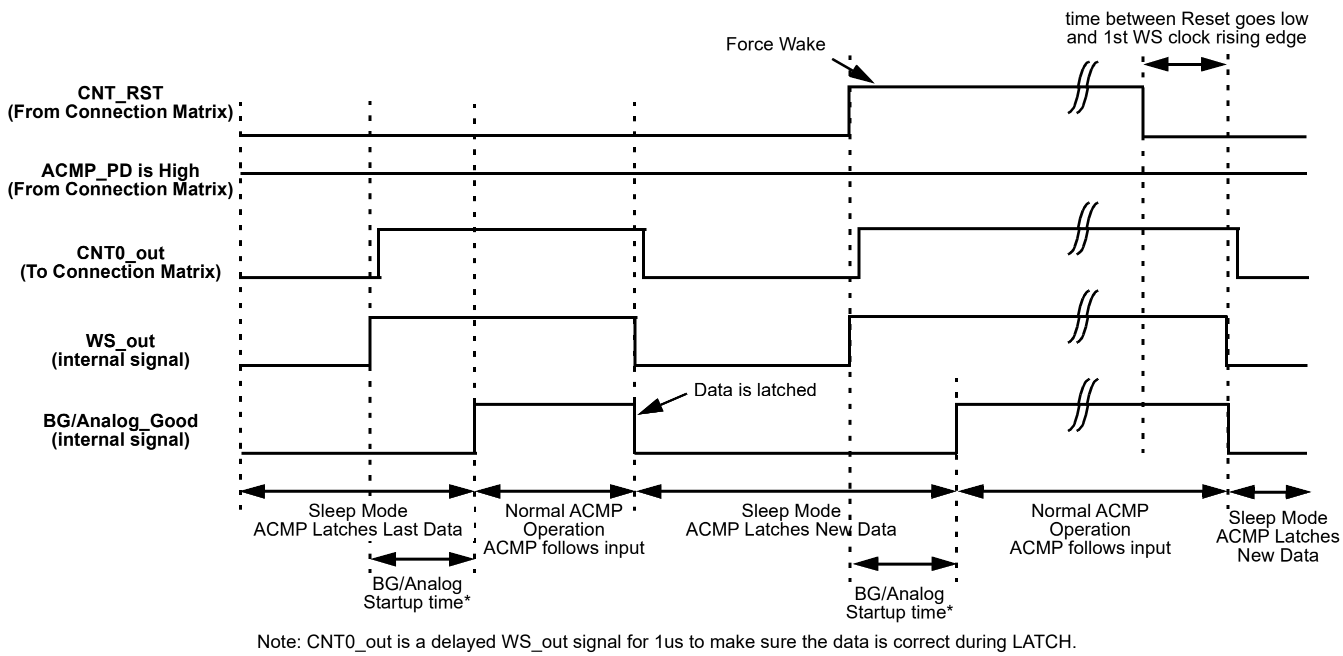


Figure 53: Wake and Sleep Timing Diagram, Normal Wake Mode, Counter Reset is Used

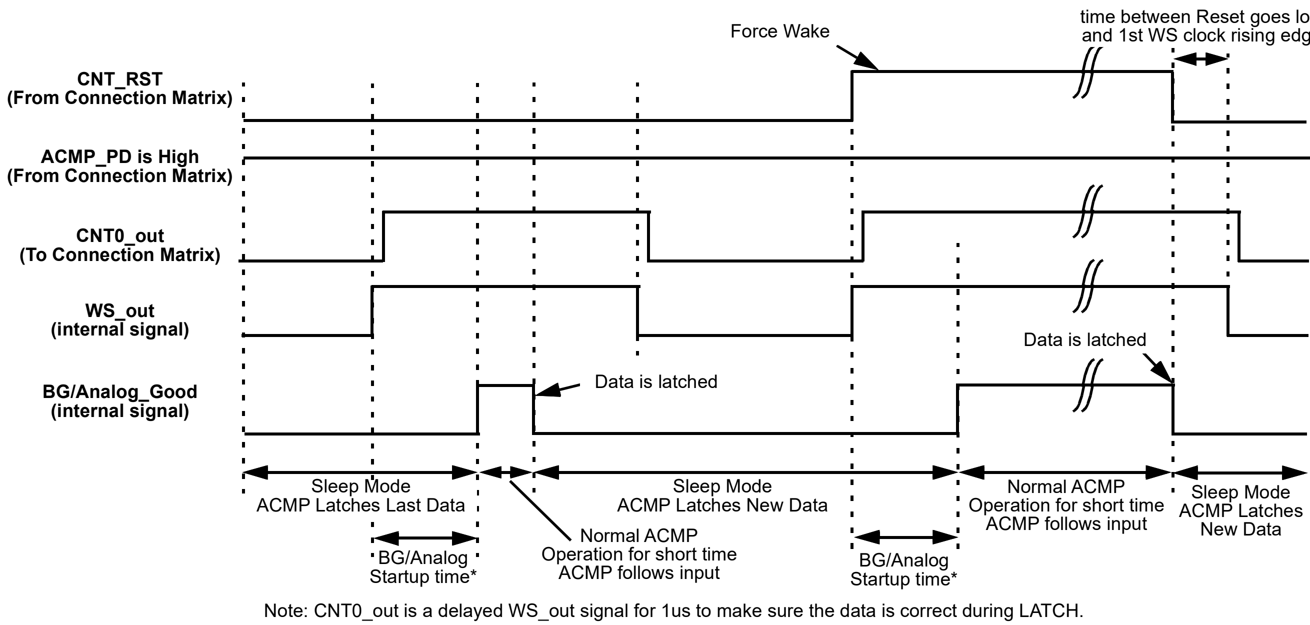
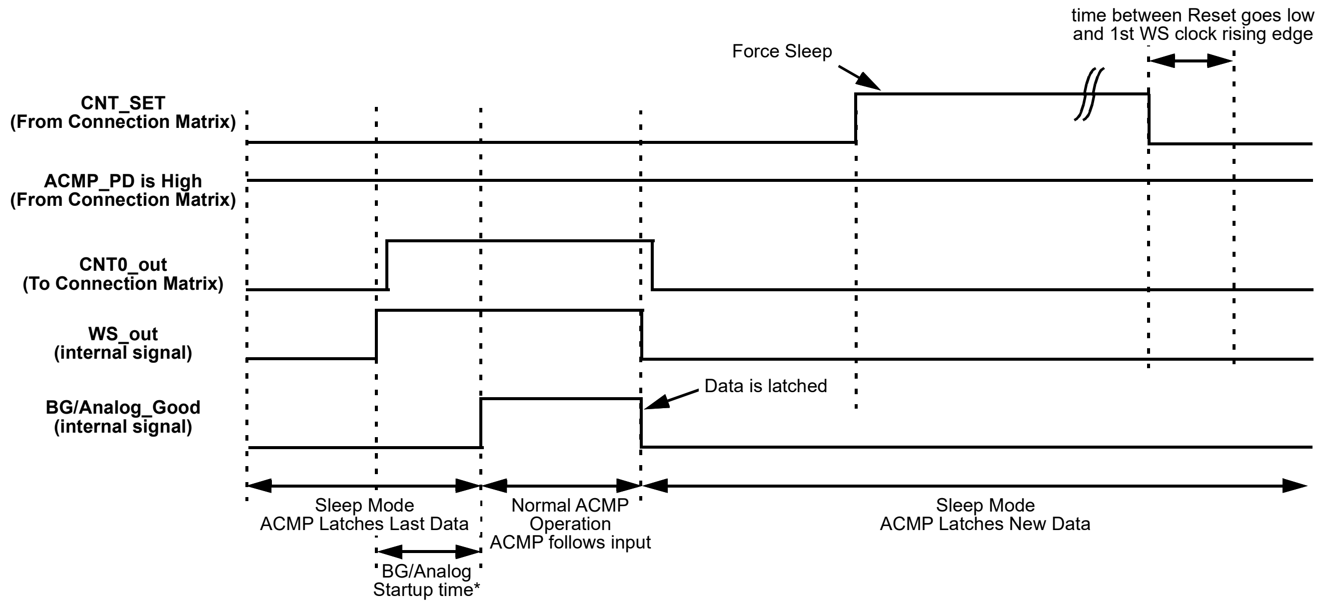
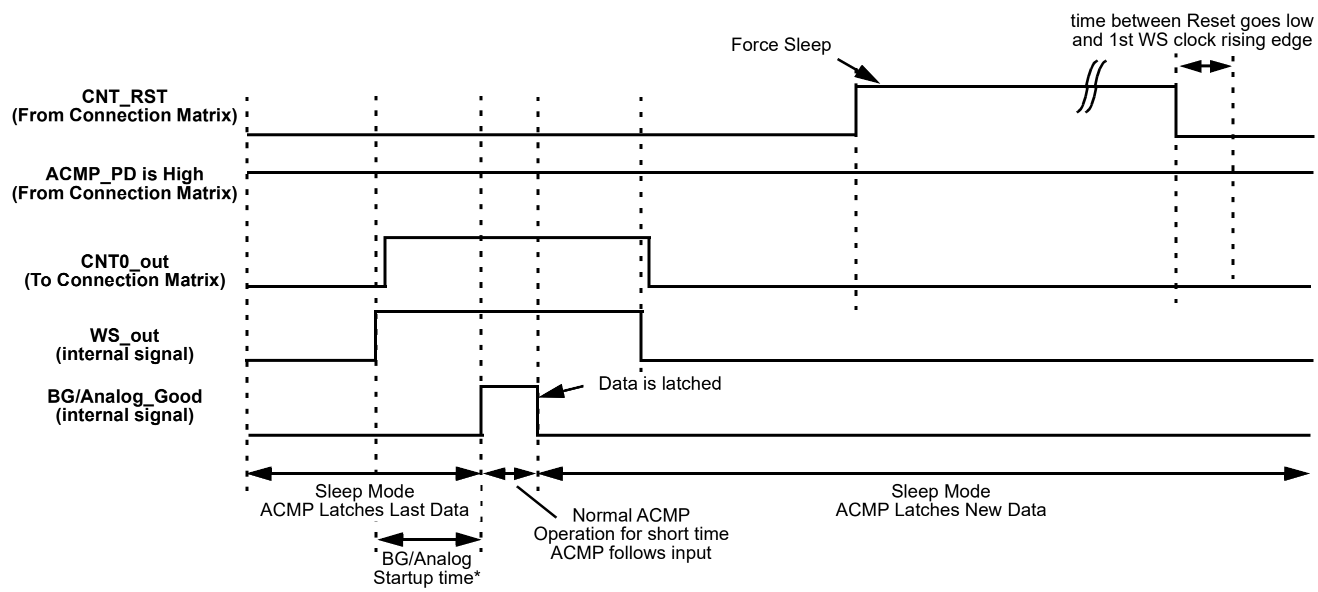


Figure 54: Wake and Sleep Timing Diagram, Short Wake Mode, Counter Reset is Used



Note: CNT0_out is a delayed WS_out signal for 1 us to make sure the data is correct during LATCH.

Figure 55: Wake and Sleep Timing Diagram, Normal Wake Mode, Counter Set is Used



Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during LATCH.

Figure 56: Wake and Sleep Timing Diagram, Short Wake Mode, Counter Set is Used

Note: If low power BG is powered on/off by WS, the wake time should be longer than 2.1 ms. The BG/analog start up time will take maximal 2 ms. If low power BG is always on, OSC0 period is longer than required wake time. The short wake mode can be used to reduce the current consumption. The short wake mode is edge triggered, when the wake signal is latched by rising edge and released the Power-On signal after the ACMP output data is latched. This allows to have a valid ACMP data for any type of wake signal and have the optimized current consumption.

To use any ACMP under WS controller, the following settings must be done:

- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMPs);
- Register WS => enable (for each ACMP separately);
- CNT/DLY0 set/reset input = 0 (for all ACMPs).

As the OSC any oscillator with any pre-divider can be used. The user can select a period of time while the ACMP is sleeping in a range of 1 - 65535 clock cycles. Before they are sent to sleep their outputs are latched, so the ACMPs remain their state (High or Low) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low)
  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = High, the ACMP is continuously on.
  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = Low, the ACMP is continuously off.
  Both cases WS function is turned off.

- Counter Data (Range: 1 to 65535)
  User can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.

- Q mode - defines the state of WS counter data when Set/Reset signal appears Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn on the ACMPs. When Reset signal goes out, the WS counter will go Low and turn off the ACMPs until the counter counts up to the end. Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn off the ACMPs. When Set signal goes out, the WS counter will go on counting and High level signal will turn on the ACMPs while counter is counting up to the end.

Note: The OSC0 matrix power down to control ACMP WS is not supported for short wait time option.

- Edge Select defines the edge for Q mode
  High level Set/Reset - switches mode Set/Reset when level is High

Note: Q mode operates only in case of "High Level Set/Reset".

- Wake time selection - time required for wake signal to turn the ACMPs on

  Normal Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on until WS signal is Low again. Wake time is one clock period. It should be longer than BG turn on time and minimal required comparing time of the ACMP.

  Short Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on for 1 μs and turn off regardless of WS signal. The WS signal width does not matter.
- Keep - pauses counting while Keep = 1
- Up - reverses counting

  If Up = 1, CNT is counting up from user selected value to 65535.

  If Up = 0, CNT is counting down from user selected value to 0.

9 Analog Comparators

9.1 ANALOG COMPARATORS OVERVIEW

There are two Low Power Rail-to-Rail General Purpose Analog Comparators (ACMP) macrocells in the SLG47004. For the ACMP macrocells to be used in a GreenPAK design, the power-up signals (ACMP0_L_pdb and ACMP1_L_pdb) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be ON continuously, OFF continuously, or switched on periodically, based on a digital signal coming from the Connection Matrix. When ACMP is powered down, its output is low. Two General Purpose Analog Comparators are optimized for low power operation.

Each of the General Purpose ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage (1x, 0.5x, 0.33x, 0.25x) before connection to the analog comparator. The gain divider is unbuffered and has an input resistance of 2 MΩ (typ) for 0.5x, 0.33x, 0.25x, and 10 GΩ for 1x. Each of the General Purpose ACMP macrocells has a negative input signal that is either created from an internal Vref or provided by any external source (from external pins). Note that the external Vref signal is filtered with a 2nd order low pass filter with 8 kHz typical bandwidth, see in Figure 57 and Figure 58.

Input bias current < 1 nA (typ).

PWR UP = 1 => ACMP is powered up.

PWR UP = 0 => ACMP is powered down.

Both General Purpose Analog Comparators have "Low Energy Power Up" setting (register [608] - ACMP0, register [630] - ACMP1). When enabled, it allows reducing average power consumption during ACMP power up process. This setting changes power up sequence of analog macrocells:

Low Energy Power Up register [608], register [630] = 0 - all analog macrocells associated with ACMP turns on simultaneously.

Low Energy Power Up register [608], register [630] = 1 - the first macrocell that begins to turn on is Bandgap. Other analog macrocells begin to turn on only after BG_OK signal is valid. This option slightly increases general ACMP Power-On time, while reducing the average current consumption.

During power-up, the ACMP output will remain LOW, and then becomes valid after power up signal goes high for ACMP0_L and ACMP1_L (see parameter t_{start} in Table 17).

Each cell also has a flexible hysteresis selection, to offer hysteresis of 32 steps, but not more than Vref voltage. It means that there are 6-bits to select Vref and independent 6-bits to select the hysteresis (no need to have an adder logic).

It's possible to enable low pass filter at the Vref input. But it's highly recommended to enable this LPF only when hysteresis Vhys > 196 mV.

ACMP0_L IN+ options are OA0_out, GPIOx (PIN), V_{DD}.

ACMP1_L IN+ options are OA1, GPIOx (PIN), ACMP0L_IN+, Temp Sensor OUT.

9.1.1 ACMP0L Block Diagram

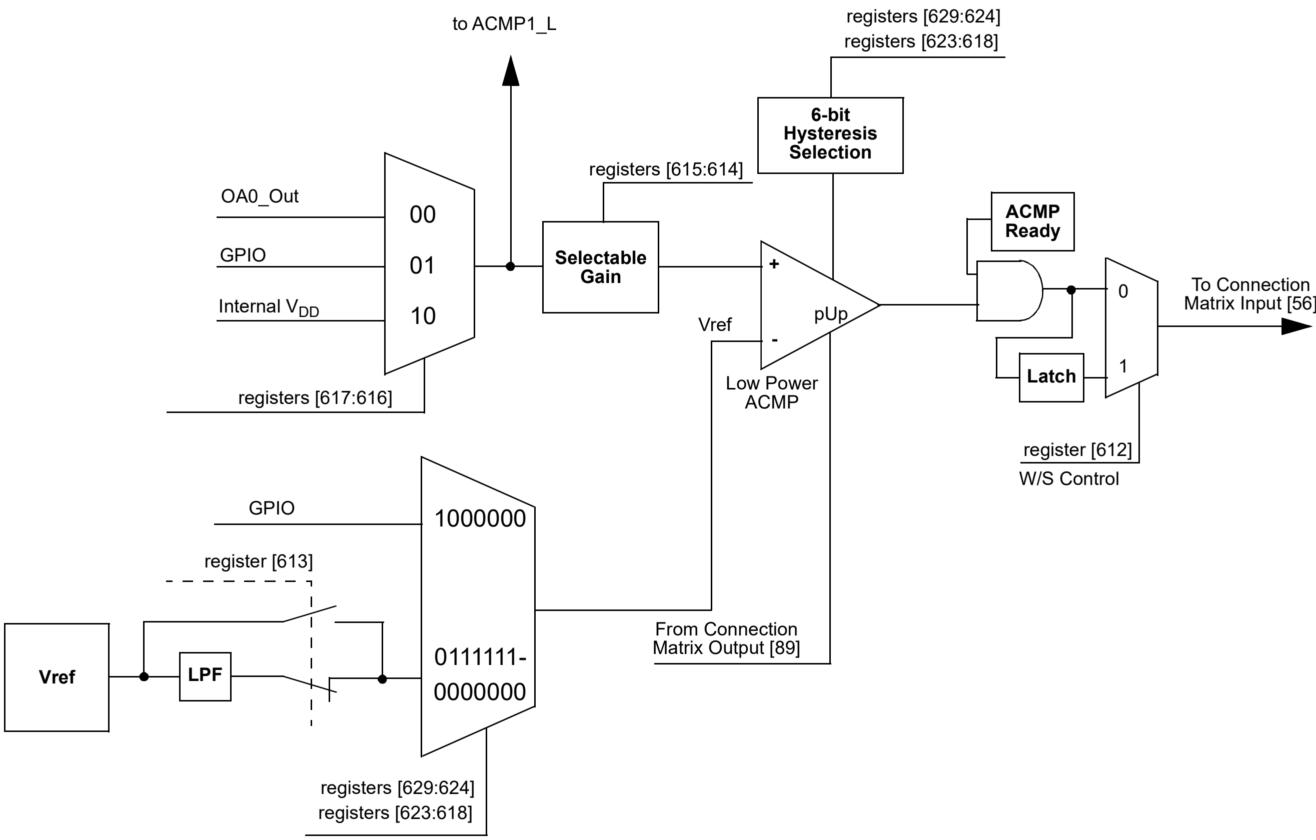


Figure 57: ACMP0L Block Diagram

9.1.2 ACMP1L Block Diagram

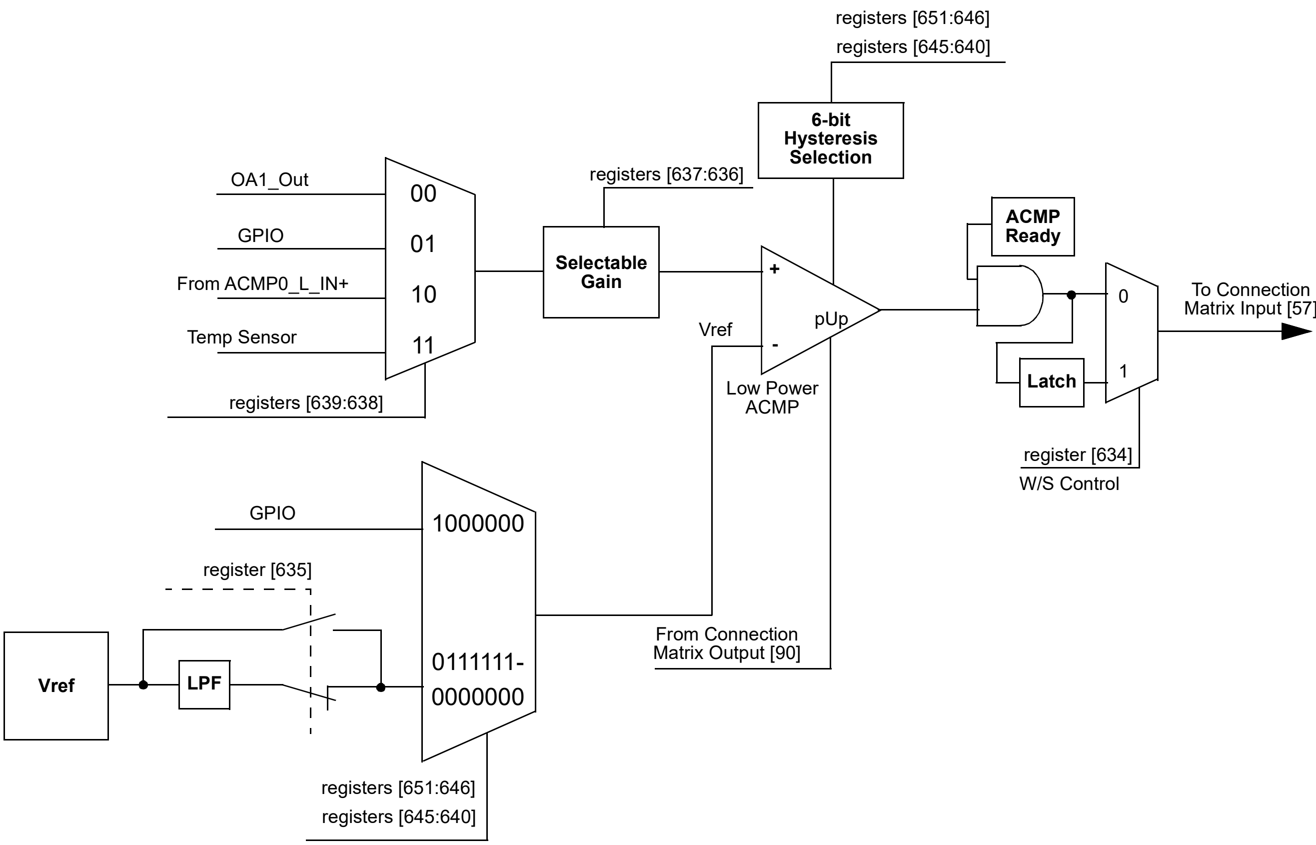


Figure 58: ACMP1L Block Diagram

9.2 CHOPPER ANALOG COMPARATOR

There is one Chopper Rail-to-Rail Analog Comparator (ACMP) macrocells in the SLG47004. It is possible to use Chopper ACMP to do in system trim by changing the Rheostat resistance in Auto-Trim mode. It is also possible to use a Chopper ACMP as a general purpose analog comparator.

The chopper ACMP power up signal is controlled either by internal Auto-Trim logic (Set 0/1 of Digital Rheostat 0/1) or by matrix input.

The chopper ACMP is automatically powered on during the calibration time to control the up/down signal of the counter/rheostat, when the Auto-Trim is enabled (register [909]= 0).

In order to use Chopper ACMP as a standalone comparator (Auto-Trim mode is disabled, register [909] = 1) user should provide the clock signal to this macrocell. Clock source can be internal oscillators or any pulses from the connection matrix.

Note that clock frequency for the Chopper ACMP shouldn't be greater than f_{ChACMP}. Please refer to Table 24.

For proper Chopper ACMP operation it is recommended to force the bandgap on. It's highly recommended to force the bandgap on when OSC1 is used as a clock source for Chopper ACMP. Also, if Vref (bandgap) is used in the project, internal Vref should be stable before the 2nd rising edge of Chopper ACMP clock signal (see Figure 59). Please consider the bandgap turn on delay (approximately 1 ms).

Output of Chopper ACMP can be optionally inverted by register [882].

The matrix output [85] is used to control chopper ACMP power up signal for the general purpose usage, see Figure 59. It is possible to use the chopper ACMP as a general purpose ACMP after Auto-Trim procedure is completed, since the power up signal is a logic OR of the latched Set (Digital Rheostat 0/1) signal and matrix signal. If Auto-Trim (Set 0/1 of Digital Rheostat 0/1) is disabled and chopper ACMP channel is set to Auto (Channel 0/1), then ACMP output defaults to Channel 0 while Channel 1 is ignored.

The power-up signals need to be active high in order to use the Chopper ACMP. By connecting to signals coming from the Connection Matrix, it is possible to have ACMP be ON continuously, OFF continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, its output is low.

There are no Gain and Hysteresis selection for chopper ACMP compared to the ACMP0L and ACMP1L.

It's possible to select different reference sources for Chopper ACMP. It can be:

- external voltage from pin;
- divided internal voltage from internal reference source (from 32 mV to 2048 mV);
- divided internal reference voltage from HD Buffer (64 steps);
- divided V_{DDA} voltage (64 steps).

For more information see Section 15.

The positive input of the Chopper ACMP can be connected to the Op Amp0 out or Op Amp1 out or In Amp out, or to the external PIN.

The inputs of Chopper ACMP can be reconfigured while operating in AutoTrim mode. There is one configuration of inputs (Figure 59) for case when Set0 (Digital Rheostat 0) signal is latched, and another configuration of Chopper ACMP inputs when Set1 (Digital Rheostat 1) signal is latched. For example, M1 MUX can be configured to operate with In Amp out when Set0 (Digital Rheostat 0) is latched and Chopper_ACMP+ pin when Set1 (Digital Rheostat 1) is latched. The same way, “-” input of Chopper ACMP can be configured to work with any of possible inputs when Set0 (Digital Rheostat 0) or Set1 (Digital Rheostat 1) are latched.

Note that the default configuration is the configuration for Set0 (Digital Rheostat 0) signal. When Chopper ACMP operates as separate ACMP and AutoTrim function is disabled, inputs of Chopper ACMP are defined by registers [893:892].

Note that Chopper ACMP will automatically enable HD Buffer if HD Buffer is selected as a source for Chopper ACMP In-signal (register 946 = 0) and Chopper ACMP is powered up.

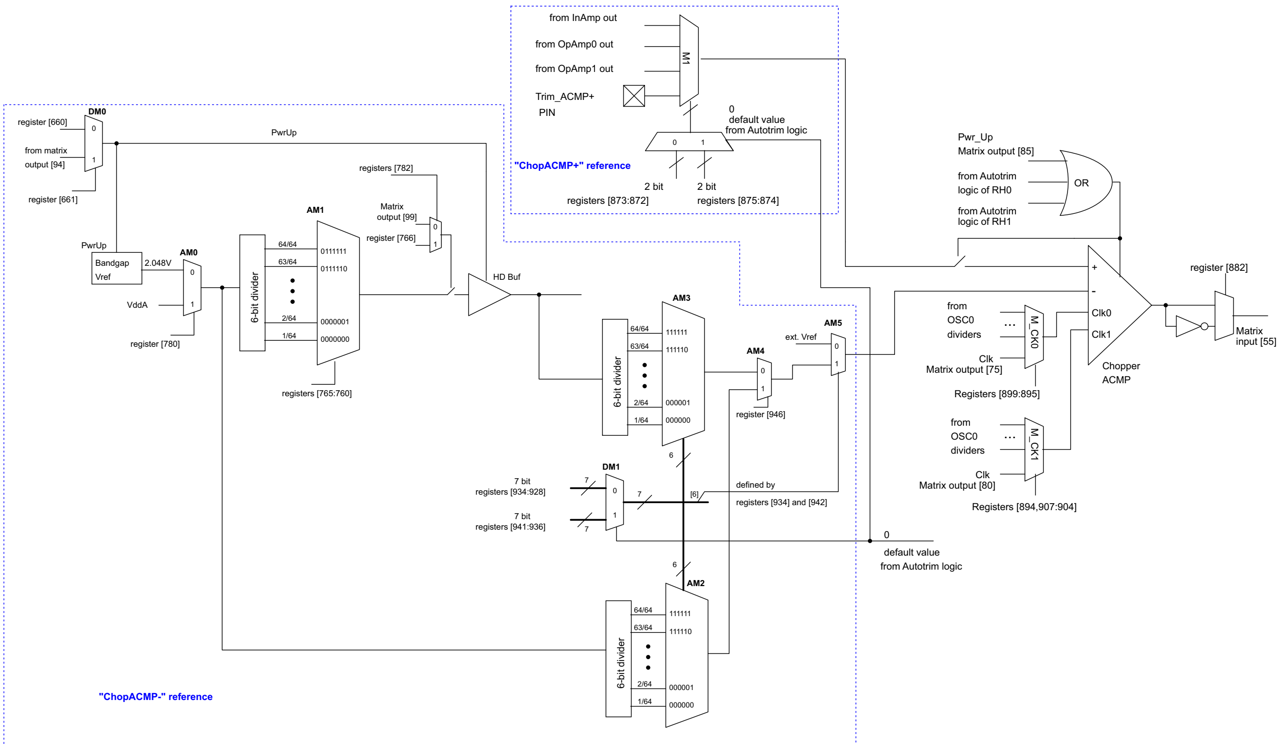


Figure 59: Chopper ACMP Block Diagram

9.3 ACMP SAMPLING MODE

Both General Purpose Analog Comparators (ACMPL0 and ACMPL1) have an optional sampling mode. In this mode, ACMP is enabled for the shortest amount of time after rising edge at Power Up input to get a valid data. Then ACMP latches its value and goes sleep again.

Registers [610], [632] enable sampling mode for two comparators.

9.4 ACMP TYPICAL PERFORMANCE

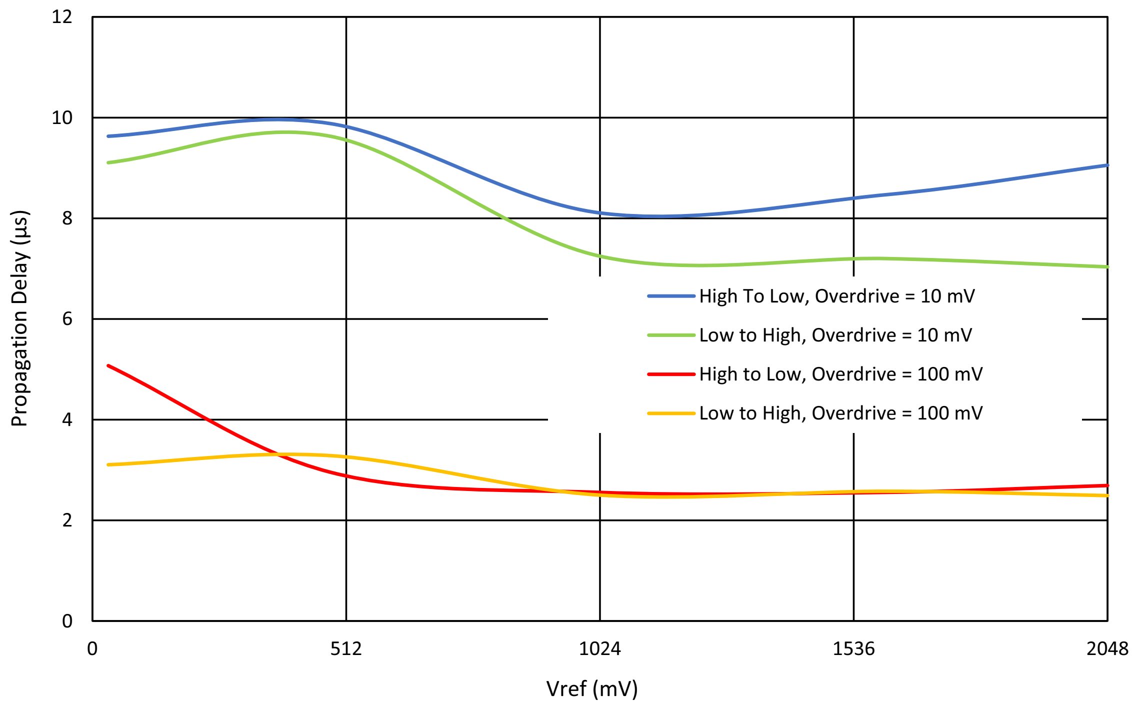


Figure 60: Propagation Delay vs. Vref for ACMPx at T = 25 °C, V_{DD} = 2.4 V to 5.5 V, Hysteresis = 0

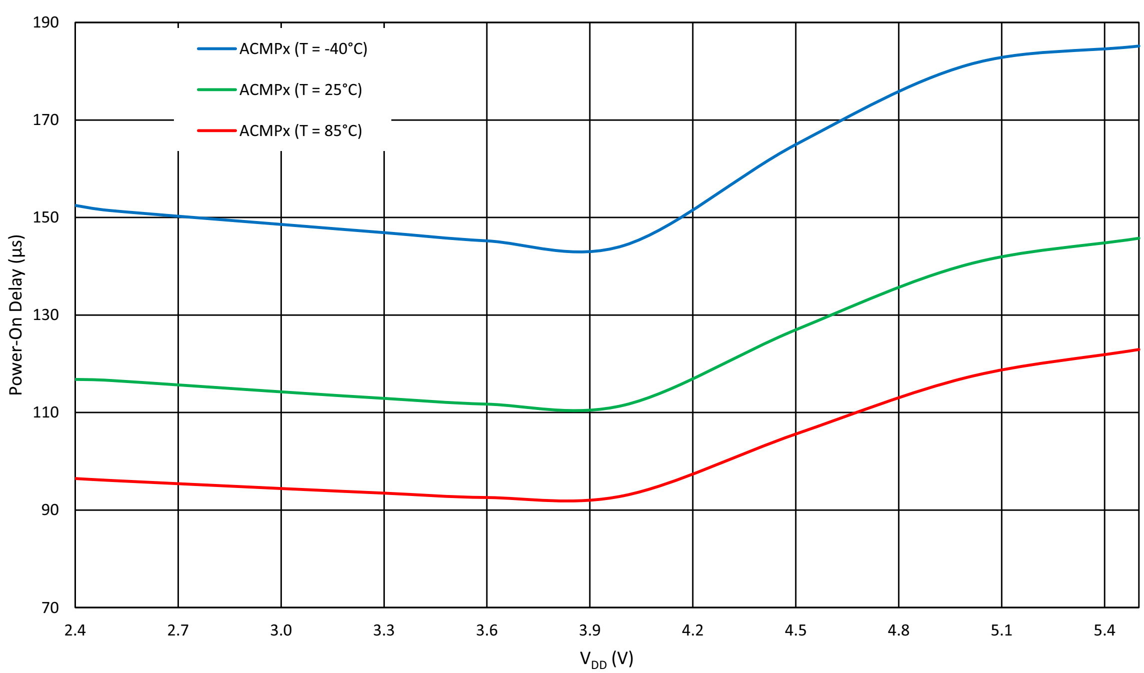


Figure 61: ACMPx Power-On Delay vs. V_{DD} at BG - Forced

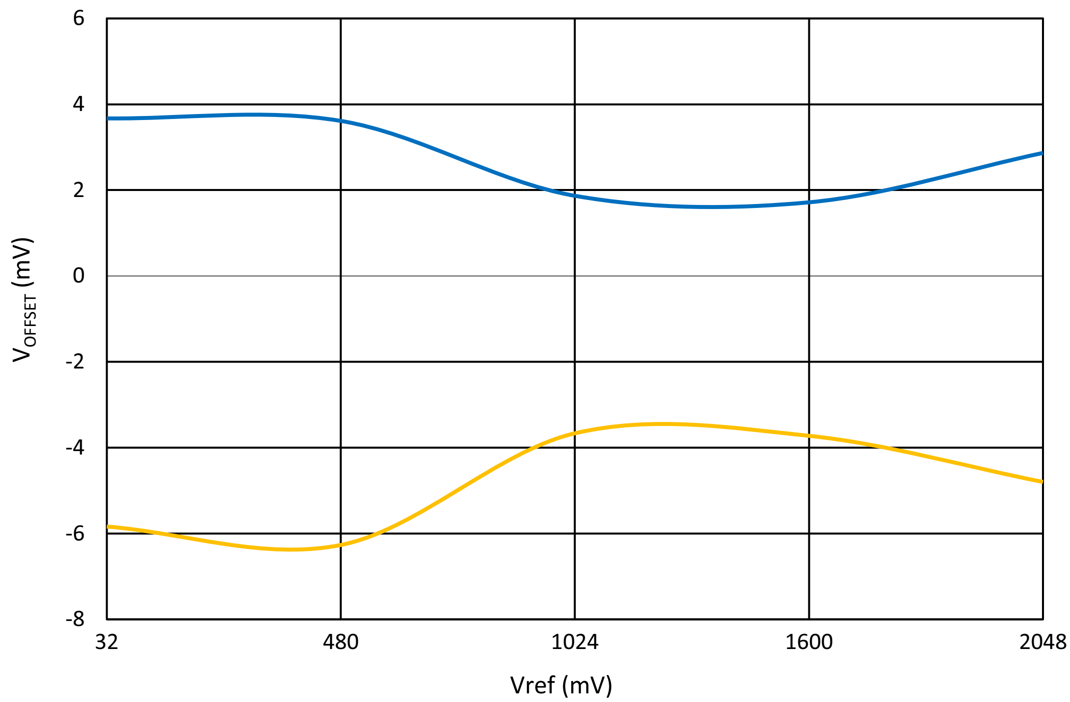


Figure 62: ACMPx Input Offset Voltage vs. Vref at T = -40 °C to 85 °C, V_{DD} = 2.4 V to 5.5 V, Gain = 1

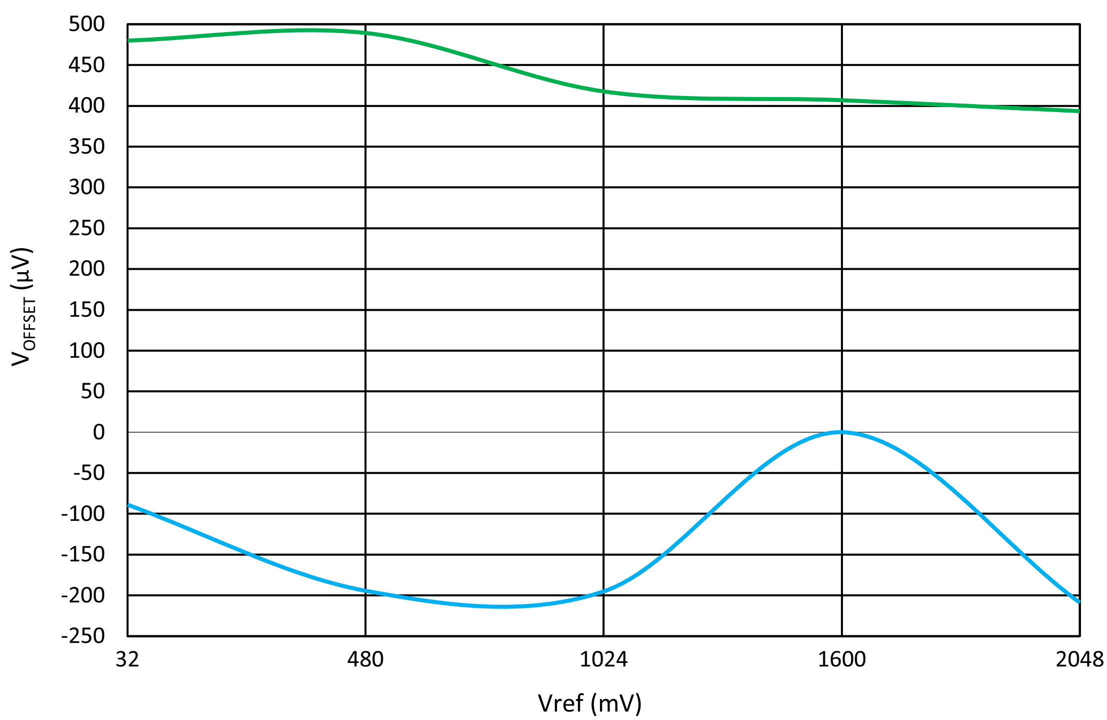


Figure 63: Chopper ACMP Input Offset Voltage vs. Vref at T = -40 °C to 85 °C, V_{DD} = 2.4 V to 5.5 V, Gain = 1

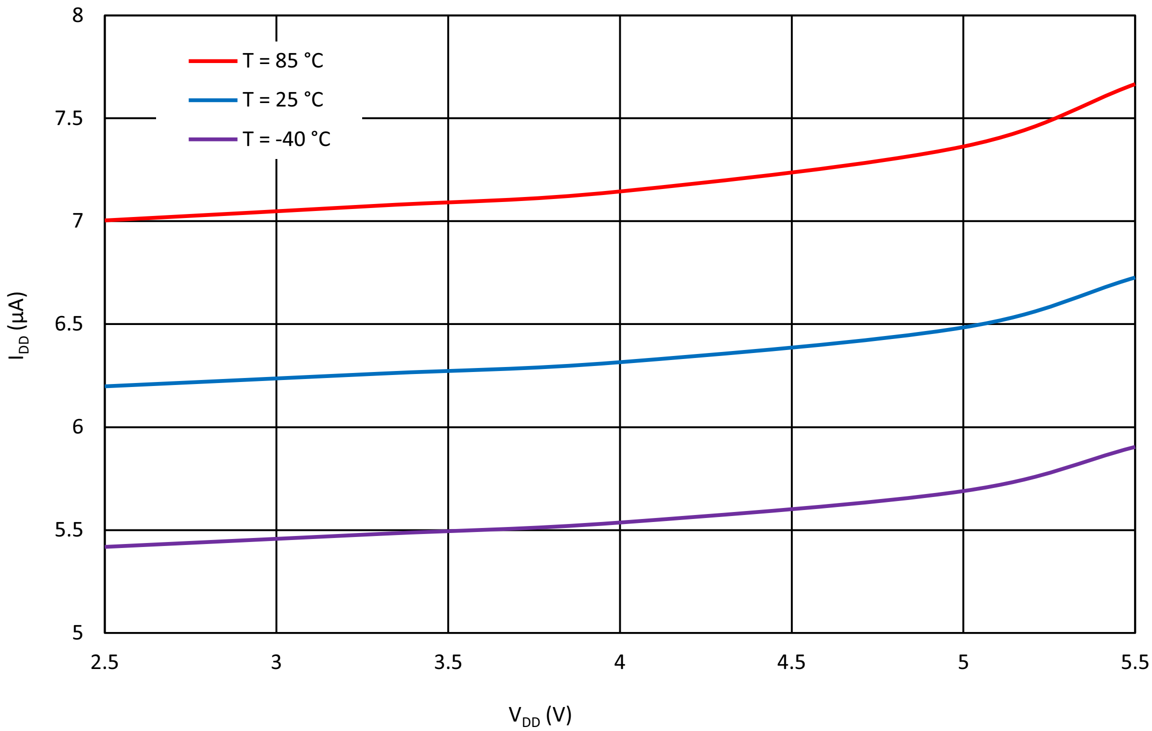


Figure 64: ACMPx Current Consumption vs. V_{DD}

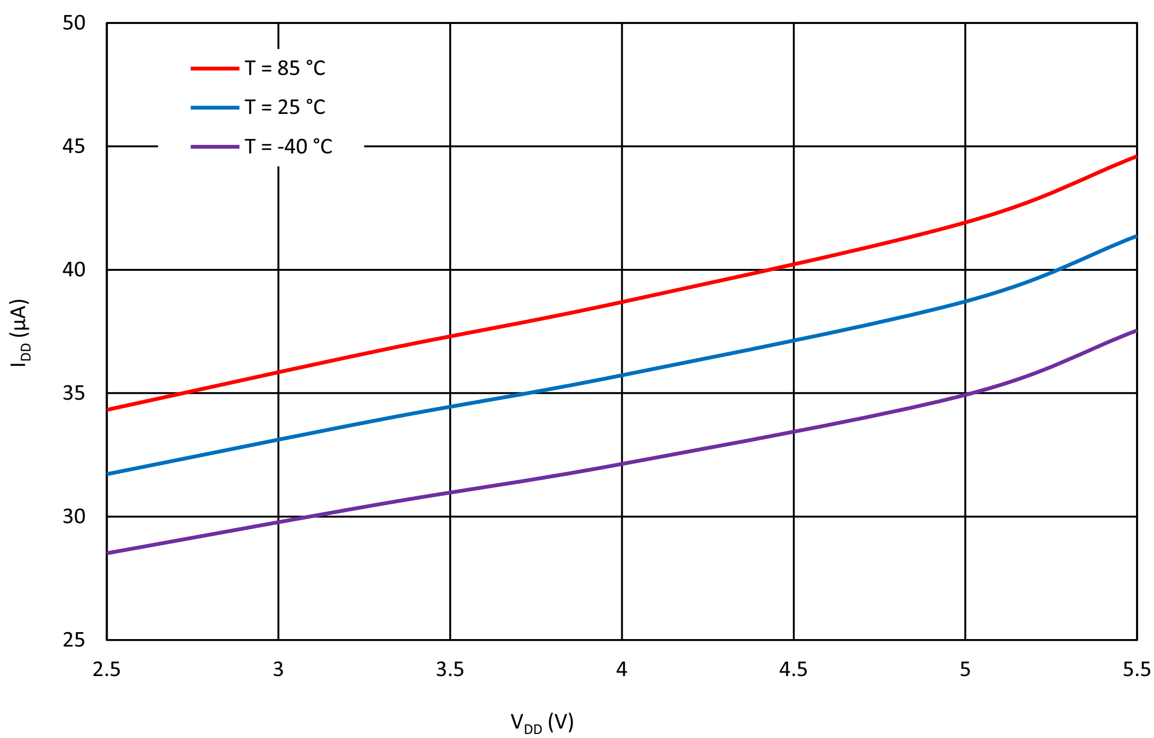


Figure 65: Chopper ACMP Current Consumption vs. V_{DD} (with 2.048 kHz Clock)

10 Programmable Operational Amplifiers

10.1 GENERAL DESCRIPTION

The SLG47004 contains three operational amplifiers with rail-to-rail input and output. Two of them (Programmable Op Amps) have the additional functions of driving internal analog FETs (Voltage Regulator and Current Sink modes) and Comparator mode. The third Internal Op Amp is an amplifier with internal resistors, and can be configured as a difference amplifier with Gain = 1. All three op amps can function as instrumentation amplifiers. The structures of the op amps are shown in Figure 66 and Figure 67.

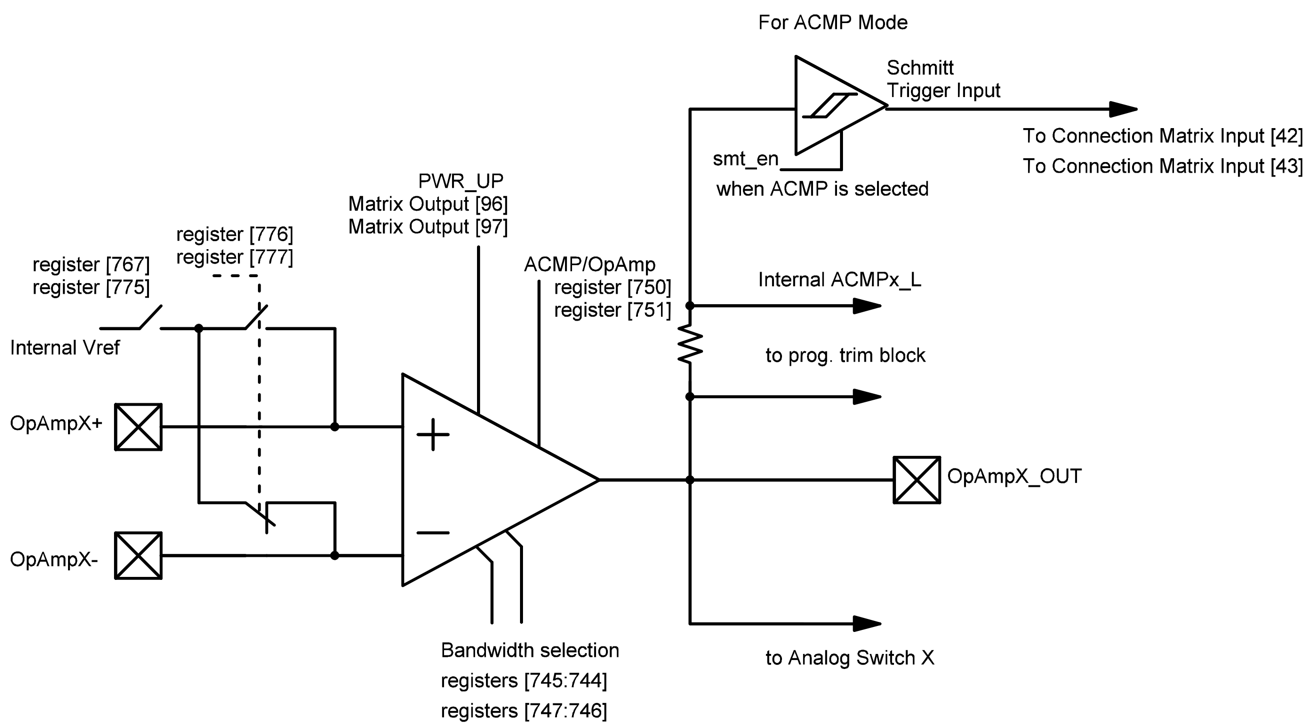


Figure 66: Programmable Operational Amplifier OA0, OA1 Internal Circuit

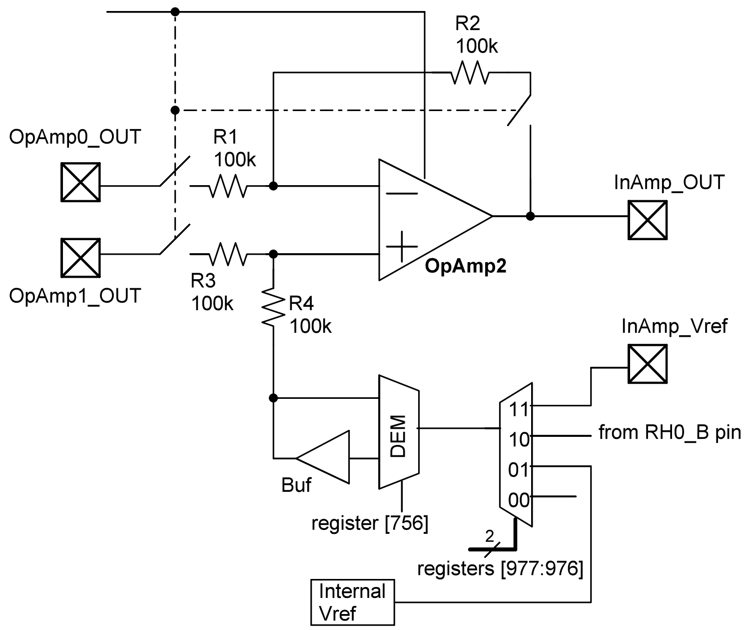


Figure 67: Internal Operational Amplifier Circuit

Each of the two Programmable Op Amp inputs has a hardware connection to the external pin and an optional connection to the internal voltage reference source, which makes it possible to create precise voltage or current source. For more detailed description of op amp Vref sources see Section 15. The output of the operational amplifier is hardwired to an external pin. This output can also be connected to the Programmable Trim block of rheostat macrocell, ACMP non-inverting input (ACMP0_L+ for OA0, ACMP1_L+ for OA1), or control the corresponding Analog Switch, depending on the mode of operation. Each Programmable Op Amp can also be configured as an analog comparator, in which case its output signal is connected to the Connection Matrix through a dedicated buffer.

Each Programmable Op Amp has a programmable bandwidth that can be set by two register bits. In addition, internal charge pump setting for each Op Amp must be changed according to bandwidth selection, see Table 55.

Internal charge pump can be disabled if input common-mode voltage V_{CM} < (V_{DDA} - 1.5 V). But it is strongly recommended to keep the default setting (enable charge pump).

The bandwidths may vary up to +/-30 % over PVT. Each operational amplifier is factory trimmed. This trimming is independent of the trimming associated with the onboard digital rheostat (system calibration).

The Internal operational amplifier shares its inputs with the Programmable Op Amps outputs. The voltage reference for the internal amplifier can be sourced from either the internal or external Vref. Note that if the internal Vref is used as a source for the instrumentation amplifier Vref, the user can optionally connect this Vref to the output pin, or disconnect the Vref from output pin and use this pin as GPIO.

Also, if the Internal Op Amp is inactive (In Amp Mode is disabled), the user can use the In Amp_Vref pin as GPIO. The In Amp_Out pin can be configured as GPI.

Table 55: Op Amp Bandwidth Settings

Op Amp Bandwidth Selection	Op Amp0				Op Amp1				Op Amp2 (Internal)			
	Bandwidth Selection		Charge Pump Frequency		Bandwidth Selection		Charge Pump Frequency		Bandwidth Selection		Charge Pump Frequency	
Register Bit →	745	744	955	954	747	746	963	962	749	748	971	970
128 kHz	0	0	0	0	0	0	0	0	0	0	0	0
512 kHz	0	1	0	1	0	1	0	1	0	1	0	1
2.048 MHz	1	0	1	0	1	0	1	0	1	0	1	0
8.192 MHz	1	1	1	1	1	1	1	1	1	1	1	1

10.2 MODES OF OPERATION

In order to use any of the op amp macrocells in the GreenPAK Designer, the power up signal (PWR_UP) must be set to logic High. By default, all op amp macrocells are turned off after SLG47004 startup. During power-up, outputs of all op amps will remain in a Hi-Z state and then become valid (see parameter t_{on} in Table 23).

Operational amplifiers turn-on time can be decreased by setting register bits [759:757] to 1. In this case op amps analog supporting blocks are always turned on. Note that current consumption of op amp will be increased when op amp is powered down and bits [759:757] is 1 (see Section 3.13).

See the list below for the op amp operation modes:

- Operational Amplifier mode;
- Instrumentation Amplifier mode;
- Analog Comparator mode;
- Voltage Regulator mode;
- Current Sink mode.

10.2.1 Operational Amplifier Mode

In this mode, the Programmable Op Amp operates as a conventional operational amplifier. Also, the Programmable Op Amp can source the corresponding non-inverting ACMP input (see ACMP macrocell settings). The output of the Programmable Op Amp macrocell is in a Hi-Z state while the macrocell is turned off.

Figure 68 shows the example of differential amplifier with input offset voltage compensation with help of digital rheostat and programmable trim block. Zero input voltage equal to output voltage $V_{OUT} = V_{DD}/2$.

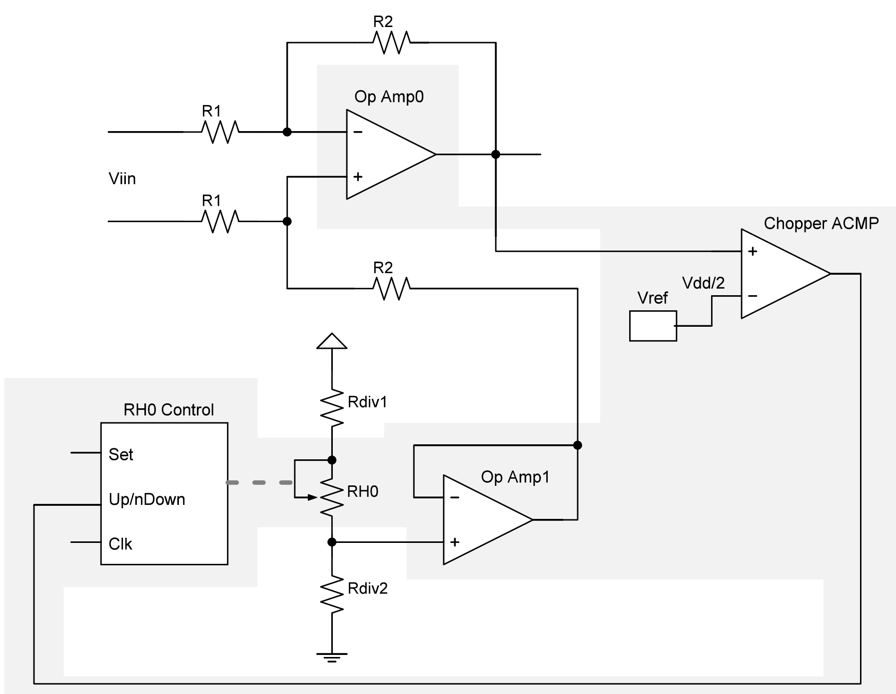


Figure 68: Example of Input Offset Voltage Compensation

10.2.2 Instrumentation Amplifier Mode

If this mode is active (Matrix Output [98] is High level), the two Programmable Op Amps and the single Internal Op Amp work together in Instrumentation Amplifier configuration, shown in Figure 69. When power up signal is logic LOW the output of In Amp is in Hi-Z state.

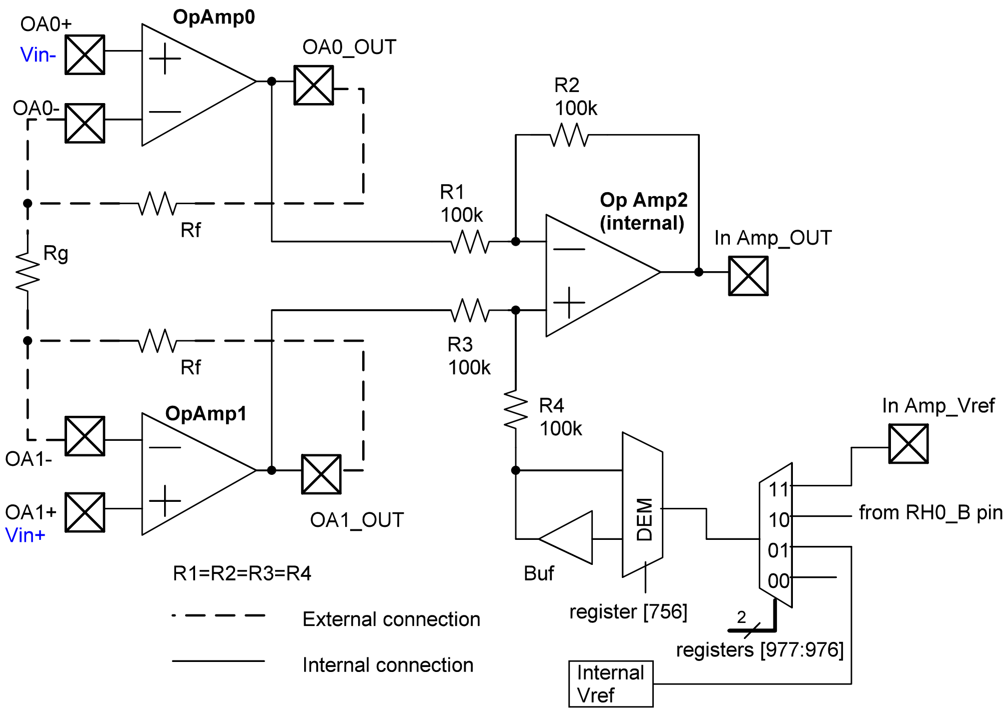


Figure 69: Instrumentation Amplifier Structure

The absolute value of internal resistors R_1, R_2, R_3, R_4 is 100 kΩ. The resistors R_f and R_g are user defined external resistors. The output voltage V_{OUT} of the instrumentation amplifier shown in Figure 69 is

$$V_{OUT} = (1 + 2R_f / R_g)(V_{IN+} - V_{IN-}) + V_{REF}$$

The user can trim both the gain and the offset error of the instrumentation amplifier using two of the Rheostats from the SLG47004. Figure 70 shows the configuration of the instrumentation amplifier in this scenario.

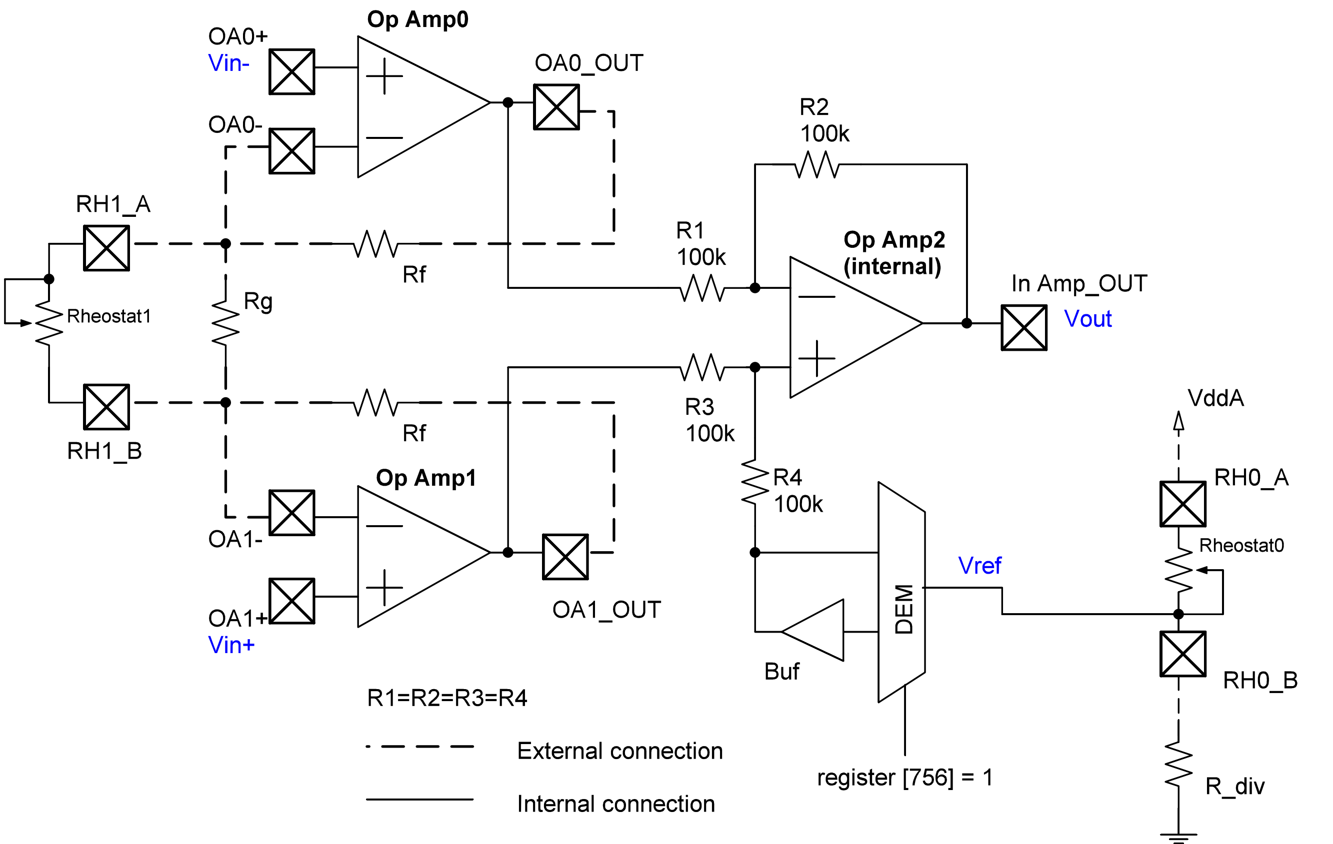


Figure 70: Instrumentation Operational Amplifier Configuration for Users Trim

Note that in Figure 70, the Demux connects to the Vref external input with an internal buffer (register [756] = 1). This allows us to eliminate the influence of resistor divider R_{div} and Rheostat0 on instrumentation amplifier.

It is possible to use a built-in Auto-Trim function for either setting the zero point of the Wheatstone bridge sensor using the In Amp or tuning a system output voltage to the desired level. However, the following limitations exist for using the built-in Auto-Trim function to trim both total system offset and system gain errors:

- The Auto-Trim procedures of total offset compensation and system gain error must be done iteratively starting and finishing with the total offset compensation: 1st iteration - offset compensation, 2nd iteration - gain trim, 3rd iteration - offset compensation. Extra iterations can be added to achieve a better accuracy. The last iteration should be an offset compensation.

- Total system offset (sensor offset + Op Amp1 offset + Op Amp2 offset) must not be greater than Vsensor_output_range/2.

It's possible to power external components like bridge or ADC from internal HD Buffer of SLG47004 to improve accuracy of system.

10.2.3 Analog Comparator Mode

Both operational amplifiers have an Analog Comparator mode in which they work as conventional rail-to-rail comparators.

10.2.4 Voltage Regulator Mode

In this mode, the op amp output drives P-FET (part of Analog Switch). Note that FETs of Analog Switches have different resistances. Analog Switch 0 has Rds_PMOS << Rds_NMOS, while Analog Switch 1 has Rds_NMOS << Rds_PMOS. That's why it is recommended to implement voltage regulator mode using Analog Switch 0. In this mode the op amp output is High when the macrocell is turned off. Figure 71 (A) shows the typical implementation of the voltage source function. Optionally, the user can use this mode to implement a constant current source with load connected to ground (Figure 71, B, C). Note that op amp must operate in operational amplifier mode (register 750 = 0 for Op Amp0, register 751 = 0 for Op Amp1).

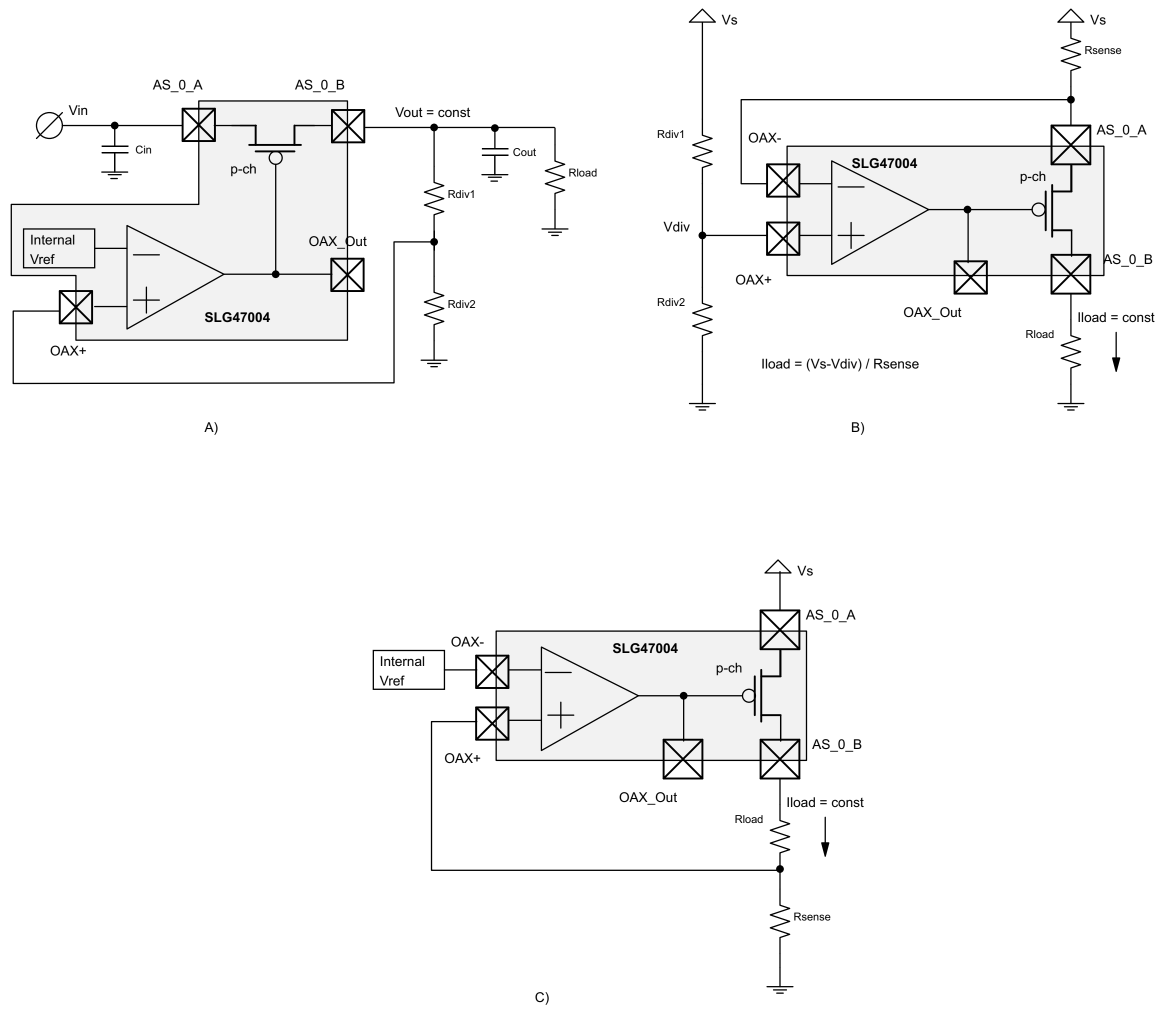


Figure 71: Typical Implementation of Voltage Regulator (A) and Current Sources (B, C)

Note that in this mode only an enhanced P channel FET of An_Sw_0 is used.

10.2.5 Current Sink Mode

Also, the op amp output can drive the N-FET (part of the Analog Switch) in order to implement a constant current sink. Note that FETs of Analog Switches have different resistances. Analog Switch 0 has Rds_PMOS << Rds_NMOS, while Analog Switch 1 has Rds_NMOS << Rds_PMOS. That's why it is recommended to implement current sink mode using Analog Switch 1. In this mode, the op amp output is LOW when the macrocell is turned off. Figure 72 shows a typical implementation of this Current Sink Function. Note that op amp must operate in operational amplifier mode (register 750 = 0 for Op Amp0, register 751 = 0 for Op Amp1).

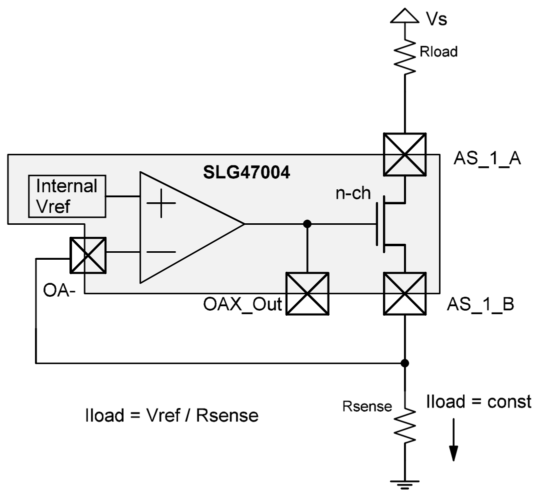


Figure 72: Constant Current Sink

Note that in this mode only an enhanced N channel FET of An_Sw_1 is used.

10.3 OP AMPS TYPICAL PERFORMANCE

T_A = 25 °C, V_{DDA} = 5.0 V, V_{SS} = GND, $_{CM}$ = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, C_L = 80 pF, unless otherwise stated.

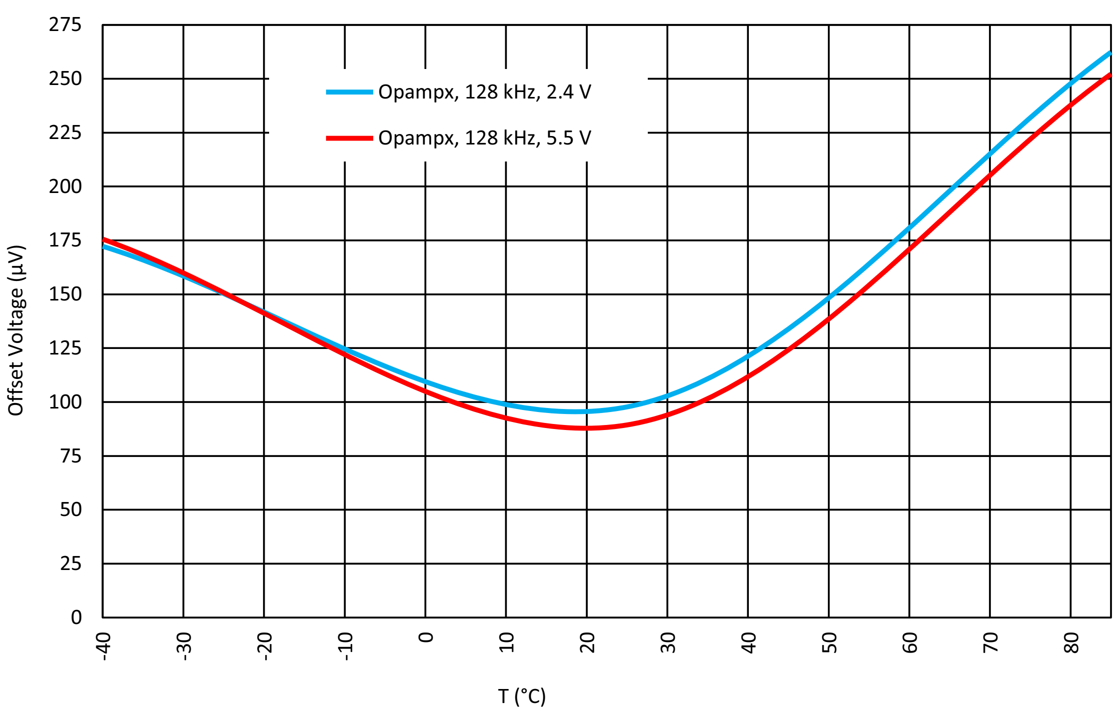


Figure 73: Op Ampx Input Offset Voltage vs. T_A at Input CM Voltage = V_{DD}/2, BW = 128 kHz

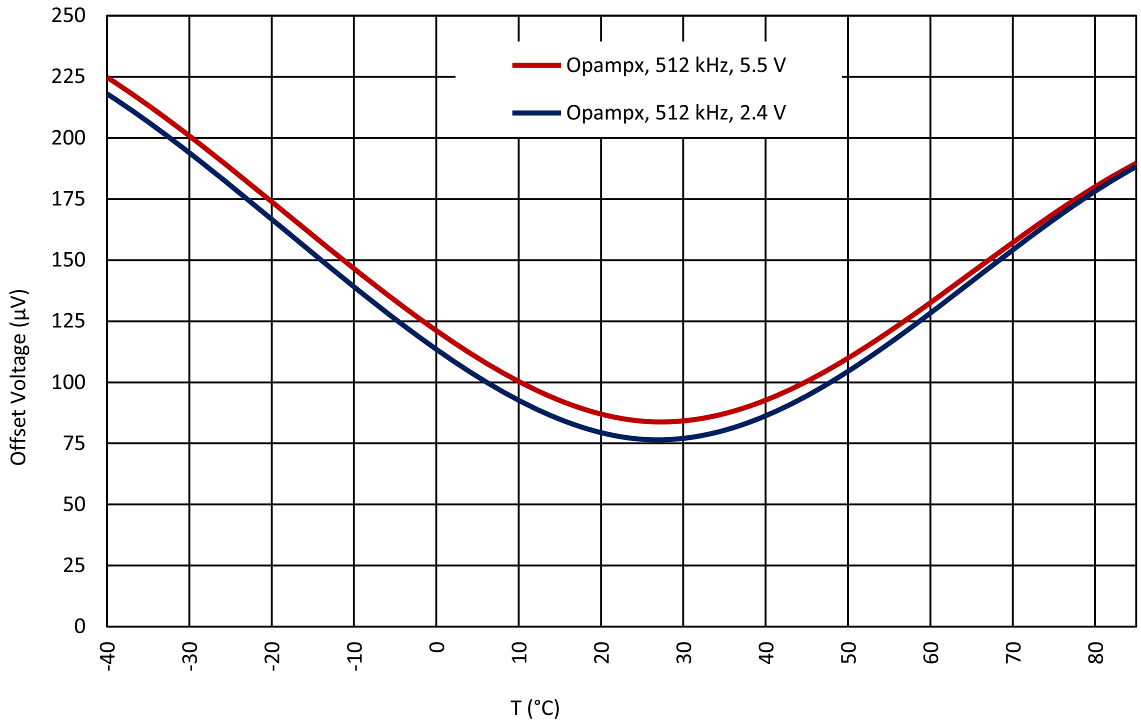


Figure 74: Op Ampx Input Offset Voltage vs. T_A at Input CM Voltage = $V_{DD}/2$, BW = 512 kHz

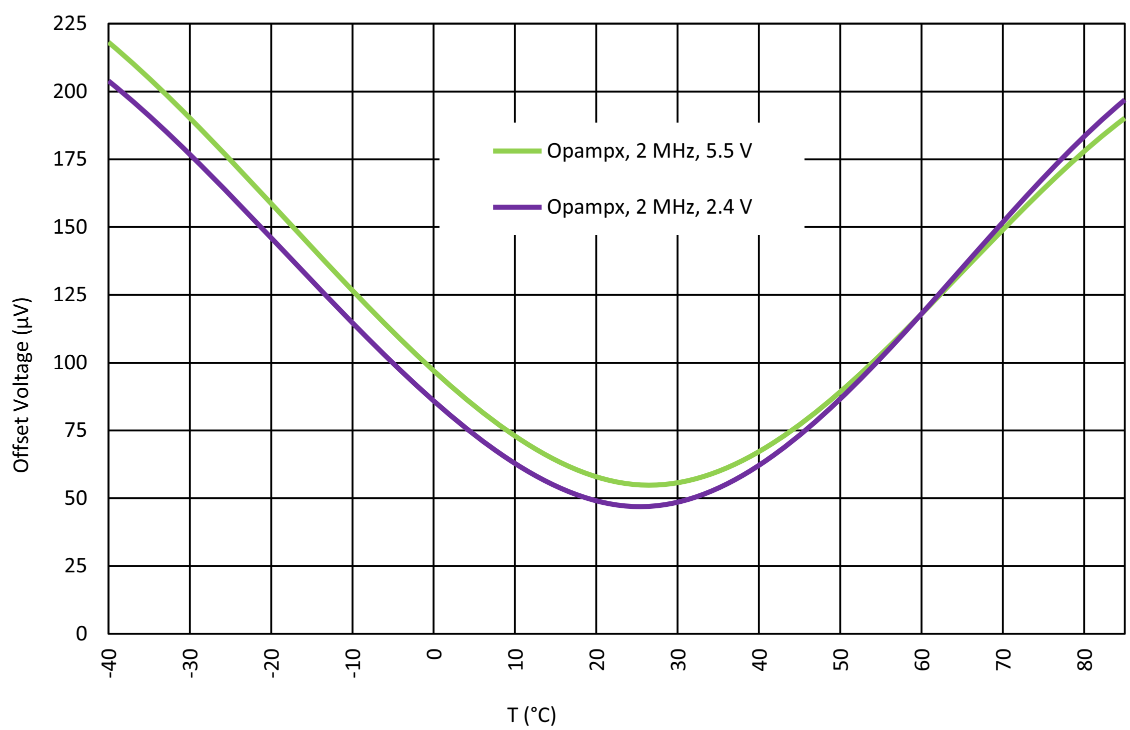


Figure 75: Op Ampx Input Offset Voltage vs. T_A at Input CM Voltage = $V_{DD}/2$, BW = 2 MHz

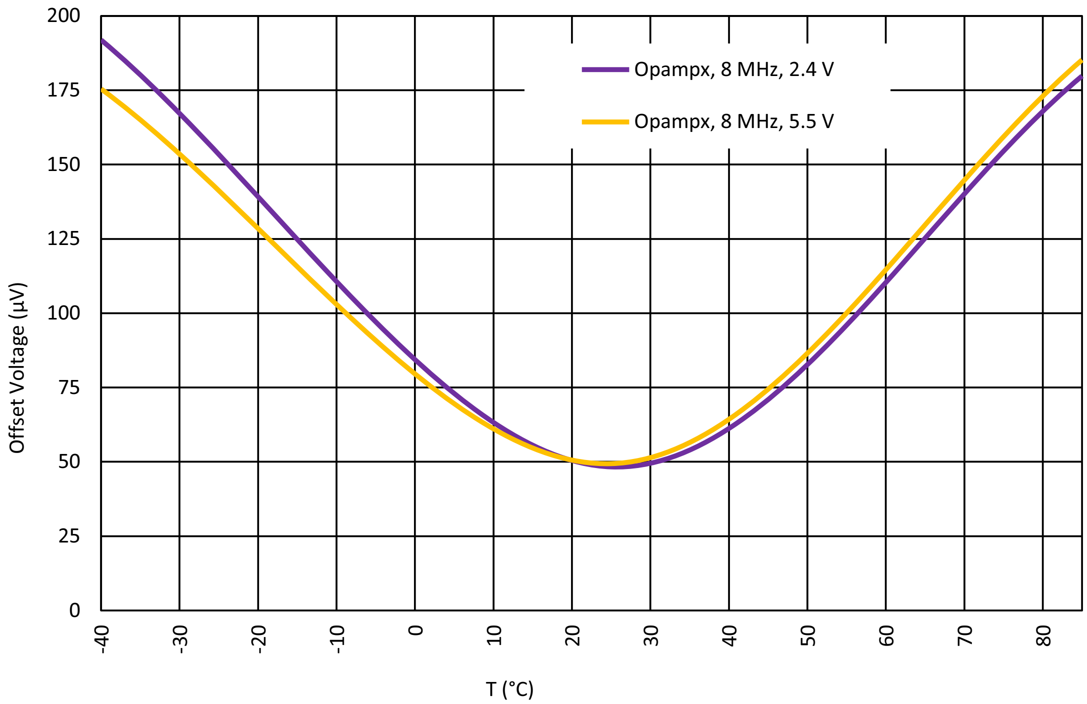


Figure 76: Op Ampx Input Offset Voltage vs. T_A at Input CM Voltage = $V_{DD}/2$, BW = 8 MHz

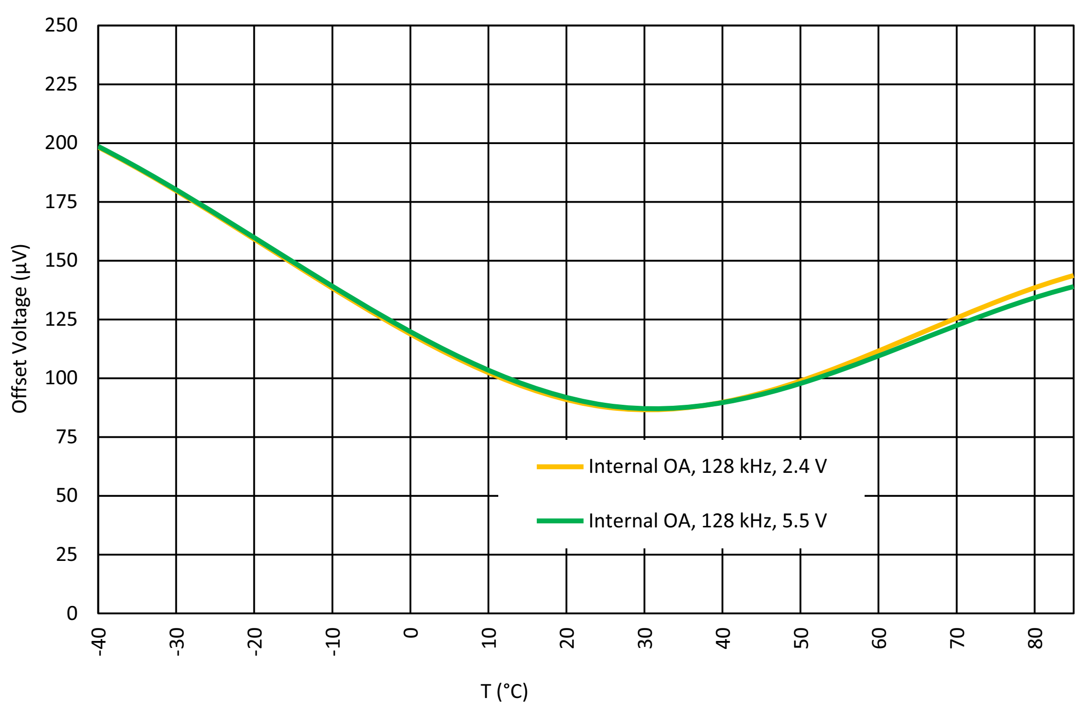


Figure 77: Internal Op Amp Input Offset Voltage vs. T_A at Input CM Voltage = $V_{DD}/2$, BW = 128 kHz

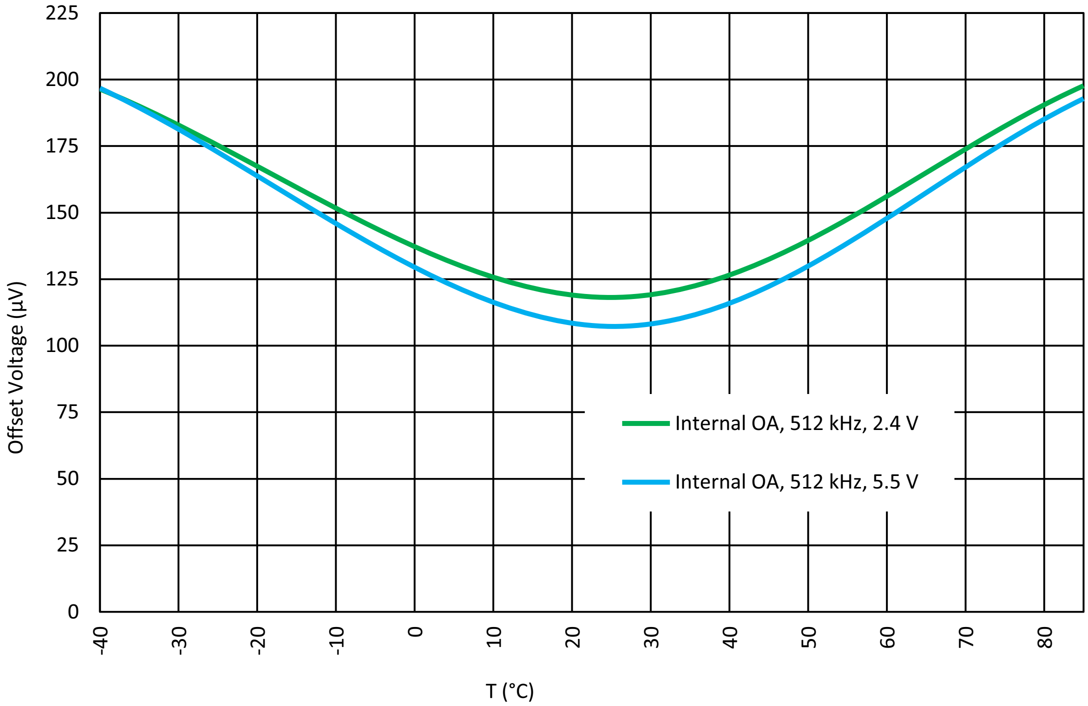


Figure 78: Internal Op Amp $_{A}$at Input CM Voltage = V_{DD}/2, BW = 512 kHz

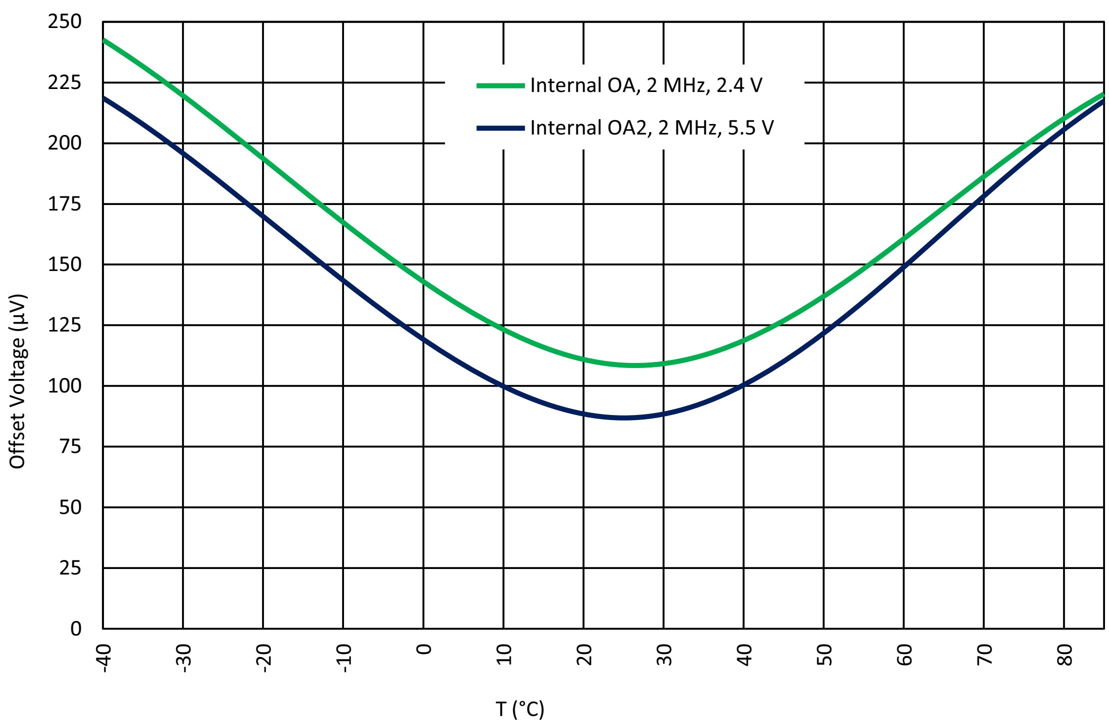


Figure 79: Internal Op Amp $_{A}$at Input CM Voltage = V_{DD}/2, BW = 2 MHz

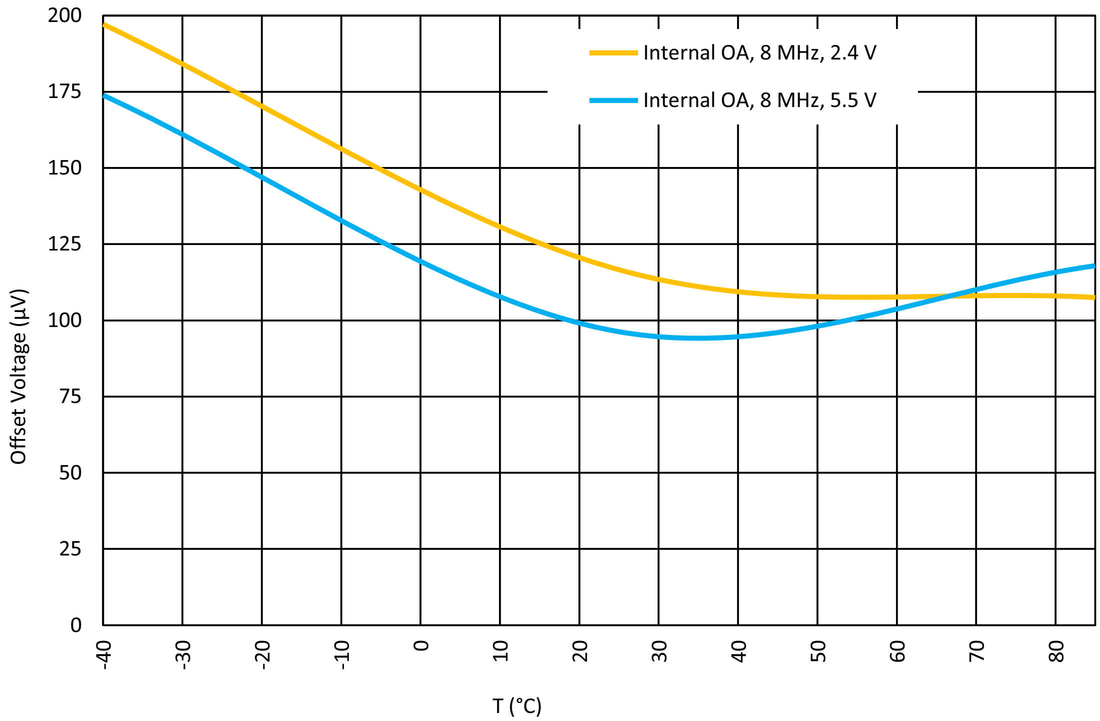


Figure 80: Internal Op Amp Input Offset Voltage vs. T_A at Input CM Voltage = V_{DD}/2, BW = 8 MHz

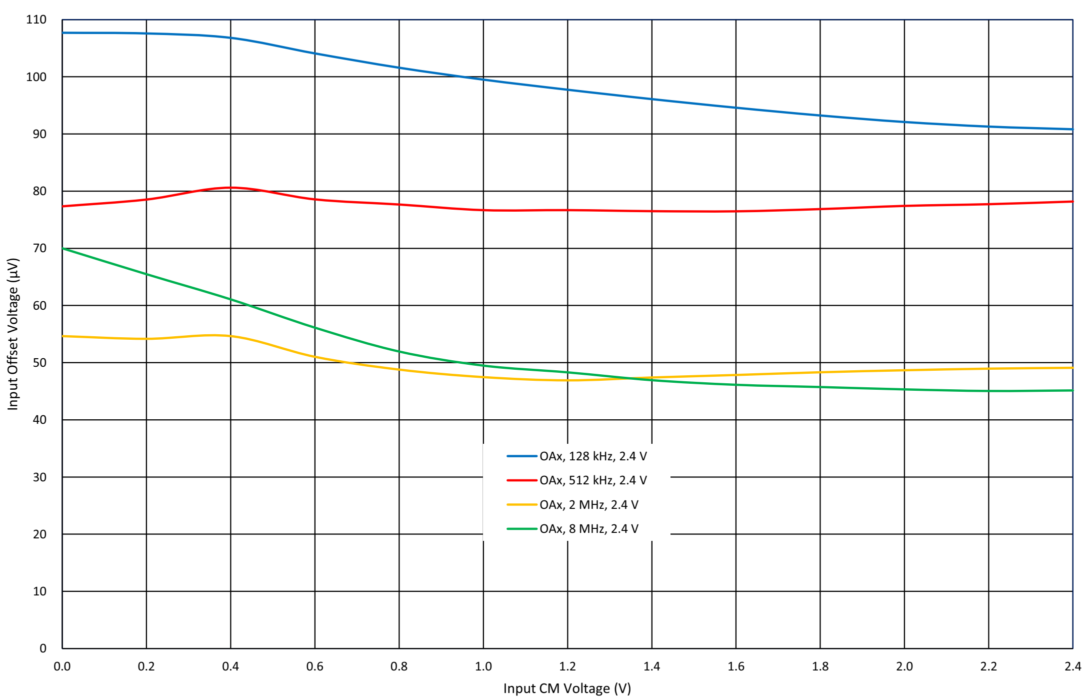


Figure 81: OpAmp0, 1 Input Offset Voltage vs. Input CM Voltage at T = 25 °C, V_{DDA} = 2.4 V

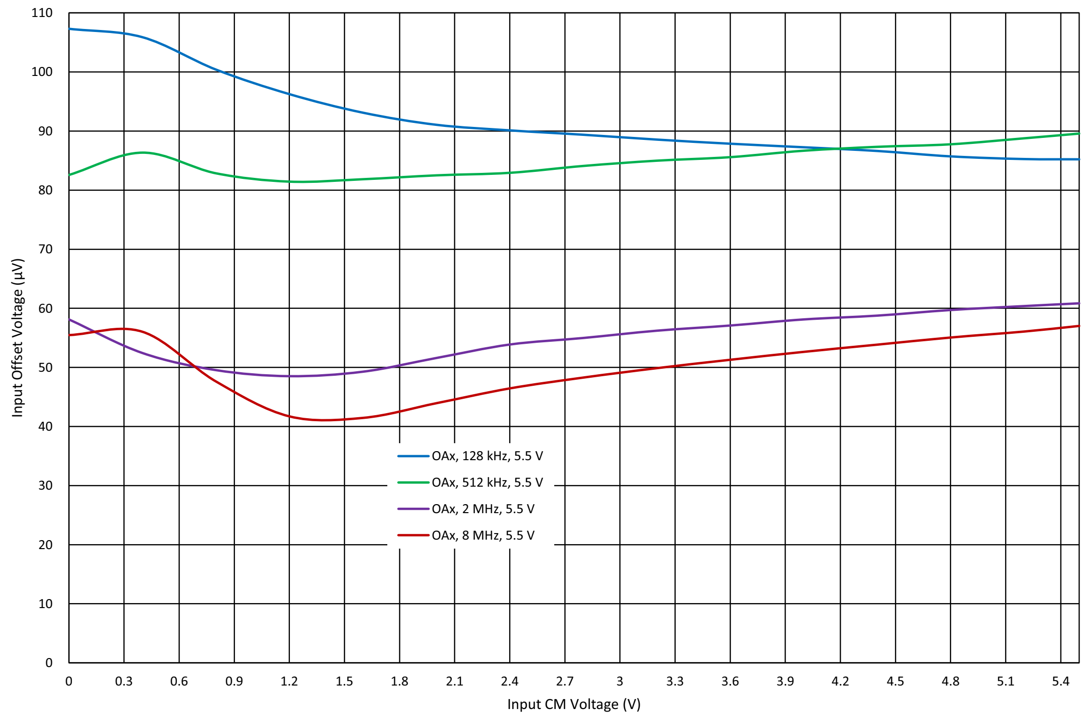


Figure 82: OpAmp0, 1 Input Offset Voltage vs. Input CM Voltage at T = 25 °C, V_{DDA} = 5.5 V

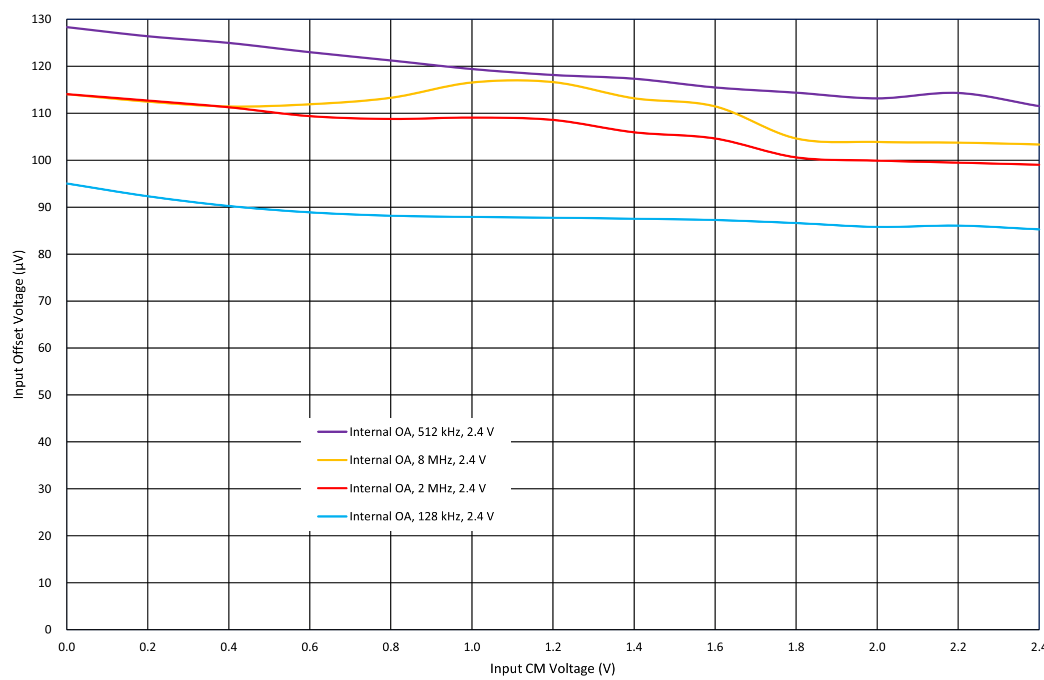


Figure 83: Internal OpAmp Input Offset Voltage vs. Input CM Voltage at T = 25 °C, V_{DDA} = 2.4 V

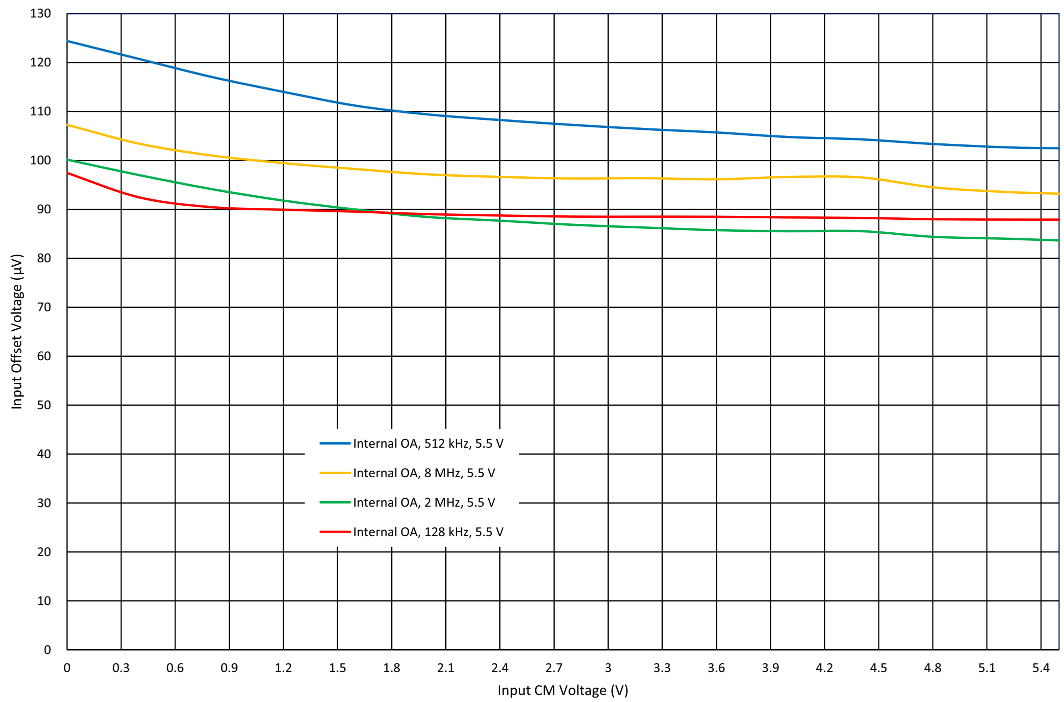


Figure 84: Internal OpAmp Input Offset Voltage vs. Input CM Voltage at T = 25 °C, V_{DDA} = 5.5 V

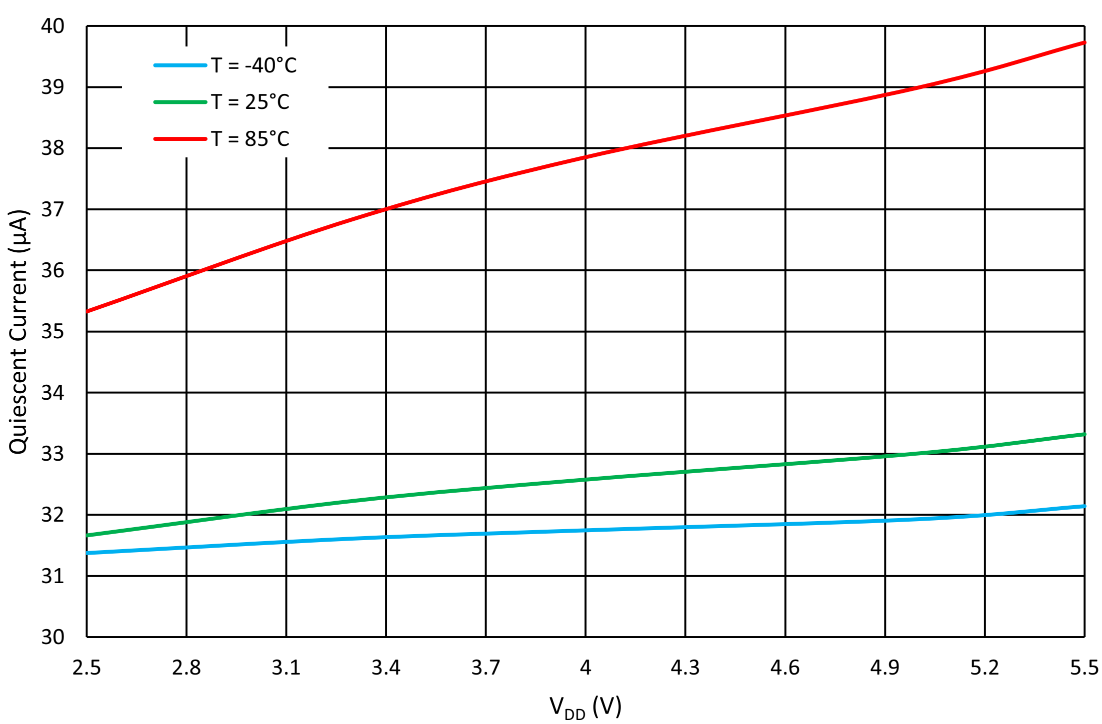


Figure 85: Quiescent Current vs. Power Supply Voltage for BW = 128 kHz

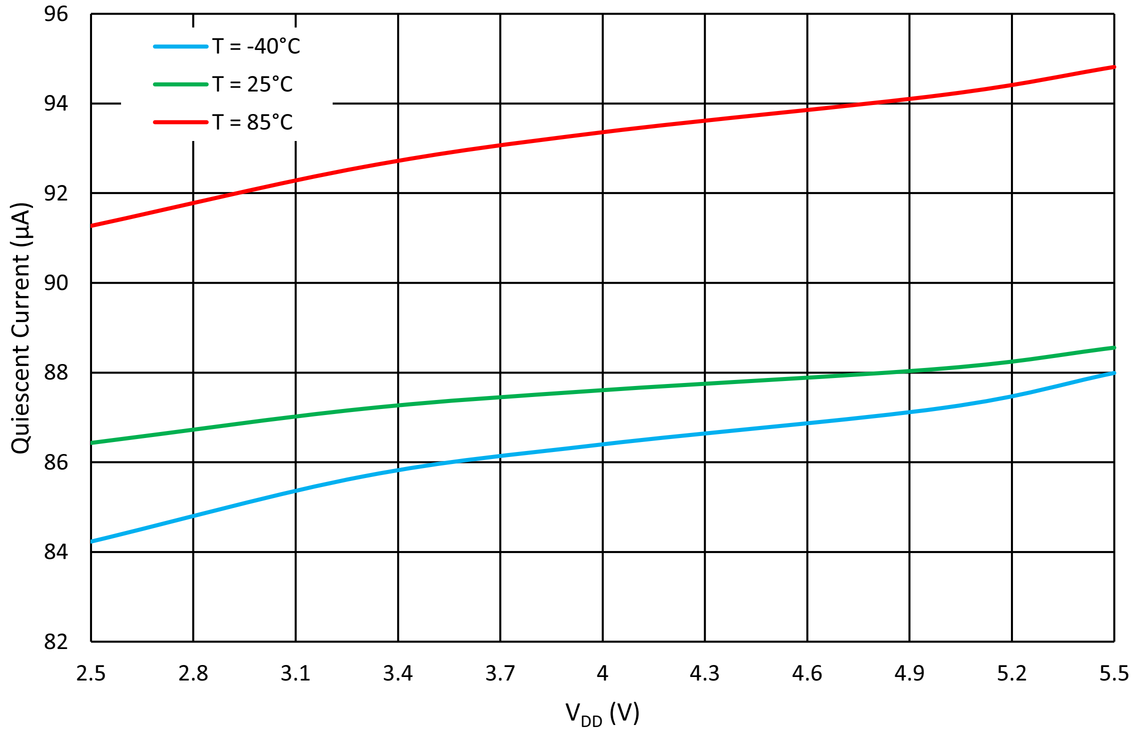


Figure 86: Quiescent Current vs. Power Supply Voltage for BW = 512 kHz

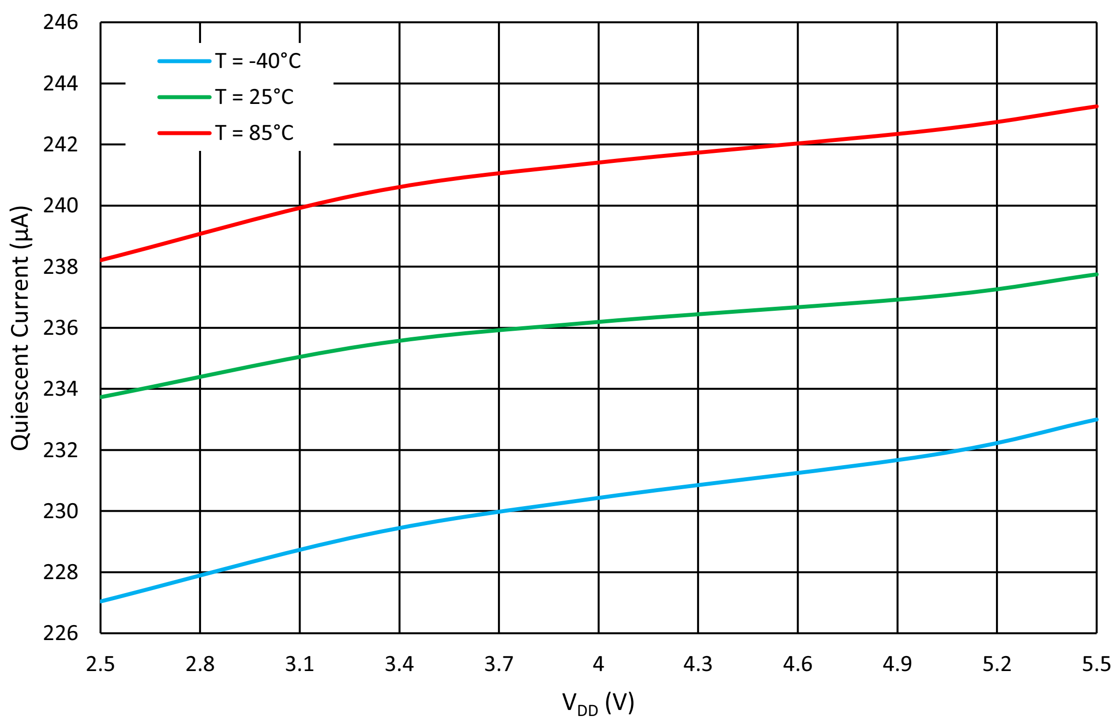


Figure 87: Quiescent Current vs. Power Supply Voltage for BW = 2 MHz

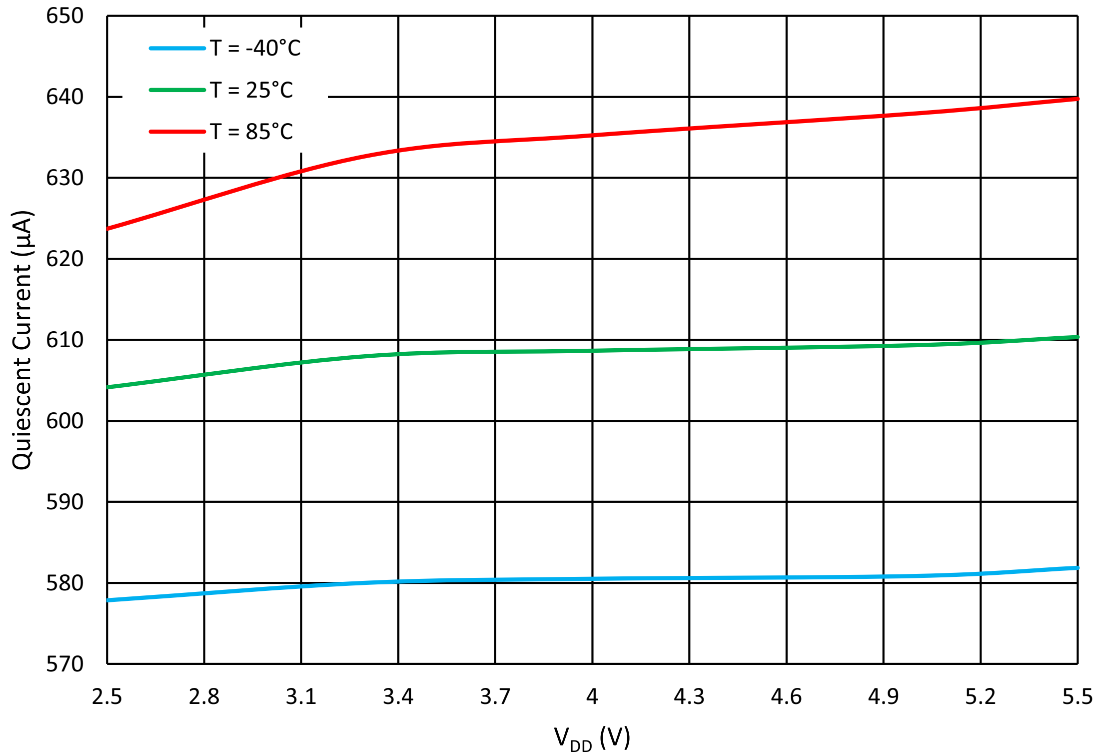


Figure 88: Quiescent Current vs. Power Supply Voltage or BW = 8 MHz

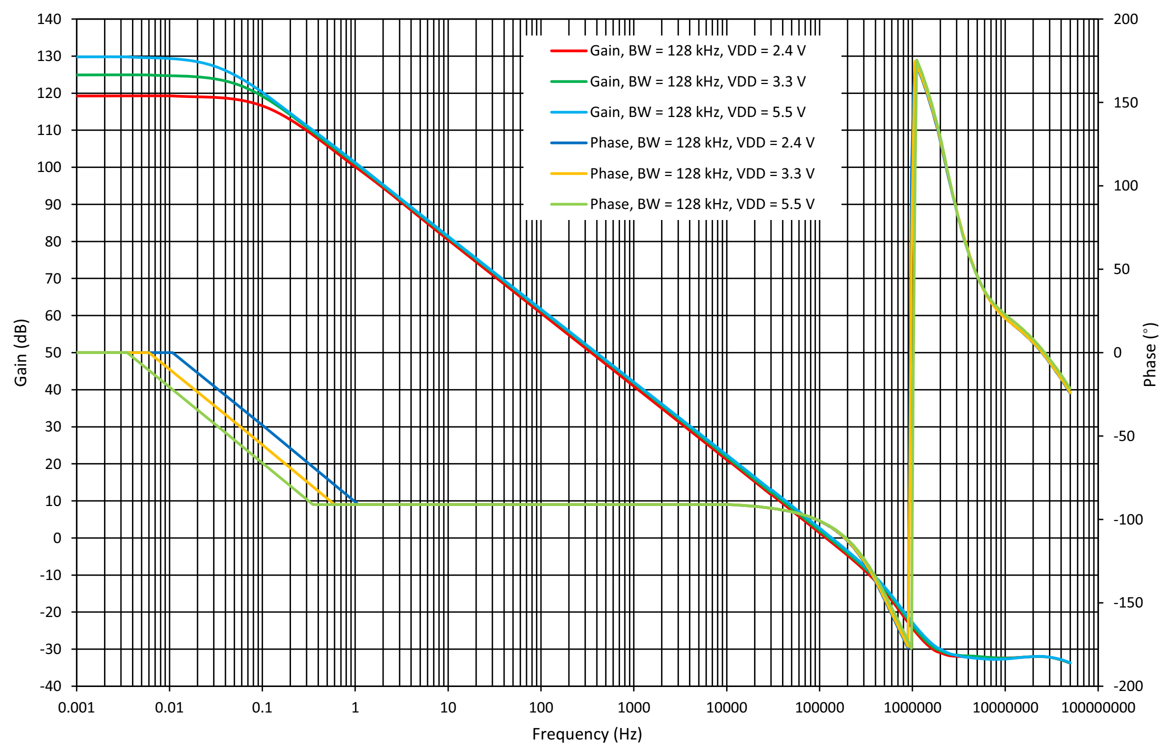


Figure 89: OA0 Open Loop Gain and Phase vs. Frequency for BW = 128 kHz

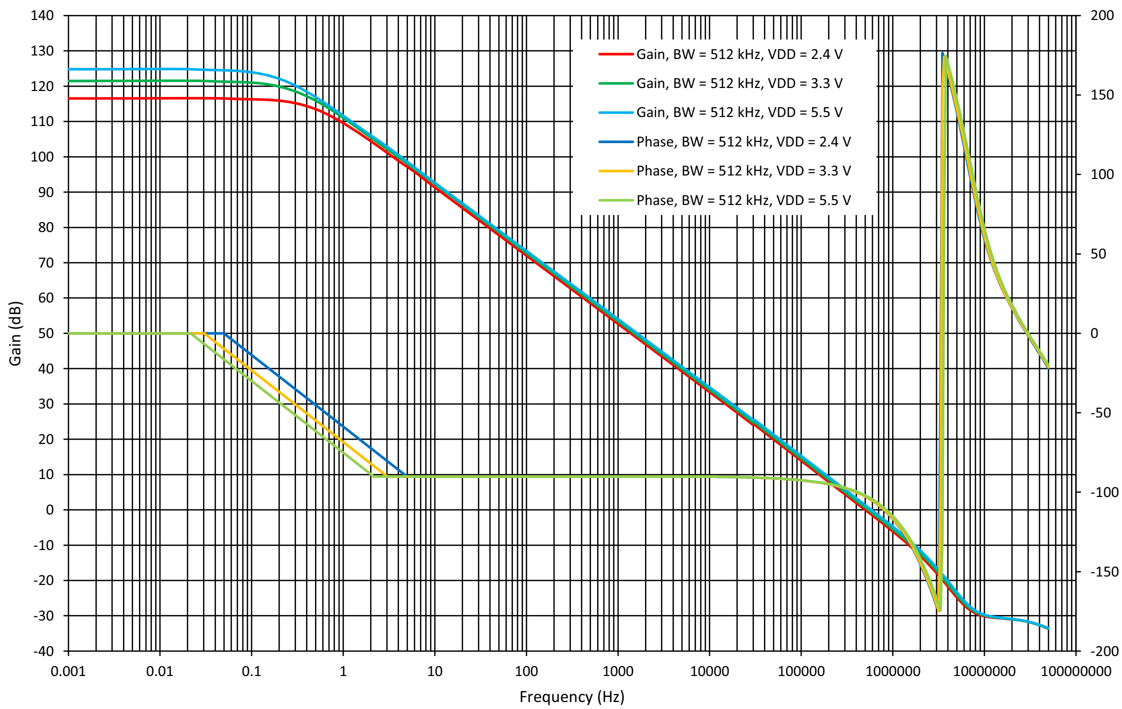


Figure 90: OA0 Open Loop Gain and Phase vs. Frequency for BW = 512 kHz

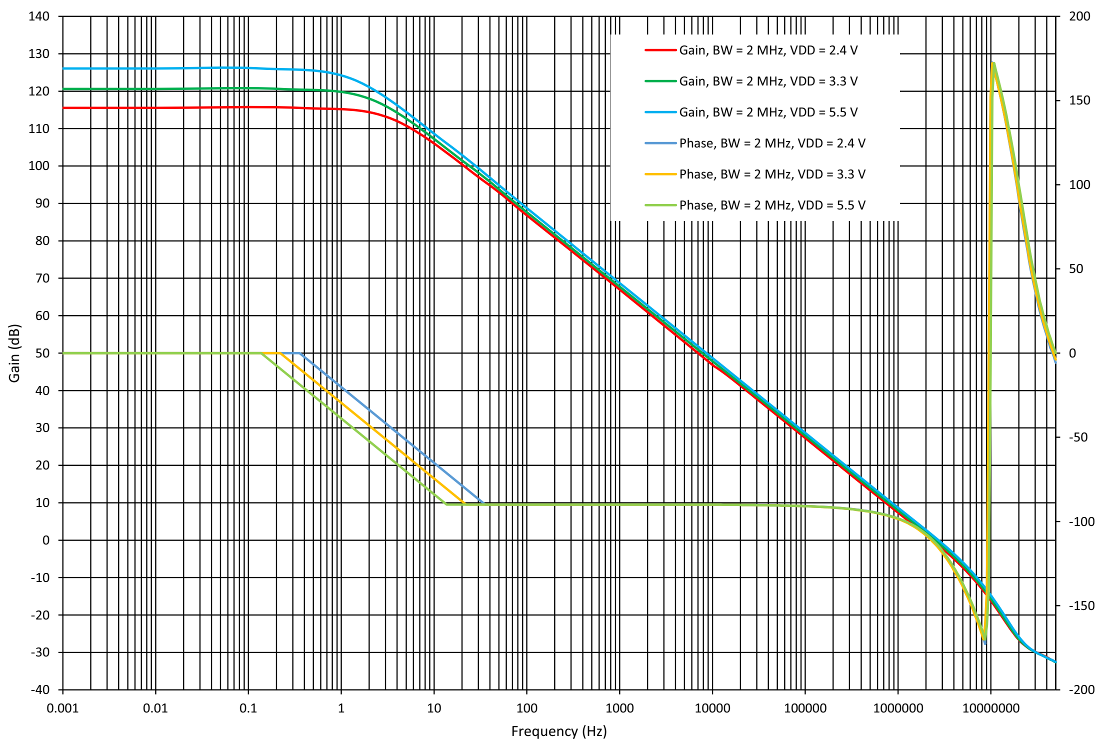


Figure 91: OA0 Open Loop Gain and Phase vs. Frequency for BW = 2 MHz

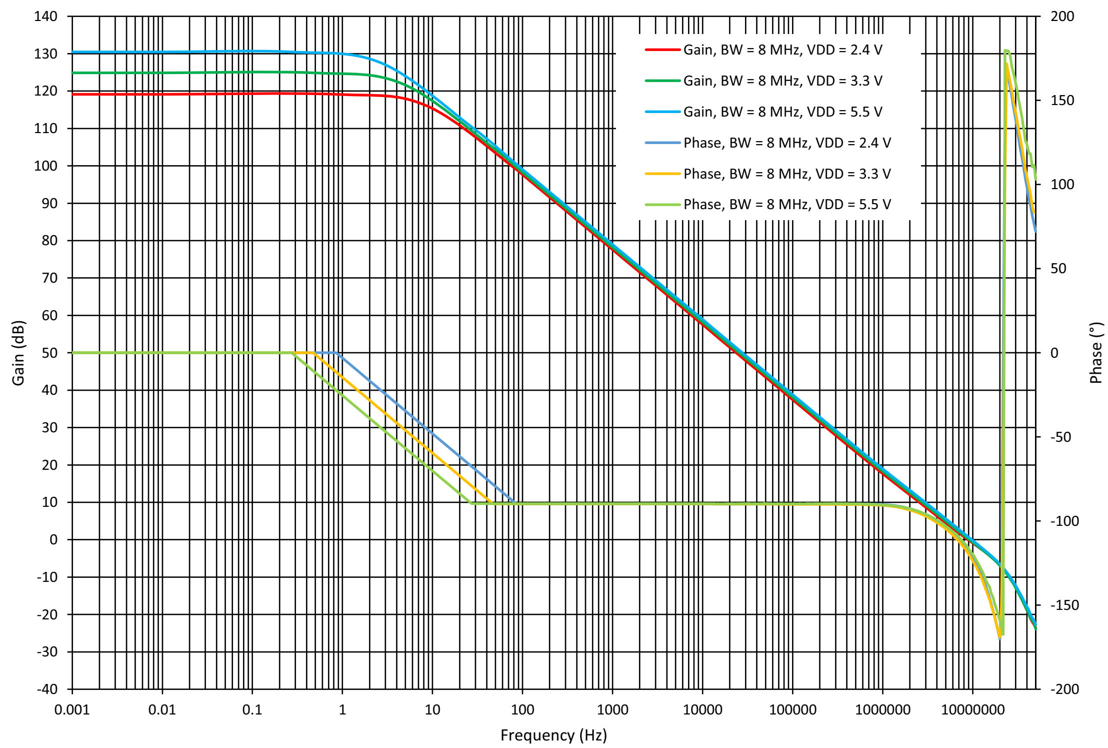


Figure 92: OA0 Open Loop Gain and Phase vs. Frequency for BW = 8 MHz

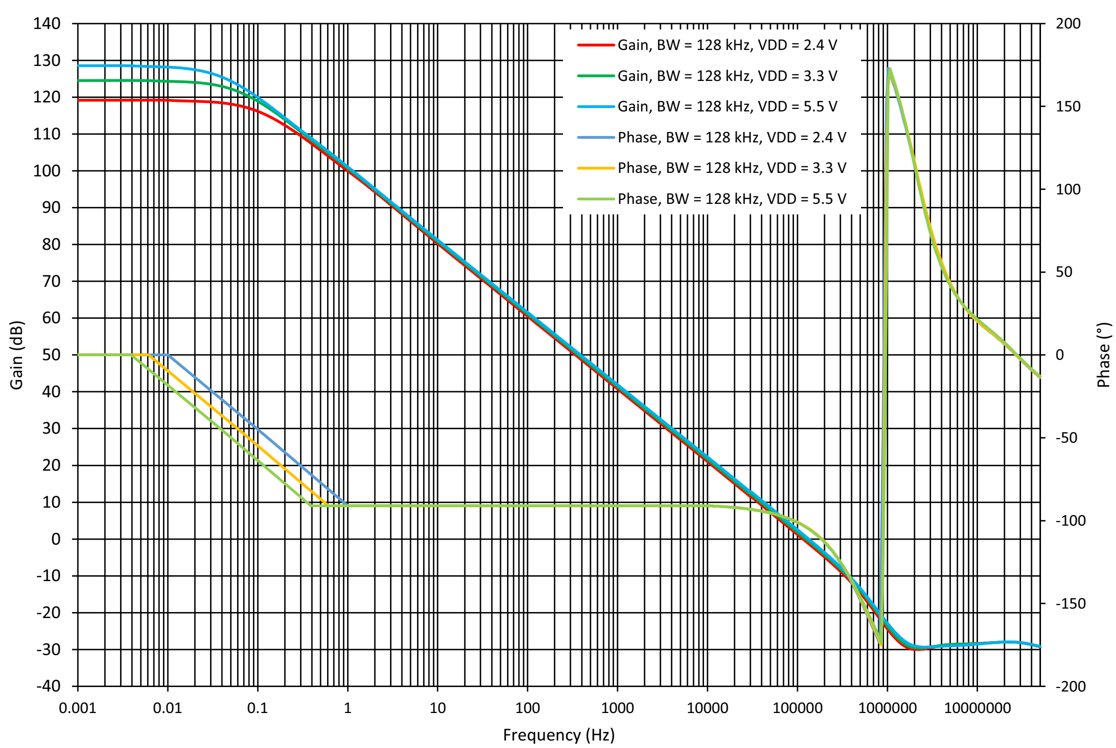


Figure 93: OA1 Open Loop Gain and Phase vs. Frequency for BW = 128 kHz

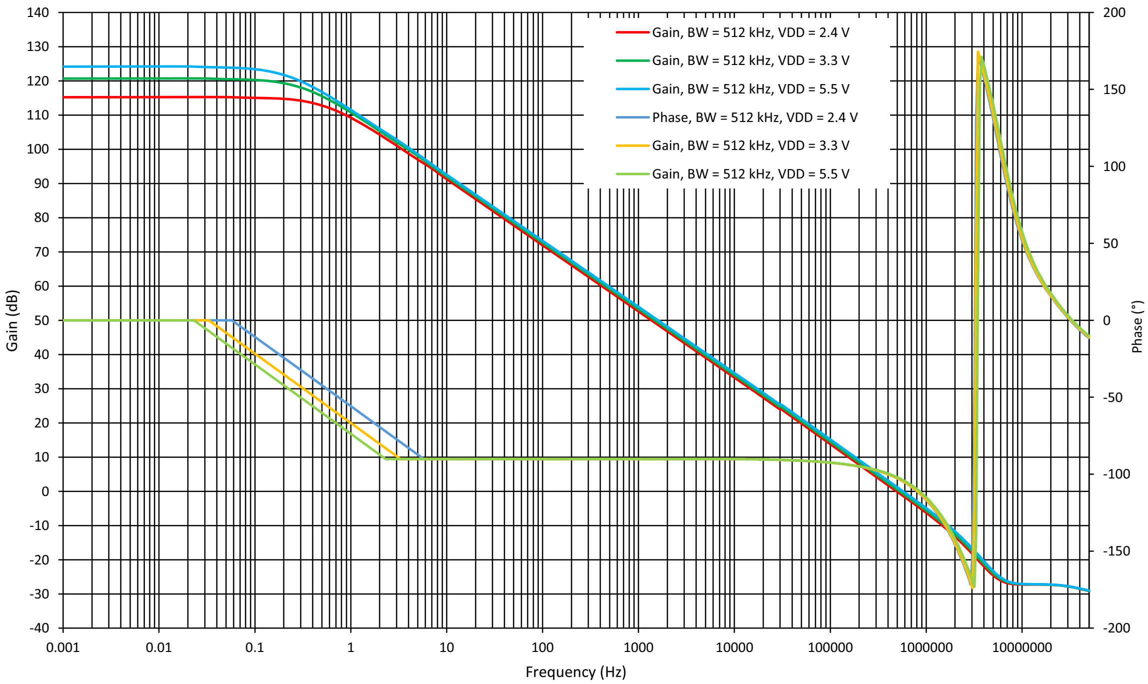


Figure 94: OA1 Open Loop Gain and Phase vs. Frequency for BW = 512 kHz

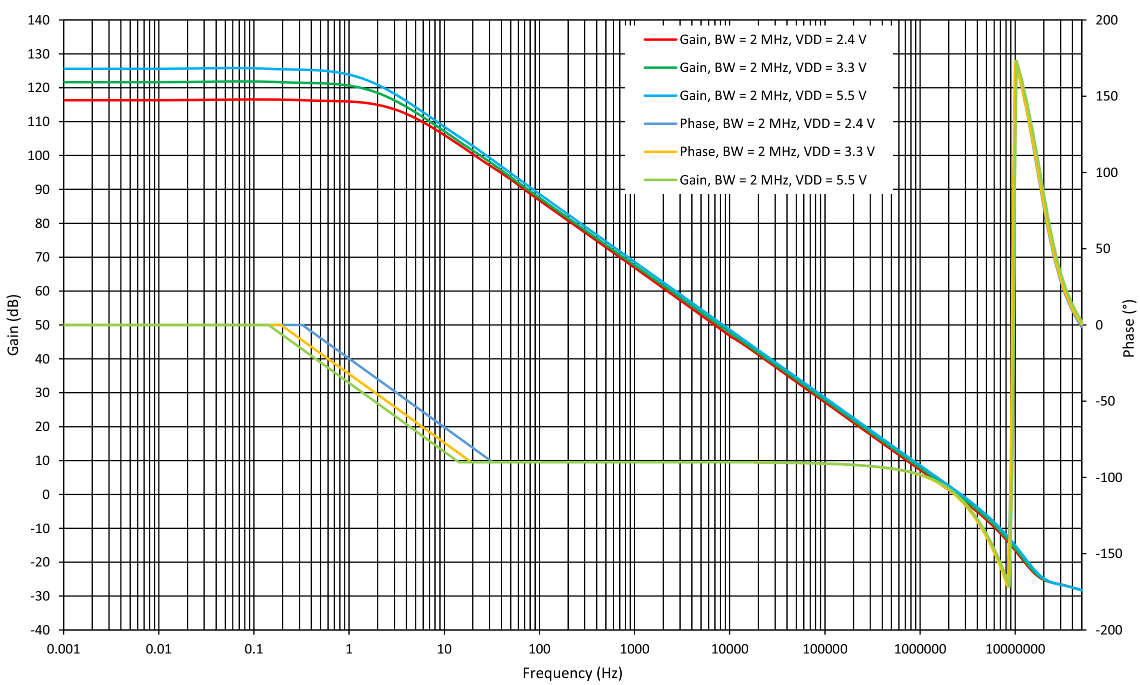


Figure 95: OA1 Open Loop Gain and Phase vs. Frequency for BW = 2 MHz

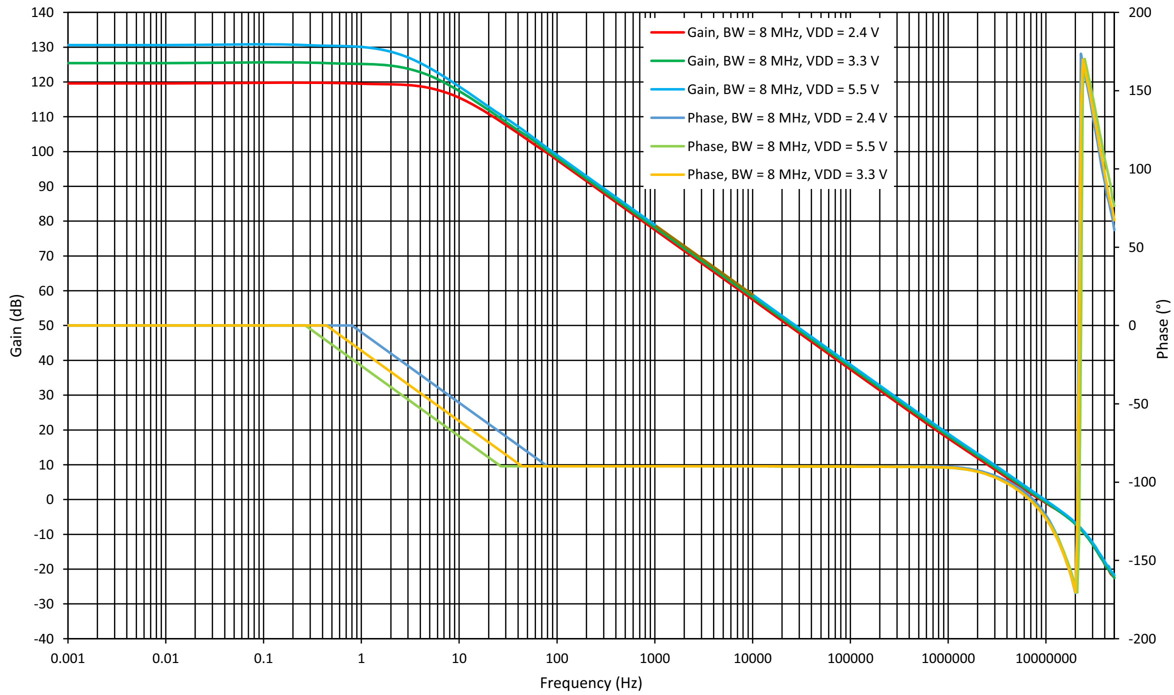


Figure 96: OA1 Open Loop Gain and Phase vs. Frequency for BW = 8 MHz

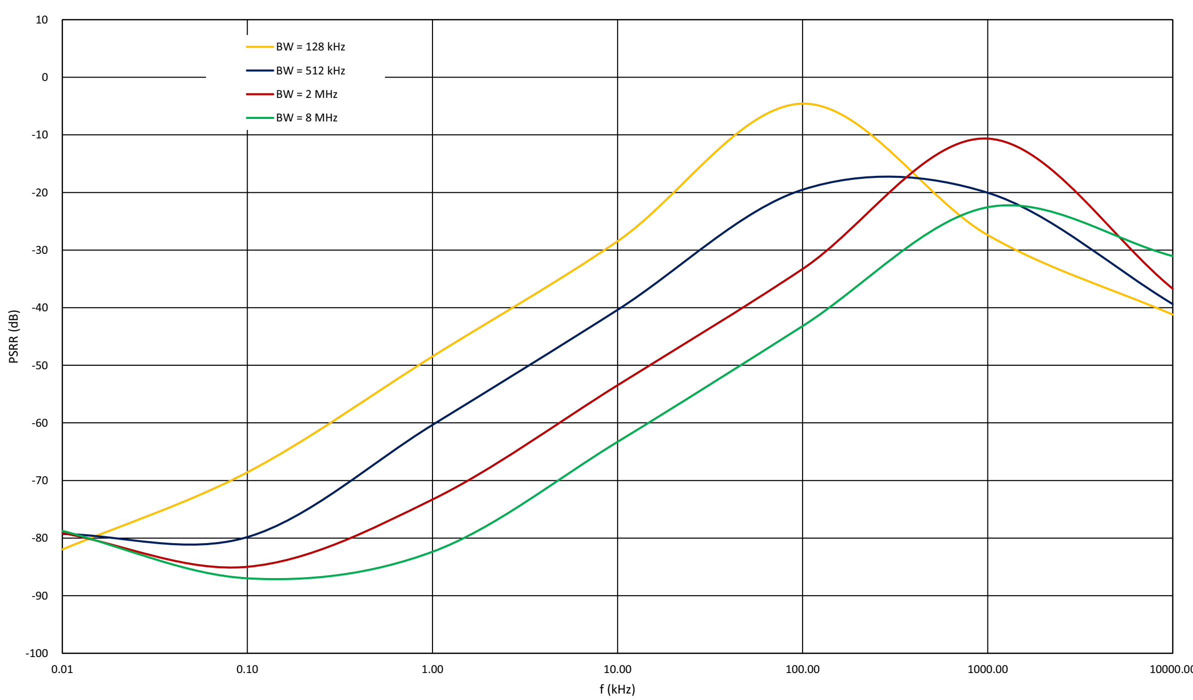


Figure 97: PSRR vs. Frequency V_{DD} = 2.4 V to 5.5 V

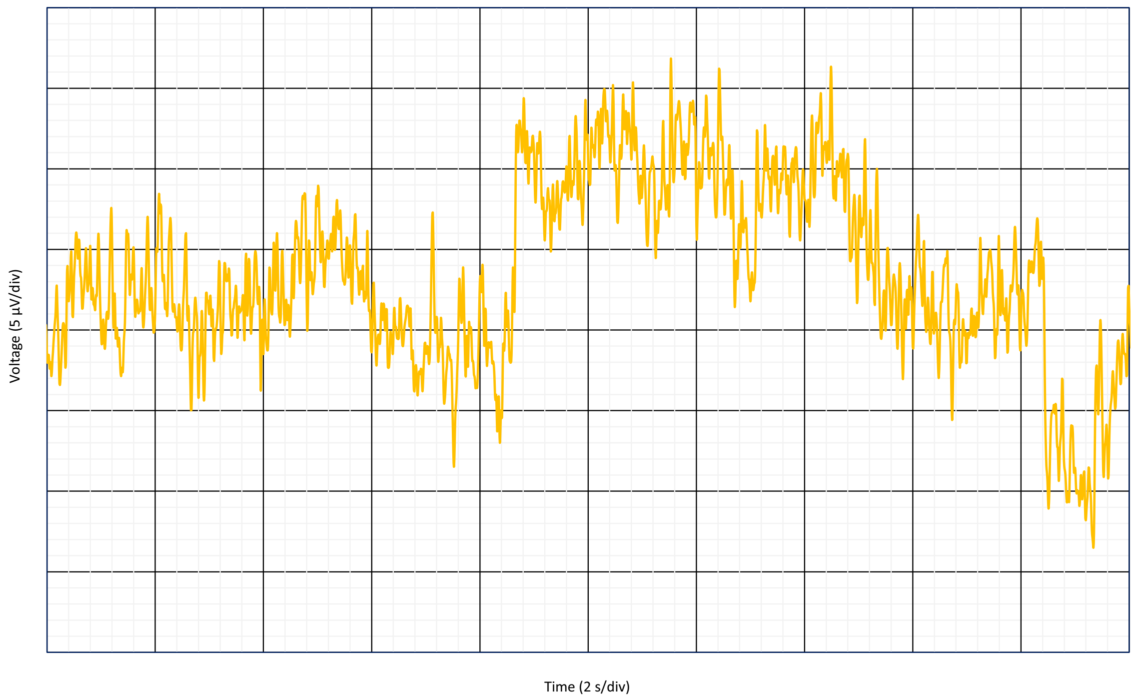


Figure 98: 0.1 Hz to 10 Hz Noise, BW = 128 kHz

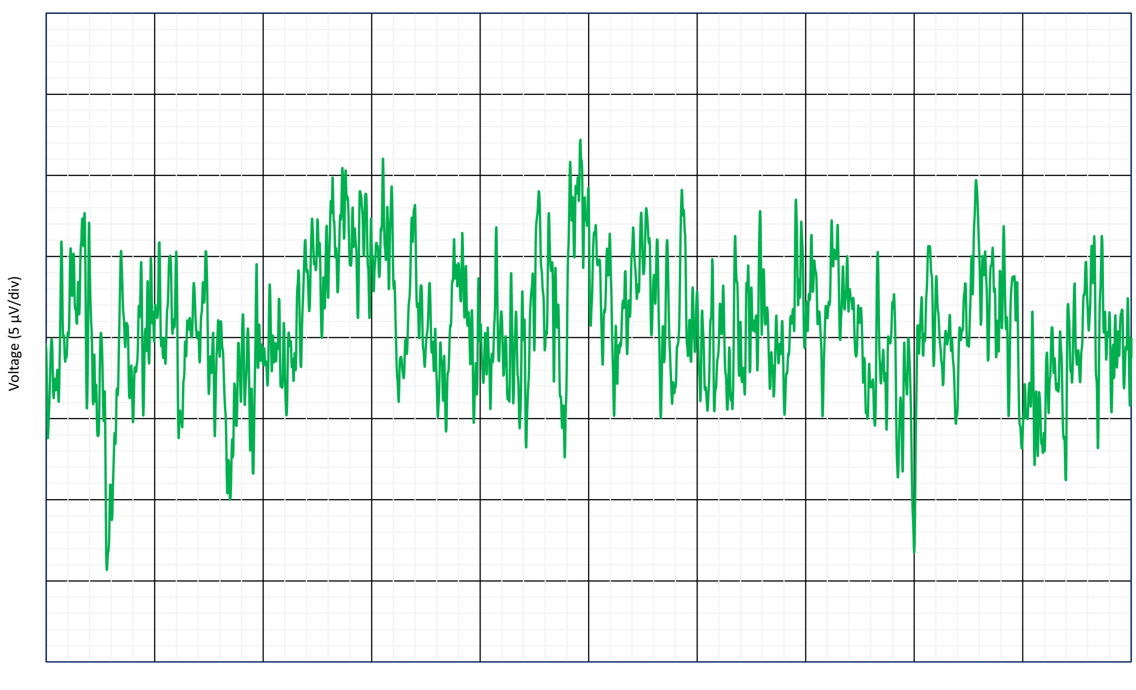


Figure 99: 0.1 Hz to 10 Hz Noise, BW = 512 kHz

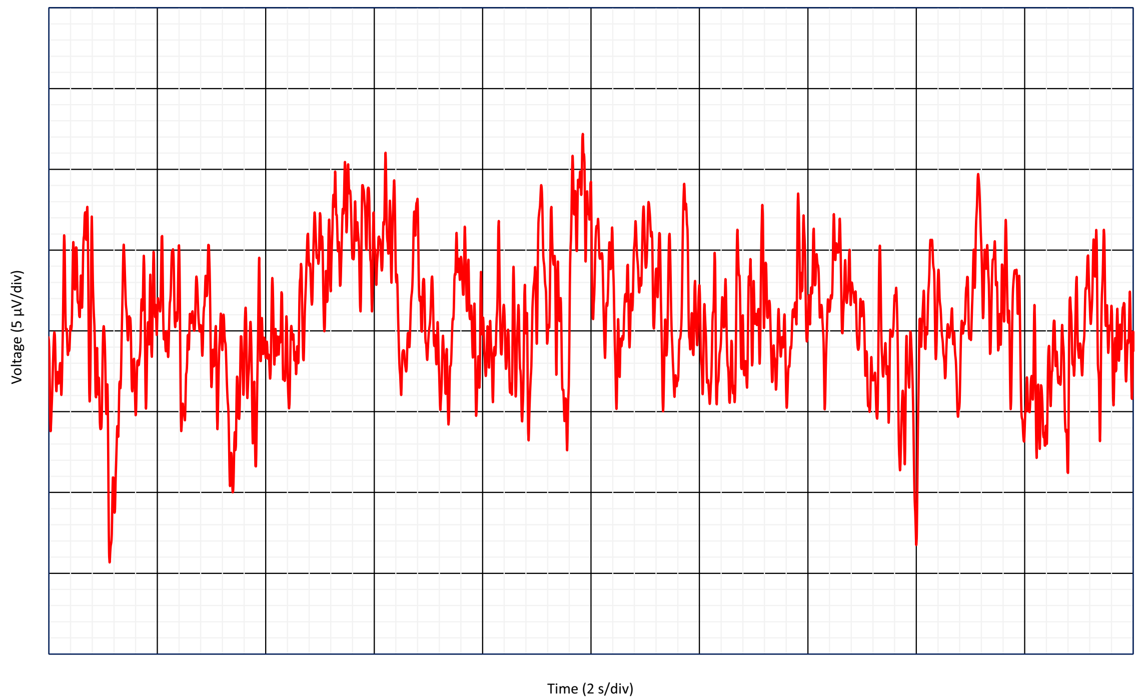


Figure 100: 0.1 Hz to 10 Hz Noise, BW = 2 MHz

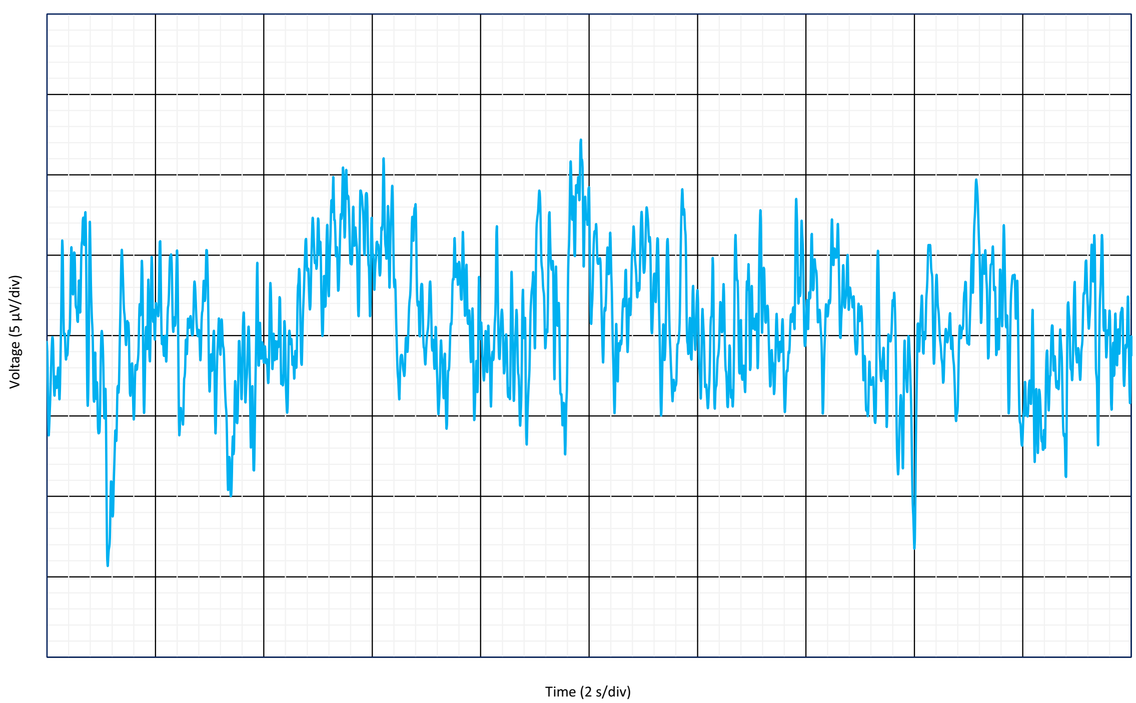


Figure 101: 0.1 Hz to 10 Hz Noise, BW = 8 MHz

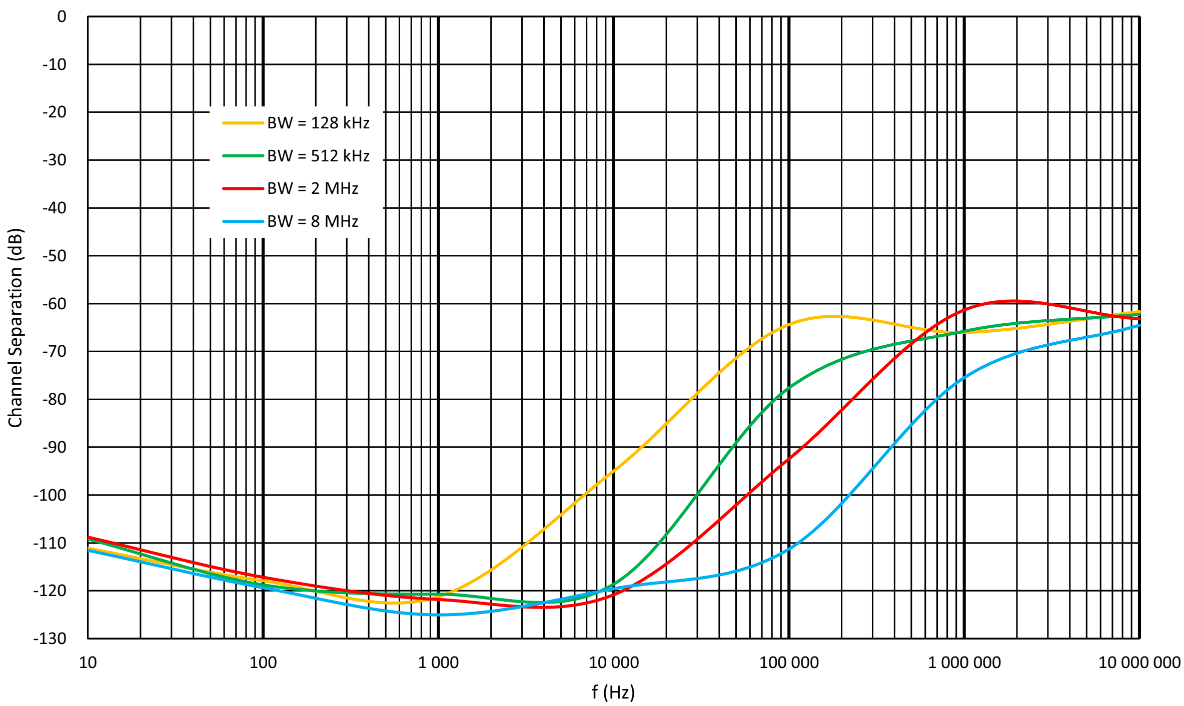


Figure 102: Channel Separation vs. Frequency

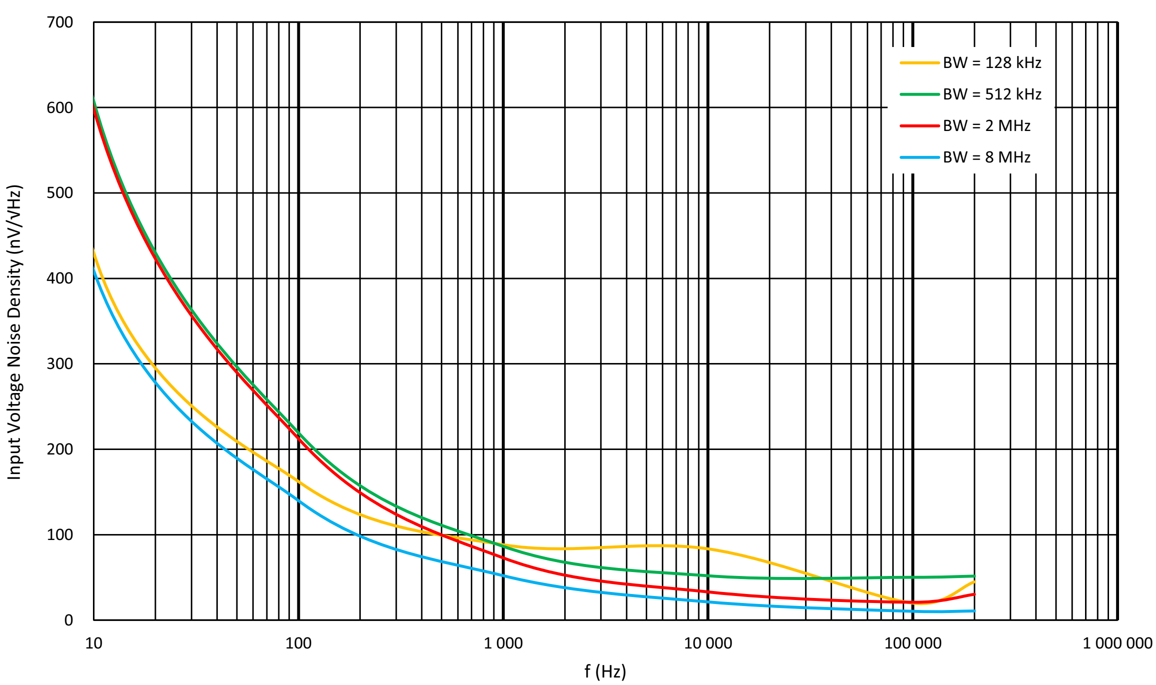


Figure 103: Op Ampx Noise Voltage Density vs. Frequency

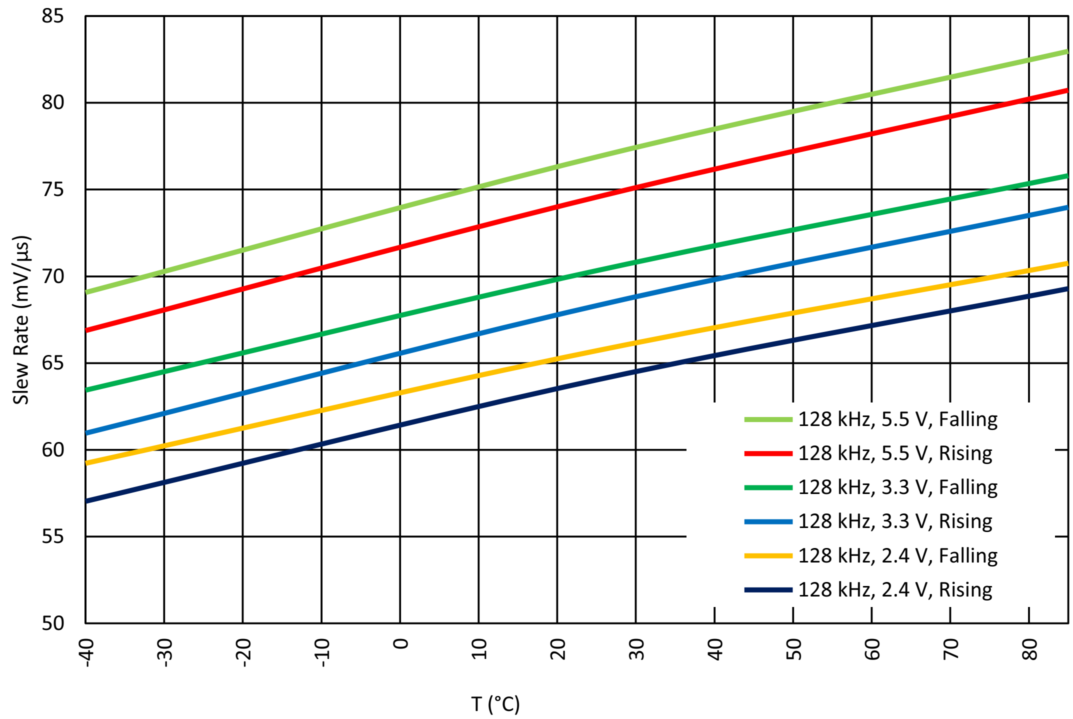


Figure 104: Slew Rate vs. Ambient Temperature G = 1 V/V; R_L = 50 kΩ for BW = 128 kHz

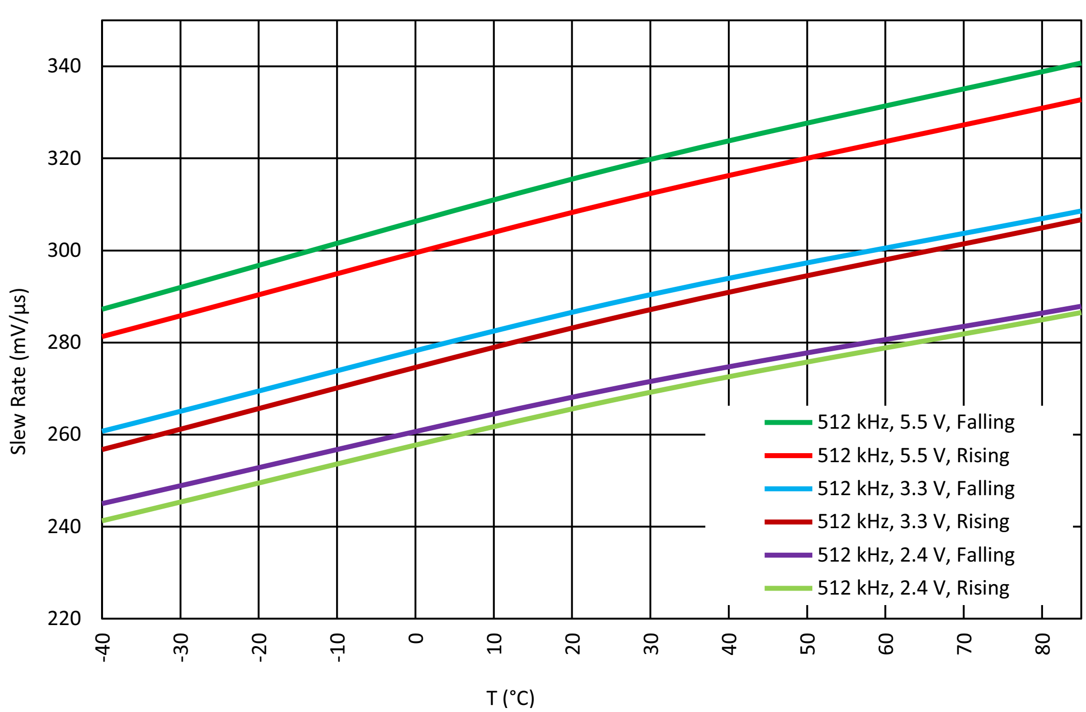


Figure 105: Slew Rate vs. Ambient Temperature G = 1 V/V; R_L = 50 kΩ for BW = 512 kHz

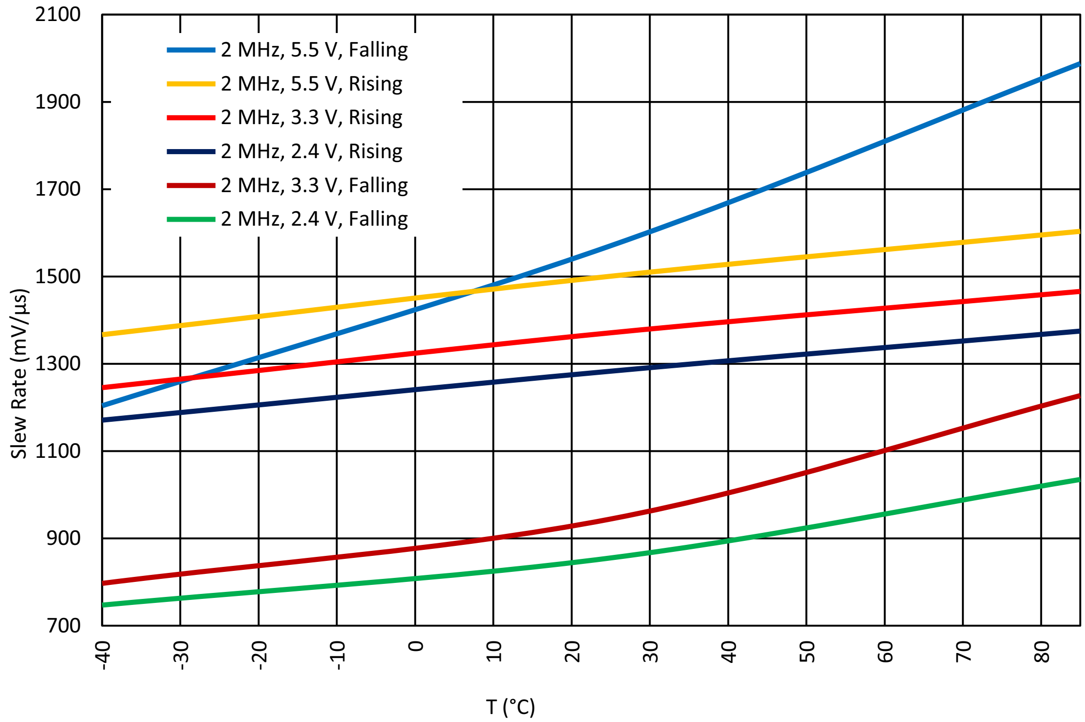


Figure 106: Slew Rate vs. Ambient Temperature G = 1 V/V; R_L = 50 kΩ for BW = 2 MHz

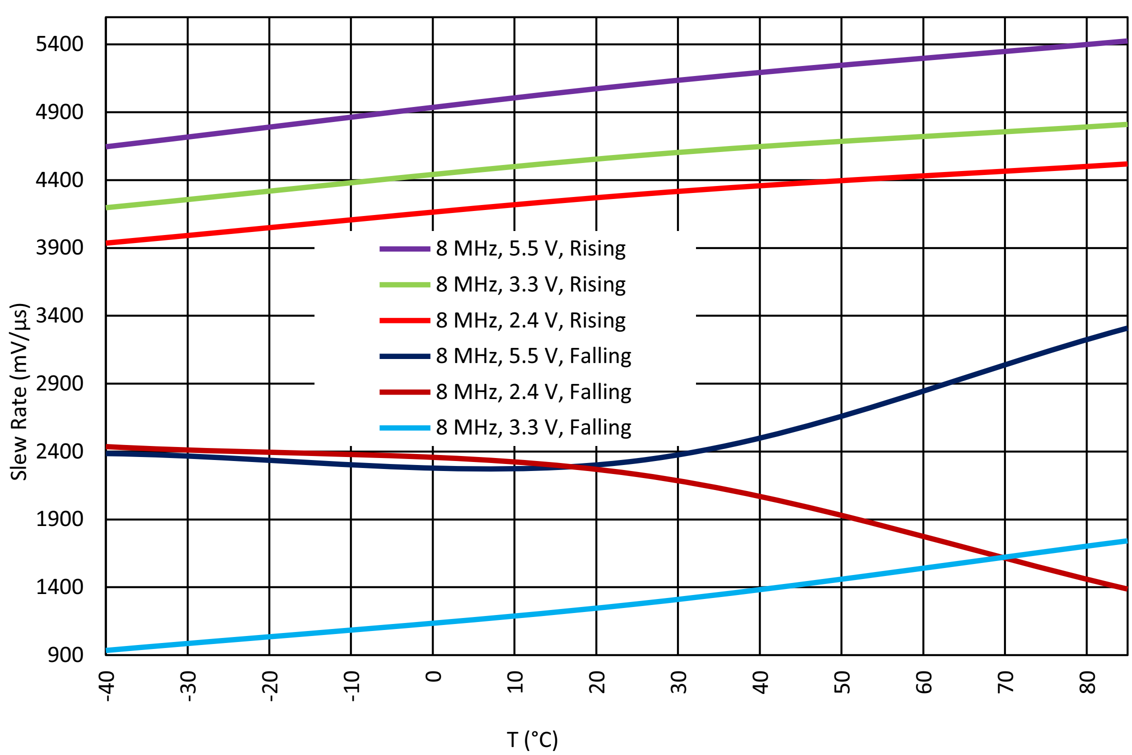


Figure 107: Slew Rate vs. Ambient Temperature G = 1 V/V; R_L = 50 kΩ for BW = 8 MHz

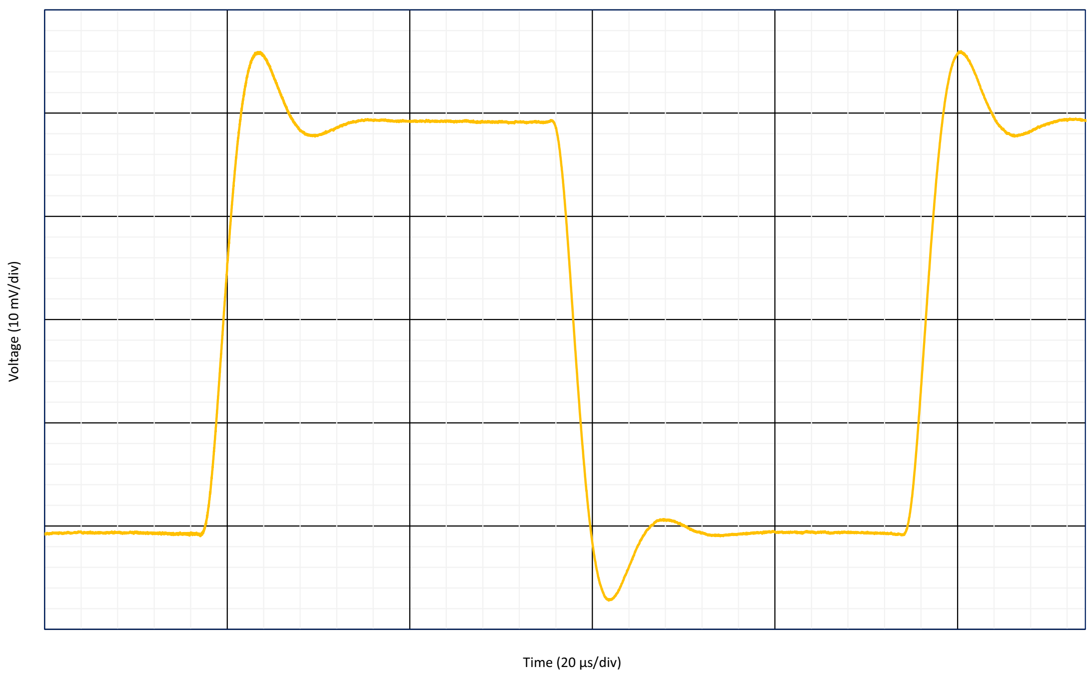


Figure 108: Small Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

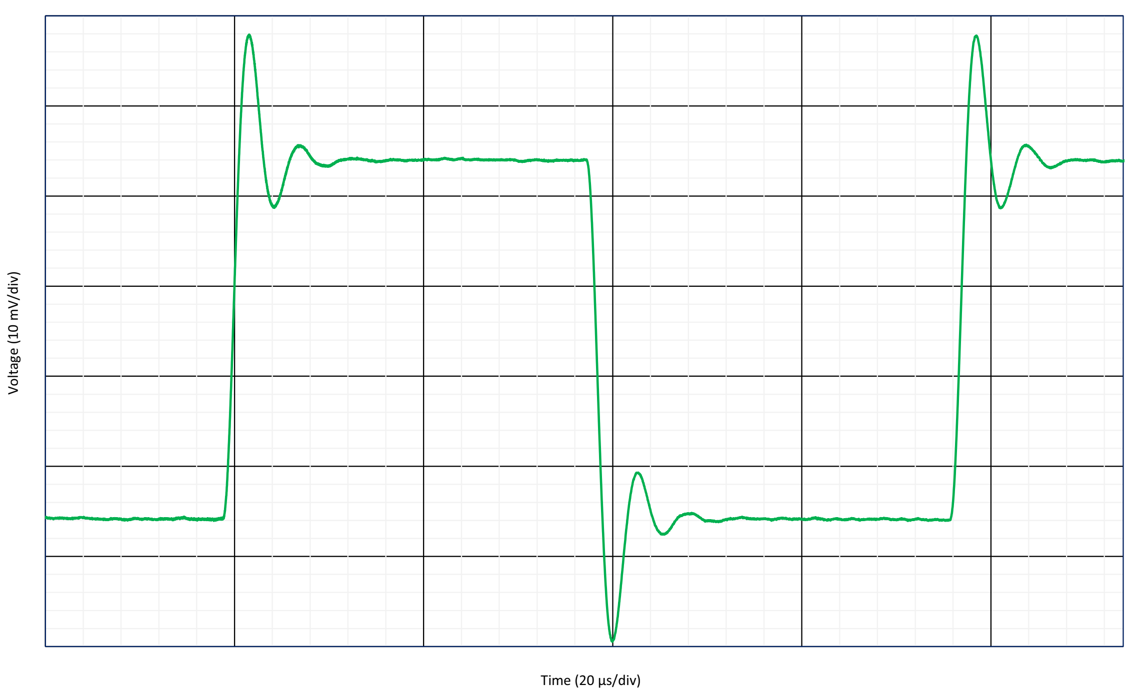


Figure 109: Small Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

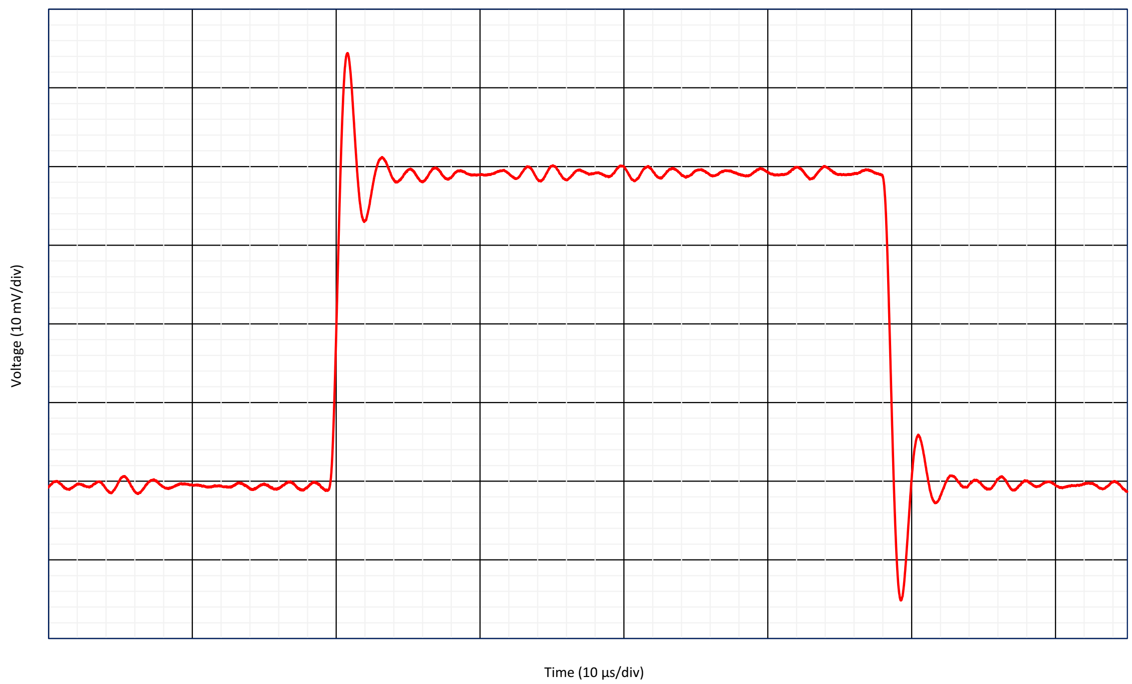


Figure 110: Small Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

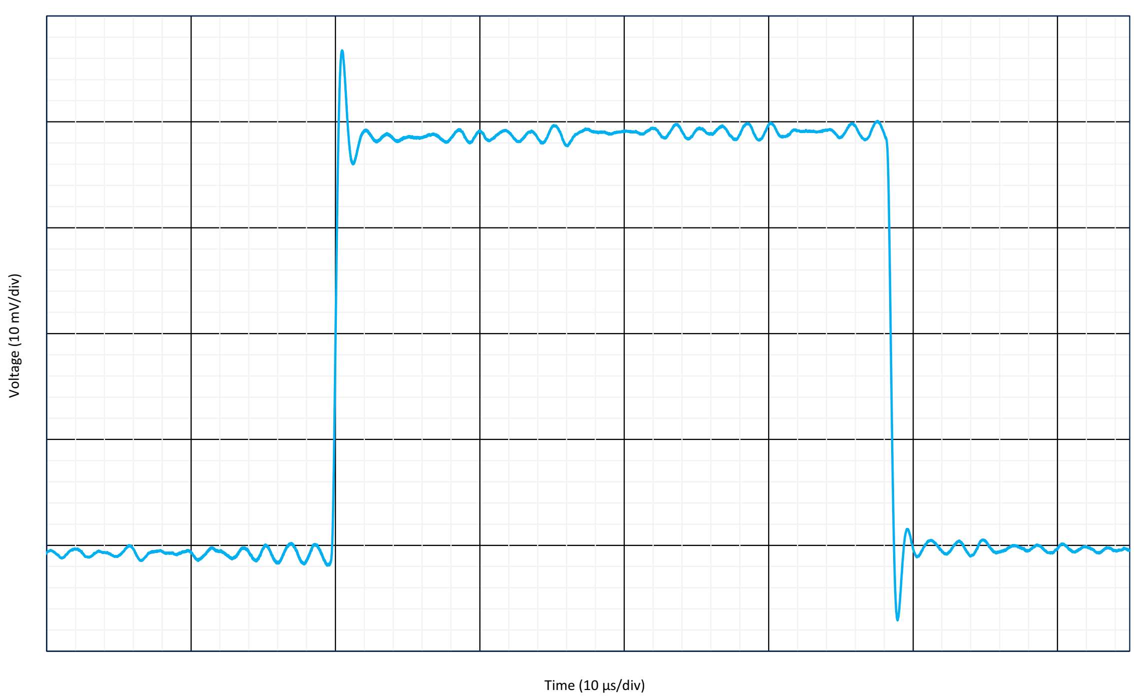


Figure 111: Small Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

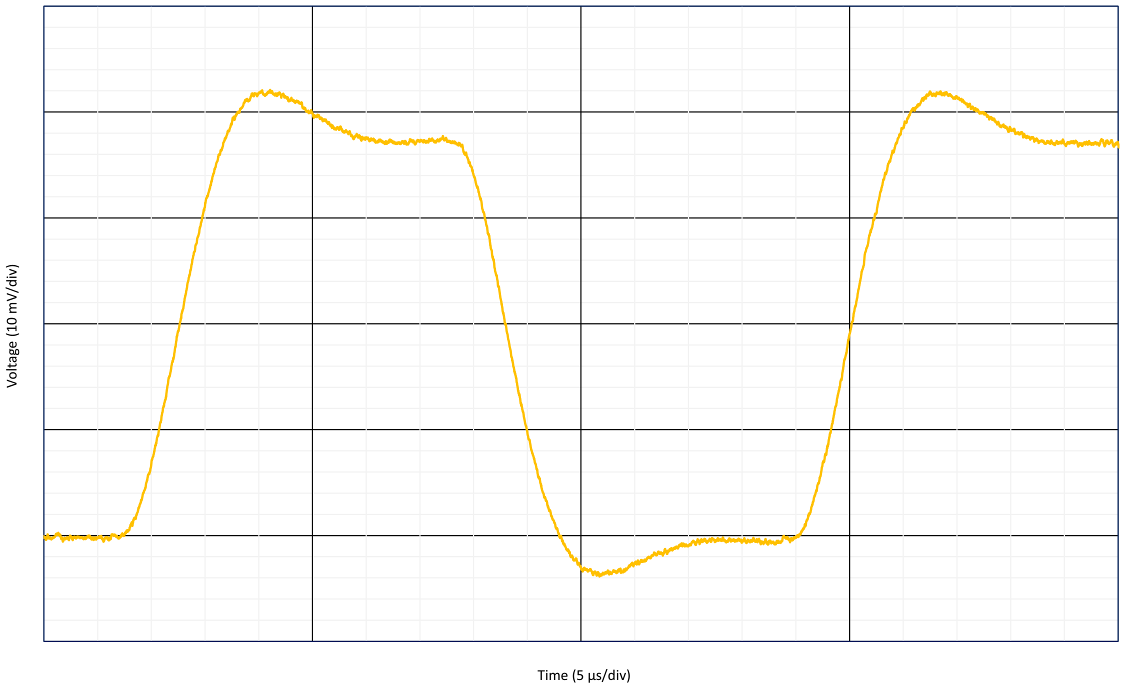


Figure 112: Small Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

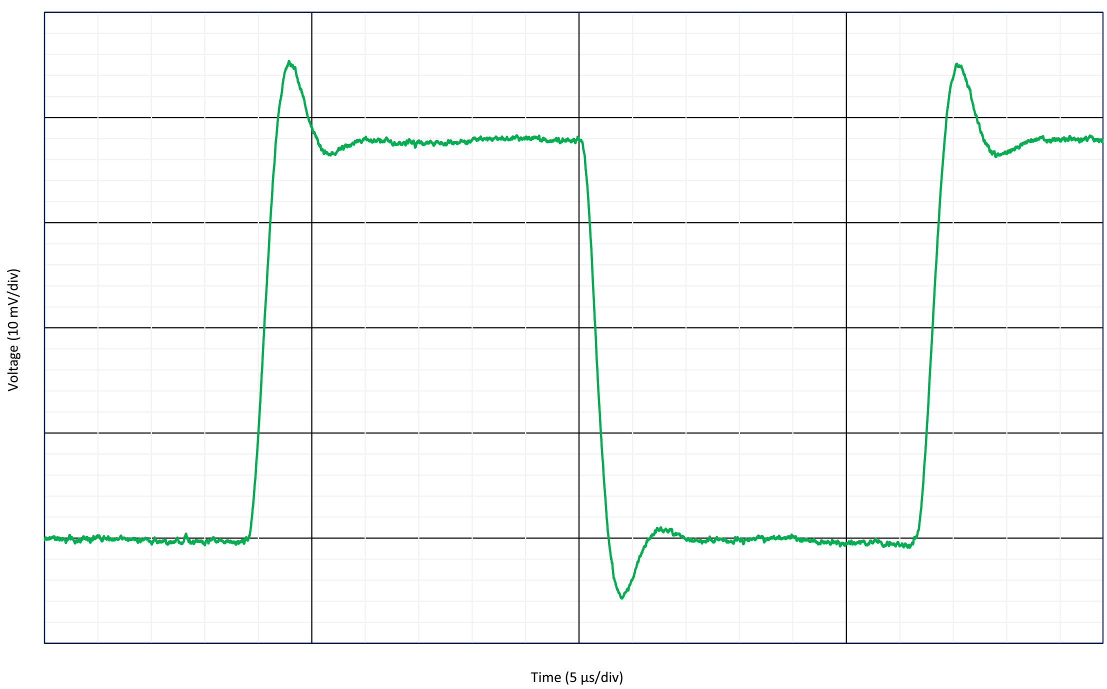


Figure 113: Small Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

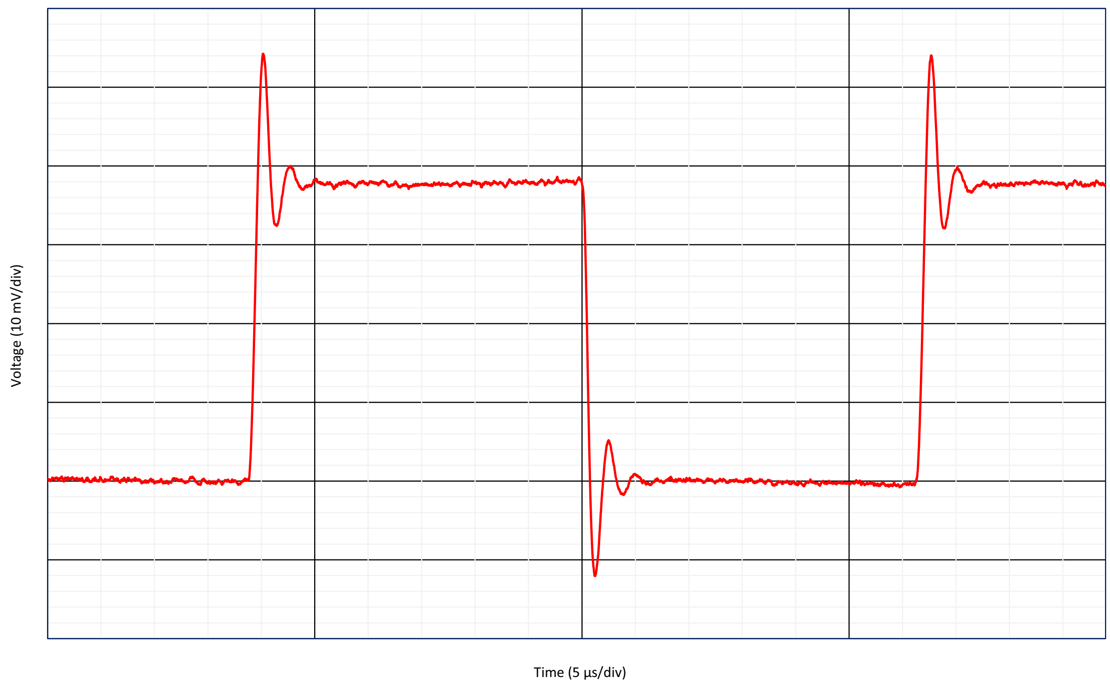


Figure 114: Small Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

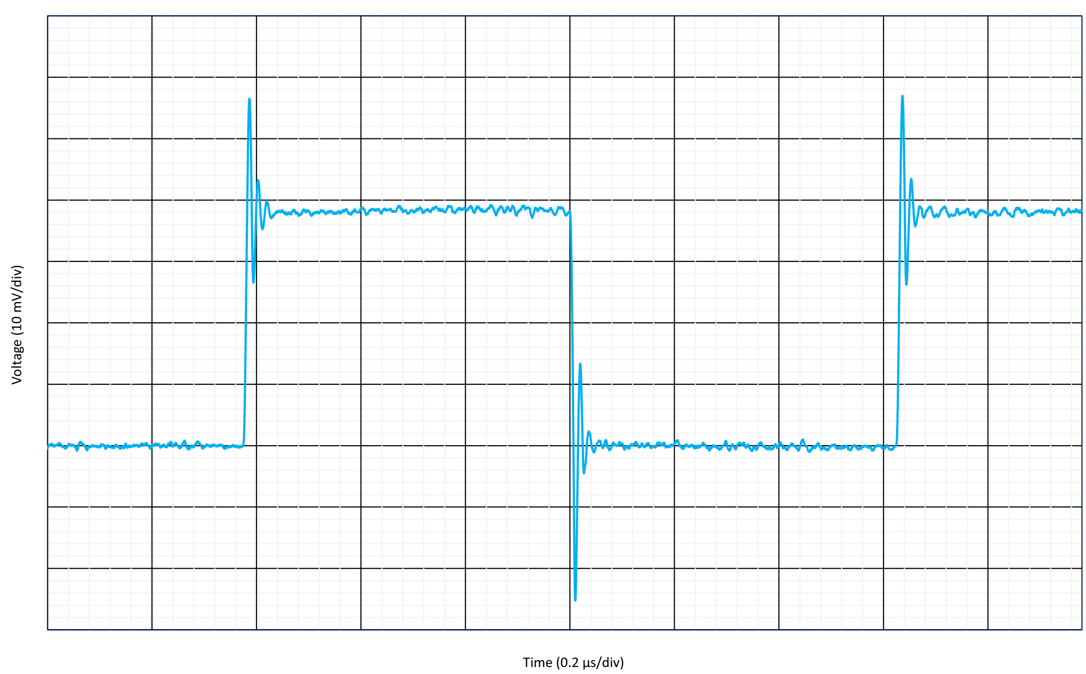


Figure 115: Small Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

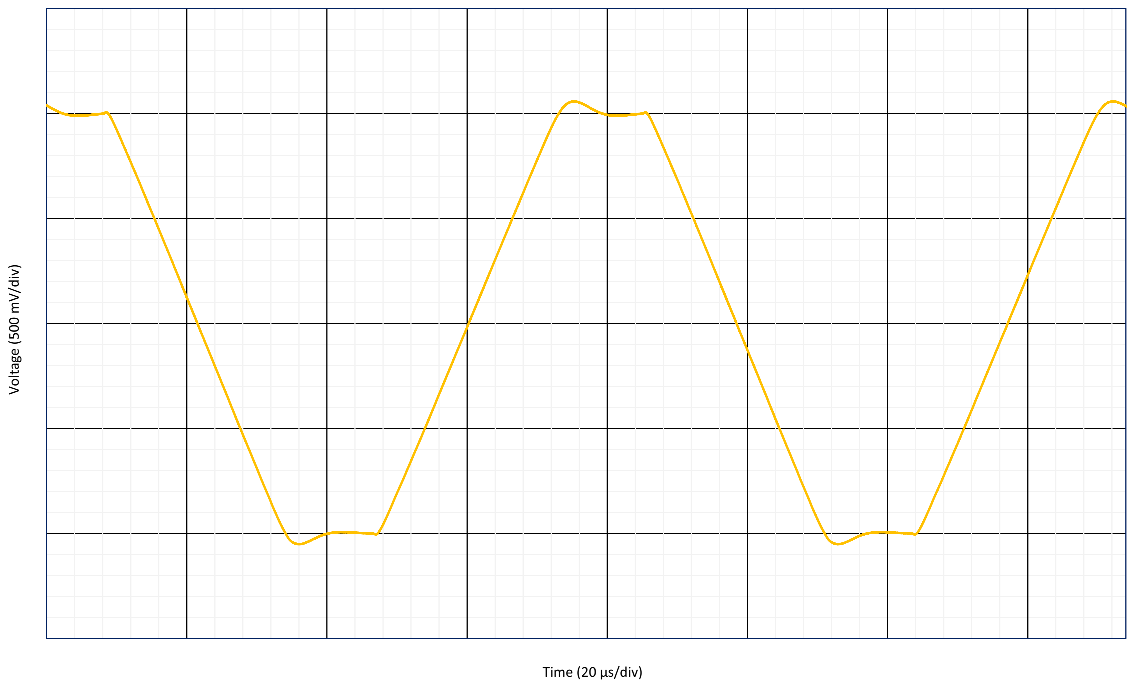


Figure 116: Large Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 80 pF, BW = 128 kHz

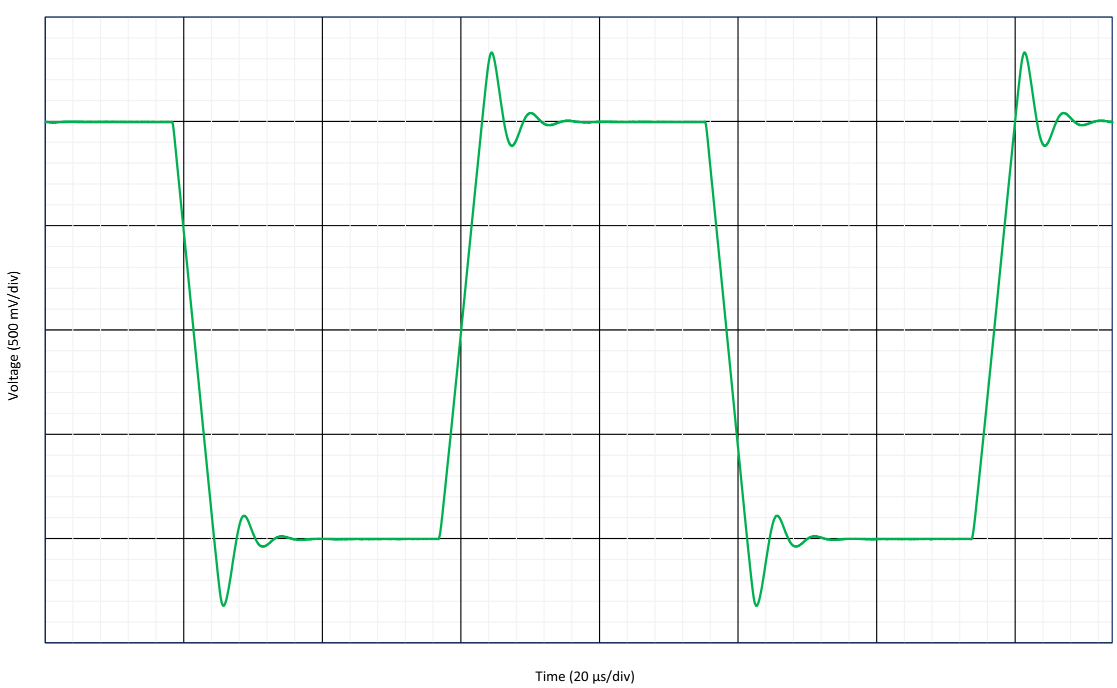


Figure 117: Large Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 80 pF, BW = 512kHz

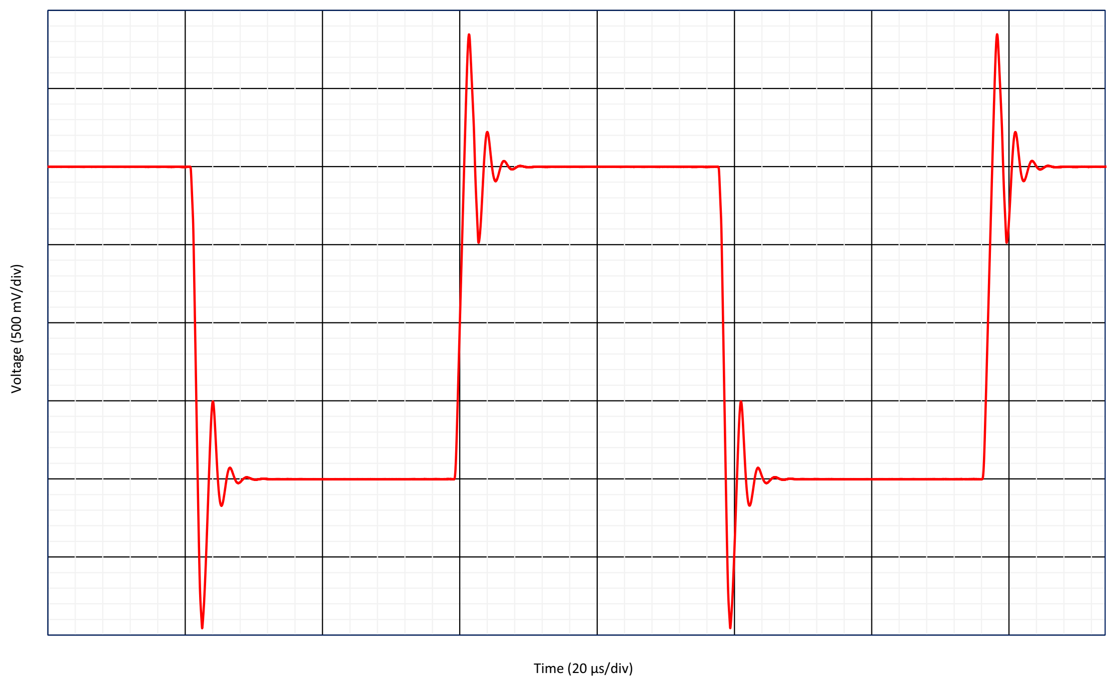


Figure 118: Large Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 80 pF, BW = 2 MHz

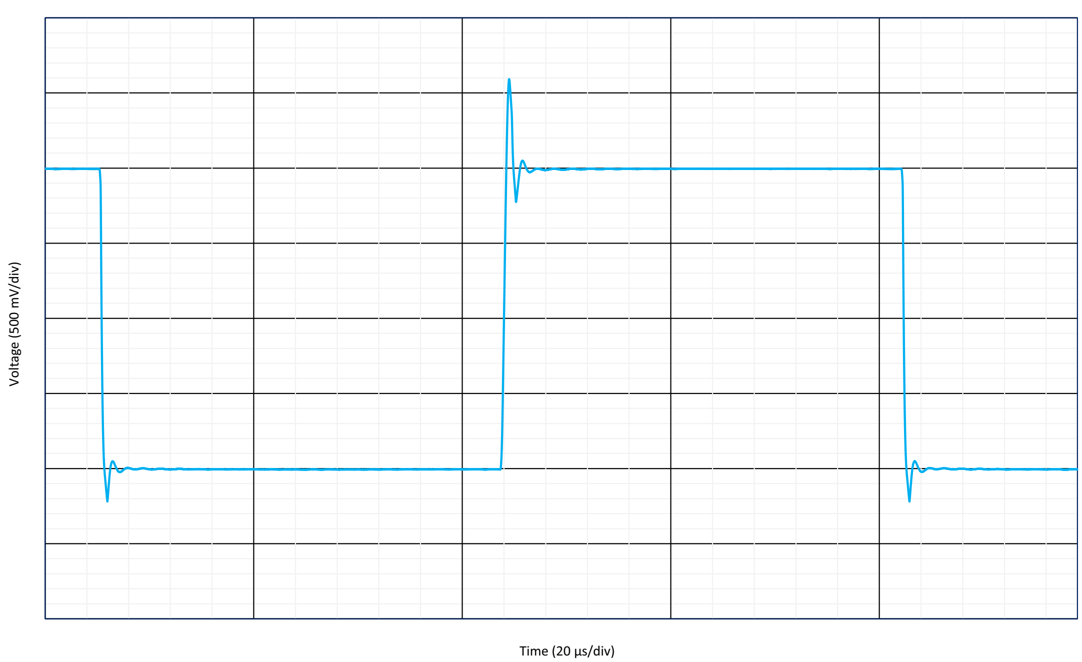


Figure 119: Large Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 80 pF, BW = 8 MHz

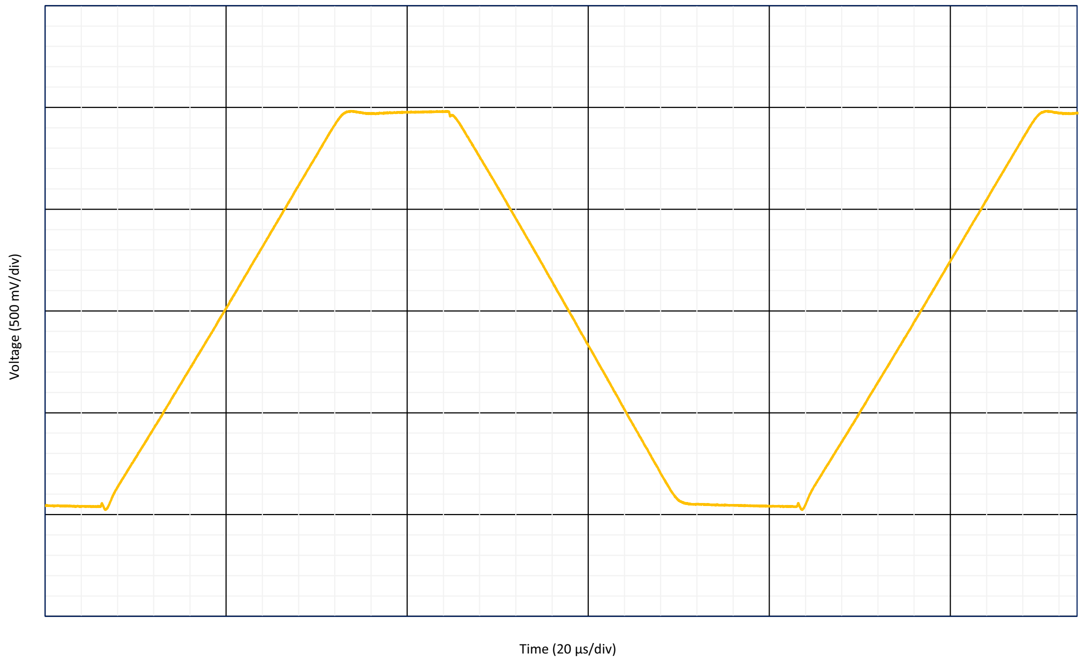


Figure 120: Large Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

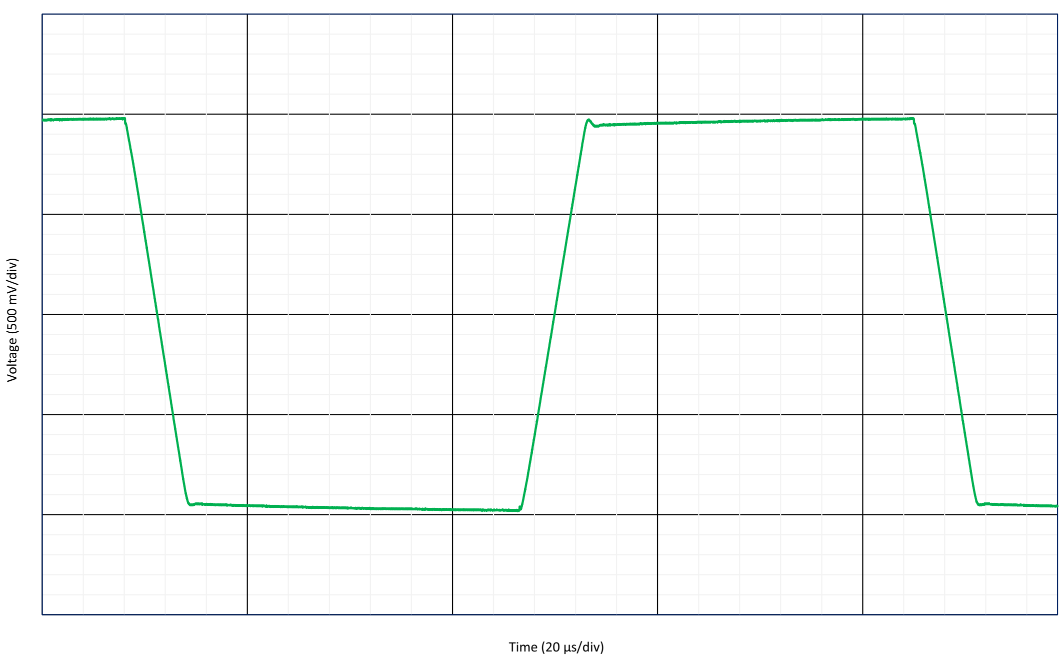


Figure 121: Large Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

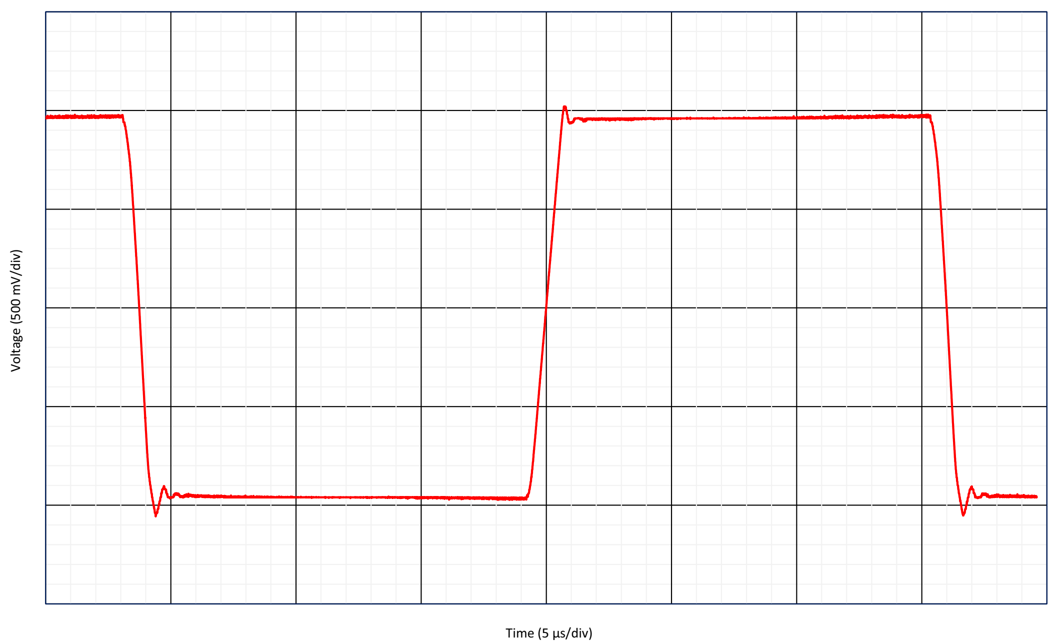


Figure 122: Large Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

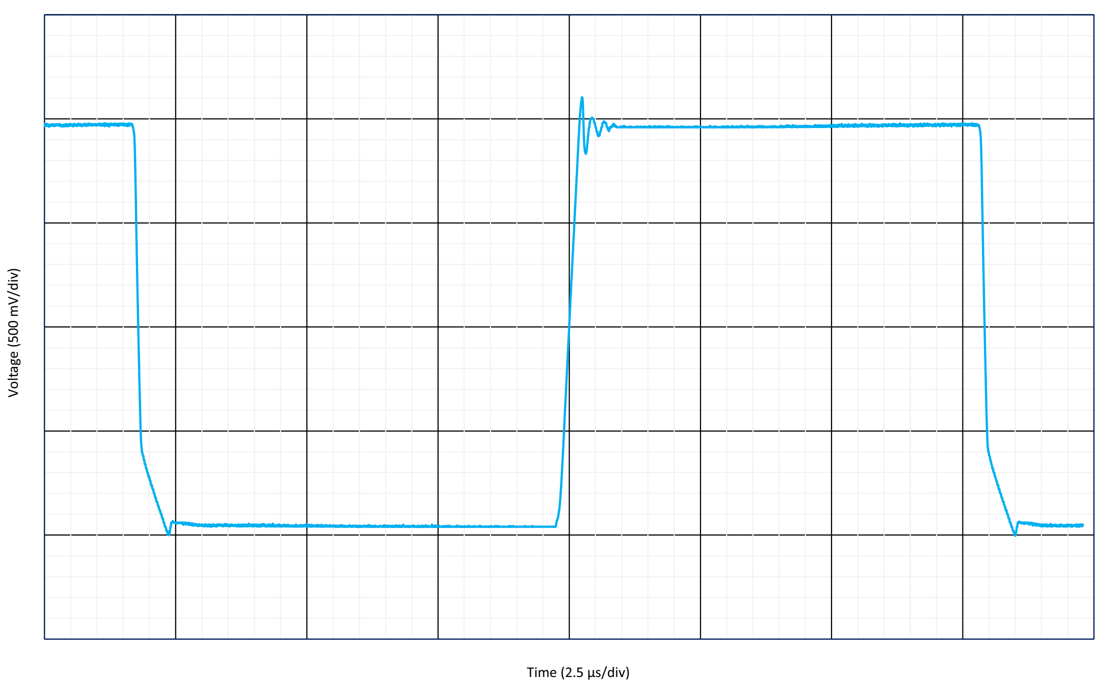


Figure 123: Large Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

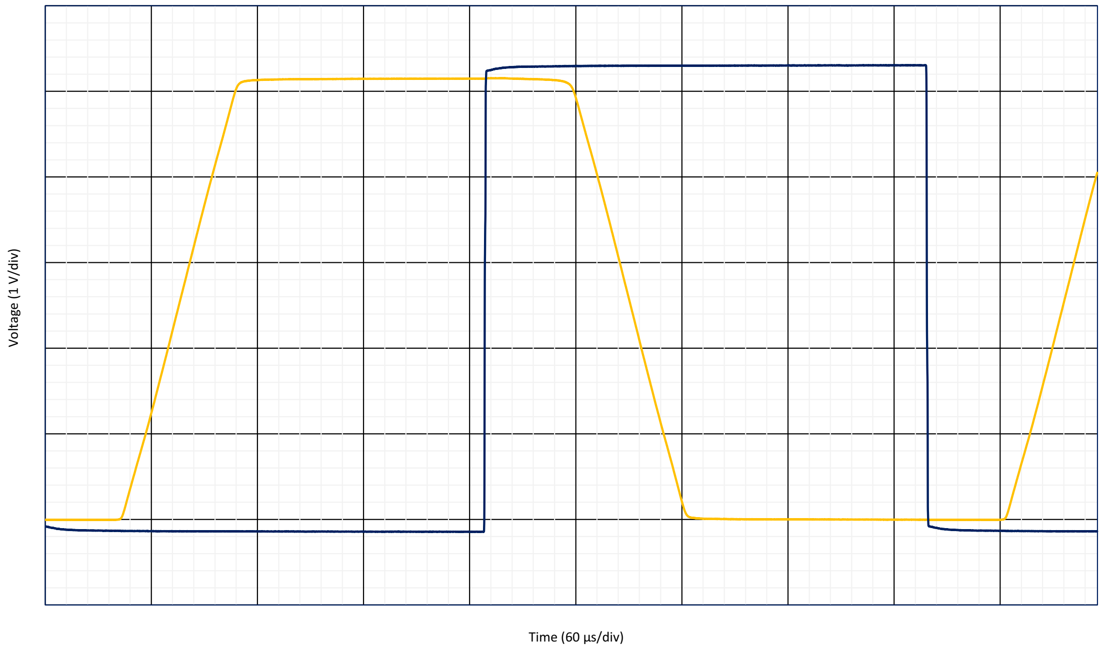


Figure 124: Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

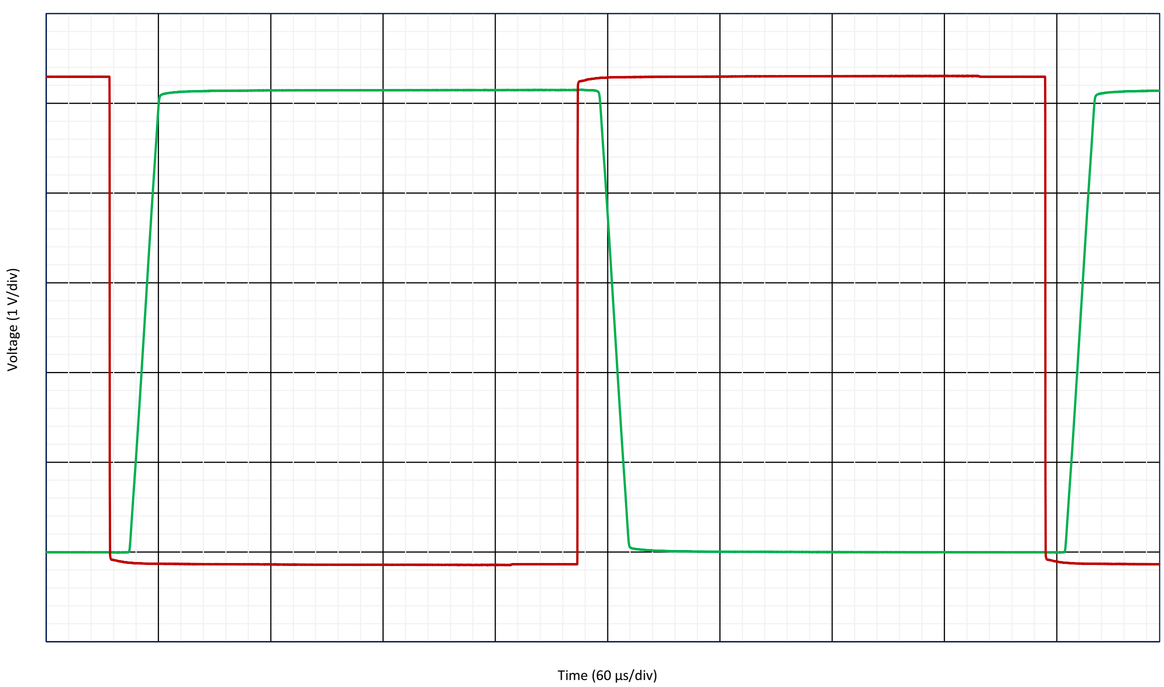


Figure 125: Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

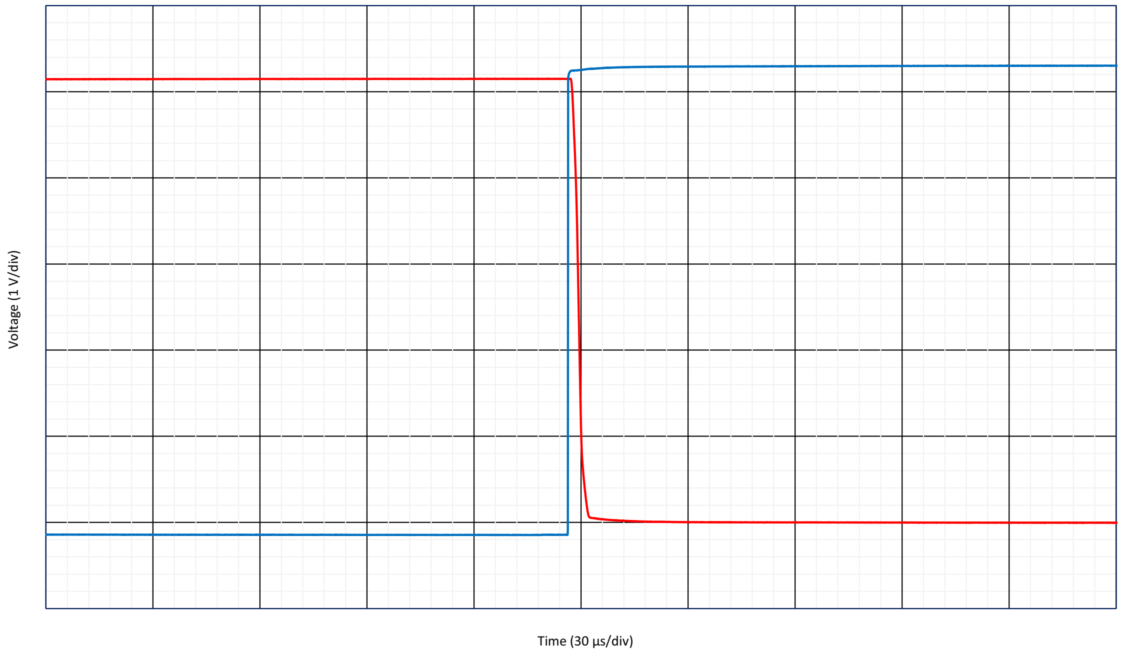


Figure 126: Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

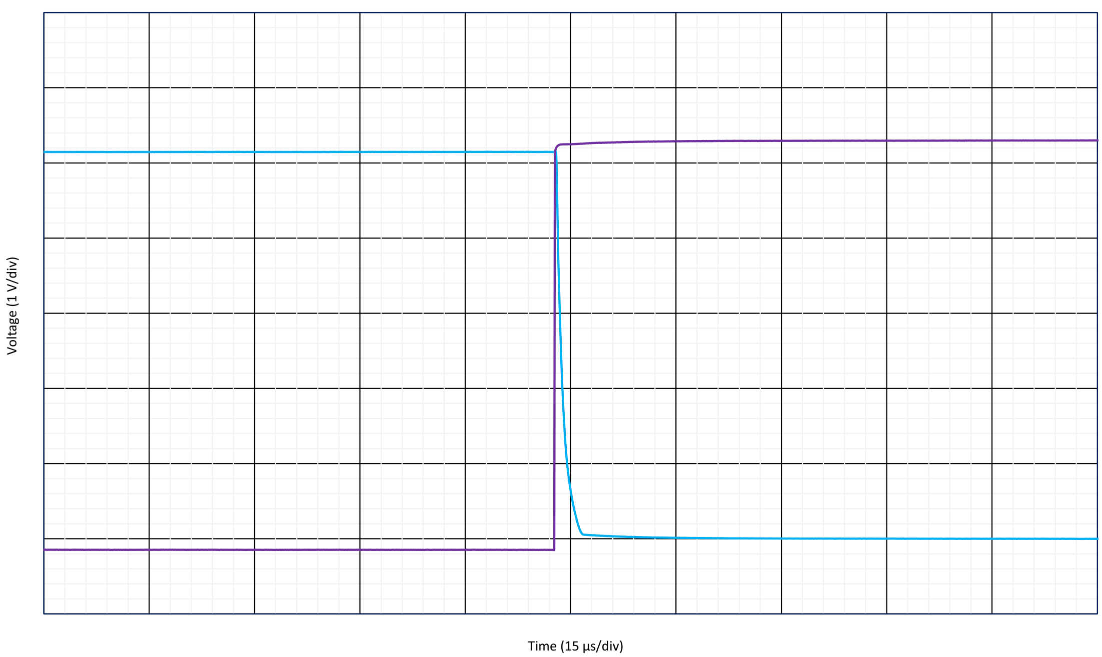


Figure 127: Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

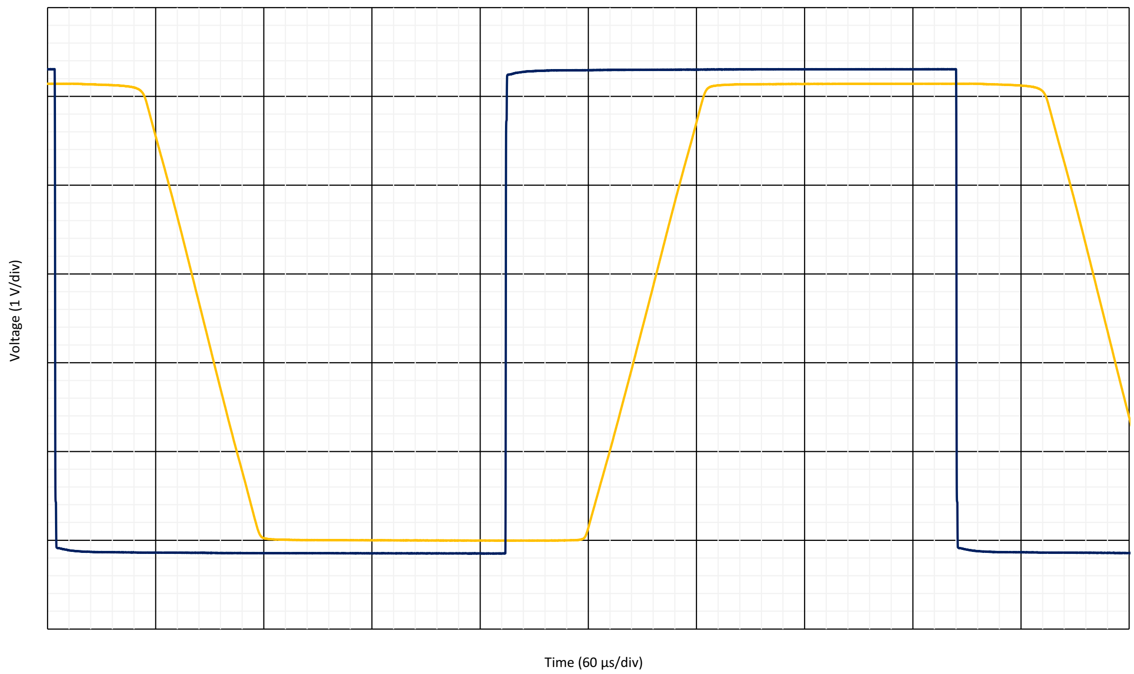


Figure 128: Non-Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

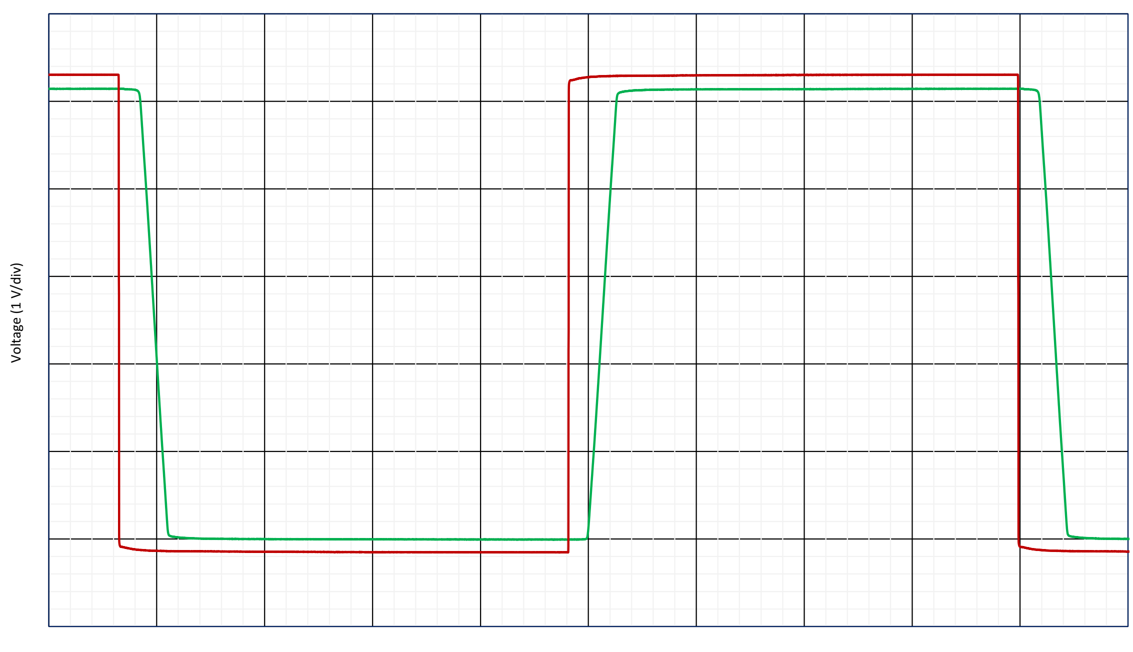


Figure 129: Non-Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

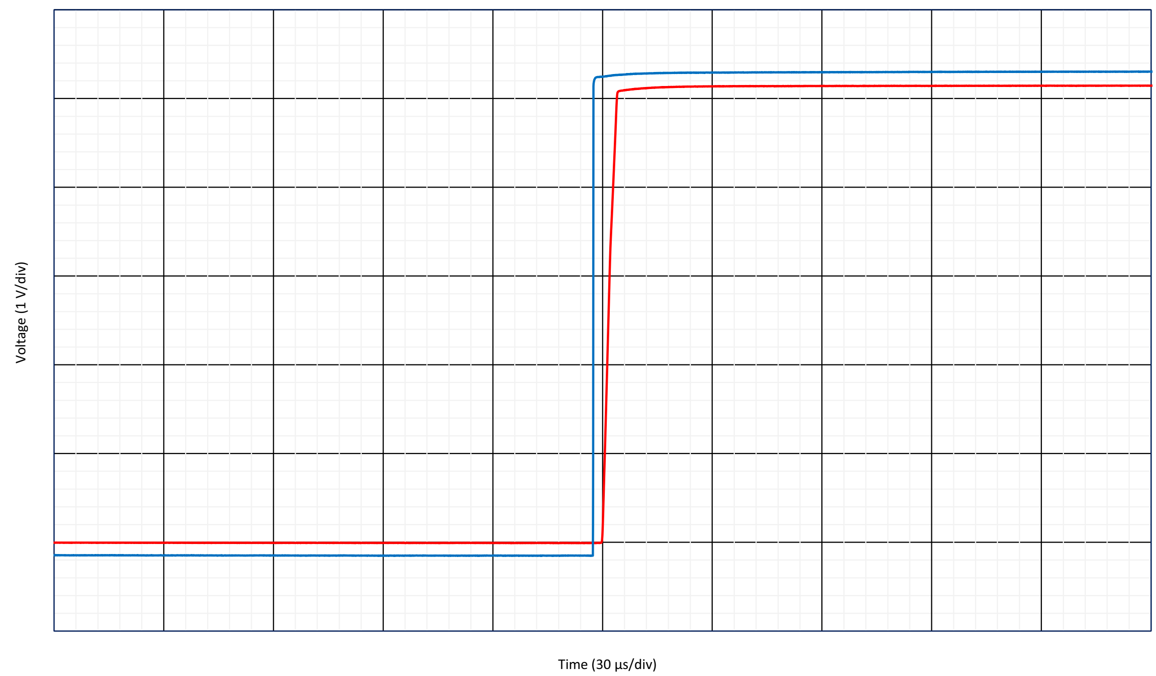


Figure 130: Non-Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

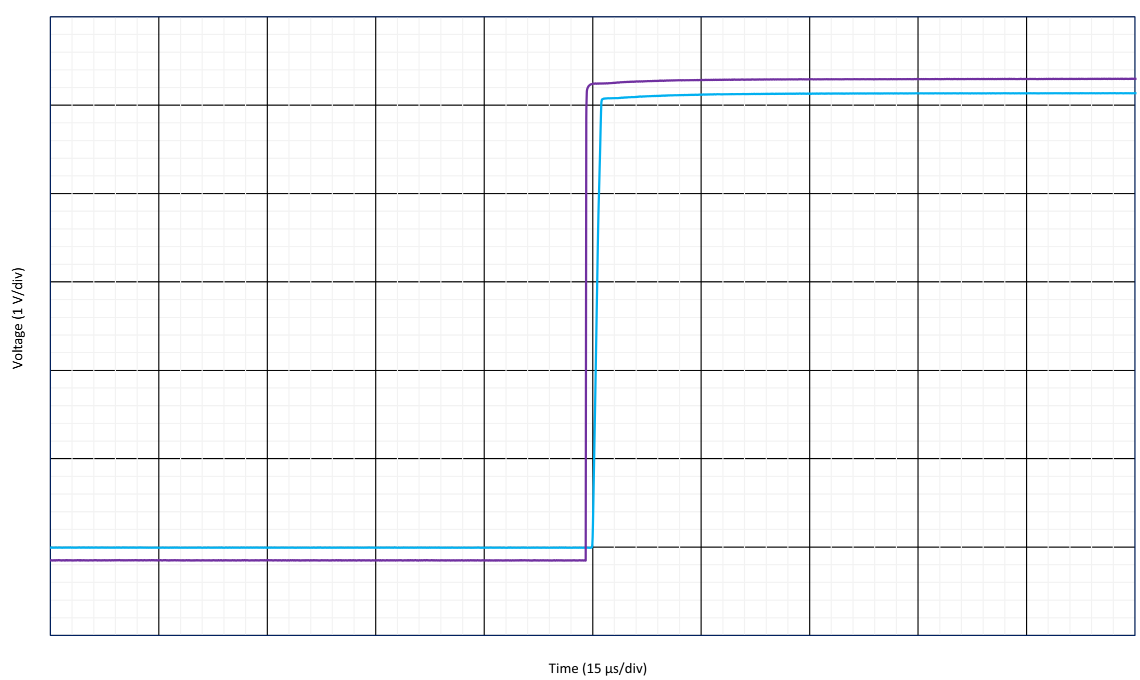


Figure 131: Non-Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

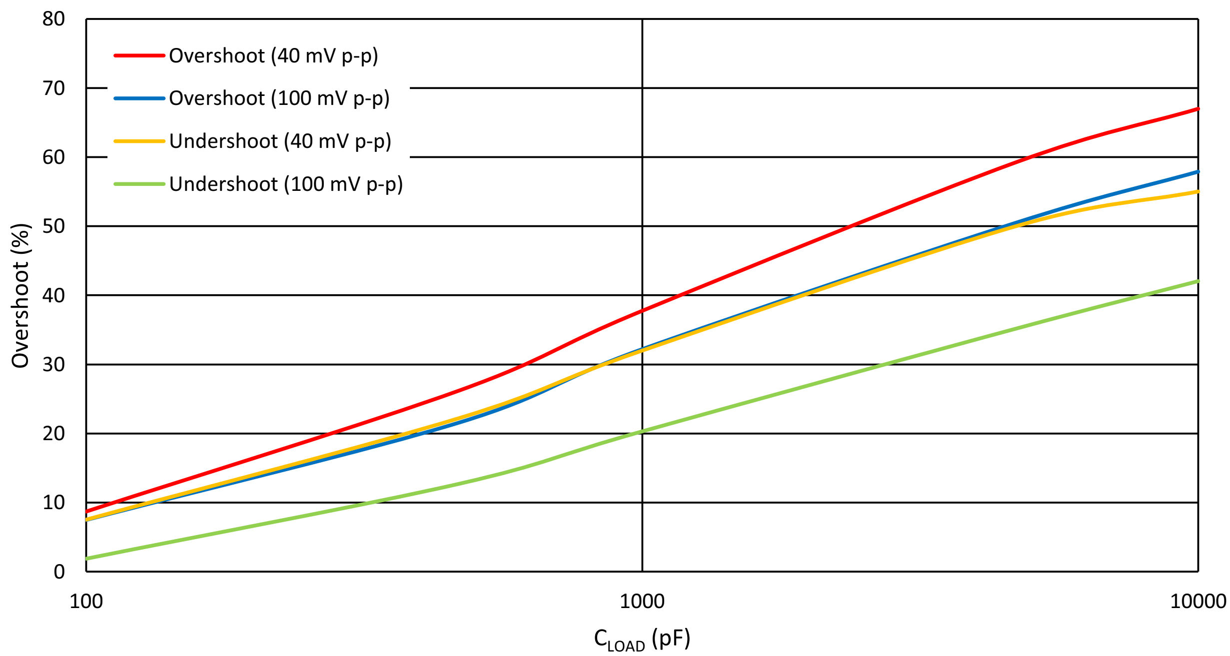


Figure 132: Small Signal Overshoot vs. Capacitive Load V_{DD} = 3.3 V, G = 1 V/V, BW = 128 kHz

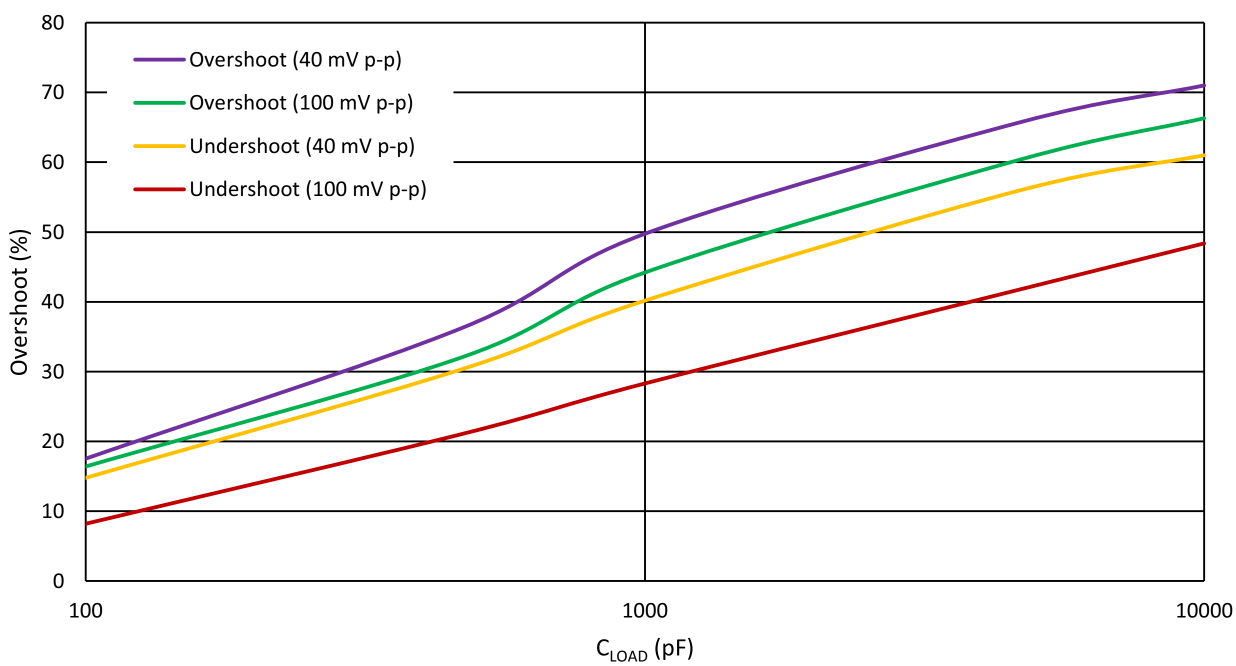


Figure 133: Small Signal Overshoot vs. Capacitive Load V_{DD} = 3.3 V, G = 1 V/V, BW = 512 kHz

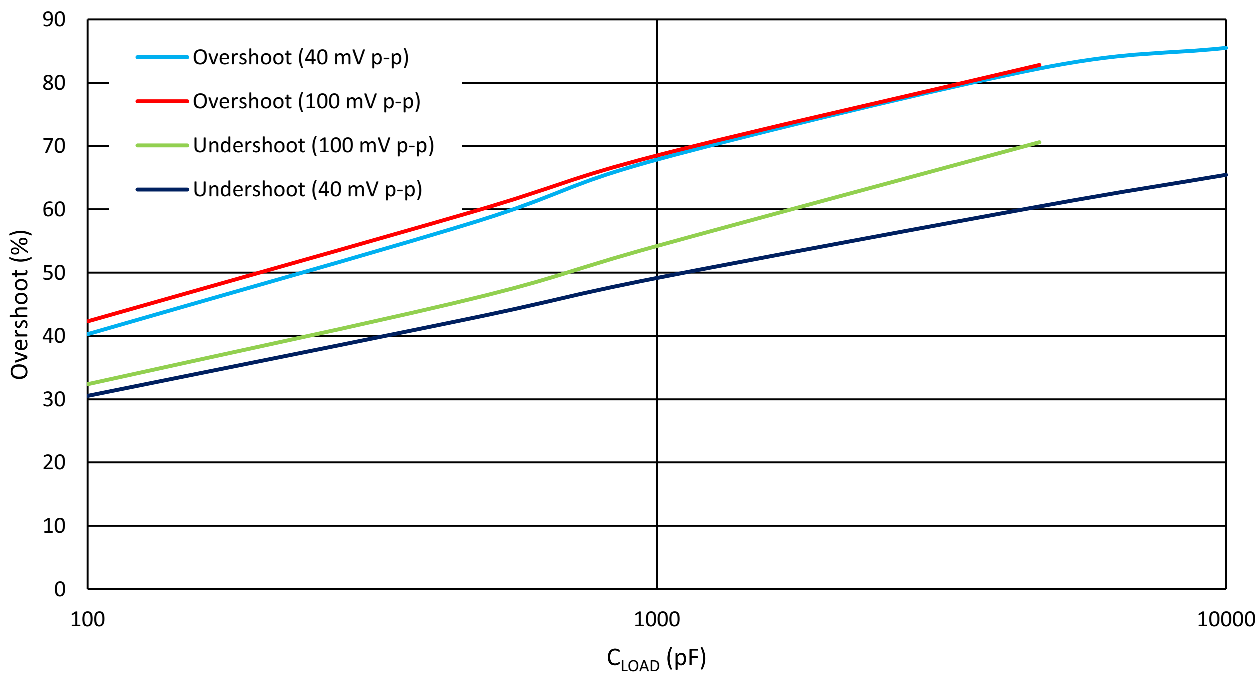


Figure 134: Small Signal Overshoot vs. Capacitive Load V_{DD} = 3.3 V, G = 1 V/V, BW = 2 MHz

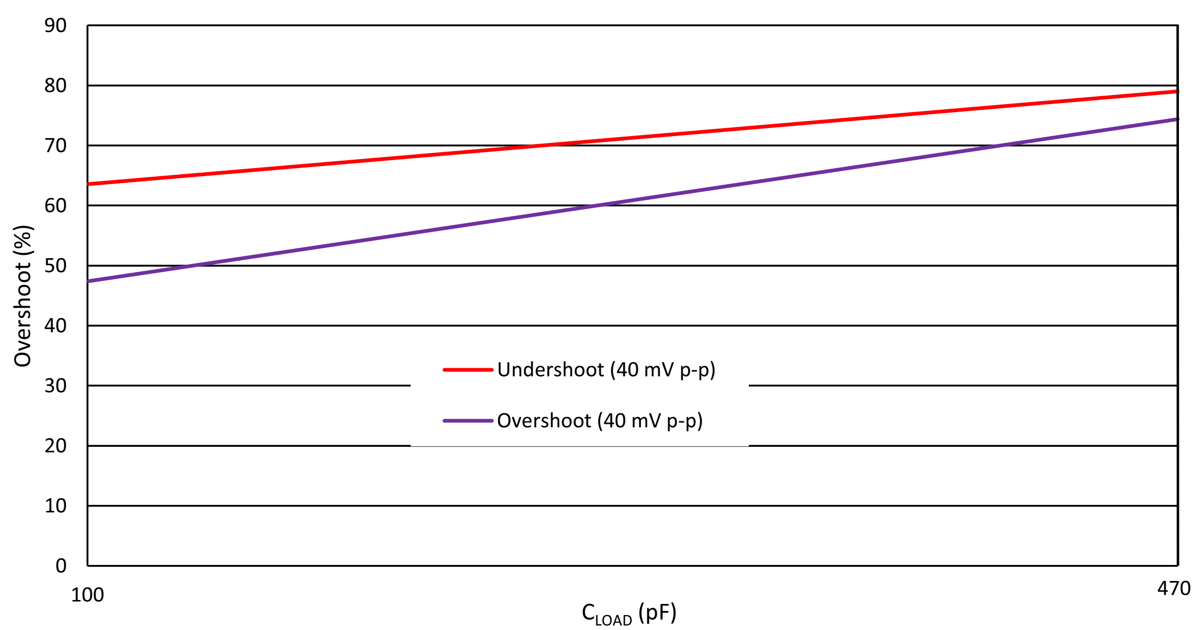


Figure 135: Small Signal Overshoot vs. Capacitive Load V_{DD} = 3.3 V, G = 1 V/V, BW = 8 MHz

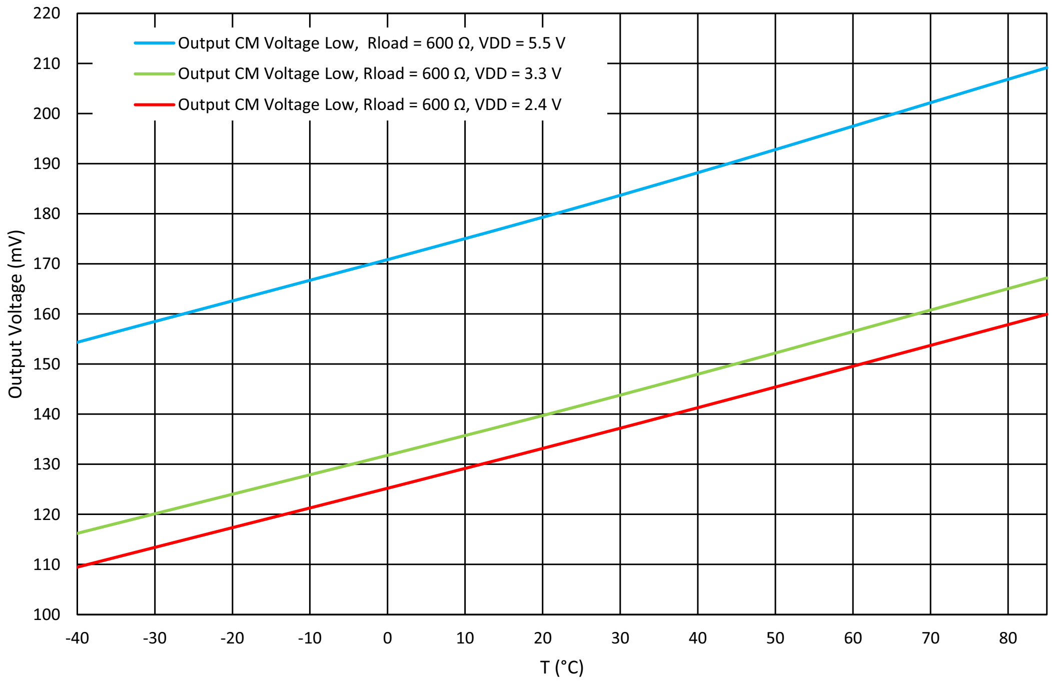


Figure 136: Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 128 kHz, R_{LOAD} = 600 Ω

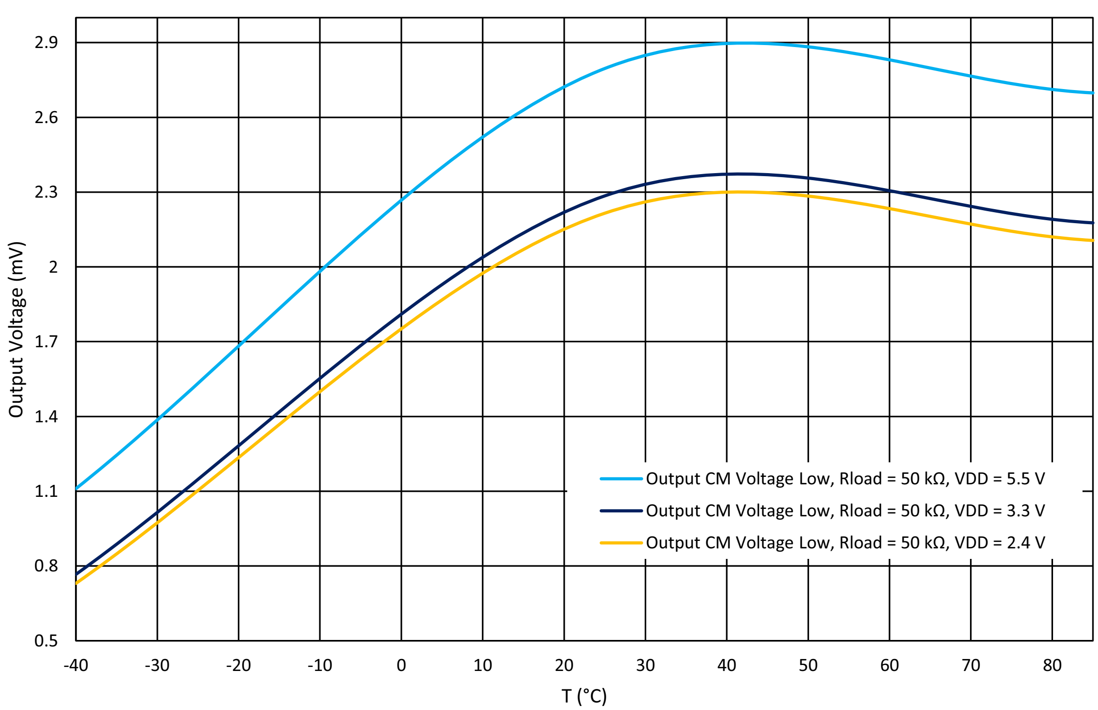


Figure 137: Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 128 kHz, R_{LOAD} = 50 kΩ

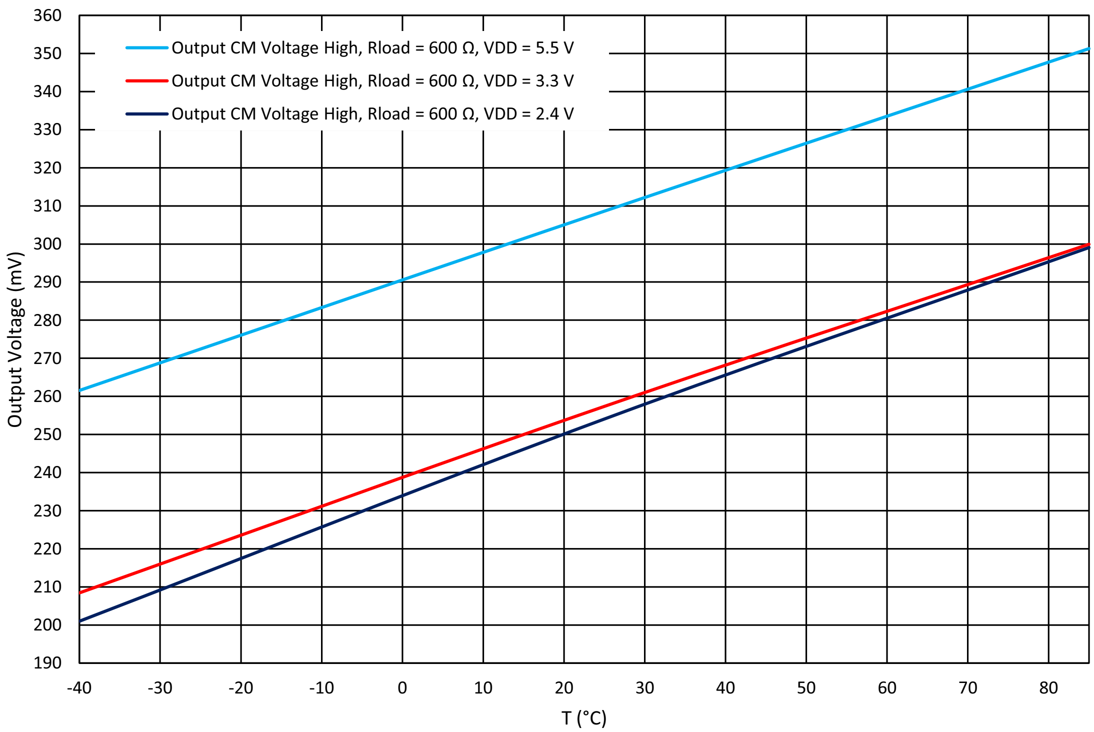


Figure 138: Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 128 kHz, R_{LOAD} = 600 Ω

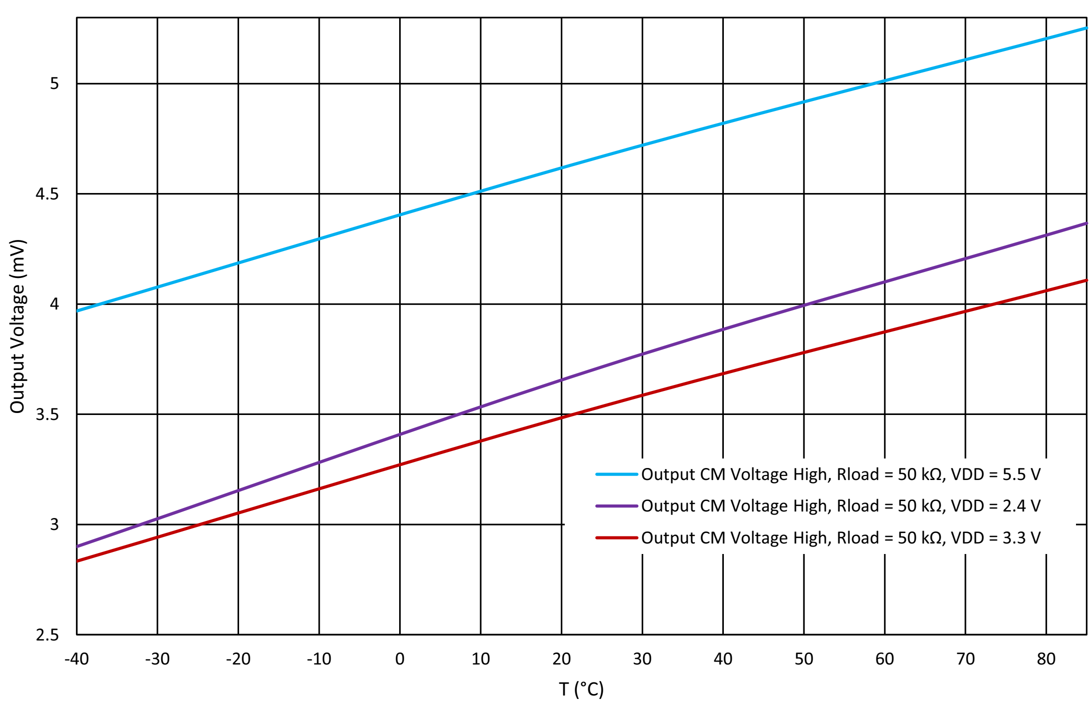


Figure 139: Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 128 kHz, R_{LOAD} = 50 kΩ

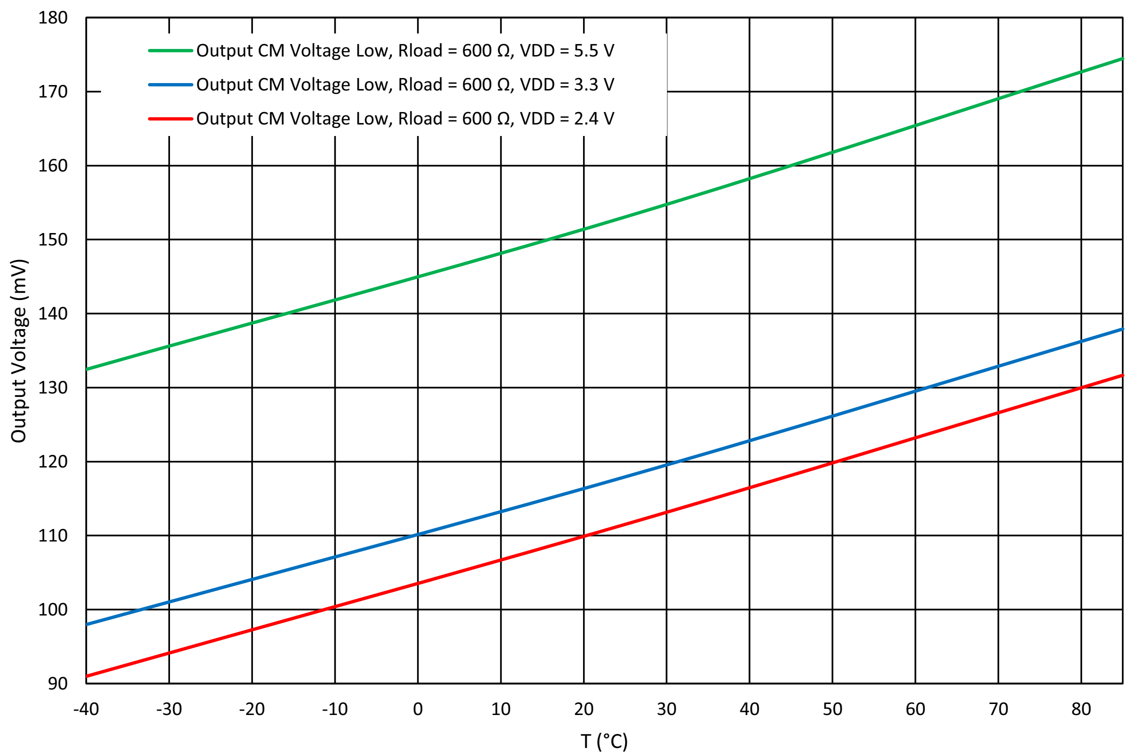


Figure 140: Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 512 kHz, R_{LOAD} = 600 Ω

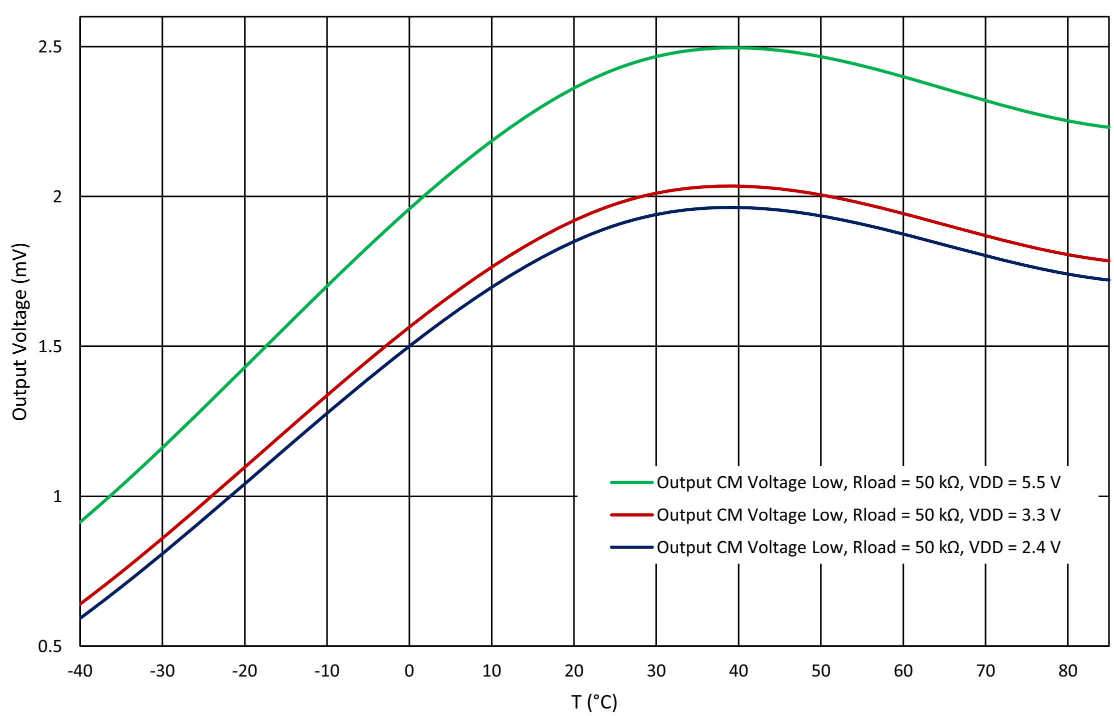


Figure 141: Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 512 kHz, R_{LOAD} = 50 kΩ

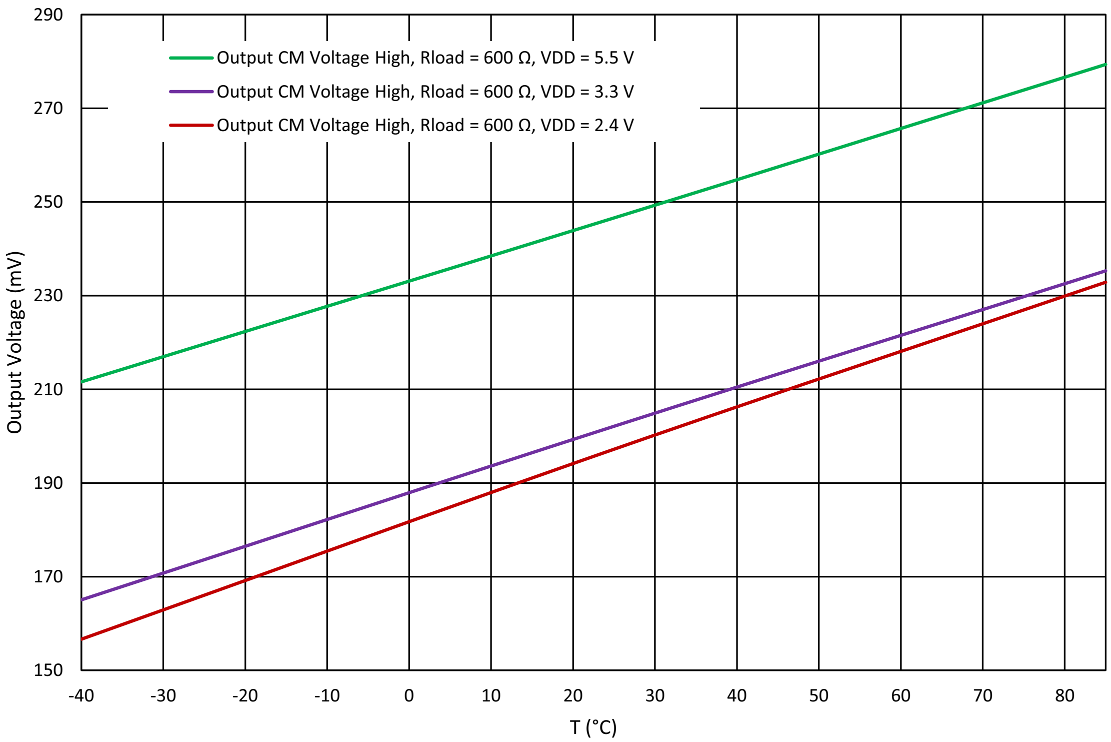


Figure 142: Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 512 kHz, R_{LOAD} = 600 Ω

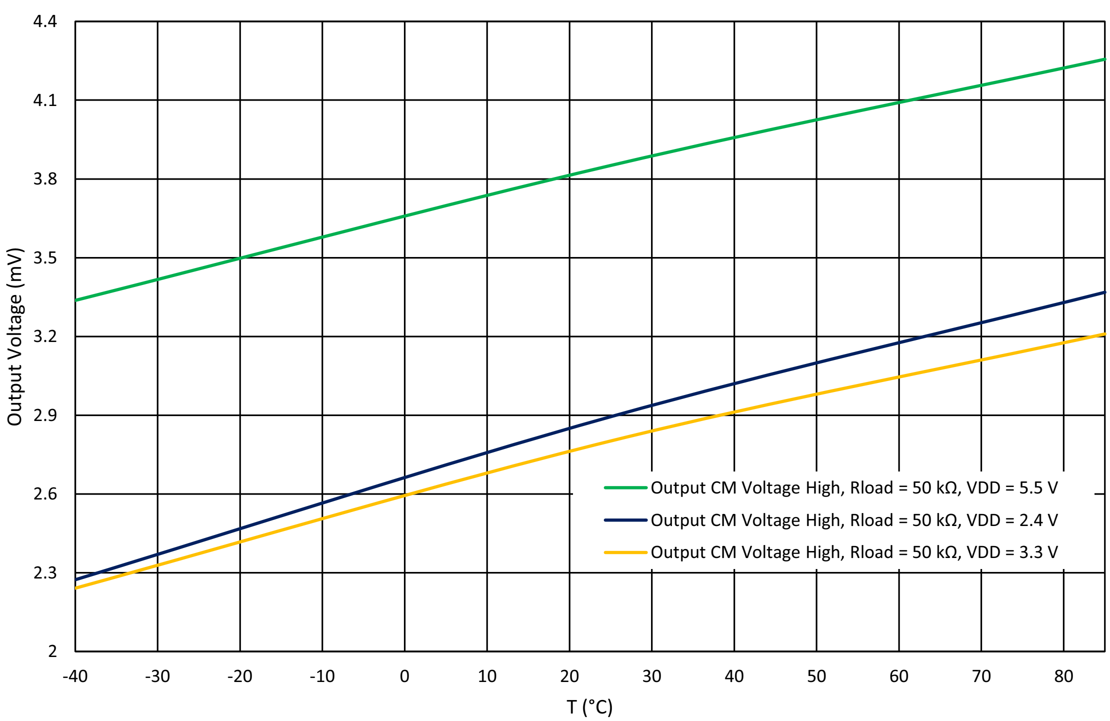


Figure 143: Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 512kHz, R_{LOAD} = 50 kΩ

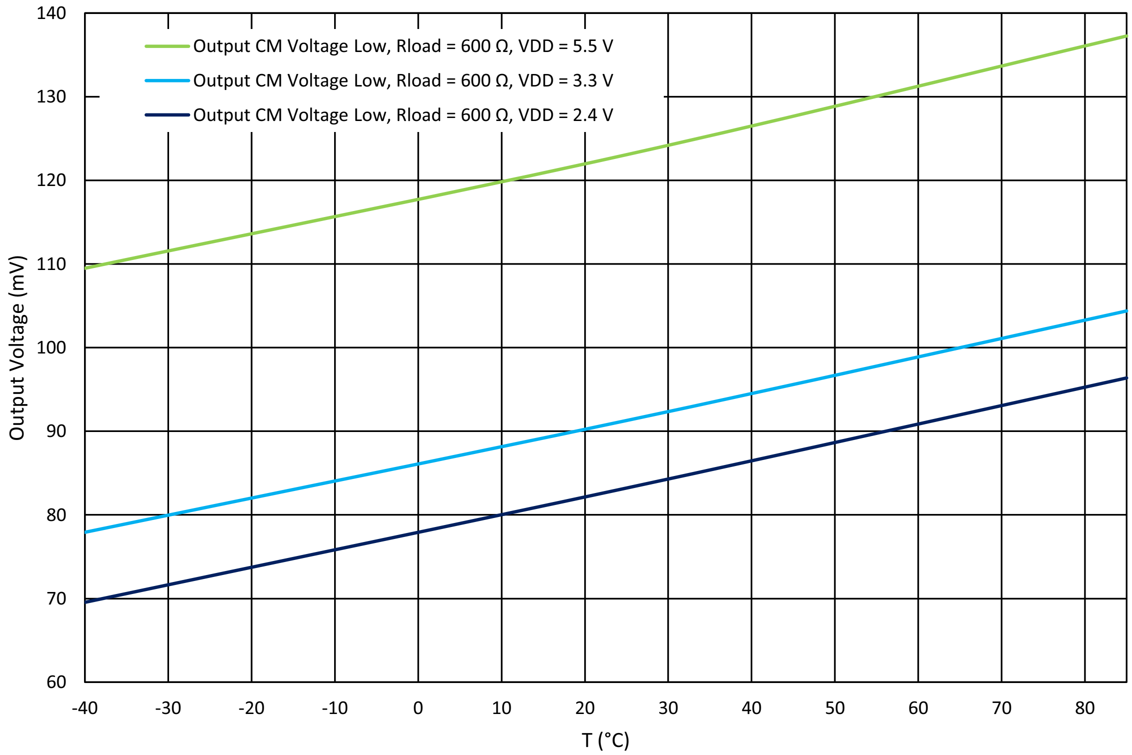


Figure 144: Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 2 MHz, R_{LOAD} = 600 Ω

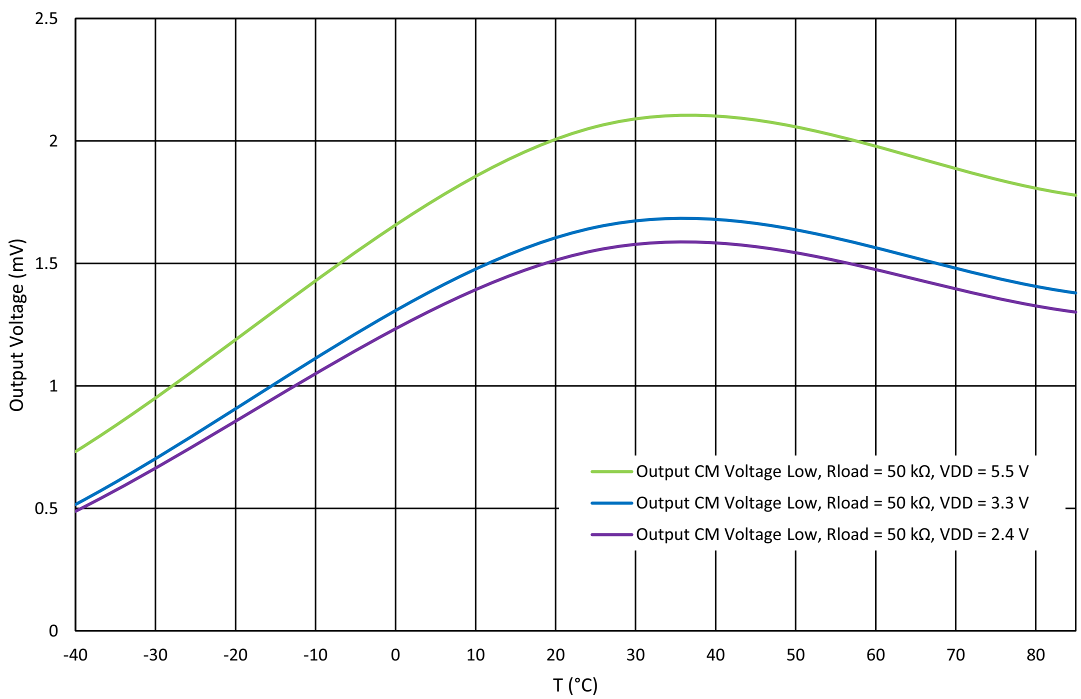


Figure 145: Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 2 MHz, R_{LOAD} = 50 kΩ

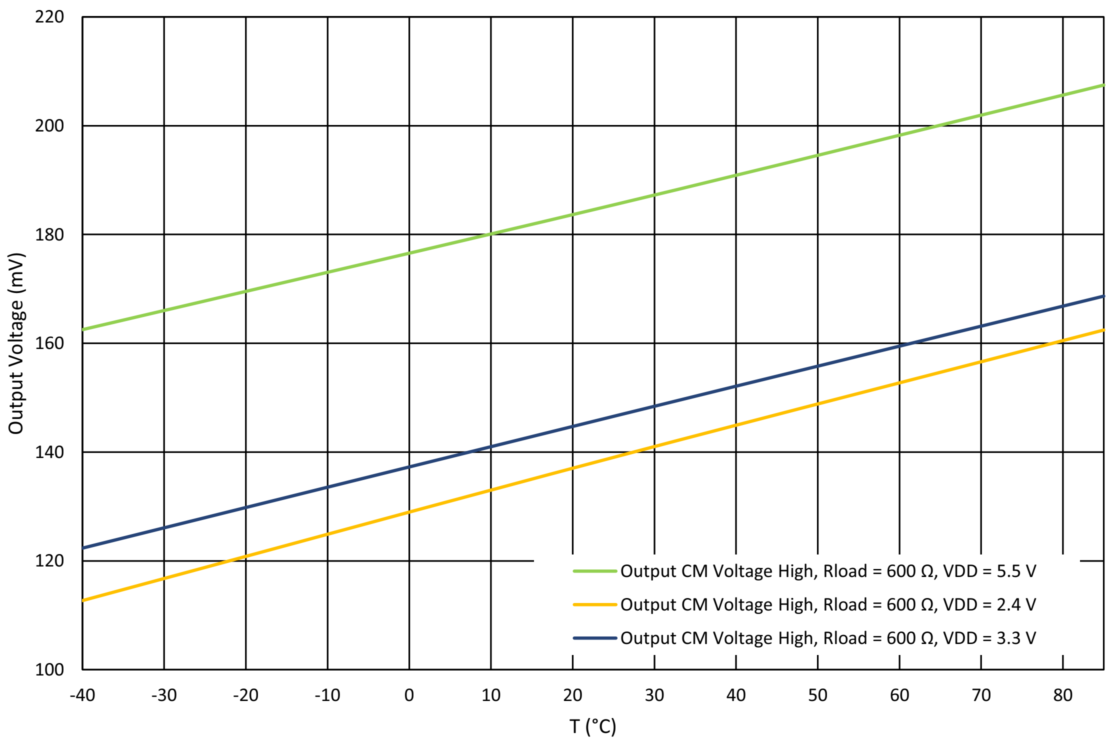


Figure 146: Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 2 MHz, R_{LOAD} = 600 Ω

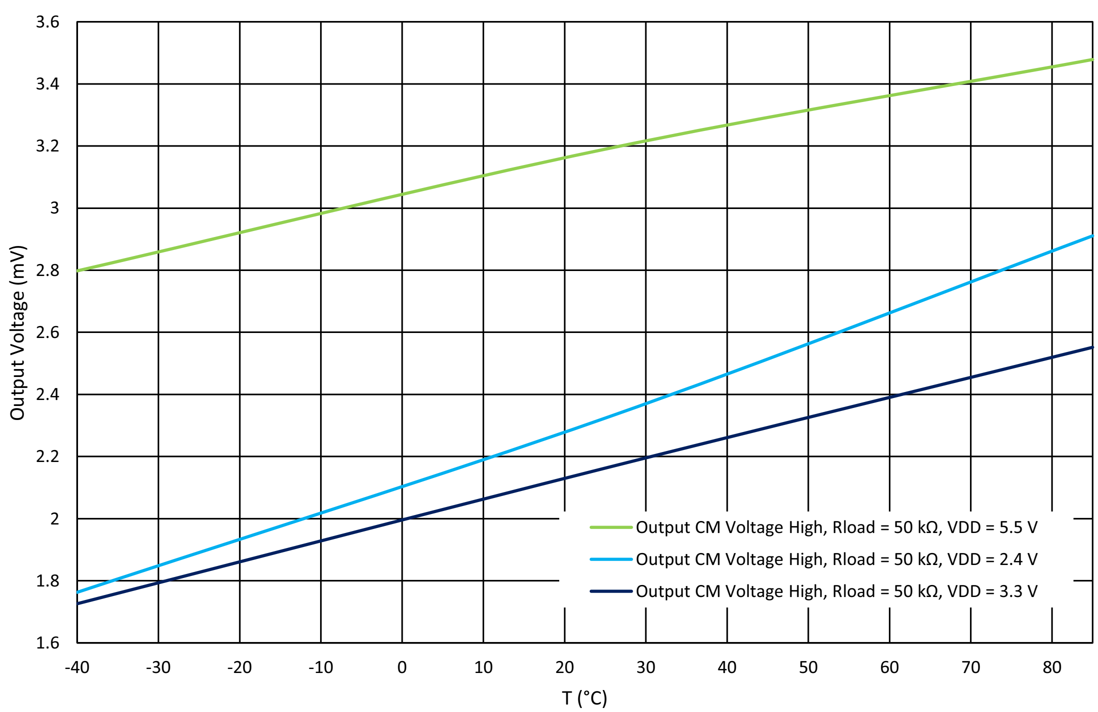


Figure 147: Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 2 MHz, R_{LOAD} = 50 kΩ

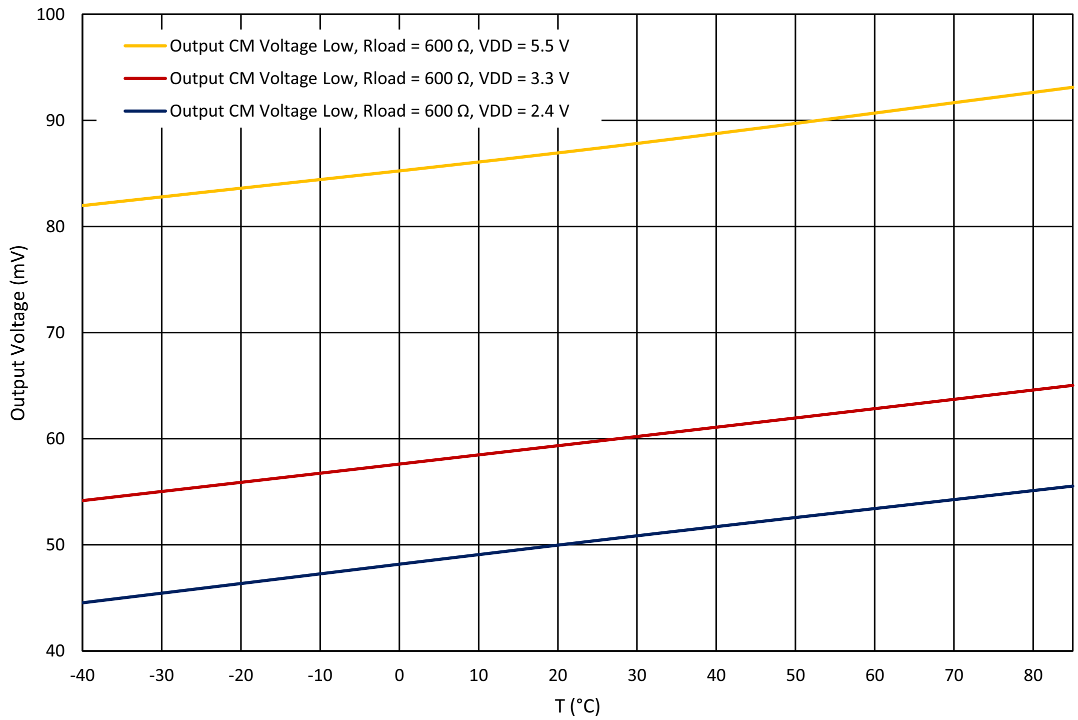


Figure 148: Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 8MHz, R_{LOAD} = 600 Ω

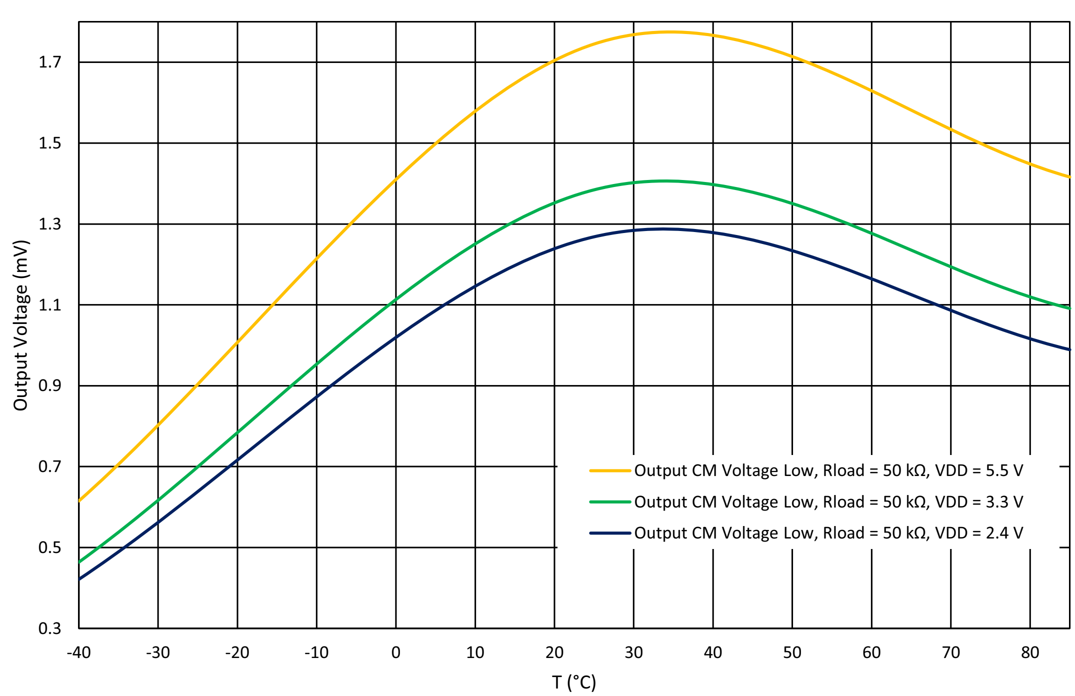


Figure 149: Output Voltage Low (V_{OUT} - GND) vs. Temperature at BW = 8 MHz, R_{LOAD} = 50 kΩ

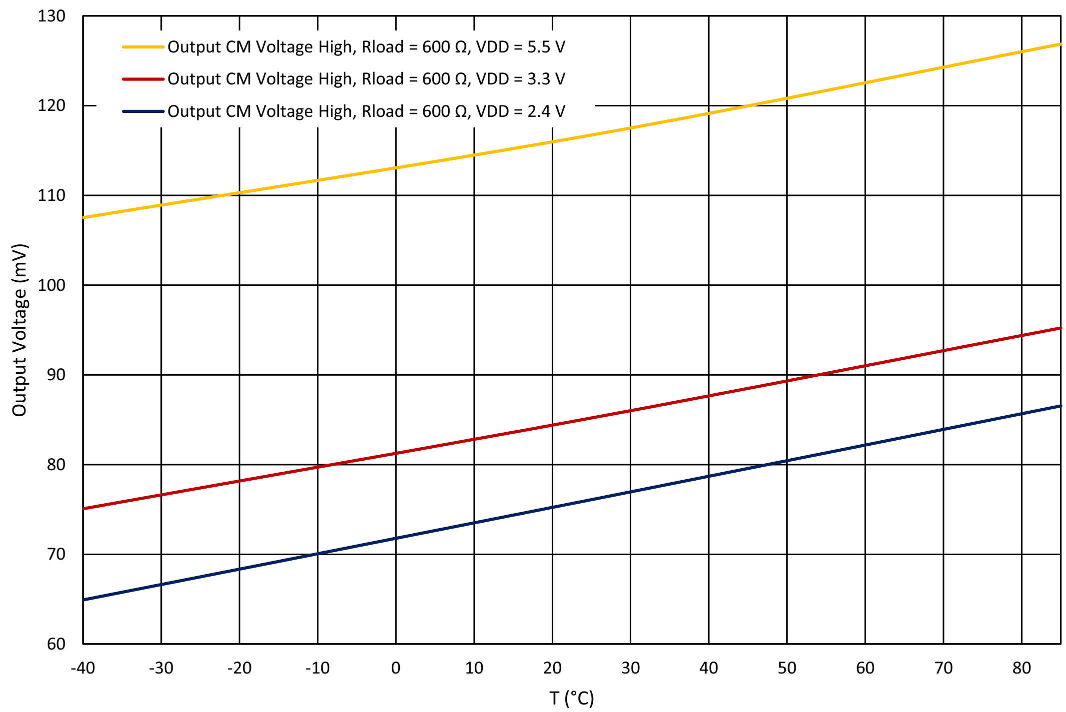


Figure 150: Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 8 MHz, R_{LOAD} = 600 Ω

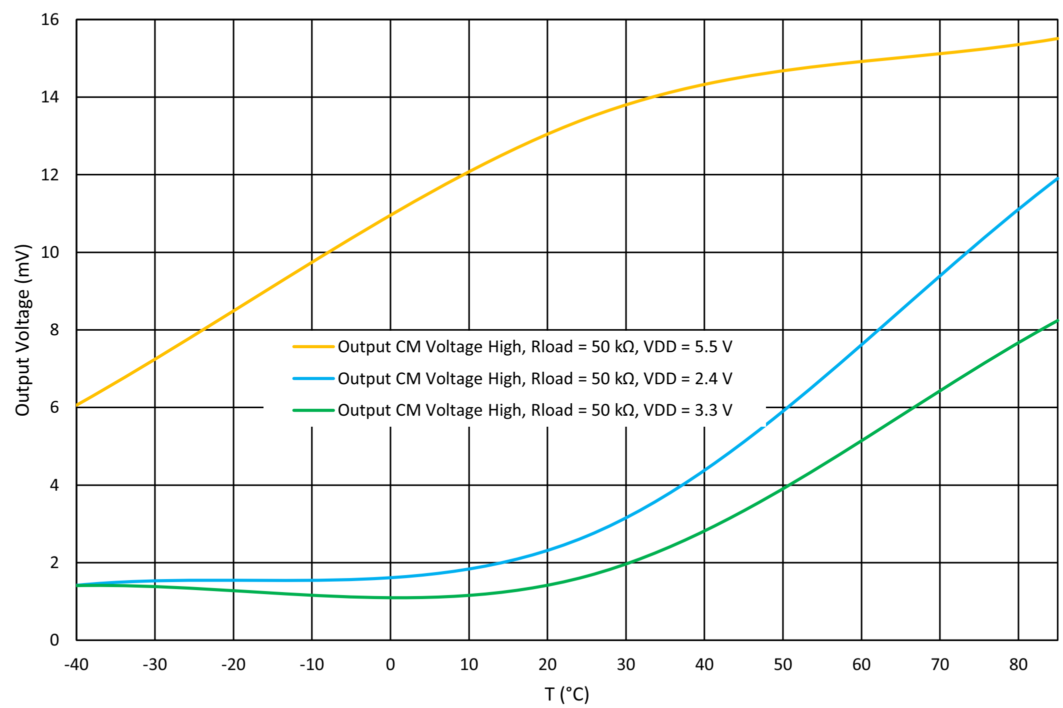


Figure 151: Output Voltage High (V_{DDA}- V_{OUT}) vs. Temperature at BW = 8 MHz, R_{LOAD} = 50 kΩ

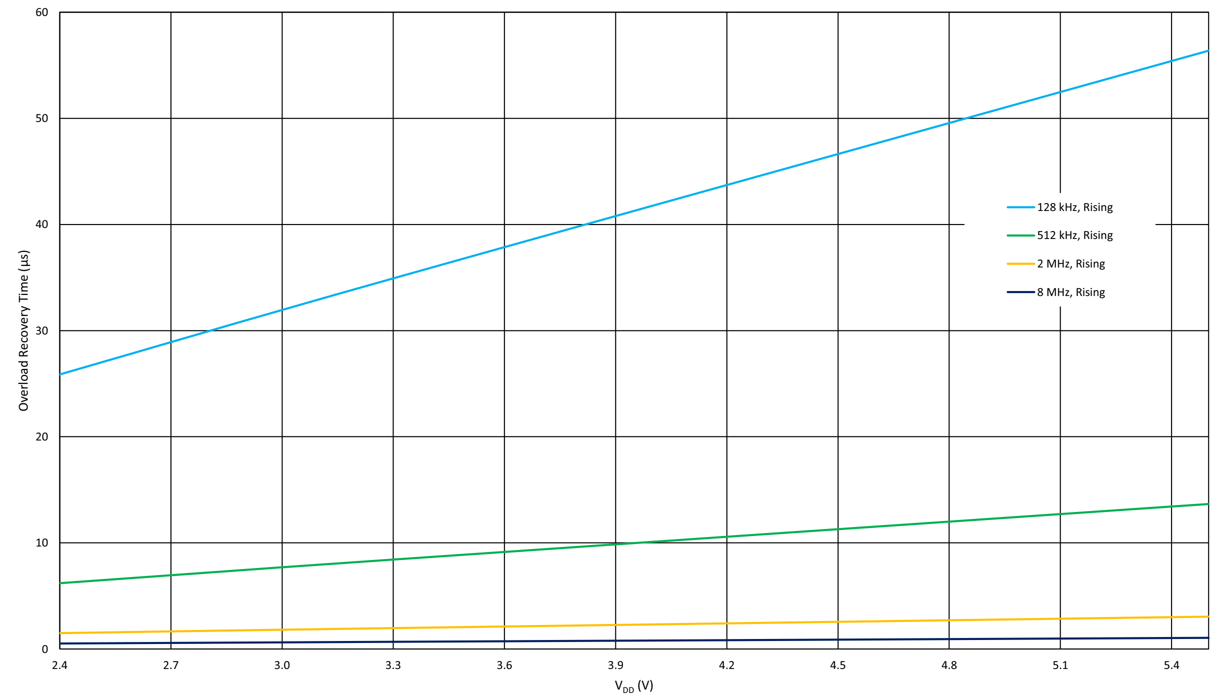


Figure 152: Overload Recovery Time vs. Power Supply Voltage R_L = 50 kΩ; G = 1 V/V, Rising

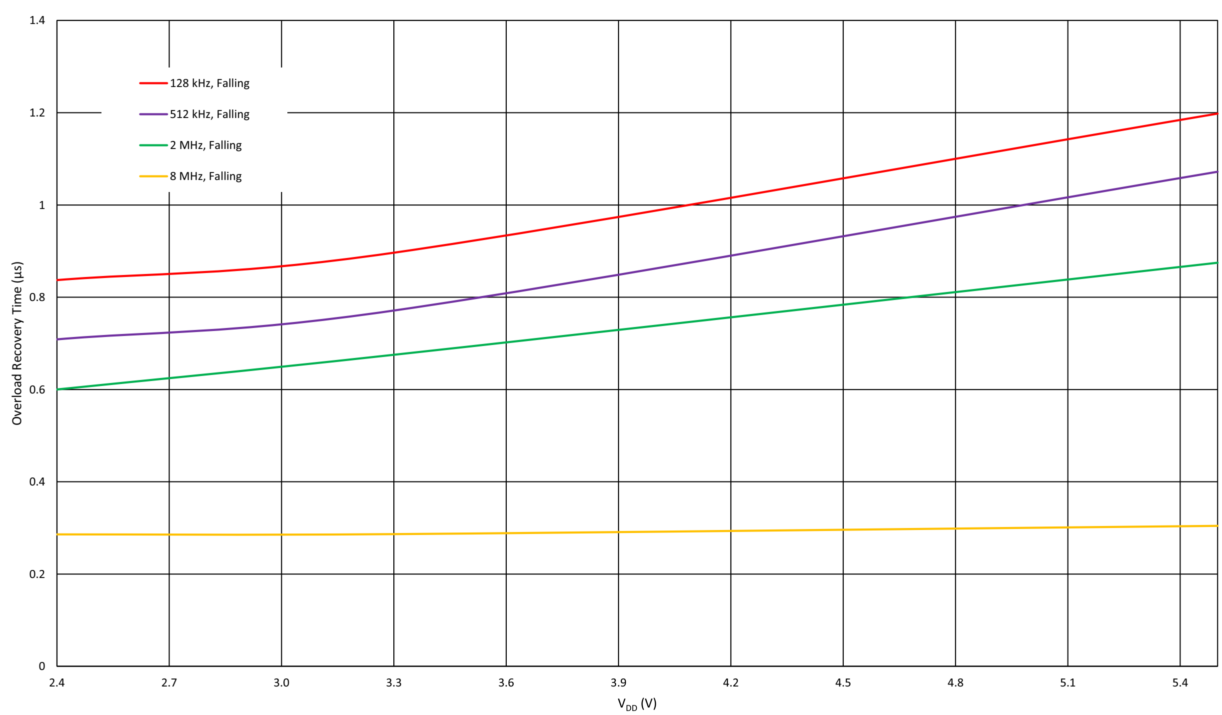


Figure 153: Overload Recovery Time vs. Power Supply Voltage R_L = 50 kΩ; G = 1 V/V, Falling

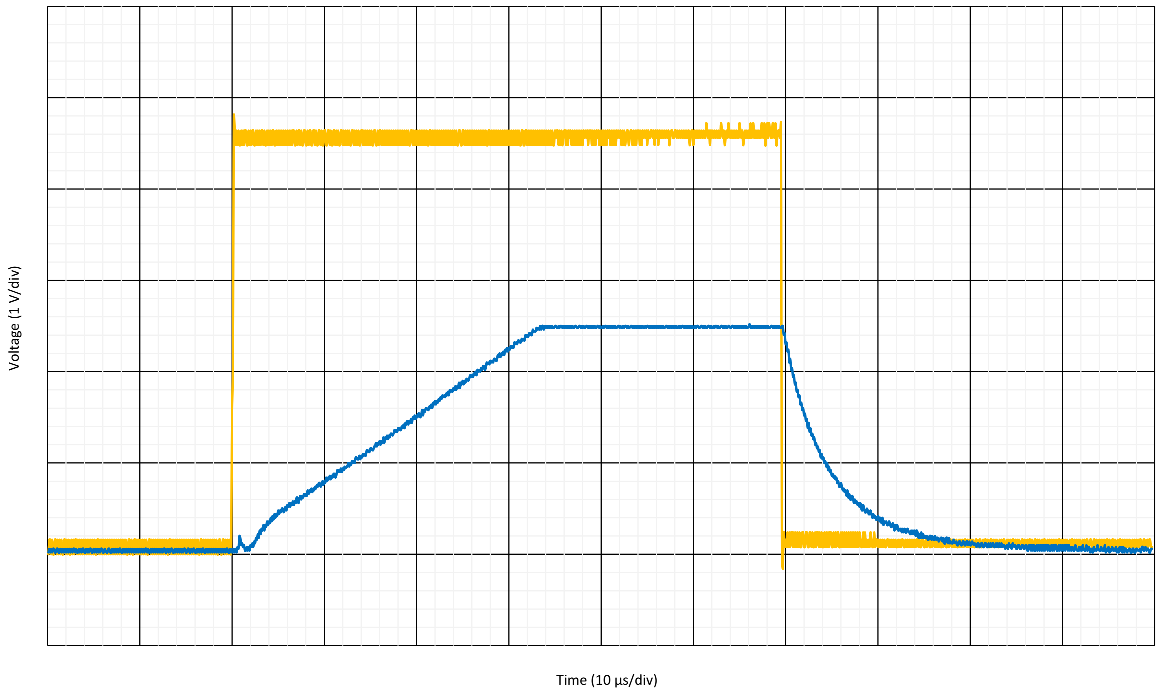


Figure 154: Output Response to Power Down Signal G = 1 V/V; R_L = 50 kΩ; C_L = 20 pF; V_{IN} = V_S/2, BW = 128 kHz

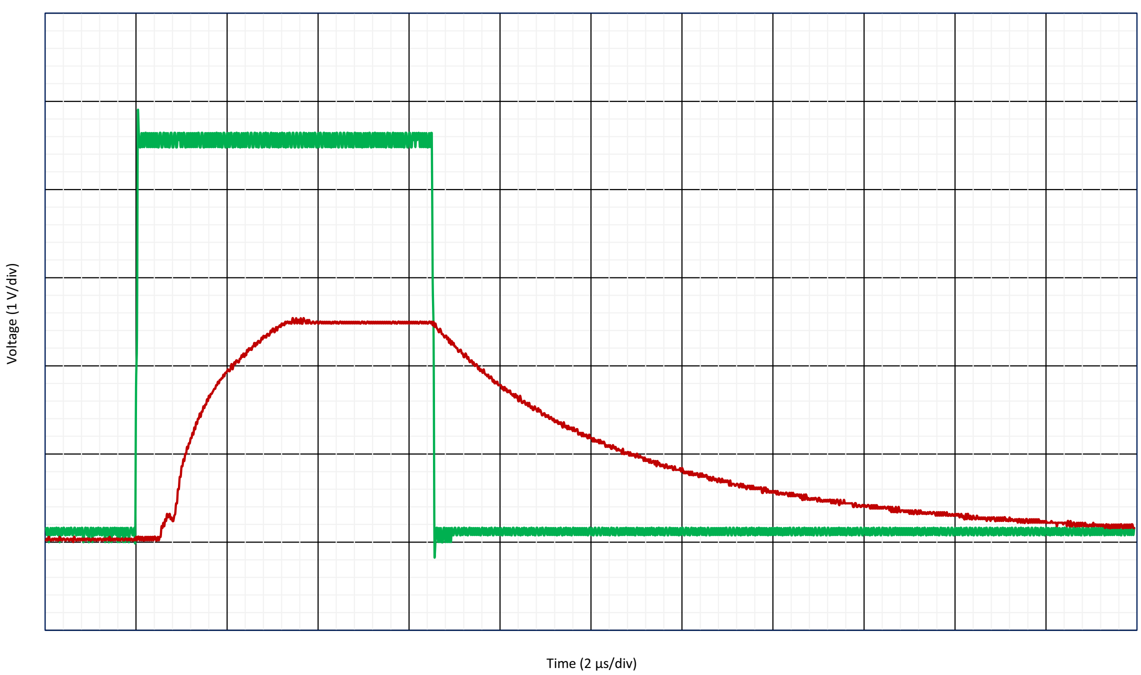


Figure 155: Output Response to Power Down Signal G = 1 V/V; R_L = 50 kΩ; C_L = 20 pF; V_{IN} = V_S/2, BW = 512 kHz

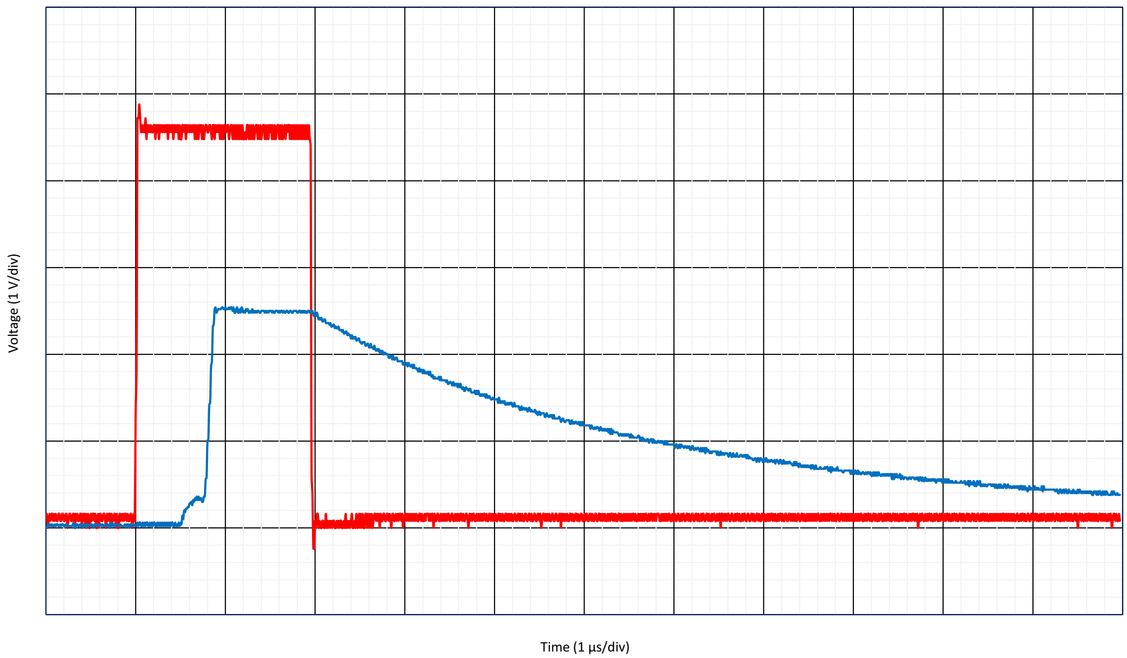


Figure 156: Output Response to Power Down Signal G = 1 V/V; R_L = 50 kΩ; C_L = 20 pF; V_{IN} = V_S/2, BW = 2 MHz

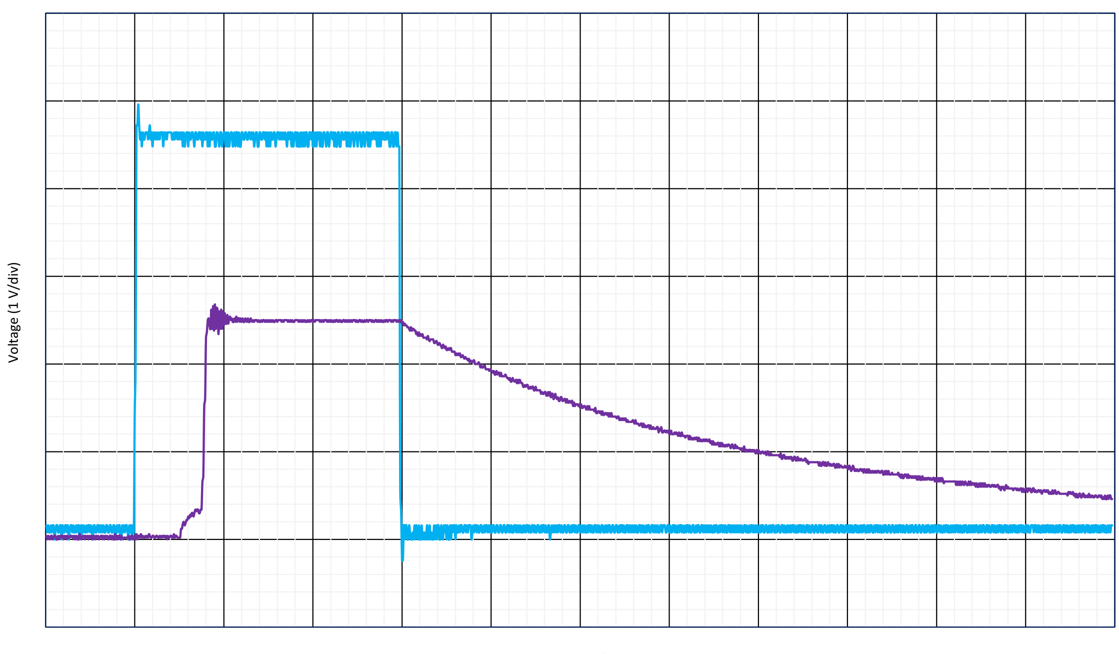


Figure 157: Output Response to Power Down Signal G = 1 V/V; R_L = 50 kΩ; C_L = 20 pF; V_{IN} = V_S/2, BW = 8 MHz

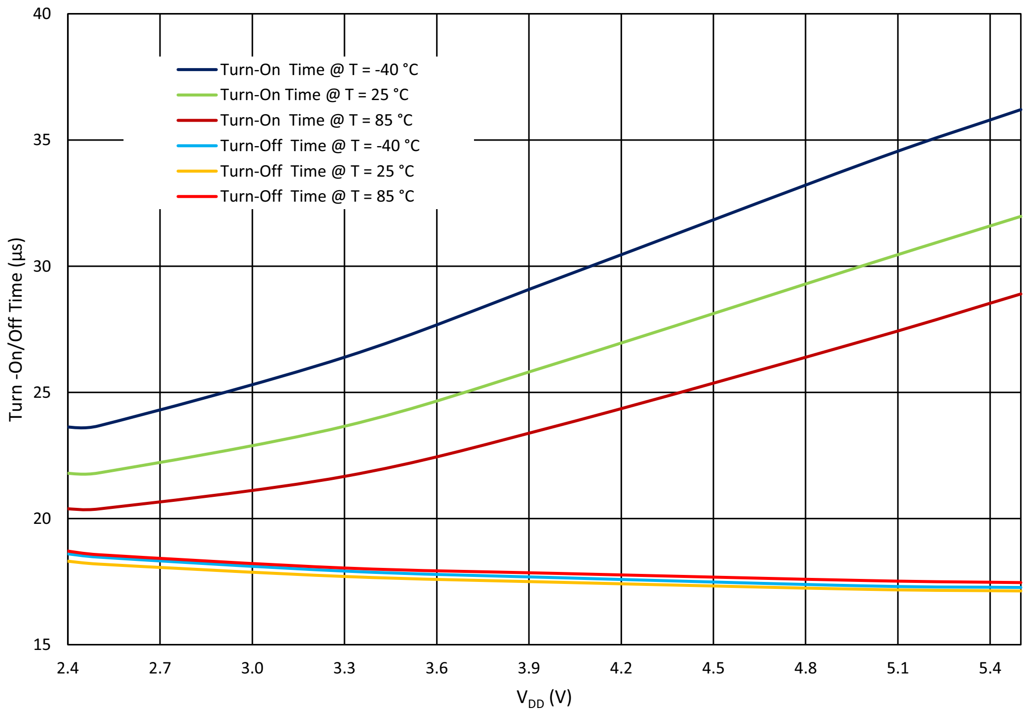


Figure 158: Opampx Turn-On/Off Time vs. V_{DD} at V_{IN} = V_{DD}/2, BW = 128 kHz

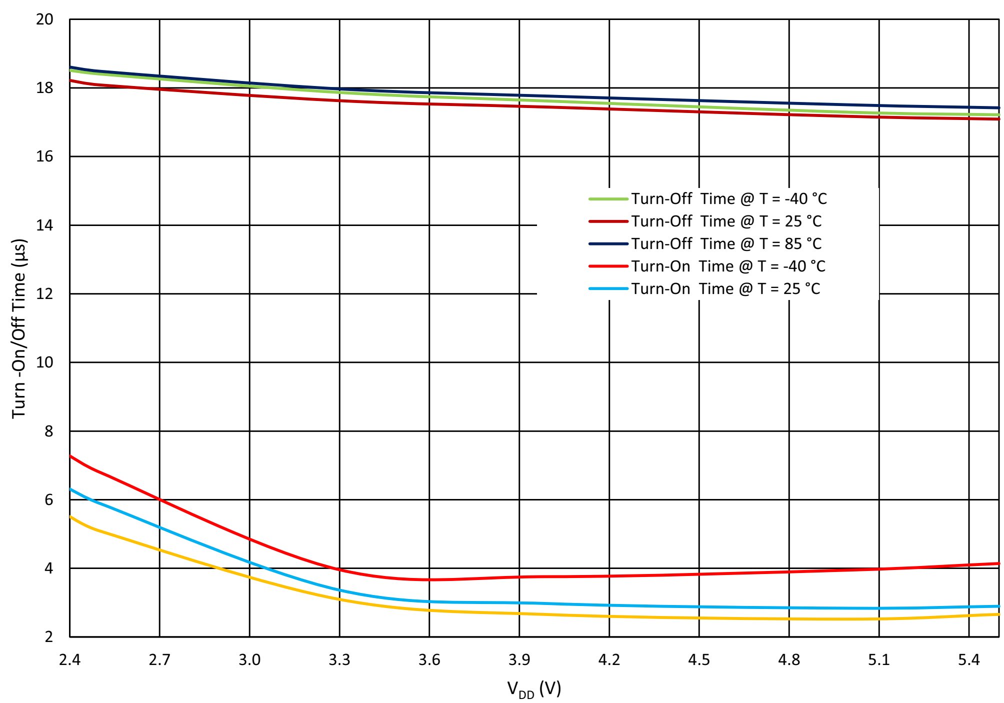


Figure 159: Opampx Turn-On/Off Time vs. V_{DD} at V_{IN} = V_{DD}/2, BW = 512 kHz

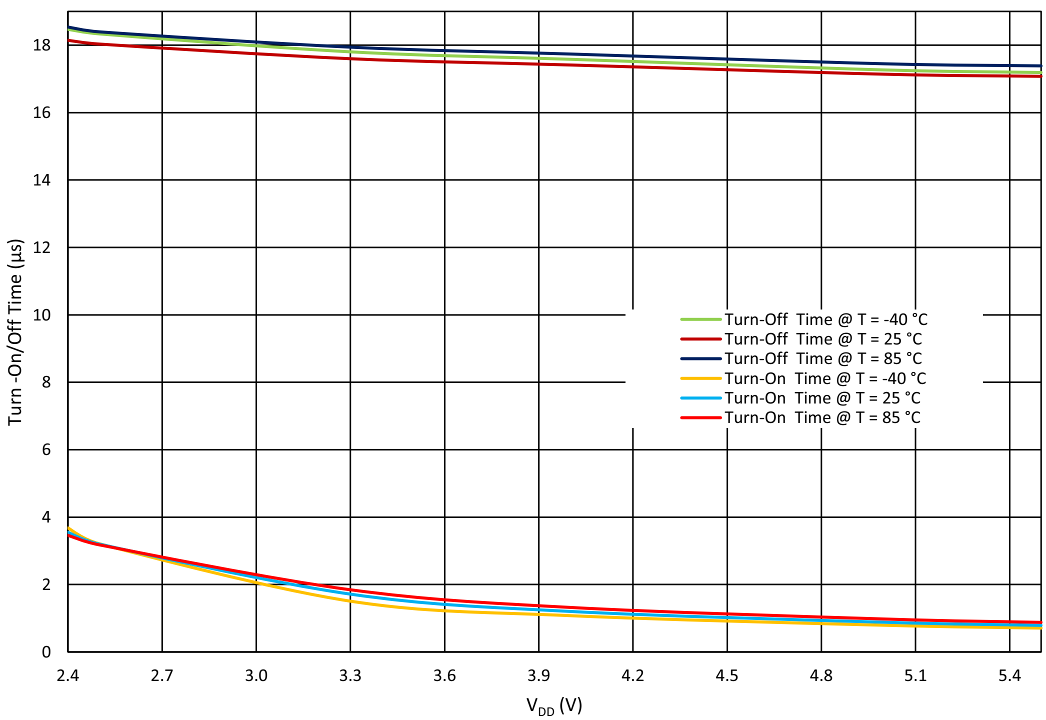


Figure 160: Opampx Turn-On/Off Time vs. V_{DD} at V_{IN} = V_{DD}/2, BW = 2 MHz

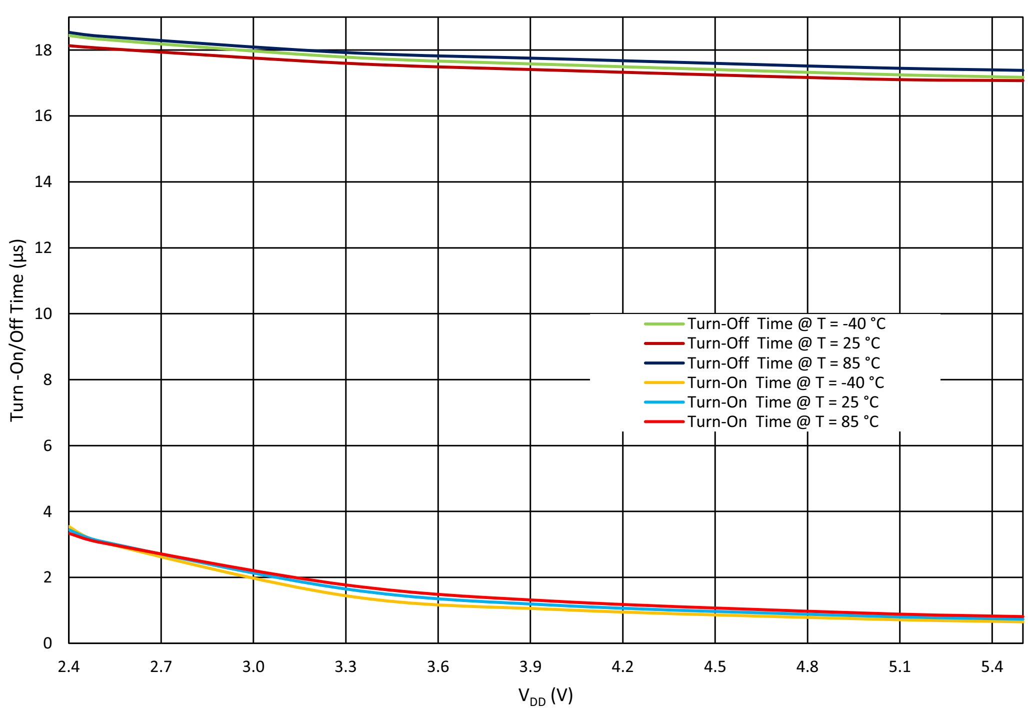


Figure 161: Opampx Turn-On/Off Time vs. V_{DD} at V_{IN} = V_{DD}/2, BW = 8 MHz

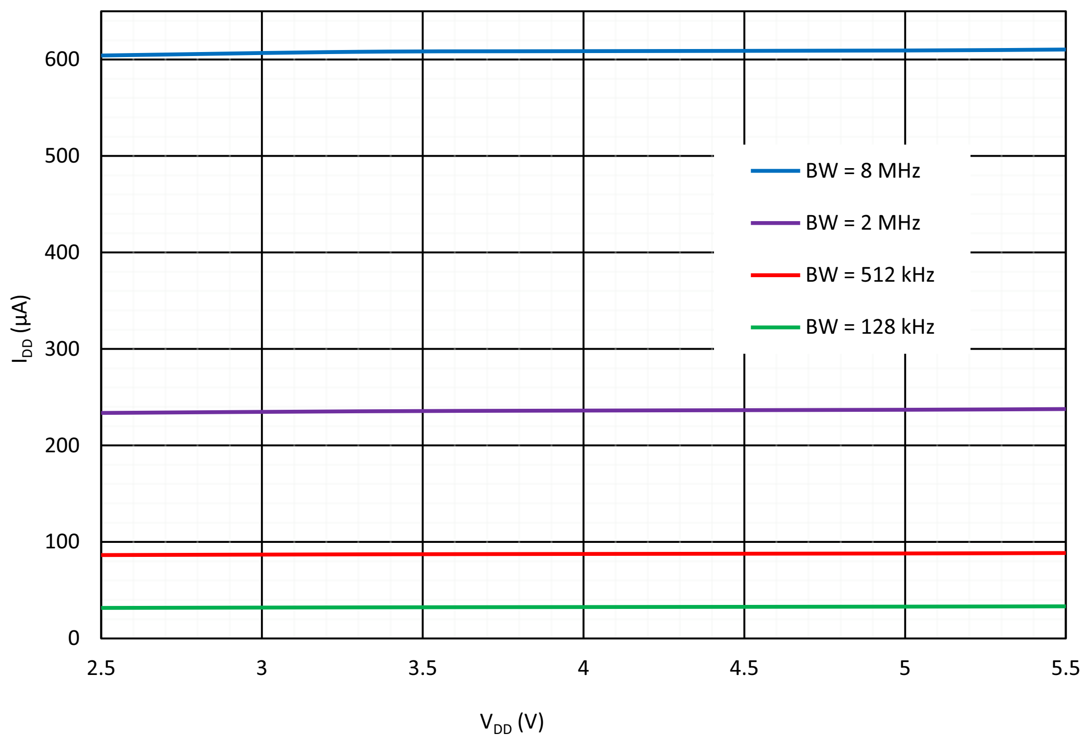


Figure 162: Opamps Quiescent Current Consumption vs. V_{DD}

11 Analog Switch Macrocell

11.1 ANALOG SWITCH GENERAL DESCRIPTION

The SLG47004 contains two single-pole/single throw (SPST) normally open analog switches (AS). The structure of the Analog Switches is shown in Figure 163 and Figure 164.

Each analog switch can be controlled from the following sources:

- Connection matrix
- Operational Amplifier macrocell.

Small NMOS (small PMOS) of Analog Switch must be enabled when macrocell is controlled by logic signal from connection matrix. Otherwise, small NMOS (small PMOS) must be disabled when macrocell is controlled by op amp.

Table 56 and Table 57 show possible operation modes of analog switches.

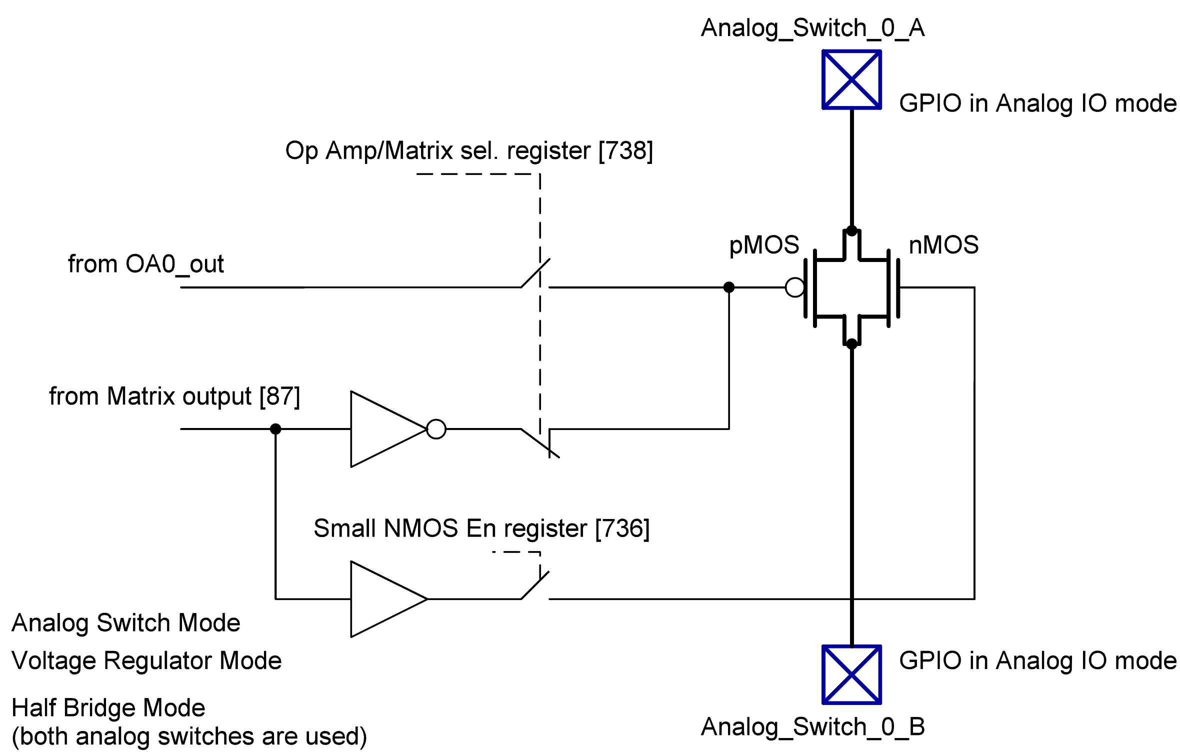


Figure 163: Analog Switch 0 Control Circuit

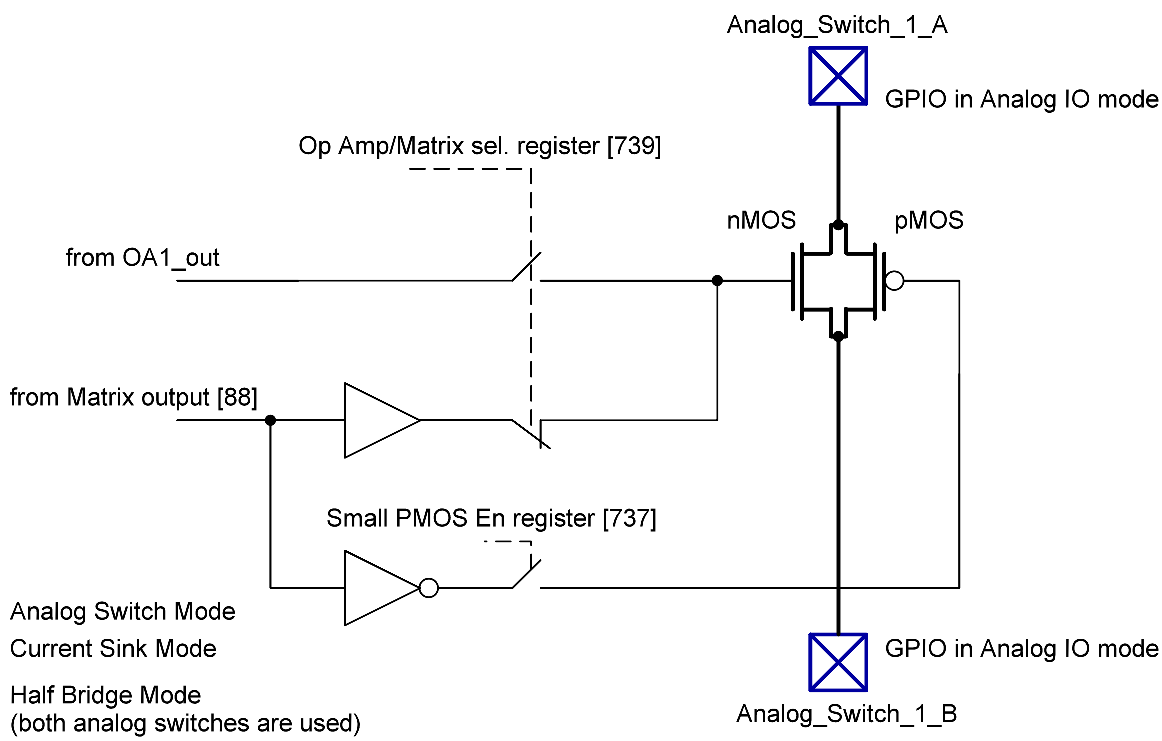


Figure 164: Analog Switch 1 Control Circuit

Table 56: Analog Switch 0 Modes of Operation

Mode of Operation	Half Bridge Mode Enable Register [740]	Matrix/Op Amp Control Register [738]	Small nMOS Enable Register [736]
Analog Switch mode with big pMOS only (control from connection matrix)	0	0	0
Analog Switch mode with all FETs enabled (control from connection matrix)	0	0	1
Voltage Regulator mode	0	1	0
Half Bridge mode with big pMOS only (control from connection matrix)	1	x	0
Half Bridge mode with all FETs enabled (control from connection matrix)	1	x	1

Table 57: Analog Switch 1 Modes of Operation

Mode of Operation	Half Bridge Mode Enable Register [740]	Matrix/Op Amp Control Register [739]	Small pMOS Enable Register [737]
Analog Switch mode with big nMOS only (control from connection matrix)	0	0	0
Analog Switch mode with all FETs enabled (control from connection matrix)	0	0	1
Current Sink mode	0	1	0
Half Bridge mode with big nMOS only (control from connection matrix)	1	x	0
Half Bridge mode with all FETs enabled (control from connection matrix)	1	x	1

11.2 HALF BRIDGE MODE

Two switches can be externally connected in series to create a half bridge. Please refer to tables Table 56 and Table 57 to enable half bridge mode. Additional logic will be connected to the analog switches to simplify control. Figure 165 shows the half bridge structure with two analog switches.

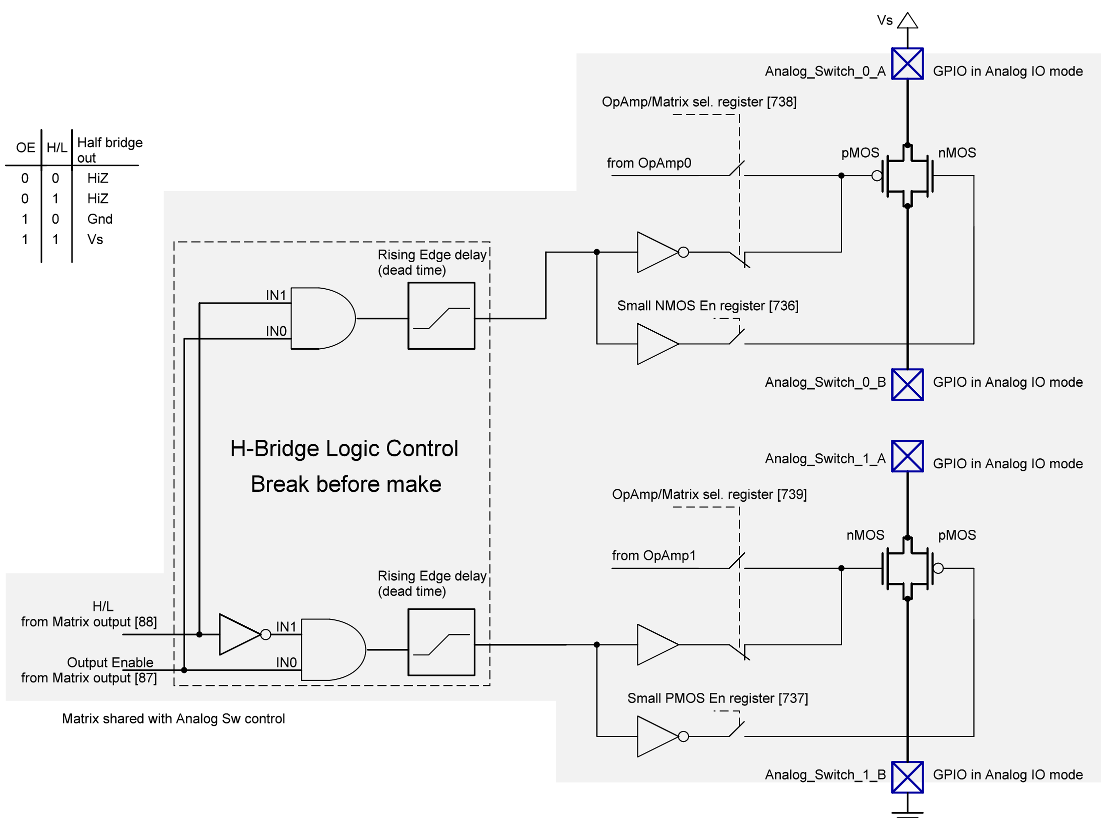


Figure 165: Structure of Half Bridge

11.3 ANALOG SWITCHES TYPICAL PERFORMANCE

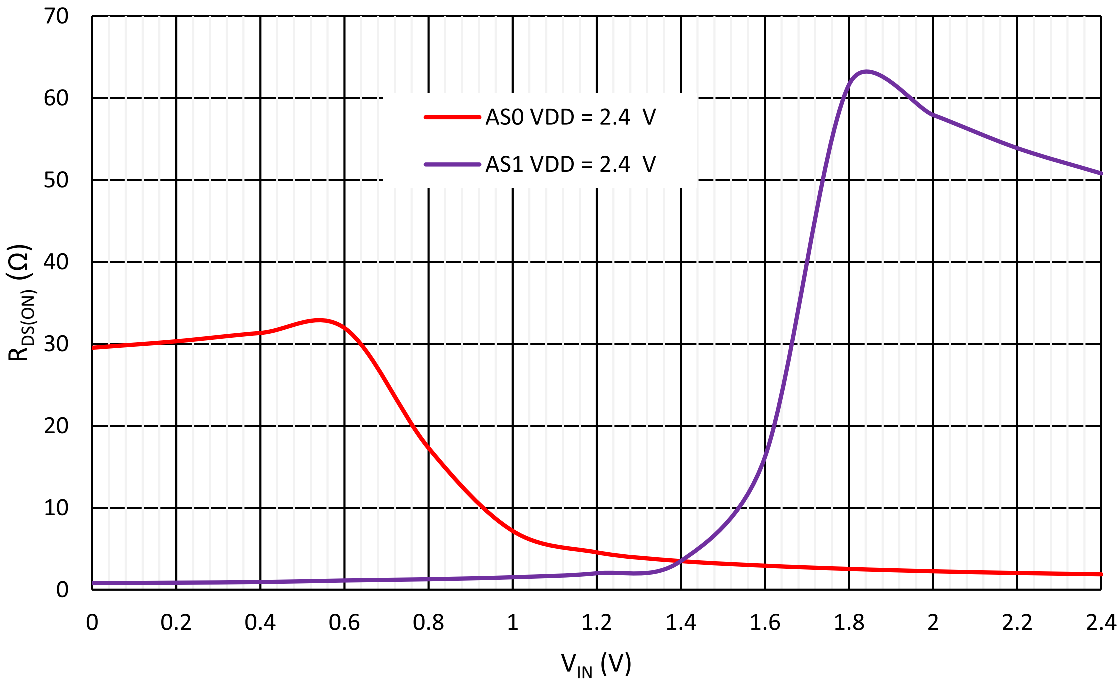


Figure 166: Typical R_{ON} vs. Input Voltage (V_i) for V_i = 0 to V_{DDA}, I_{LOAD} = 1 mA, V_{DDA} = 2.4 V

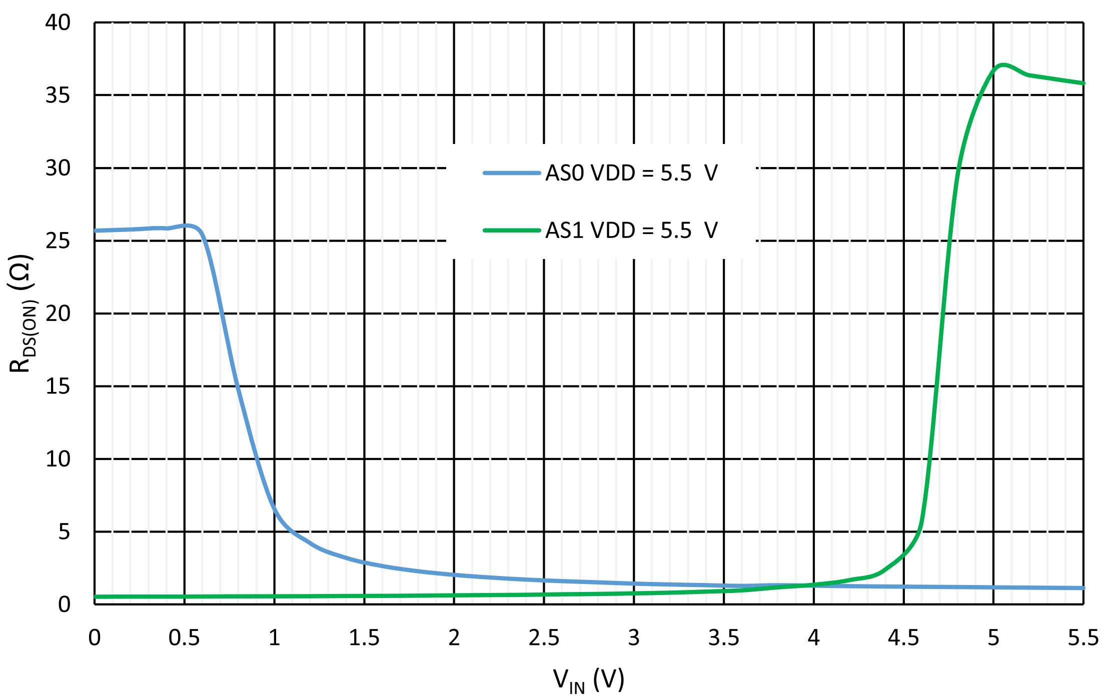


Figure 167: Typical R_{ON} vs. Input Voltage (V_i) for V_i = 0 to V_{DDA}, I_{LOAD} = 1 mA, V_{DDA} = 5.5 V

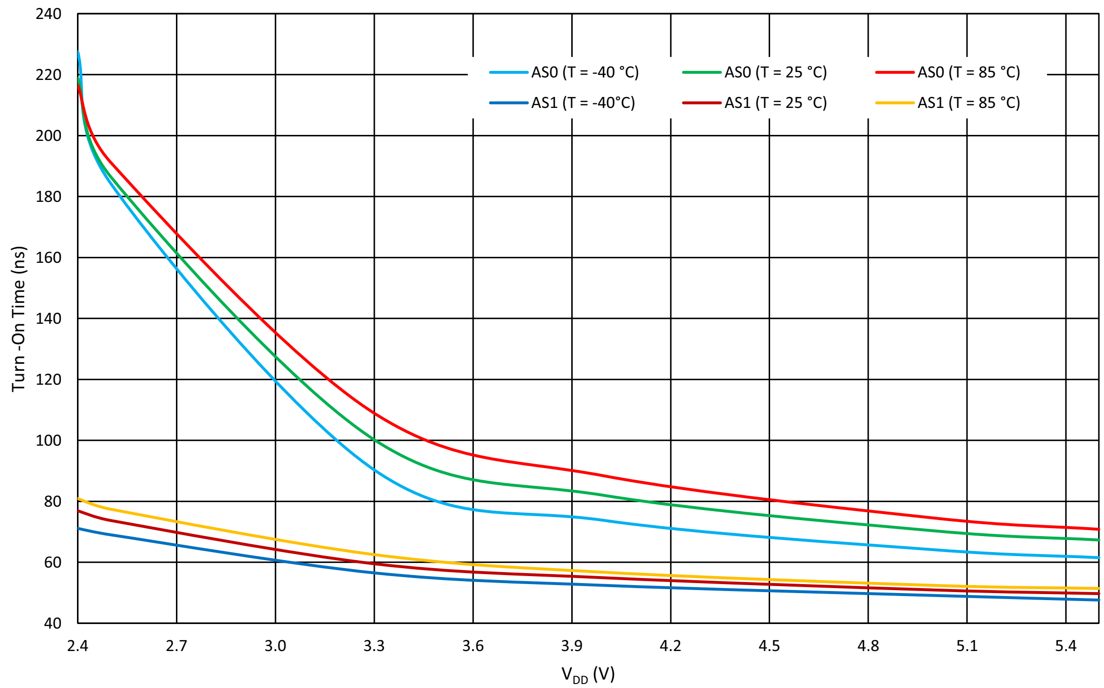


Figure 168: Turn-On Time vs. V_{DD} at R_{LOAD} = 100 Ω to GND, V_{IN} = V_{DD}/2

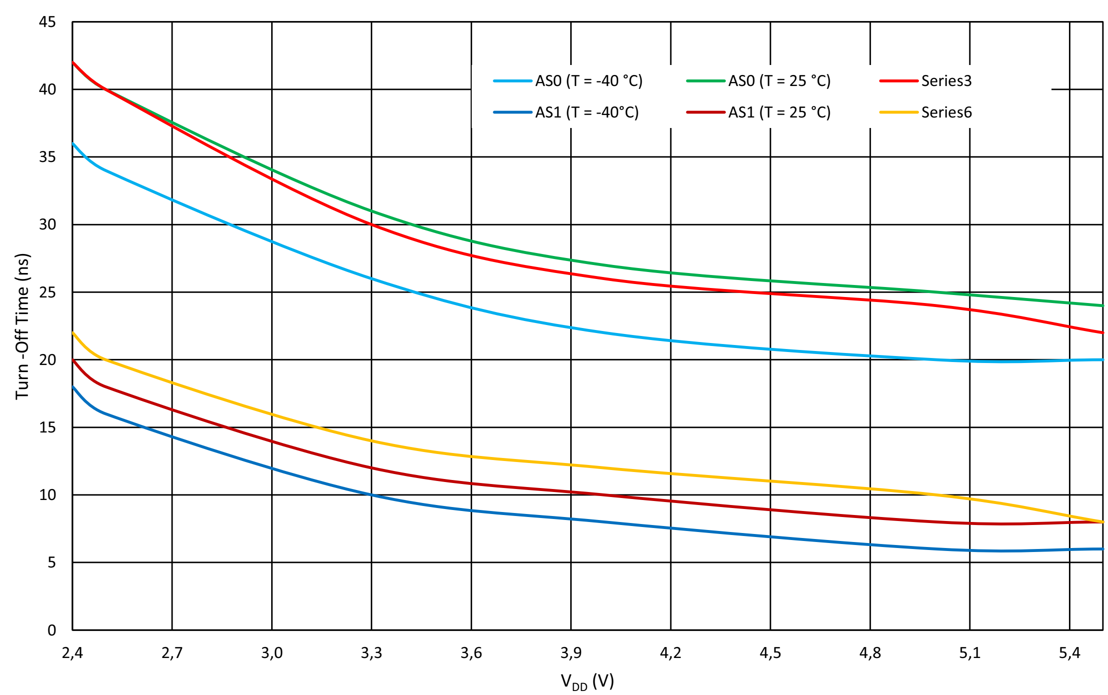


Figure 169: Turn-Off Time vs. V_{DD} at R_{LOAD} = 100 Ω to GND, V_{IN} = V_{DD}/2

12 Digital Rheostats and Programmable Trim Block

The SLG47004 contains two 10-bit Digital Rheostats. The structure of both macrocells is shown in Figure 170. The range of digital code that corresponds to the rheostat resistance ranges from 0 to 1023 (1024 taps). Code 0 corresponds to the minimum resistance between the RHx_A and RHx_B terminals. As the code value increases, the resistance between the RHx_A and RHx_B terminals monotonically increases. Consequently, when the code value decreases, the resistance between the RH0_A and RH0_B terminals decreases as well (see Section 12.2). The voltage on any rheostat pin can be in the range from AGND to V_{DDA}, as well as be dynamically changed during operation.

To guarantee proper operation of digital rheostats charge pump must be turned on (matrix input [86] must be logic High or registers [912] = 1, [913] = 1). Optionally user can turn off rheostats charge pump to decrease energy consumption. But it's strongly recommended to use the charge pump if V_{DD} < 4.5 V.

The rheostat resistance can be changed in three ways:

- Changing the Rheostat value using the I^{2}C interface;
- Manually changing the rheostat value using clock and up/down signals, similar to the counter;
- Using the Built-in Auto-Trim mode, where the rheostat value change is done using a special logic based on the signal from the Chopper ACMP.

Each rheostat also has three Switching Speed Modes:

- Regular mode (Register [915] = 0, Register [914] = 0) - up to 1 kHz. In this mode, Low Power Bandgap Chopper Oscillator that oscillates around 120 kHz is used as a source for the charge pump clock. This setting has a lower quiescent current at the expense of a longer recovery time after input voltage spikes.
- Fast mode (Register [915] = 0, Register [914] = 1) - up to 100 kHz. In this mode, the 2 MHz OSC is used as a source for the charge pump clock. This setting has a faster recovery time for input voltage spikes at the expense of a larger quiescent current. Please note that this selection forces On the OSC1 (2.048 MHz).
- Auto Selection (Register [915] = 1, Register [914] = either) when trim is used. When Auto-Trim is active, the fast mode is used. After the Auto-Trim process completes, the regular mode is used.

Note: The maximum switching speed can be achieved if no external capacitive load is connected to the rheostat terminals.

The Programmable Trim (PT) blocks of rheostats macrocell contain analog MUXs, digital MUXs, Chopper ACMP, and additional logic. The two analog MUXs (M1 and M2) and the Chopper ACMP are both shared between the two rheostats. All analog and digital MUXs are set by NVM bits and can be overwritten with I^{2}C.

The M_CK0 and M_CK1 MUXs select the clock source from internal pre-dividers of the internal oscillators or from the connection matrix. The internal clock sources for the rheostats are OSC0, OSC0/8, OSC0/64, OSC0/512, OSC0/4096, OSC0/32768, OSC0/262144, OSC1, OSC1/8, OSC1/64, and OSC1/512. The PT blocks of the rheostat use the same clock scheme as Counter/Delay Macrocells (refer to 16.5). M_CH0 and M_CH1 select the Chopper comparator or a matrix output as the signal source for the main rheostat up/down counter direction. The output of the Chopper ACMP is connected with the Up/Down inputs of the PT blocks by default. The output of the Chopper ACMP can be optionally inverted by setting register [882] to “1”.

M1 MUX selects the input for the Chopper comparator to be connected either internally to one of 3 integrated op amps (Op Amp0 out, Op Amp1 out, In Amp Out) or externally to a PIN. M2 MUX is simplified symbol of Chopper ACMP reference selection blocks. The Chopper ACMP reference ("-" input) can be: analog signal from pin, divided internal Vref voltage (6-bit divider), or divide V_{DDA} voltage (6-bit divider). In Auto-Trim mode each of Rheostats has it own settings for Chopper ACMP inputs. For more information about Chopper ACMP Vref see Section 9.2.

The power-up signal for the Chopper ACMP can be handled either by matrix output signal or Set0/Set1 signal from the PT macrocell. In Auto-Trim mode (Auto_Cal _Dis_RHx NVM bit = 0) additional internal logic enables the clocking of the corresponding PT macrocell counter and disables clocking when one of the stop conditions is reached. See a detailed description in Section 12.4. In Figure 170 when Auto_Cal _Dis_RHx NVM bit = 0 (Auto-Trim mode is enabled), the clocking pulses for the internal PT macrocell counter are under control of additional logic. When Auto_Cal _Dis_RHx NVM bit = 1 (Auto-Trim mode is disabled), all additional logics (Set signal, internal Set signal, Idle/Active signal) operate the same way, but clock pulses are always enabled and generated externally by the user. Calibration channel can be selected automatically (1st channel is channel 0, second channel is channel 1) or can be set manually by registers [893:892].

The inputs of Chopper ACMP can be reconfigured while operating in Auto-Trim mode. There is one configuration of inputs (M1, M2 configuration, Figure 170) for the case when Set0 signal is latched, and another configuration of M1, M2 MUXs when Set1 signal is latched. For example, M1 MUX can be configured to operate with In Amp out when Set0 is latched and Chopper_ACMP+ pin when Set1 is latched. The same way, M2 can be configured to work with any of M2 inputs when Set0 or Set1 are latched. Note that the default configuration is the configuration for Set0 signal. When Chopper ACMP operates as separate ACMP and Auto-Trim function is disabled, M1 and M2 MUXs operates with configuration for Set0 signal.

Keep in mind that two Auto-Trim processes cannot be done simultaneously. When the Auto-Trim process for one rheostat is active, all signals on the Set input for another rheostat will be ignored. See a detailed description in 12.4.1. The initial user defined value of Digital Rheostat resistance can be programmed into the NVM. The initial value will be loaded during the Power-On event and this value will be used as the initial rheostat resistance, as well as a starting point for count down or count up.

Both read and write operations are allowed for rheostat resistance value, stored in NVM. Also, both read and write operations are allowed for current rheostat resistance value. RH0 read operation - registers [1561:1552], write operation - registers [1545:1536]. RH1 read operation - registers [1689:1680], write operation - registers [1673:1664].

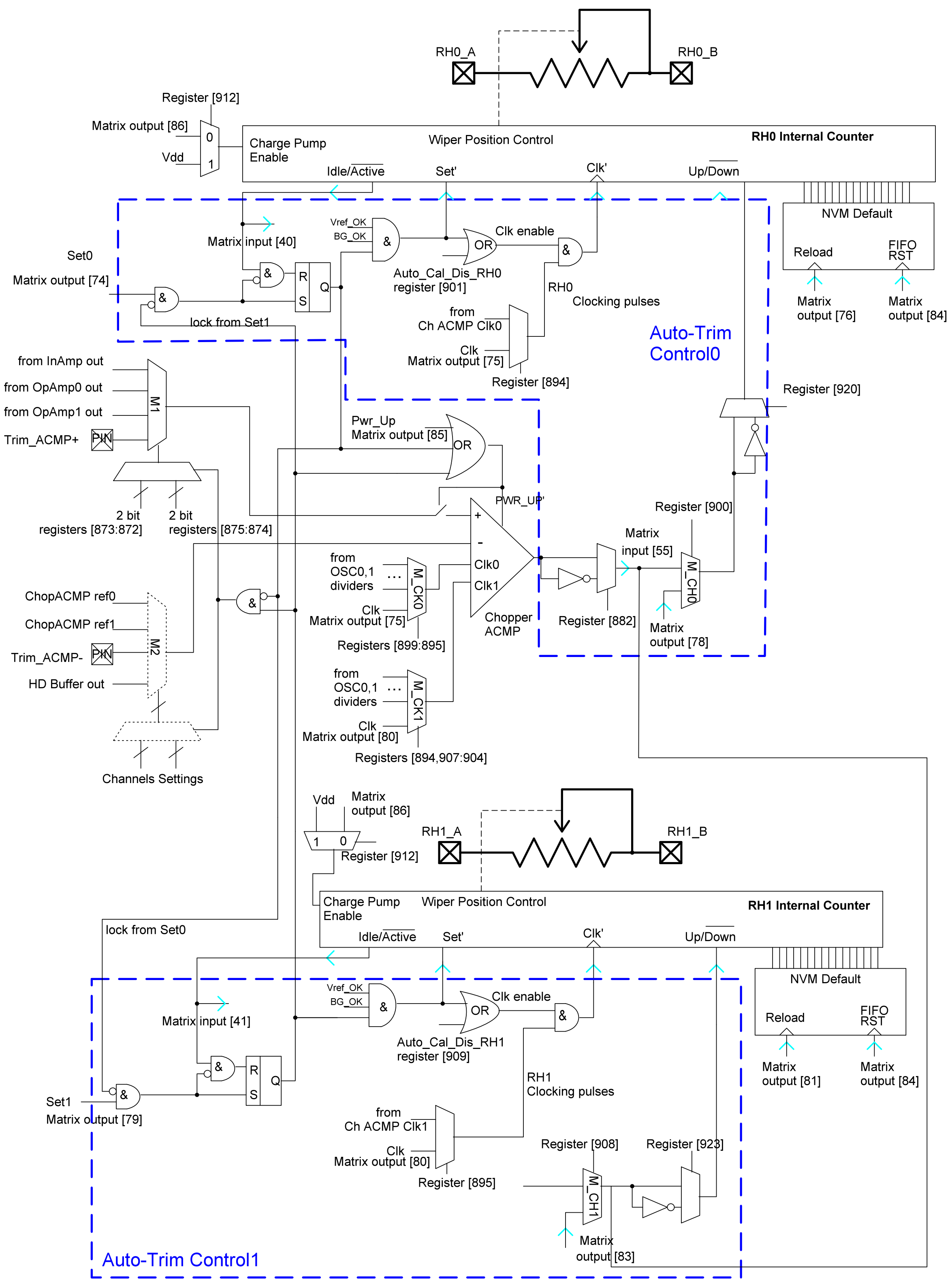


Figure 170: Programmable Trim Blocks and Digital Rheostat's Internal Circuit

PT macrocell signals:

- "Set": external Set signal begins the Auto-Trim process when Auto_Cal _Dis_RHx bit is cleared (registers [901]). Otherwise, this signal has no effect. The behavior of the PT macrocell in Auto-Trim mode is described below.
- "Reload": when Reload goes high the rheostat value stored in the MTP NVM will be loaded into the rheostat (Register and Counter) overwriting any current setting. This signal is edge sensitive. It has no effect while the Auto-Trim procedure is active. For detailed information see Section 12.3.
- "Program": when Program goes high the Internal Counter value of the rheostat will be programmed into the MTP overwriting any current value in the NVM. This procedure can be done up to 1000 times. This signal is also edge sensitive. It has no effect while the Auto-Trim procedure is active. For detailed information see 12.3. To enable "Program" signal from connection matrix RH_PRB register must be cleared (RH_PRB [1796] = 0). If RH_PRB [1796] register is set to 1, the access to NVM is disabled for "Program" signal. Refer to Section 19.6 for more details.
- "Clock": this input has the following options: the PT macrocell can be clocked internally or from matrix. When clocked internally, the clock is automatically enabled/disabled by the Set input logic in Auto-Trim mode. The internal clock is synchronized with the Chopper ACMP clock.
- "Up/Down": the rheostat counter counts up when the signal is High and down when the signal is Low.
- "Idle/Active": this is the connection matrix input, that is logic HIGH by default. It goes LOW with rising edge on SET input if Auto-Trim mode is enabled (Auto_Cal _Dis_RHx NVM bit = 0). After the end of Auto-Trim procedure (one of stop conditions occurs) this signal sets to logic HIGH again.
- "FIFO nReset": low level at this input clears internal FIFO buffer for commands Reload and Program for both rheostats. User should provide high logic level at this input for the normal rheostat operation.

There is also an overflow protection option, for which the counter will stop counting up when the maximum value (0x3FF) is reached or stop counting down when the minimum value (0x00) is reached. The digital rheostat is initialized/powered in the first place. The rheostat value is Hi-Z (or highest resistance if it is impossible to disconnect the rheostat) during the Power-On sequence.

12.1 POTENTIOMETER MODE

This mode allows two 2-pin rheostats to work as one 3-pin potentiometer. When this mode is active (register [917] = 1), user changes the value of RH0 internal counter. In this mode, the value of RH1 counter is the inverted value of RH0 counter (Figure 171). Note that the RH0_B pin and the RH1_A pin must be connected externally. Also, note that the Auto-Trim function isn't allowed in Potentiometer Mode.

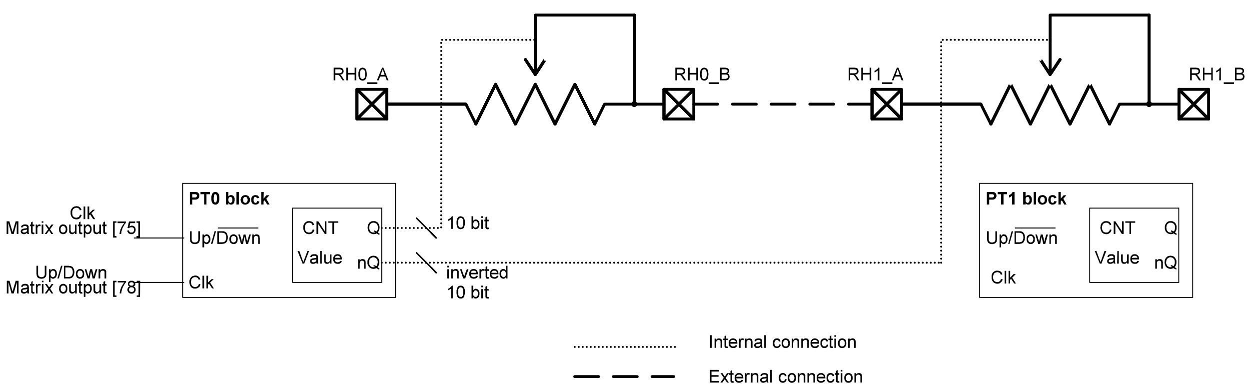


Figure 171: Rheostats in Potentiometer Mode

12.2 CALCULATING ACTUAL RESISTANCE

In applications where the absolute rheostat resistance is critical, the user can calculate it using the rheostat tolerance data, the minimum rheostat resistance, and the desired code.

The 16-bit tolerance data for both rheostats has been programmed into registers 0xE6 to 0xE9. These registers can be used to calculate the total rheostat resistance. The 16th bit defines the sign (0 = +, 1 = -) of the tolerance. The other fifteen bits correspond to the absolute value of the rheostat tolerances variation from 100 kΩ measured at 25 °C.

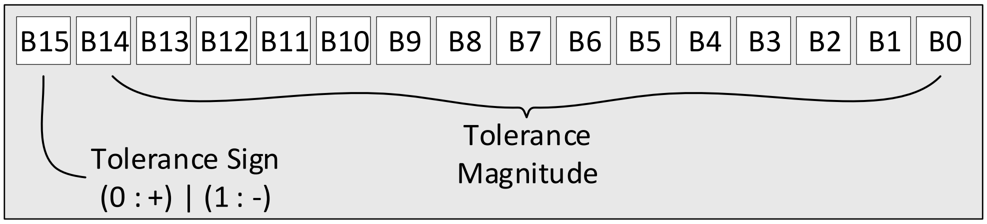


Figure 172: Rheostat Tolerance Registers

Note that the rheostat tolerance data is programmed into registers 0xE6 to 0xE9. To avoid losing this tolerance data, special attention must be paid when erasing and reprogramming page 14 in the NVM.

The rheostat value at a given code depends on the total digital rheostat resistance. The equations below can be used to calculate the rheostat resistance.

$$R_{Code} = (R_{DR} - R_{DR\ MIN}) \times (code/1023) + R_{DR\ MIN}$$

$$R_{DR} = 100 \times 10^3 + (sign_{RH\_Tolerance} \times R_{RH\_Tolerance})$$

where:

R_{Code} - Rheostat Resistance at a Given Code;

R_{DR} - Total Digital Rheostat Resistance;

$R_{DR\ MIN}$ - Minimum Rheostat Resistance;

code - Rheostat Position Ranging from 0x000 to 0x3FF;

$sign_{RH\_Tolerance}$ - the MSB of the Rheostat’s Tolerance Data;

$R_{RH\_Tolerance}$ - the 15 LSBs of the Rheostat’s Tolerance Data.

For example, let's say that 0x2B67 has been written into the rheostat tolerance registers within the GreenPAK's NVM. B15 corresponds to a positive sign while B14:0 translates into a decimal value of 11111. R_{DR} calculates to approximately 111,111 Ω and can be used with the minimum rheostat resistance to calculate the resistance at a given code. Note that the minimum rheostat resistance must be measured to obtain precise results, but a range is provided in Table 24.

12.3 DIGITAL RHEOSTAT VALUE SELF-PROGRAMMING INTO THE NVM

The current value of rheostat is stored in the Internal Counter. This value can be programmed into the MTP by setting logic HIGH at "Program" input. In this case, SLG47004 will generate a specific memory control sequence to rewrite a new value into the NVM. There is a separate NVM page that is dedicated for the Digital Rheostat value.

There is a dedicated bit RH_PRB, that enables/disables "Program" signal of PT block to change NVM rheostats resistance values. If RH_PRB[1796] = 0, "Program" signal is enabled. If RH_PRB[1796] = 1, "Program" signal is disabled. Note that RH_PRB bit has no effect on I^2C access to NVM. To enable/disable I^2C access to rheostat resistance value, stored in NVM, user must change NPRB0, NPRB1 bits. Refer to Section 18.5.

SLG47004 can latch up to four "Program" and "Reload" signals of RH0 and RH1 (Reload RH0, Program RH0, Reload RH1, Program RH1). The same signal can't be latched second time, until it is processed. All latched signals will be processed in the order of arrival (FIFO buffer), since only one signal can access NVM at the same time. If Auto-Trim process of RH0 or RH1 is active and one or more "Reload", "Program" signals for corresponding rheostat come, SLG47004 will wait until the end of Auto-Trim process and then process will latch "Reload", "Program" signals. Set0 or Set1 signal can be latched at any time and processed when rheostat clocking isn't disabled by "Program" or "Reload" signals.

User can clear the FIFO buffer by setting low logic level at FIFO nReset input of PT blocks.

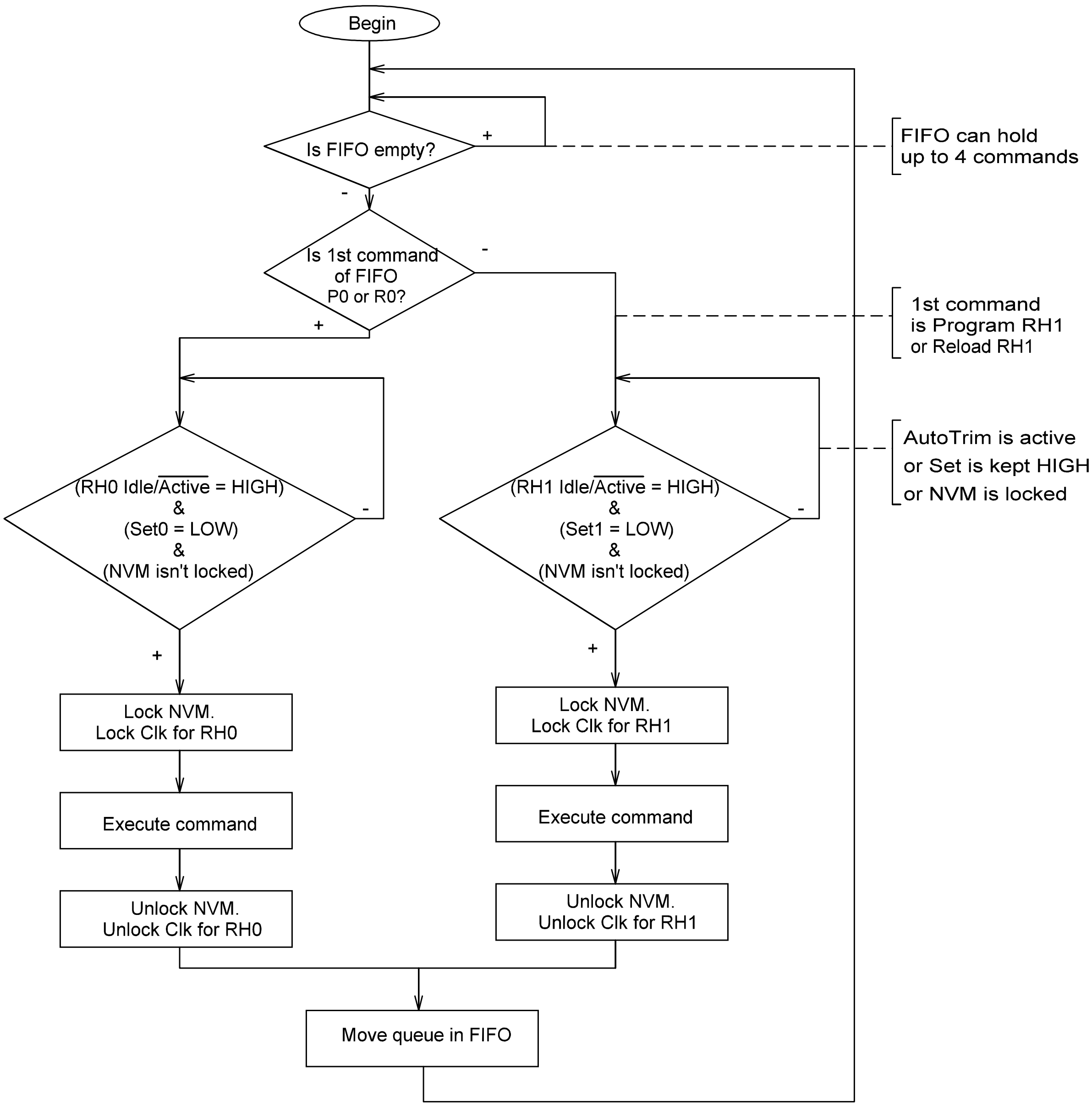


Figure 173: Flowchart of "Program" and "Reload" Signals

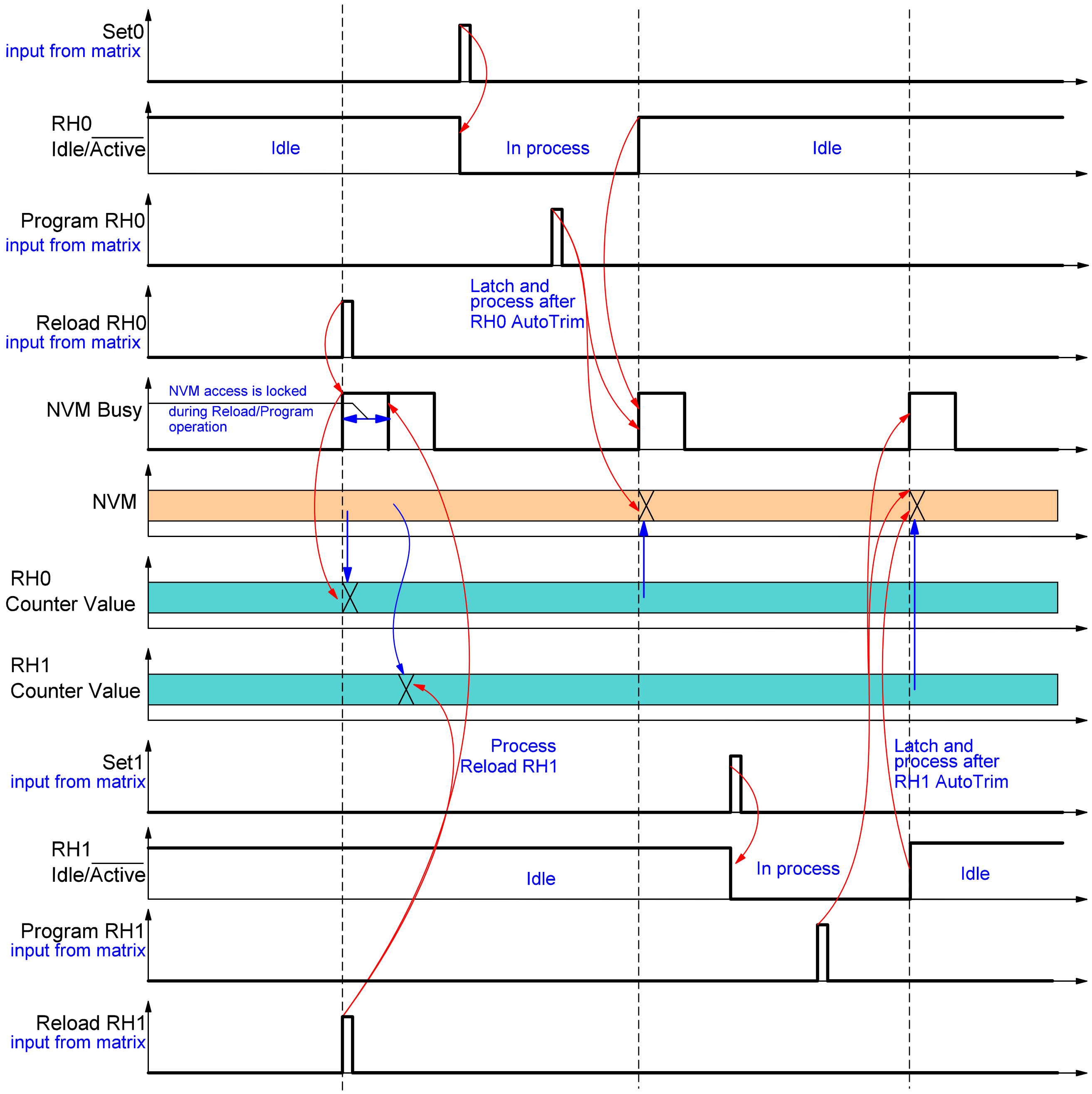


Figure 174: Example of Latching and Processing "Program" and "Reload" Signals

Since the access to the MTP NVM is disabled during NVM self-programming procedure, the device will not acknowledge it via I^2C interface. This can be used to determine when the erase/programming cycle is completed (this feature can be used to maximize bus throughput). ACK polling can be used in this case.

If the device is still busy during the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be re-sent. Once the cycle is complete, then the device will return the ACK and the master can proceed with the next Read or Write command.

12.4 TRIMMING PROCESS USING PROGRAMMABLE TRIM BLOCK

There are several ways of implementing the trimming process using the PT block. One of the essential features of the PT macrocell is the Auto-Trim function described below. It allows the user to design simple calibration circuits for a wide variety of applications.

12.4.1 Trimming Process with Auto-Trim Option Enabled

For using the Auto-Trim function the following preliminary steps must be taken:

- Clear Auto_Cal _Dis_RHx NVM bit (0 is default value). This enables Auto-Trim function.
- Configure M1 MUX (registers [875:872]). It can be user system voltage feedback. If Auto-Trim function is used for two rheostats, M1 MUX must be configured for both rheostats (for cases when Set0 is latched and when Set1 is latched).
- Configure M2 MUX. It can be user desired set point threshold. If Auto-Trim function is used for two rheostats, M2 MUX must be configured for both rheostats (for cases when Set0 is latched and when Set1 is latched). Remember, that M2 MUX is simplified symbol of Chopper ACMP reference selection blocks.
- Configure M_CH0 (M_CH1) MUX to work with Chopper ACMP (M_CH0,1 MUXs are configured to work with Chop ACMP by default).
- Configure inverting or non-inverting Chopper ACMP output (registers [923], [920] and [882]);
- Select clock source (internal clock from internal pre-dividers or from connection matrix). Note that in Auto-Trim mode clock source frequency for the PT Block is limited by the Chopper Comparator time response. Therefore, the clock source frequency must not be greater than <f_{ChACMP}> kHz.
- Start the Auto-Trim process by setting the Set0 (Set1) input of PT block to a High level. The Auto-Trim process stops if one of three stop conditions occur:

  1) 2nd time change on Up/Down input at the moment of rising edge on Clock input (see Figure 175).

  2) the value of rheostat reaches its maximum (1023).

  3) the value of rheostat reaches its minimum (0).

  Stop conditions result in a change of the Idle/Active signal, which resets the internal Auto-Trim logic.

  Note that the Set input is edge sensitive, but if the user keeps a High logic level at this input after reaching the set point, the PT block will continue to operate and continue to switch rheostat around the set point.

- To start new Auto-Trim process user should reapply a High level on Set input.

The detailed flow of Auto-Trim process is shown in Figure 175, Figure 176, Figure 177.

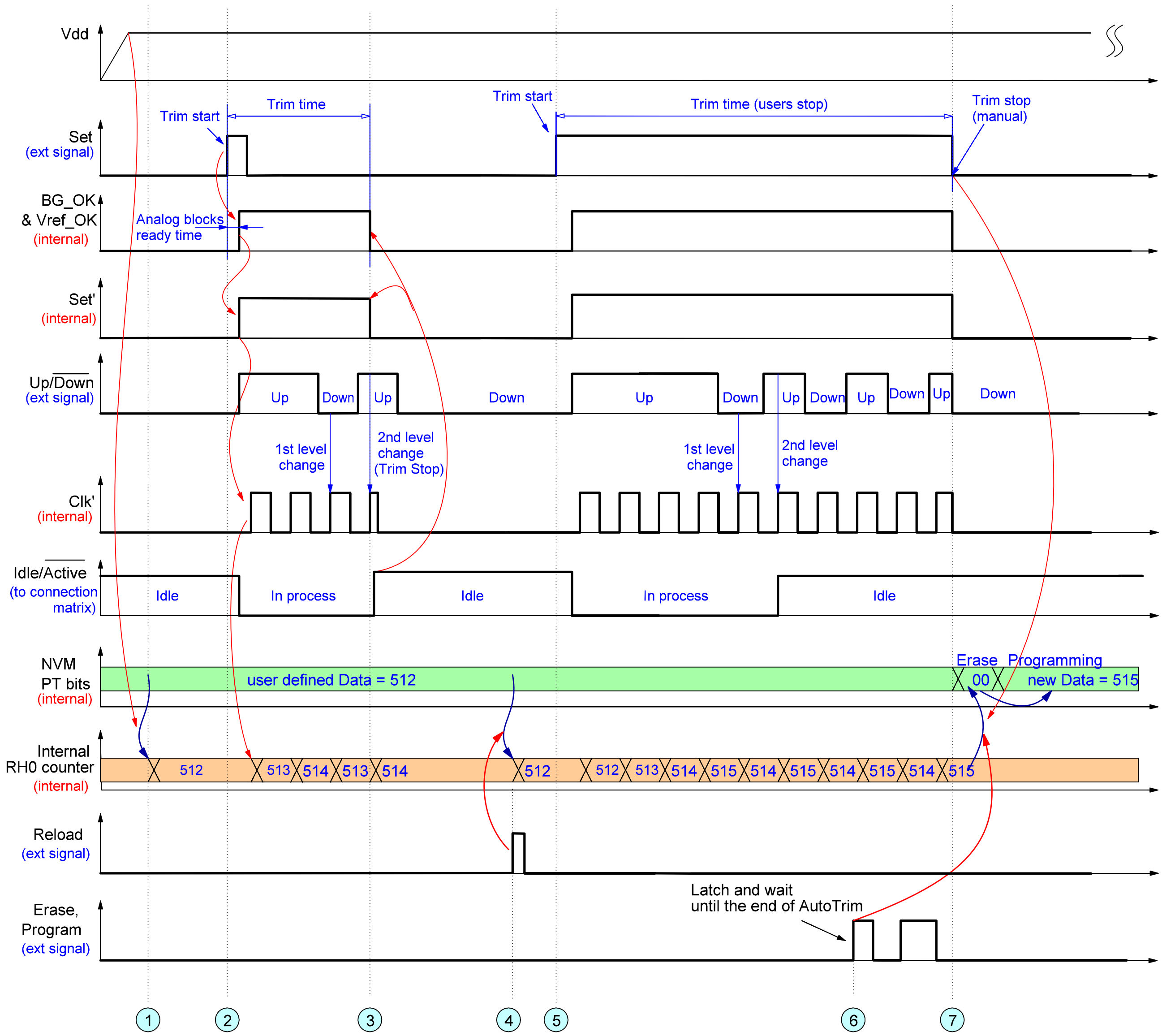


Figure 175: Example of Auto-Trim Process for a Single Rheostat

The key events of the Auto-Trim process are the following (see Figure 175):

1. During the startup event the SLG47004 loads the rheostat value from NVM to Internal Counter. In this example this value is 512.

2. The Trim process starts with a rising edge on Set input. This Set signal is latched until the end of the Auto-Trim process. The Set signal will enable the Chopper ACMP and the Vref, if they were not enabled earlier. After a ready signal from analog blocks (BG_OK & Vref_OK), the clock pulses for the internal counter are enabled. The counter starts to count up or down depending on the level at the Up/Down input. If user selected the “Internal Clock” option for Clock input, these clock pulses are generated automatically during trim time. Each rising edge of the Clock pulse changes the value of the counter and, consequently, the value of the rheostat.

3. There are three stop conditions for the Auto-Trim process:

   1) A subsequent change on Up/Down input at the moment of rising edge on Clock input.

2) The value of the rheostat reaches its maximum (1023).

3) The value of the rheostat reaches its minimum (0).

If the Set input signal is shorter than the trim time, the Auto-Trim process stops automatically after a stop condition occurs (event 3, Figure 175). However, if a stop condition comes and High logic level holds on the Set input, the rheostat value will be switched near the set point until a Low level on the Set input occurs (event 7, Figure 175). Note that the Idle/Active signal changes its level to High (Auto-Trim is done) even if the user keeps a High logic level at the Set input.

After the end of the Auto-Trim process, Chopper ACMP powers down and its output goes to a Low logic level.

4. After a rising edge at the "Reload" signal, the value from NVM is copied to the rheostat Internal Counter overwriting current rheostat settings.

5. During this event user starts Auto-Trim process, but holds High logic level at Set input for a time longer than Auto-Trim process.

6. A "Program" signal comes. The "Program" command is latched and will be executed at the end of the Auto-Trim process.

7. The Auto-Trim process stops when the signal at the Set input goes to Low level. Note that a logic High level at the Set input was held longer than the time that was needed for the Auto-Trim process. At the end of the Auto-Trim process, the SLG47004 starts the NVM self-programming routine to copy the rheostat value from Reg LATCH to MPT NVM.

Figure 176 shows a similar Auto-Trim example. The only difference is that the user defined clock source as "External clock" from connection matrix. The clock pulses are present at the Clock input all the time, but have effect (rheostat value changes) during Trim time only. The stop condition for this case is the following: PT block reaches boundary value of 1023 and the logic level at change Set input is Low.

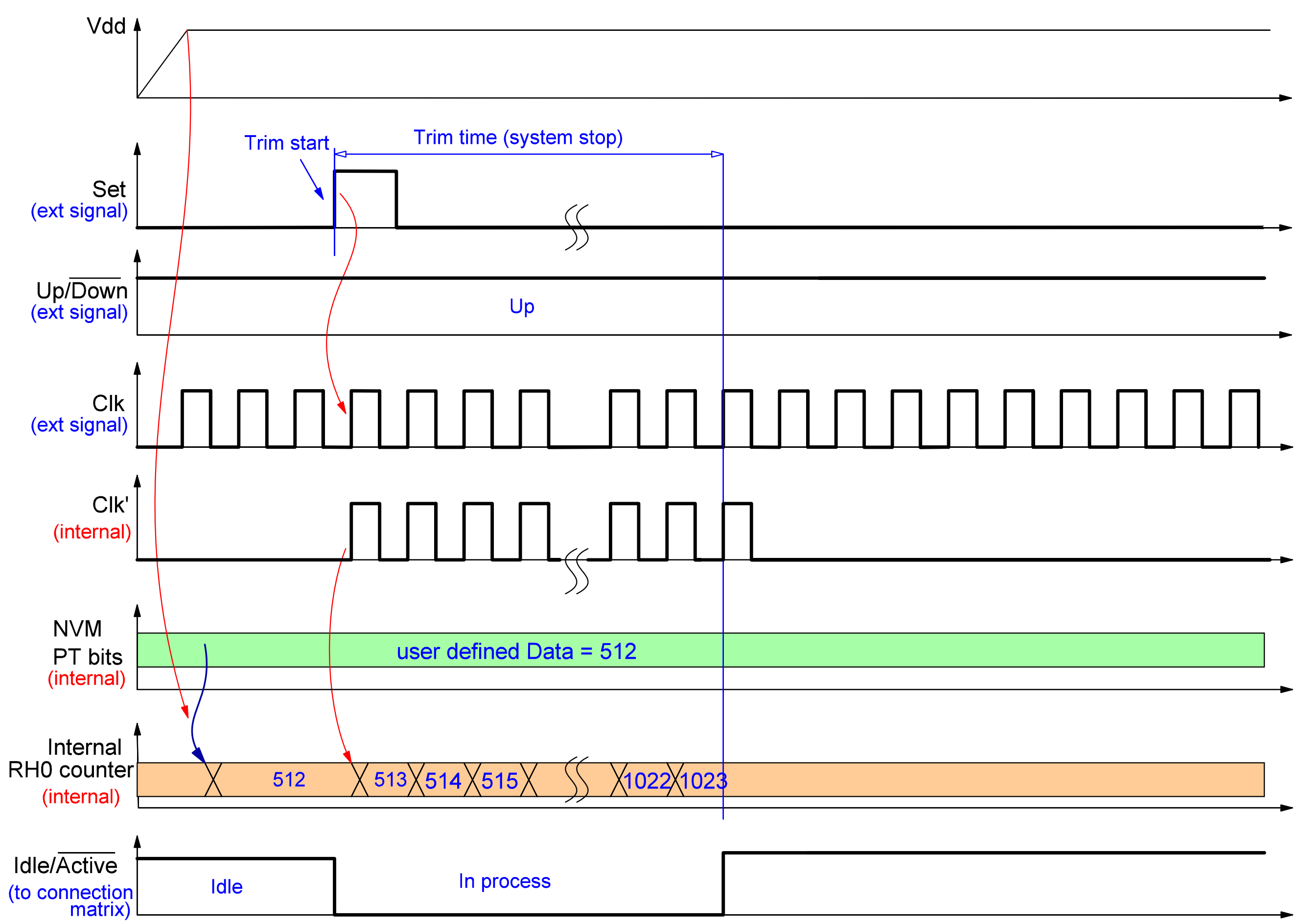


Figure 176: Example of Auto-Trim Process with External Clock Signal

Figure 177 shows Auto-Trim process flow for two rheostats.

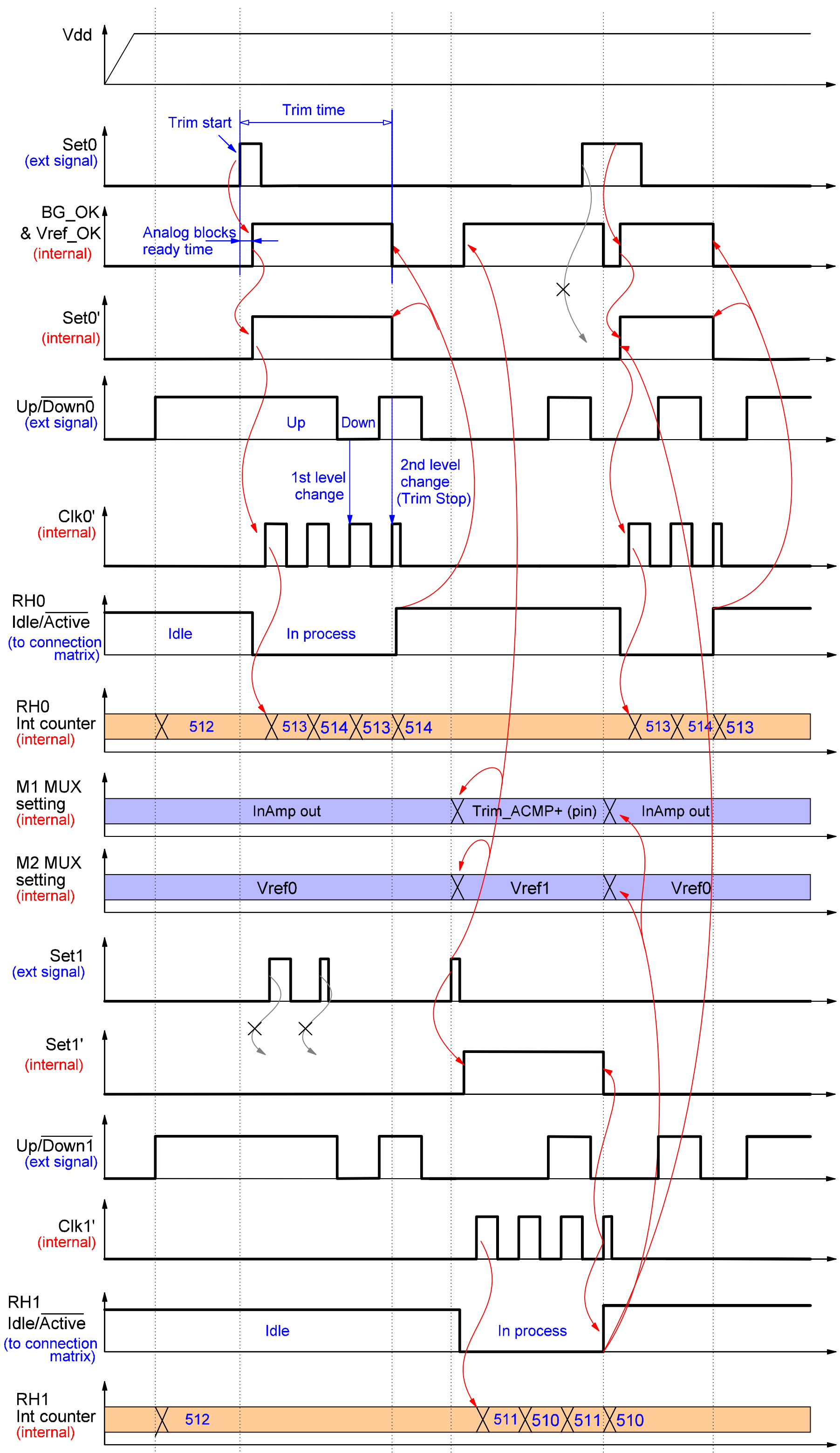


Figure 177: Example of Auto-Trim Process for Two Rheostats

12.4.2 I^{2}C Controlled Trimming Process with Auto-Trim Option Enabled

It's possible to start the Auto-Trim process via I^{2}C interface. In this case the user must configure the SLG47004 PT macrocell as described in Section 12.4.1. To start the Auto-Trim process via I^{2}C interface the user can use I^{2}C virtual inputs.

Also, an external I^{2}C master device can force the SLG47004 to reload the rheostat value from NVM ("Reload" command) or to copy rheostat value to NVM ("Program" command) using I^{2}C virtual inputs.

See Figure 178 for an example of the Auto-Trim process under external I^{2}C master control.

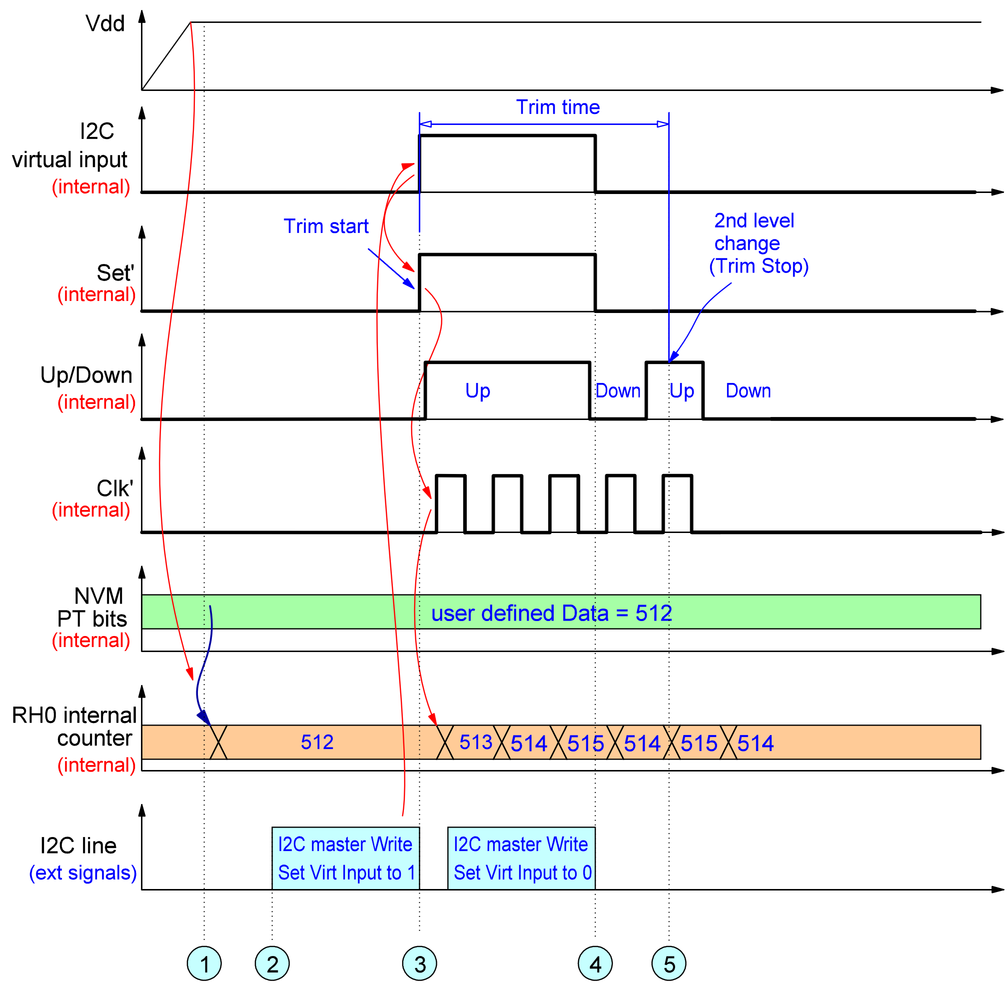


Figure 178: Example of Auto-Trim Process via I^{2}C

The key events of the Auto-Trim process under external I^{2}C master control are as follows:

1. During the startup event the SLG47004 loads the rheostat value from the NVM to the Internal Counter. In the example this value is 512.

2. I^{2}C master sends the message to set High one of the I^{2}C virtual inputs that is connected with Set input of the PT macrocell.

3. After the I^{2}C message is received and processed, the I^{2}C virtual input and the Set input will be at a High logic level. The Auto-Trim process begins.

4. I^{2}C master clears the virtual input and, consequently, the Set input. The Auto-Trim process goes on until a trim stop condition occurs.

5. The Auto-Trim process ends. The stop condition in this example is a 2nd change on Up/Down input at the moment of rising edge on the Clock input and Low level at the Set input.

12.4.3 Changing Rheostat Value Directly via I^{2}C

The user can perform their own trim algorithm setting the rheostat value directly via I^{2}C interface. In the example below, a microcontroller uses a user defined trim algorithm to change SLG47004's rheostat via I^{2}C interface (Figure 179). Note that during Auto-Trim process SLG47004 will return nACK, if master tries to get access (both read and write) to rheostats registers via I^{2}C.

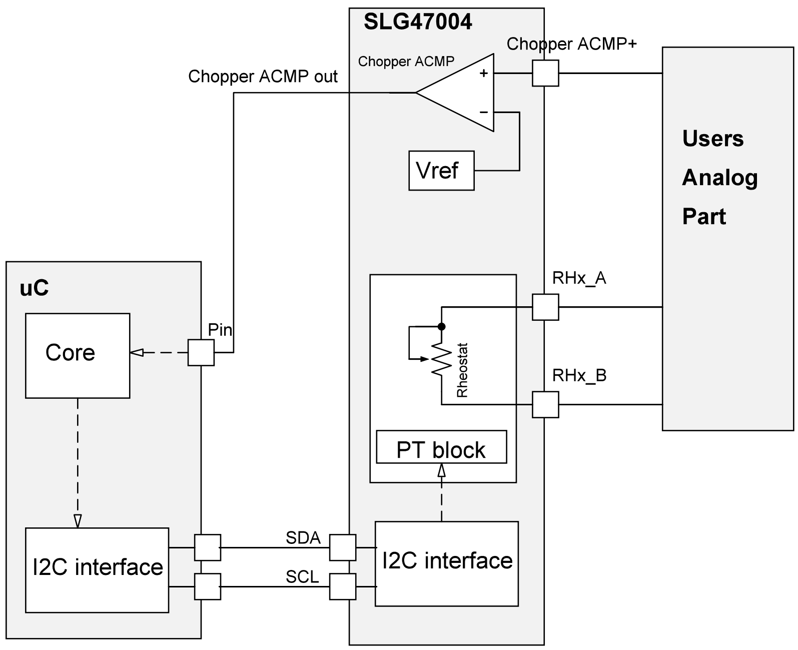


Figure 179: Example of Hardware Configuration

Note that the PT Registers are allowed to read and write via communication interface, if not protected.

The preliminary configuration of system shown in Figure 179 is the following:

- Auto_Cal _Dis_RHx bit is set to 1 (disable Auto-Trim mode);
- M1 MUX (registers [875:872])) is configured to work with user system voltage feedback (pin Chop_ACMP+);
- M2 MUX is configured to work with SLG47004 programmable Vref. Note that M2 MUX is simplified symbol of Chopper ACMP reference selection blocks (see Section 9.2);
- Chopper ACMP is powered up from connection matrix. Chopper ACMP out is connected to output pin;
- No Clock source for PT block.

The example of a system trim via I^{2}C is shown in the figure below. In this example the I^{2}C master uses a simple approximation algorithm for reaching the set point. Every next step the rheostat code is changed by ±(Previous rheostat code step value/2). The sign depends on the Chopper ACMP output. The algorithm steps are as follows:

- Set rheostat code to 1024/2 = 512;
- Wait until the system settles down and check if Chopper ACMP output = 1, then Next_rheostat_code = 512 + (512/2). If Chopper ACMP output = 0, then Next_rheostat_code = 512 - (512/2);
- Repeat previous step until Next_rheostat_code = Prev_rheostat_code ± 1;

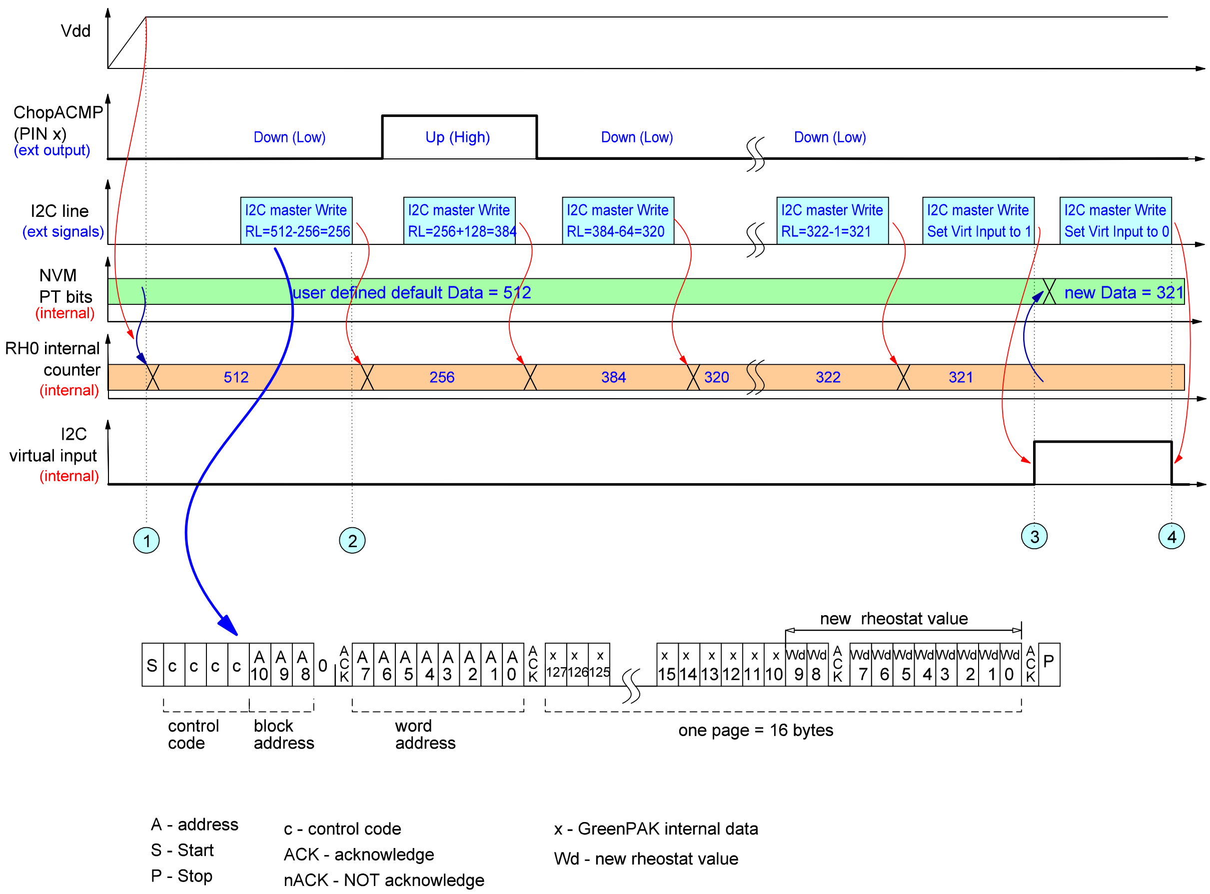


Figure 180: Example of User Specific Trimming Process under I^{2}C Master Control

The key events of a user specific trimming process under I^{2}C master control are as follows:

1. During the startup event the SLG47004 loads the rheostat value from NVM to Internal Counter. In the example this value is 512.

2. I^{2}C master writes a new value to the Rheostat's Internal Counter according to Chopper ACMP output. Note that the minimum time for changing the rheostat code depends on the time response of the user system.

3. After the trim process is completed, the I^{2}C master sets the I^{2}C virtual input to logic "1". This input is connected to the "Program" signal of the PT macrocell. The rising edge on this input starts the NVM self-programming routine.

4. The I^{2}C master clears the I^{2}C virtual input.

Additionally, the I^{2}C Master macrocell can use internal resources such as an ADC to read the system data, find the error, and then adjust the Rheostat value. Also, it is possible to change the Rheostat value for different conditions. For example, the I^{2}C Master macrocell can change the Rheostat value based on the temperature change to reduce the system error.

12.5 USING CHOPPER ACMP

When the Auto-Trim Function is disabled, the Chopper comparator can be used as a standalone analog comparator. Inputs of the Chopper ACMP are selected by the M1 and M2 analog MUXs. Output of the Chopper ACMP can be optionally inverted by register [882]. This comparator output is the input [55] of the connection matrix. In case of a disabled Auto-Trim Function, the power up source for the Chopper ACMP comes from connection matrix. Please refer to Section 9 for more details.

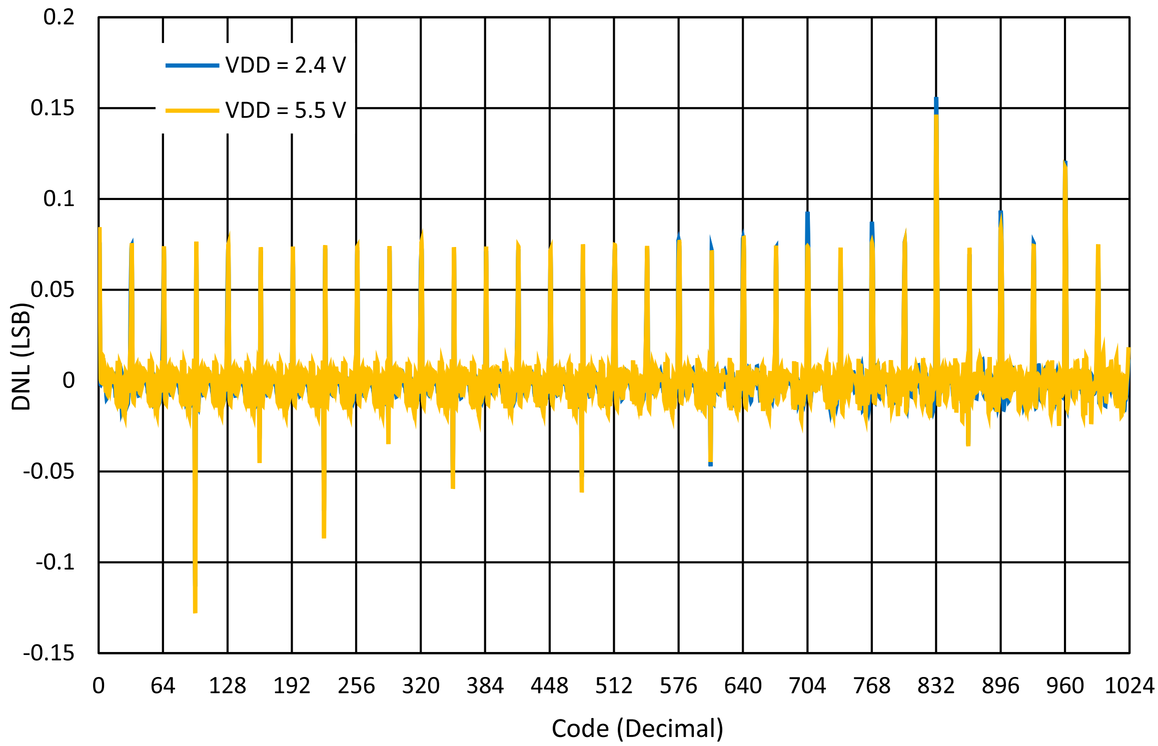


Figure 181: DNL vs. Digital Code, Rheostat Mode (V_{AB} = 1 V) at T = 25 °C

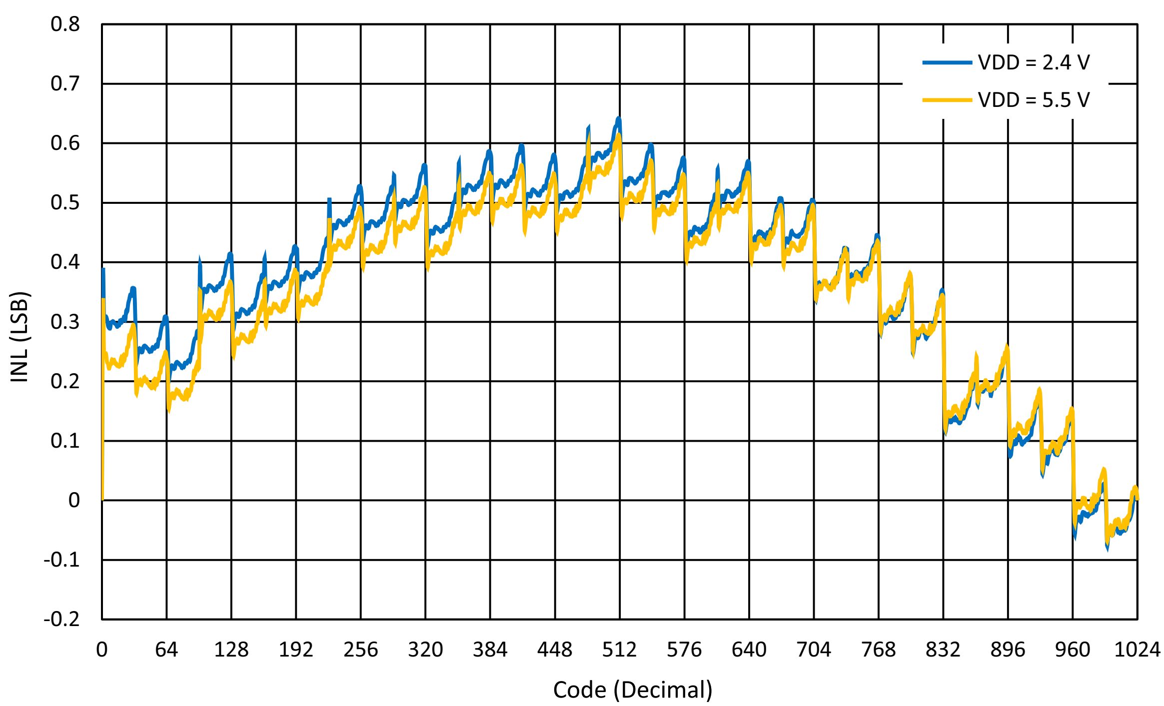


Figure 182: INL vs. Digital Code, Rheostat Mode (V_{AB} = 1 V) at T = 25 °C

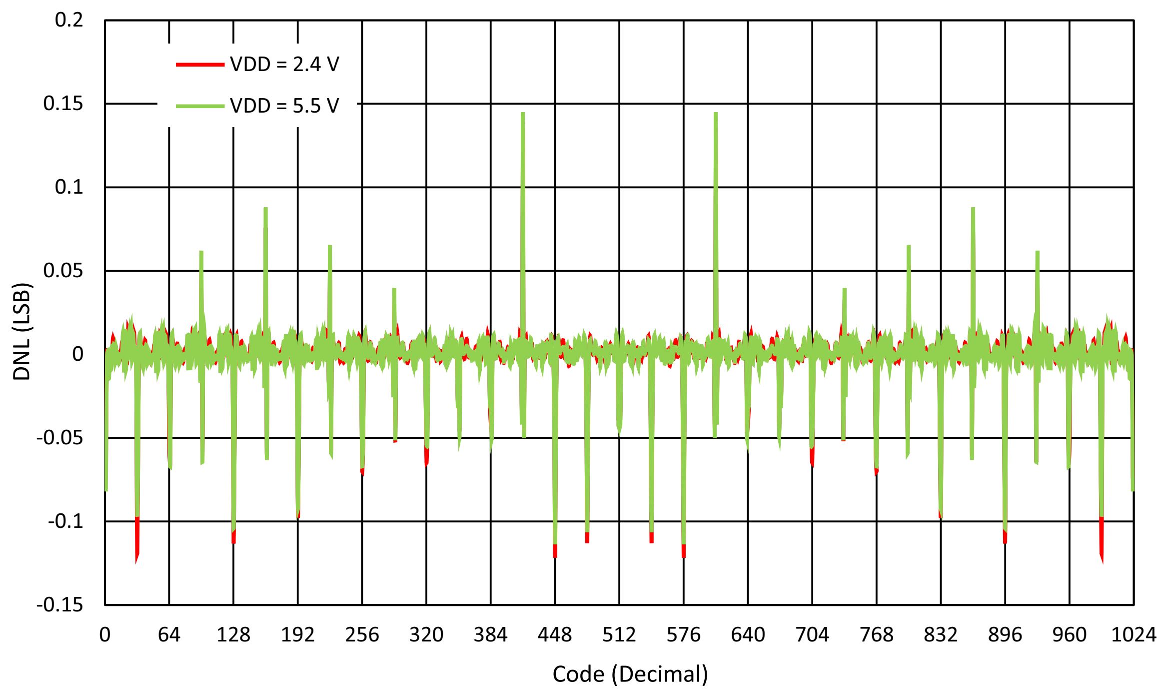


Figure 183: DNL vs. Digital Code, Potentiometer Mode (V_{AB} = 1 V) at T = 25 °C

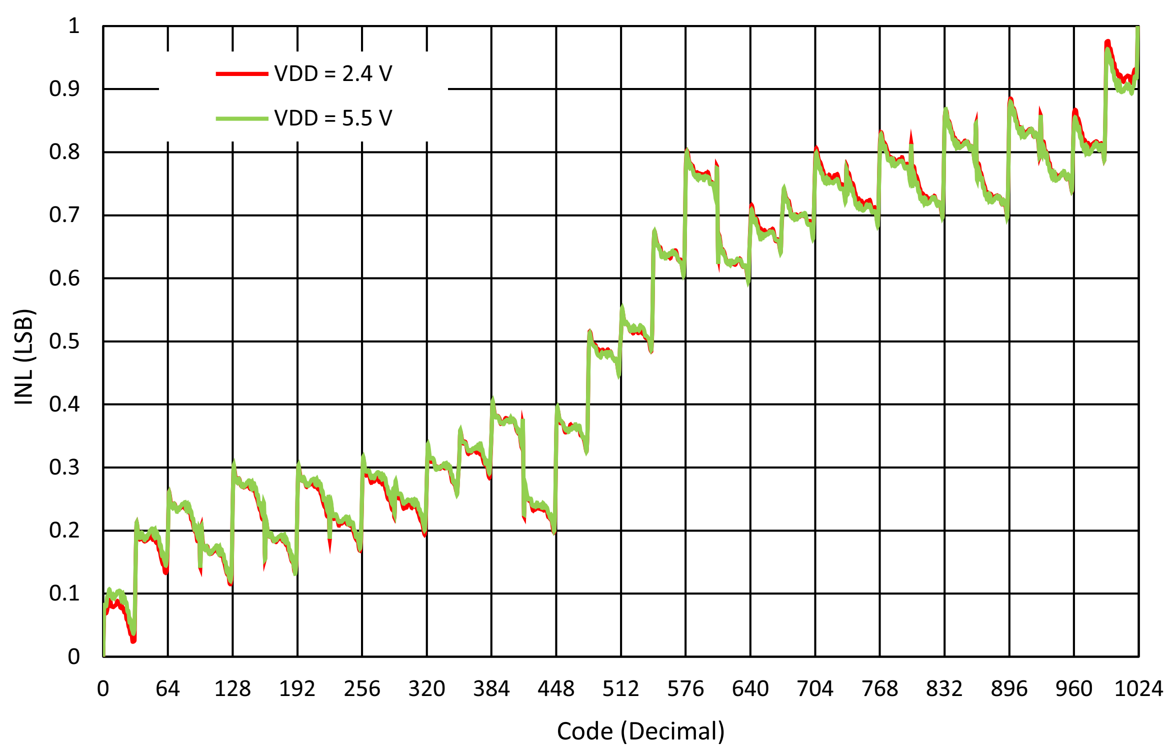


Figure 184: INL vs. Digital Code, Potentiometer Mode (V_{AB} = 1 V) at T = 25 °C

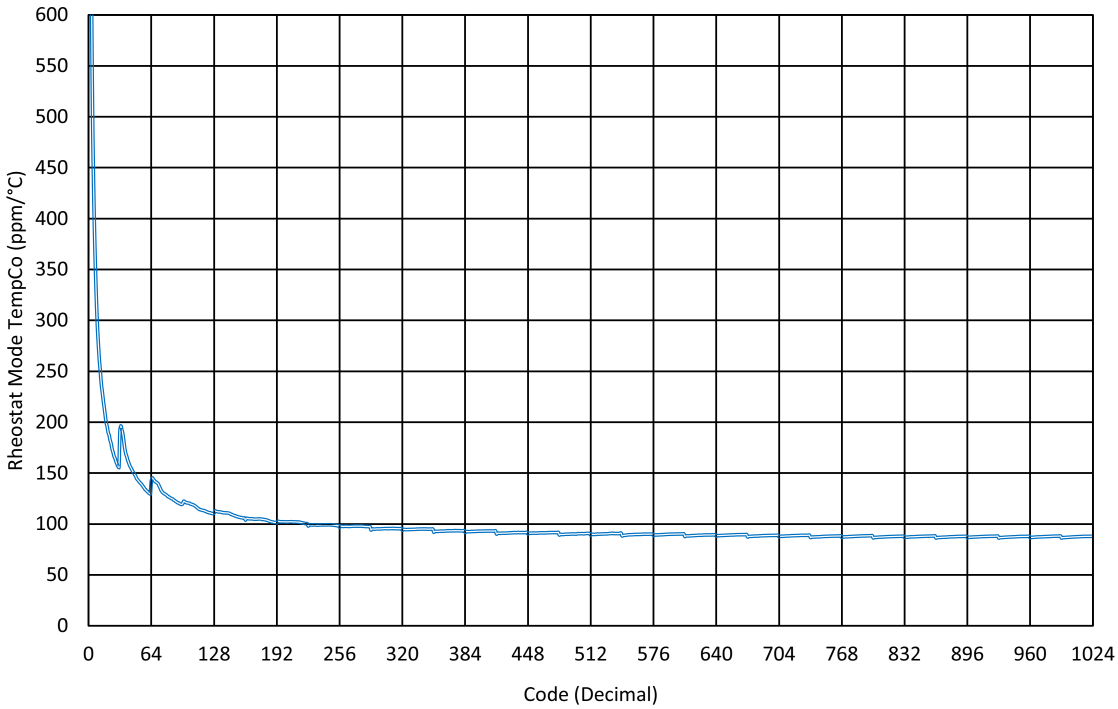


Figure 185: $(\Delta R_{AB}/R_{AB})/\Delta T_A$ Rheostat Mode Tempco

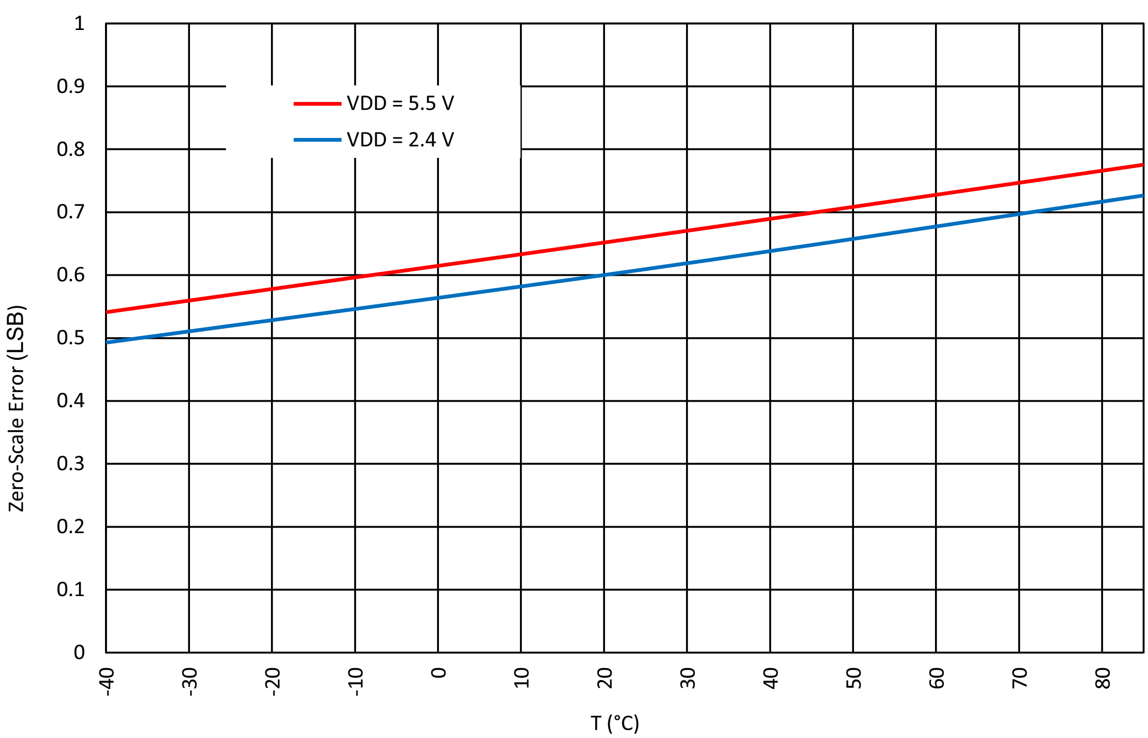


Figure 186: RHx Zero Scale Error vs. Temperature (V_{IN} = 1 V)

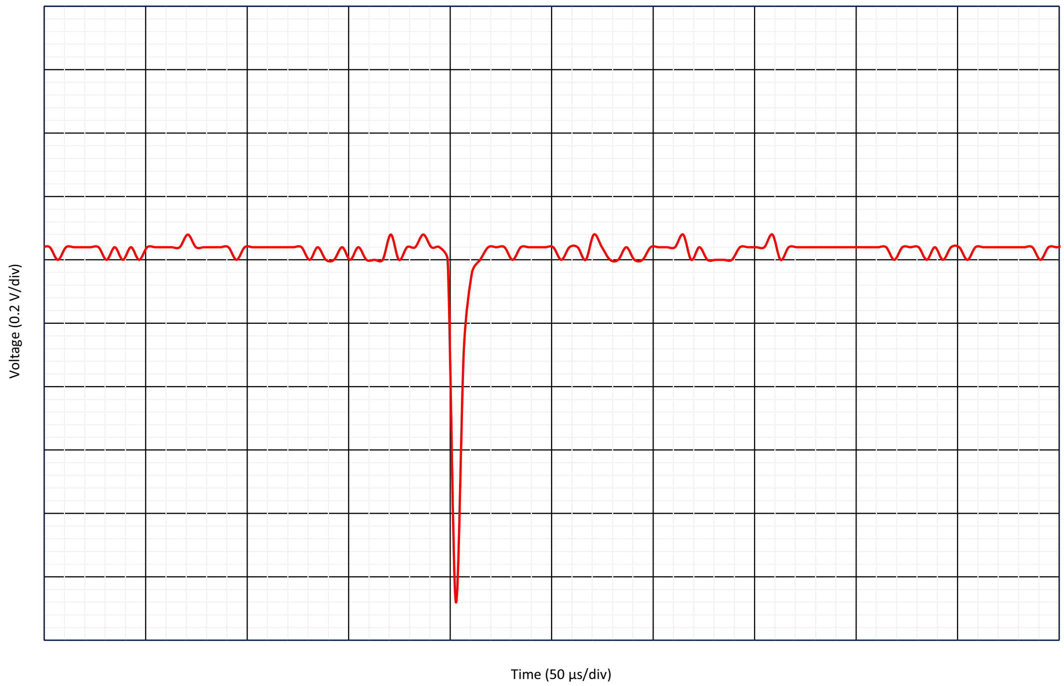


Figure 187: Transition Glitch in Worst Case (Code = 511 to Code = 512)

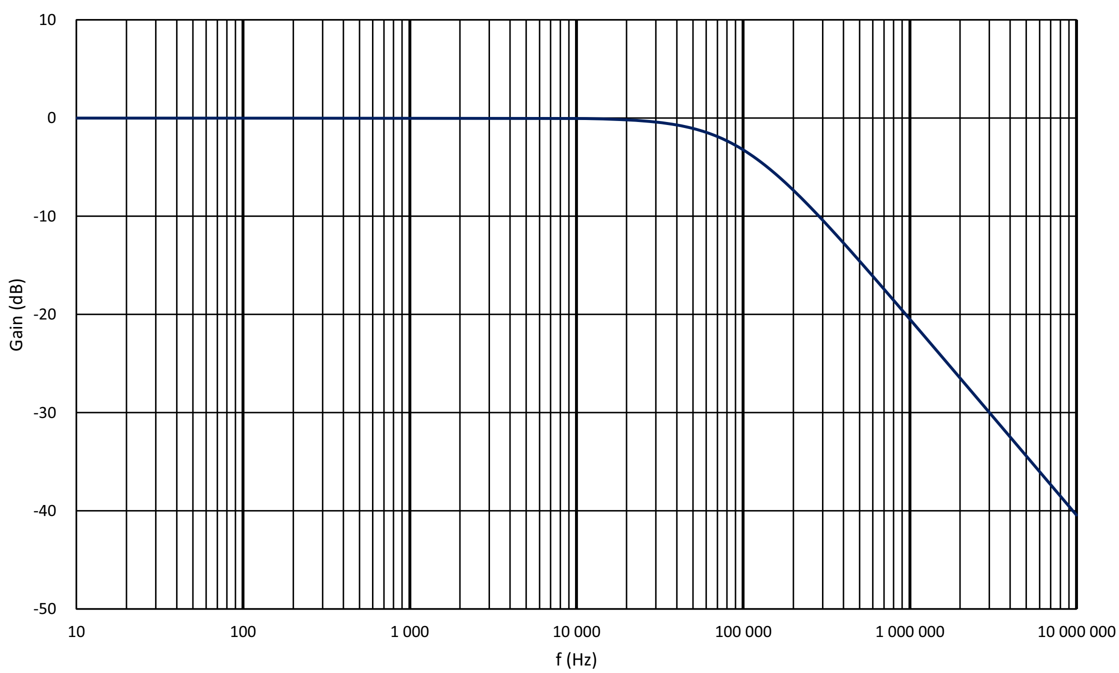


Figure 188: Gain vs. Frequency (Code = 512) at T = 25 °C, V_{DDA} = 5 V

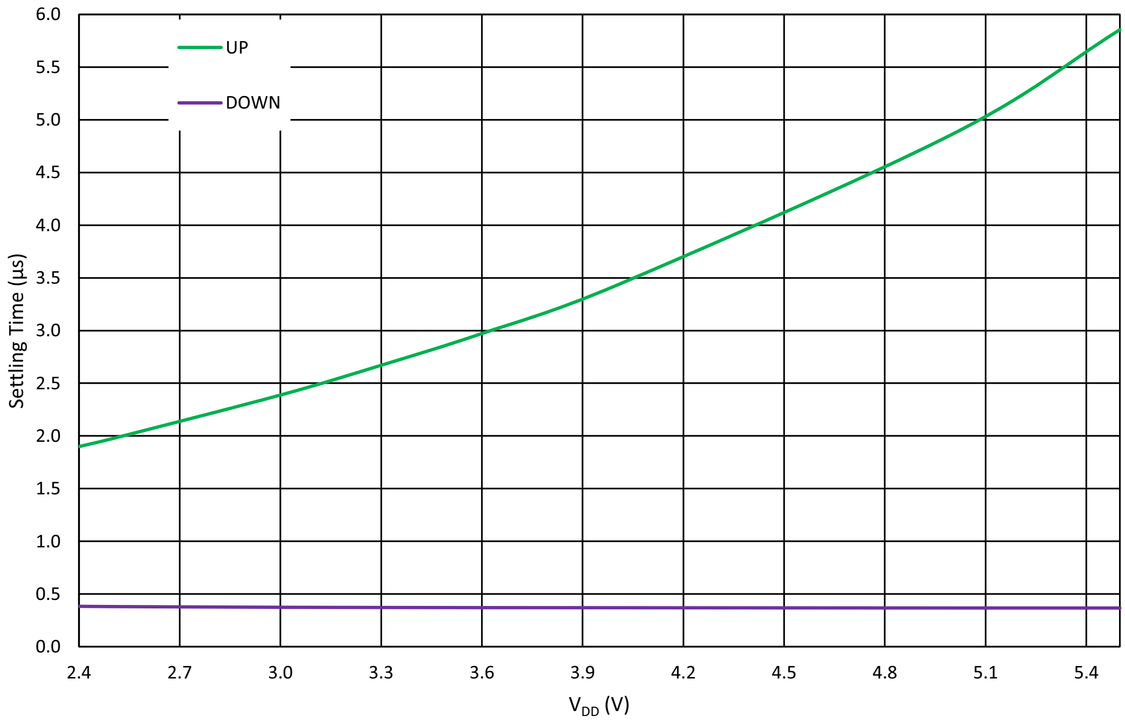


Figure 189: RHx Settling Time vs. V_{DD} at I_{LOAD} = 1 mA, T = 25 °C

13 Programmable Delay/Edge Detector

The SLG47004 has a programmable time delay logic cell available, that can generate a delay that is selectable from one of four timings (time 2) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay, as well as glitch rejection during the delay period. See Figure 191 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

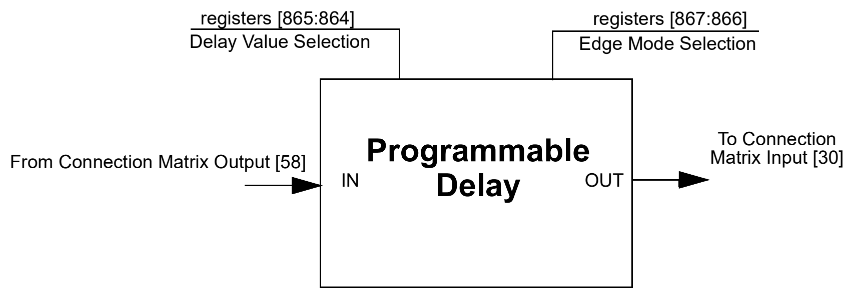


Figure 190: Programmable Delay

13.1 PROGRAMMABLE DELAY TIMING DIAGRAM - EDGE DETECTOR OUTPUT

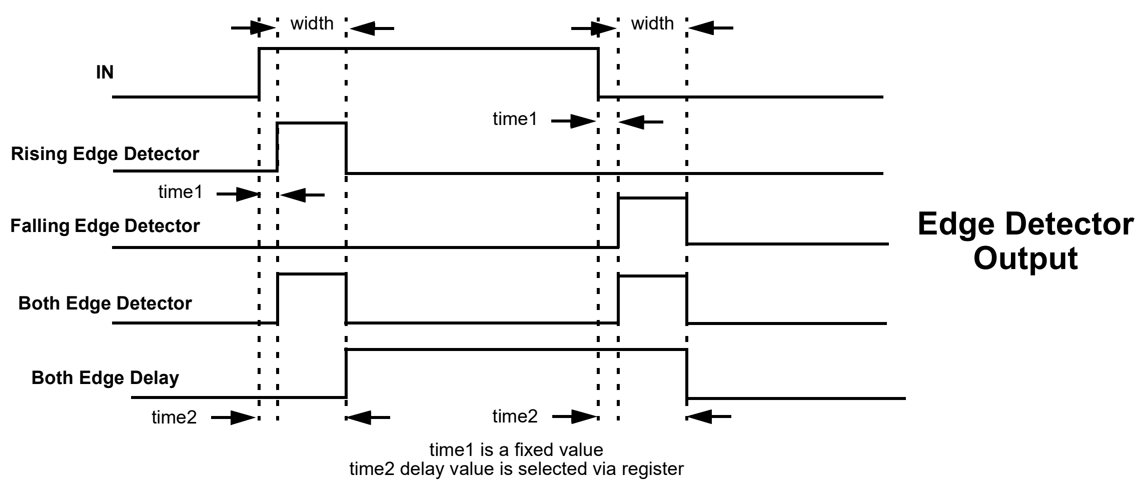


Figure 191: Edge Detector Output

Please refer to Table 12.

14 Additional Logic Function. Deglitch Filter

The SLG47004 has one Deglitch Filter macrocell with inverter function that is connected directly to the Connection Matrix inputs and outputs. In addition, this macrocell can be configured as an Edge Detector, with the following settings:

- Rising Edge Detector
- Falling Edge Detector
- Both Edge Detector
- Both Edge Delay

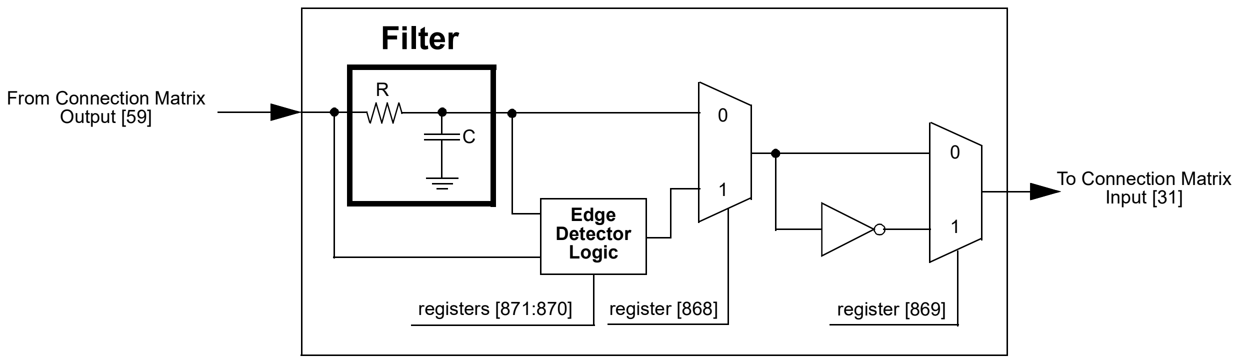


Figure 192: Deglitch Filter or Edge Detector

15 Voltage Reference

15.1 VOLTAGE REFERENCE OVERVIEW

The SLG47004 has a Voltage Reference (Vref) Macrocell to provide reference to analog comparators and operational amplifiers. The macrocell also has the option to output reference voltages on external pins (see Table 1). Vref0 and Vref1 share output buffers with Temperature sensor. Note that user can use any of output buffers, but Temperature sensor is calibrated for Vref1 output buffer. See Table 58 for the available selections for each analog comparator. Also, see Figure 193, Figure 194, and Figure 195, which show the reference output structure.

Also there is a high drive voltage reference macrocell called HD Buffer. The purpose of this macrocell is to provide stable voltage to the relatively high-power load (Please refer to the Table 19). HD Buffer has shared voltage reference source with the Op Amp0 Vref. User can select output voltage in the range from $V_{DD}/64$ to V_{DD} with a step $V_{DD}/64$, or output voltage in a range from 32 mV to 2.048 V with a step 32 mV (see Figure 195).

Note that Chopper ACMP will automatically enable HD Buffer if HD Buffer is selected as a source for Chopper ACMP In-signal (register 946 = 0) and Chopper ACMP is powered up.

15.2 VREF SELECTION TABLE

Table 58: Vref Selection Table

SEL[5:0]	Vref	SEL[5:0]	Vref
0	0.032	33	1.088
1	0.064	34	1.12
2	0.096	35	1.152
3	0.128	36	1.184
4	0.16	37	1.216
5	0.192	38	1.248
6	0.224	39	1.28
7	0.256	40	1.312
8	0.288	41	1.344
9	0.32	42	1.376
10	0.352	43	1.408
11	0.384	44	1.44
12	0.416	45	1.472
13	0.448	46	1.504
14	0.48	47	1.536
15	0.512	48	1.568
16	0.544	49	1.6
17	0.576	50	1.632
18	0.608	51	1.664
19	0.64	52	1.696
20	0.672	53	1.728
21	0.704	54	1.76
22	0.736	55	1.792
23	0.768	56	1.824
24	0.8	57	1.856
25	0.832	58	1.888
26	0.864	59	1.92
27	0.896	60	1.952

Table 58: Vref Selection Table(Continued)

SEL[5:0]	Vref	SEL[5:0]	Vref
28	0.928	61	1.984
29	0.96	62	2.016
30	0.992	63	2.048
31	1.024	64	External
32	1.056		

15.3 VREF BLOCK DIAGRAM

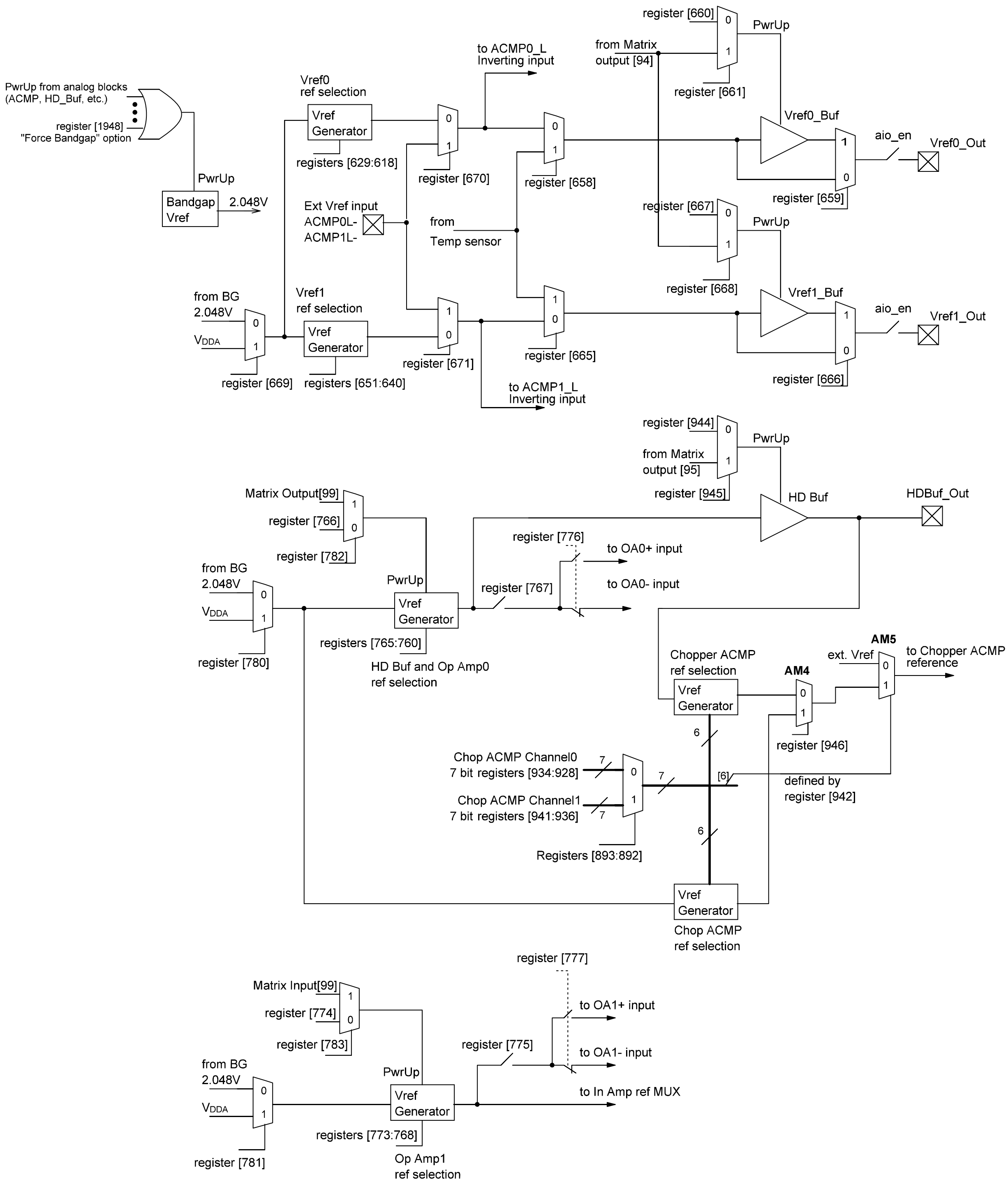


Figure 193: Generalized Vref Structure

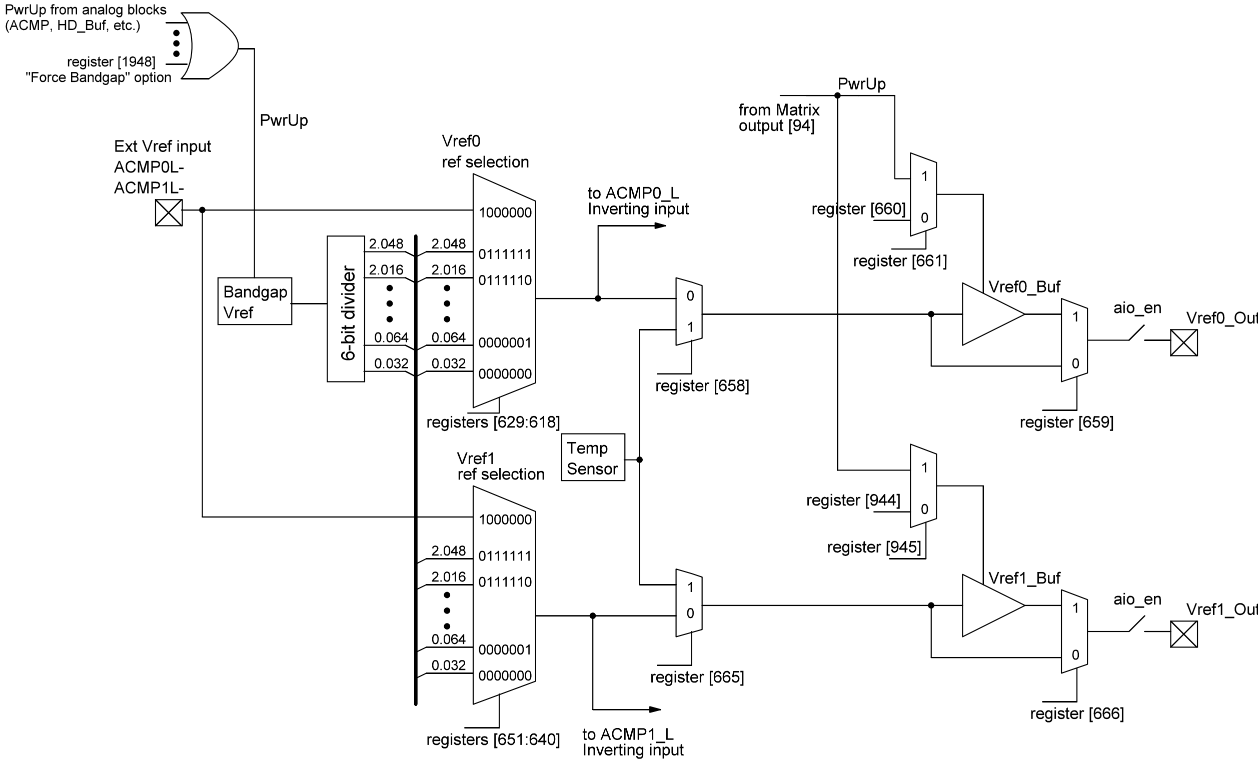


Figure 194: ACMP0L, ACMP1L Voltage Reference Block Diagram

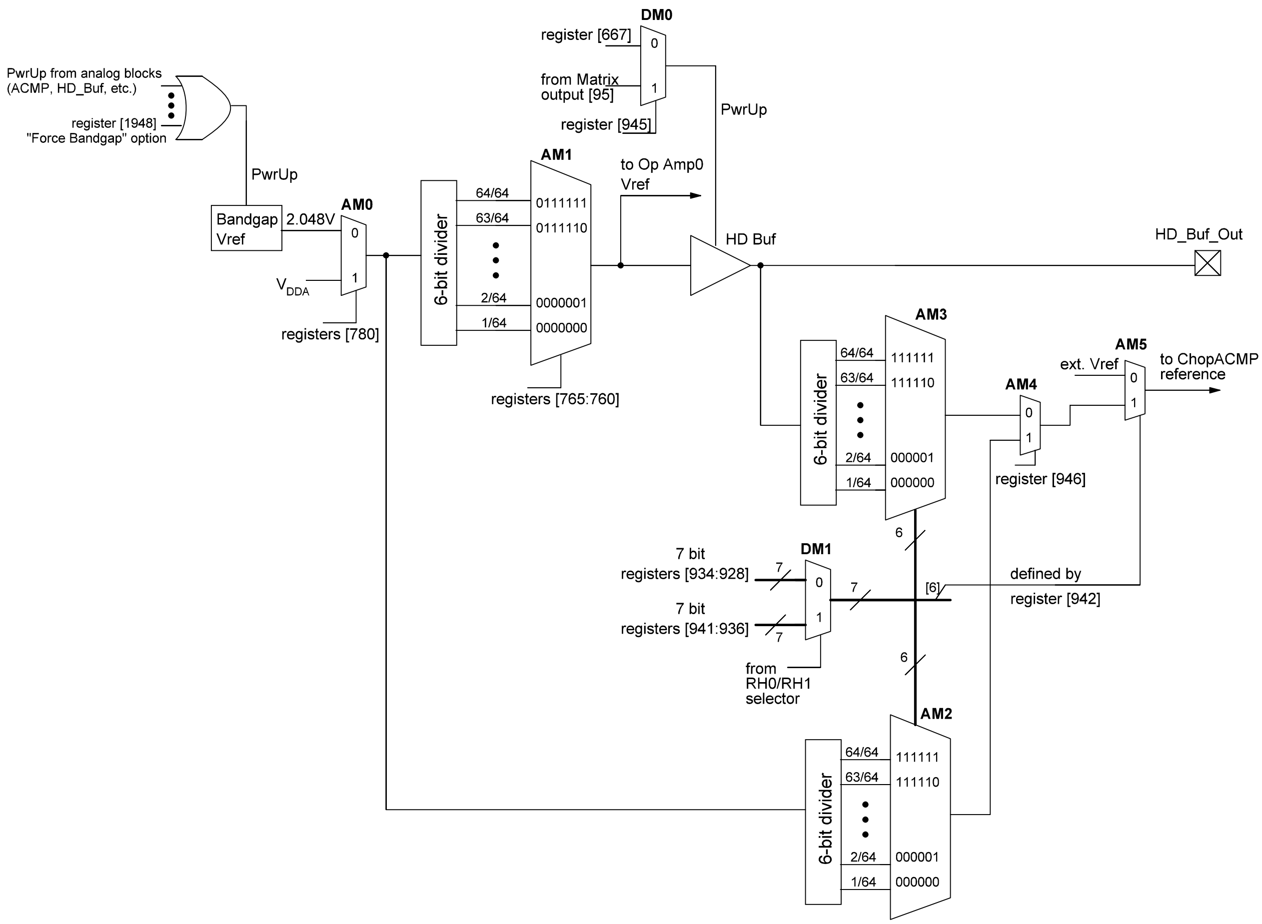


Figure 195: HD Buffer and Chopper ACMP Reference Block Diagram

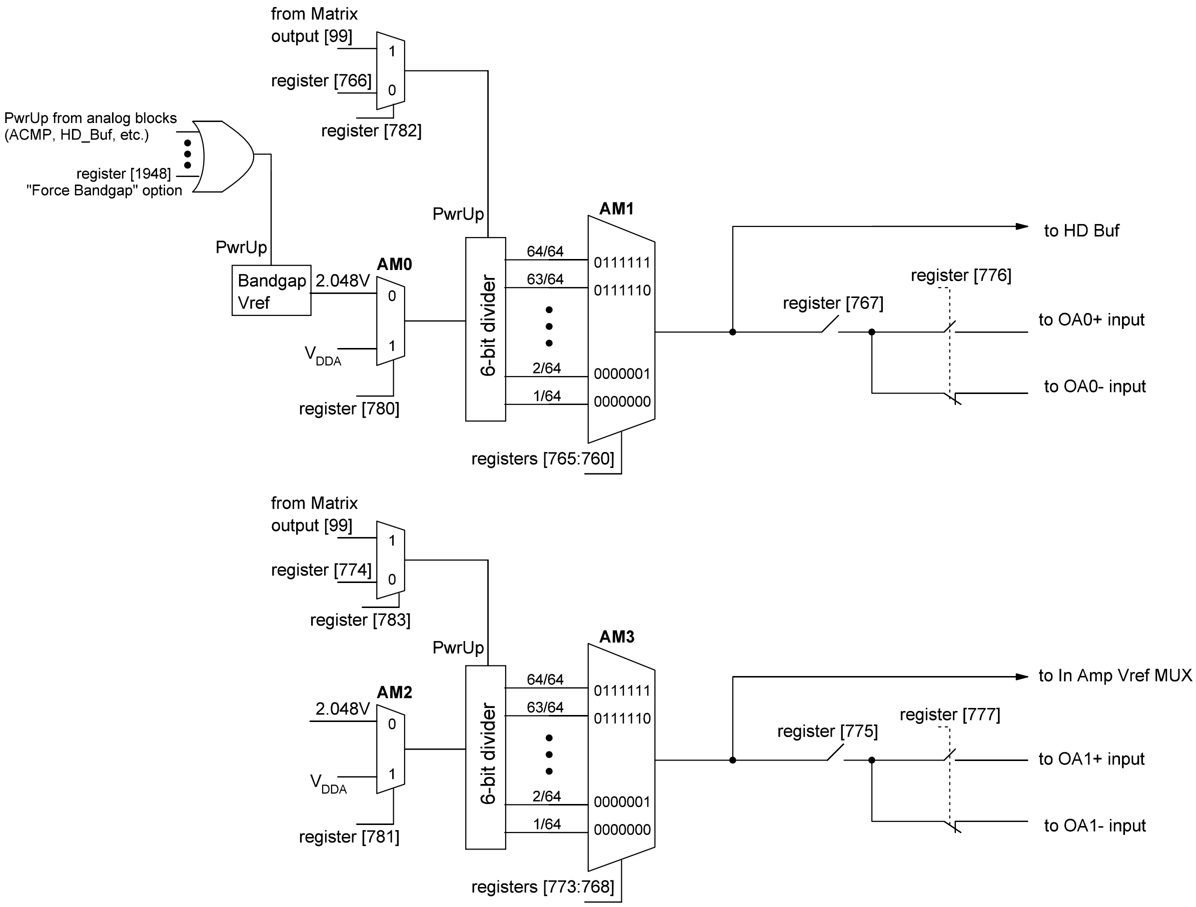


Figure 196: Operational Amplifiers Voltage Reference Block Diagram

15.4 VOLTAGE REFERENCE TYPICAL PERFORMANCE

Note 1 It is not recommended to use Vref connected to external pin without buffer.

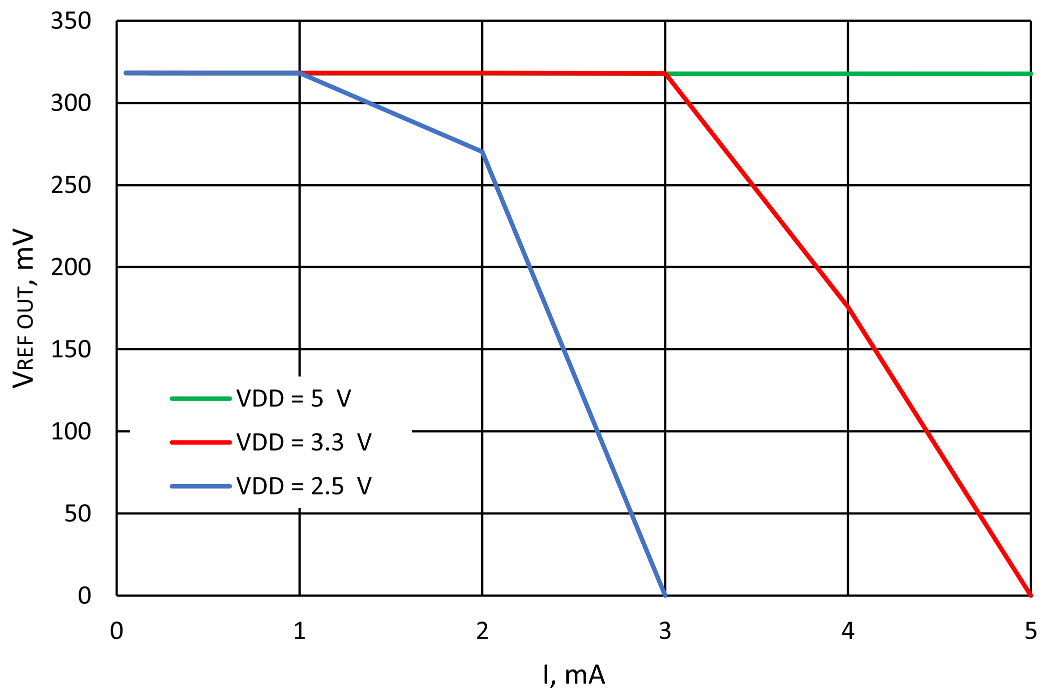


Figure 197: Typical Load Regulation, Vref = 320 mV, T = -40 °C to +85 °C, Buffer - Enable

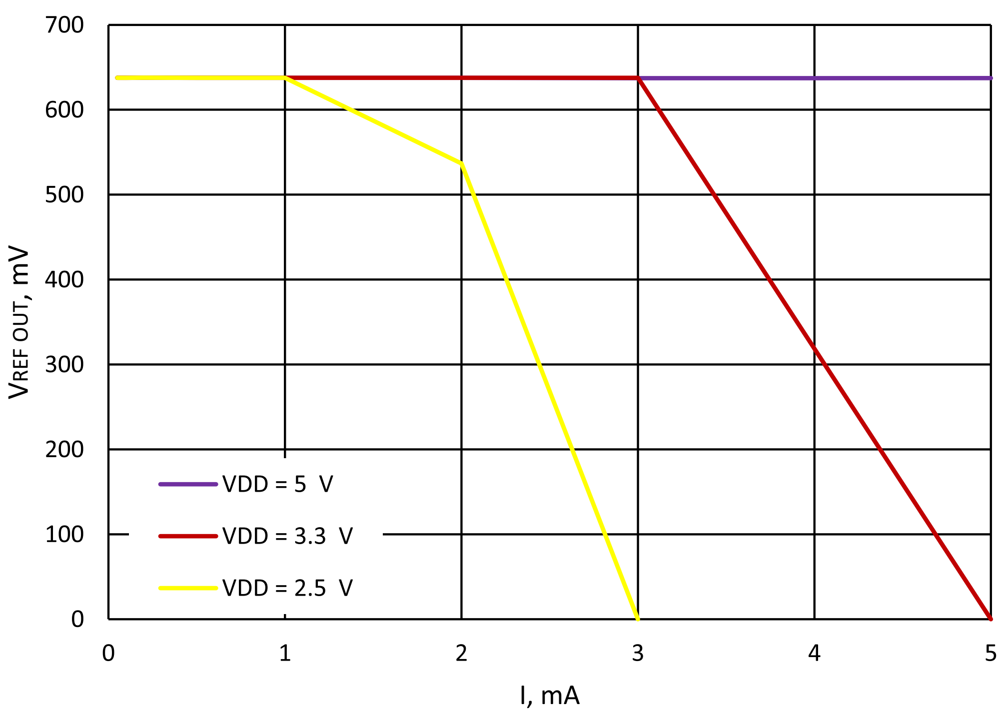


Figure 198: Typical Load Regulation, Vref = 640 mV, T = -40 °C to +85 °C, Buffer - Enable

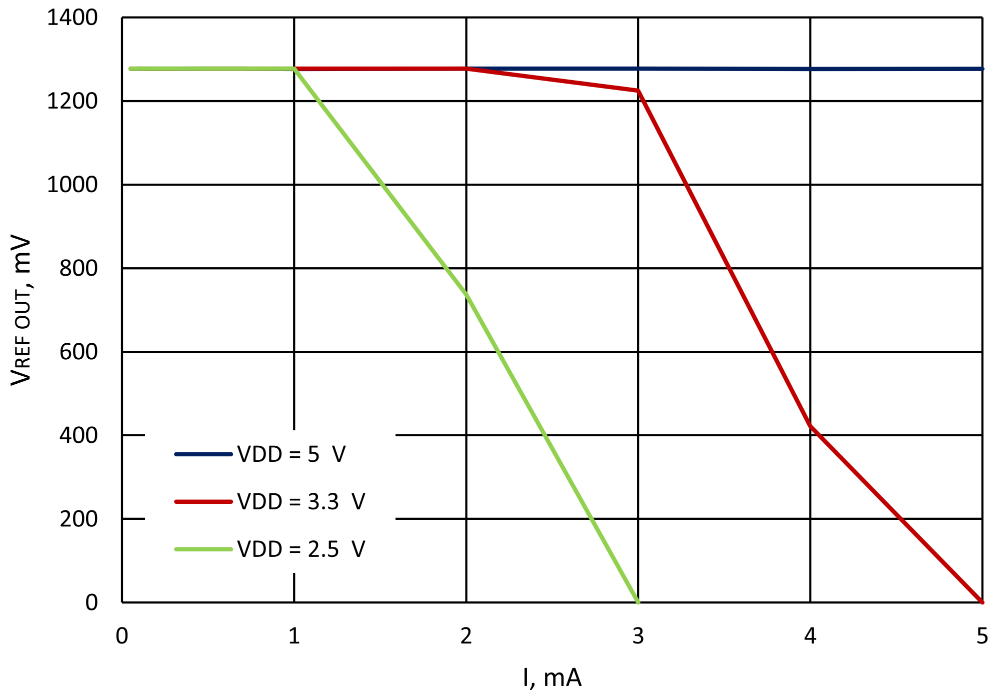


Figure 199: Typical Load Regulation, Vref = 1280 mV, T = -40 °C to +85 °C, Buffer - Enable

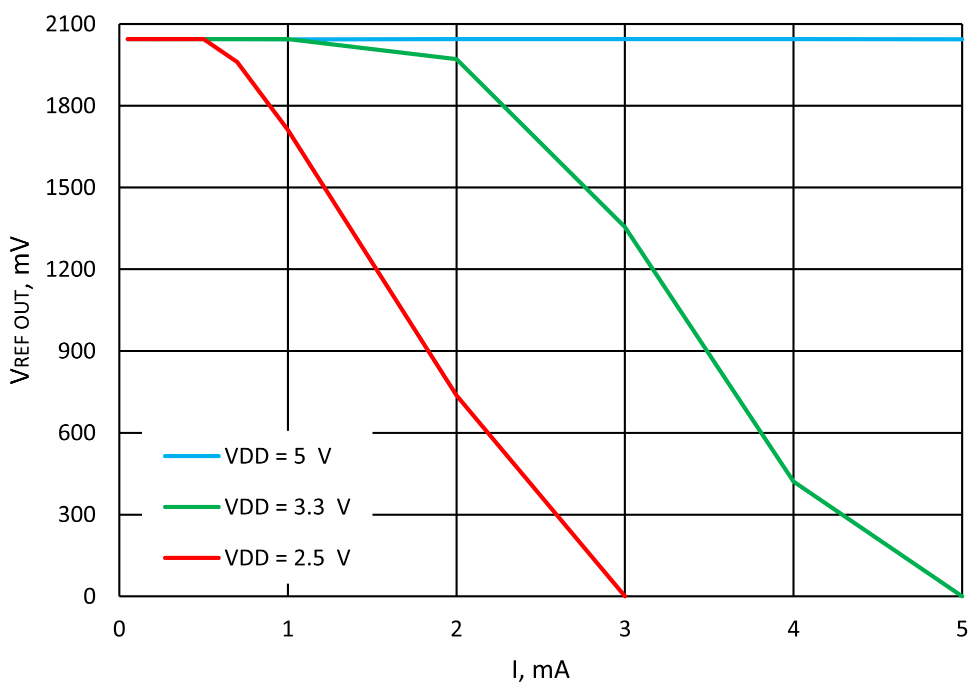


Figure 200: Typical Load Regulation, Vref = 2048 mV, T = -40 °C to +85 °C, Buffer - Enable

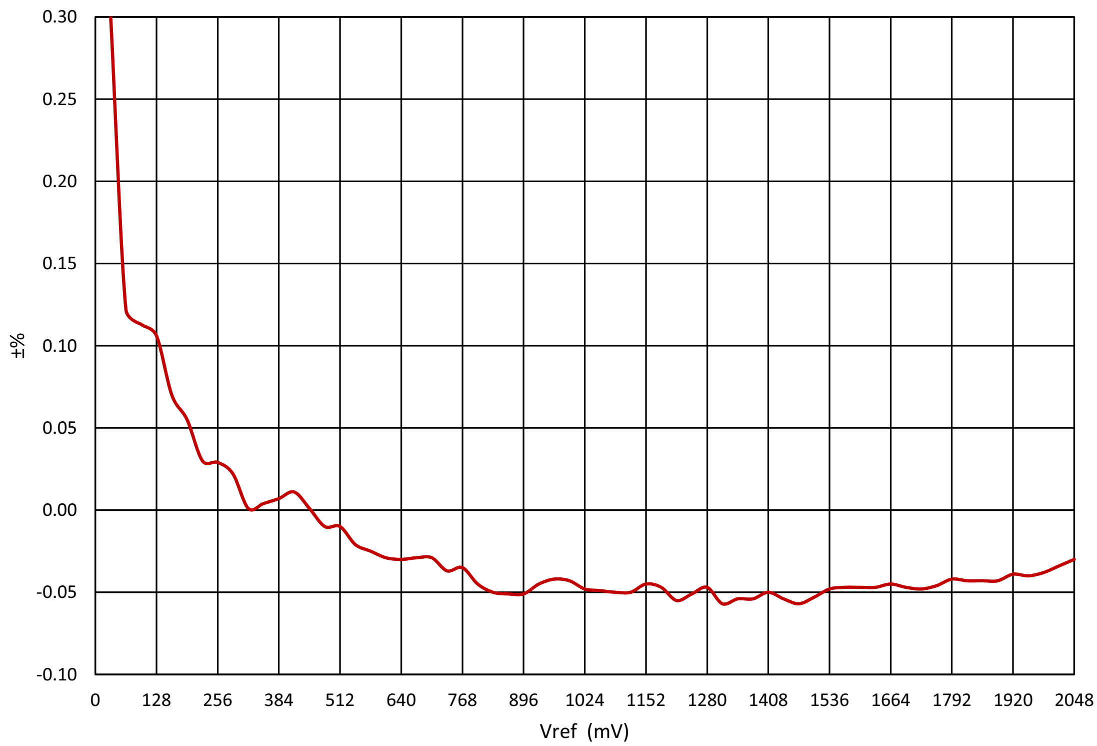


Figure 201: Typical Input Offset Voltage vs. Vref at V_{DD} = 2.4 V to 5.5 V, T = 25 °C, Buffer Disabled

.

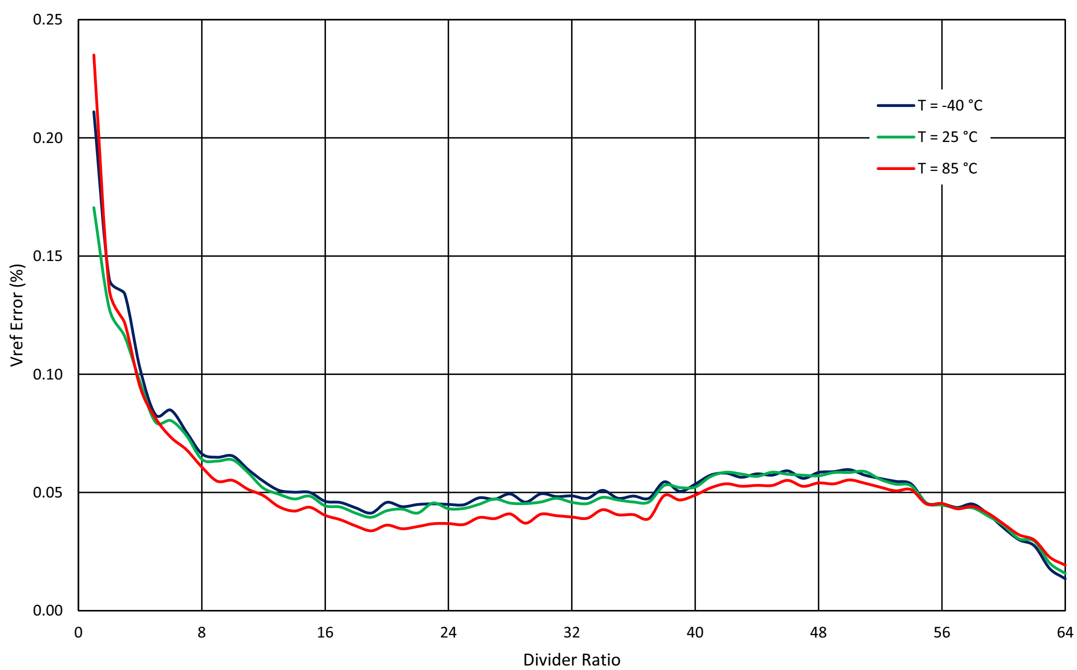


Figure 202: Op Ampx Vref Divider Acuuracy at V_{DD} = 3.3 V

15.5 HD BUFFER TYPICAL PERFORMANCE

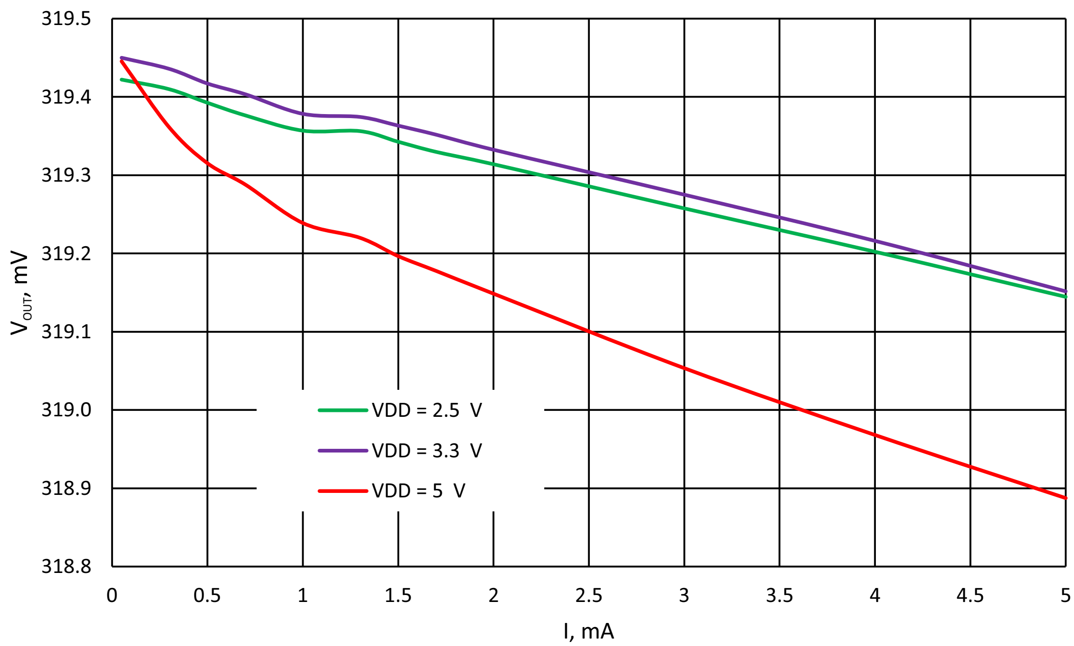


Figure 203: HD Buffer Typical Load Regulation, Vref = 320 mV, T = -40 °C to +85 °C

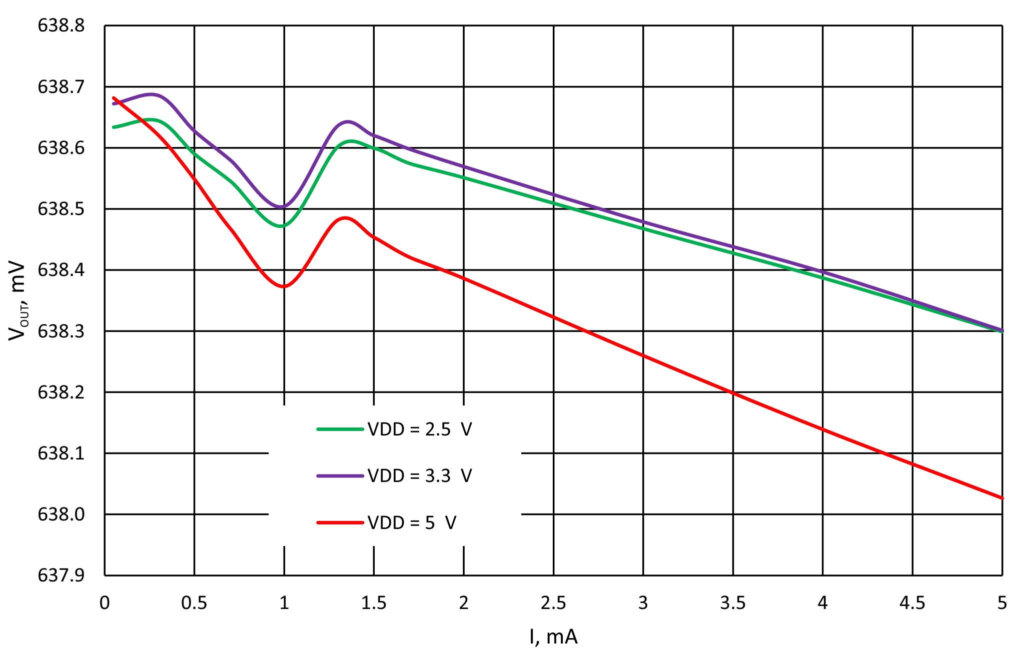


Figure 204: HD Buffer Typical Load Regulation, Vref = 640 mV, T = -40 °C to +85 °C

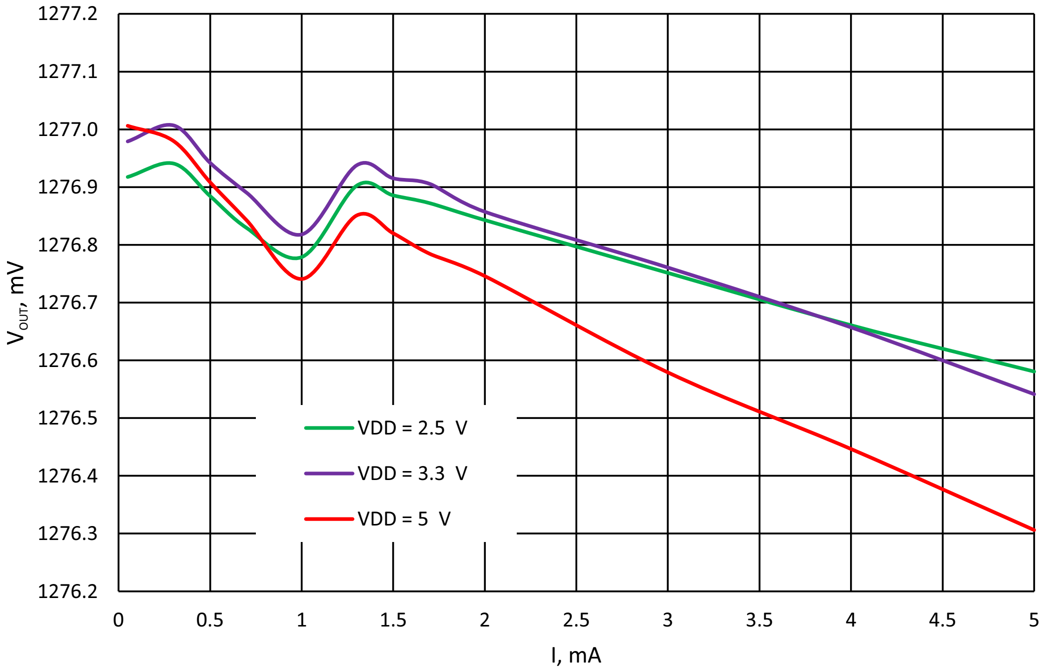


Figure 205: HD Buffer Typical Load Regulation, Vref = 1280 mV, T = -40 °C to +85 °C

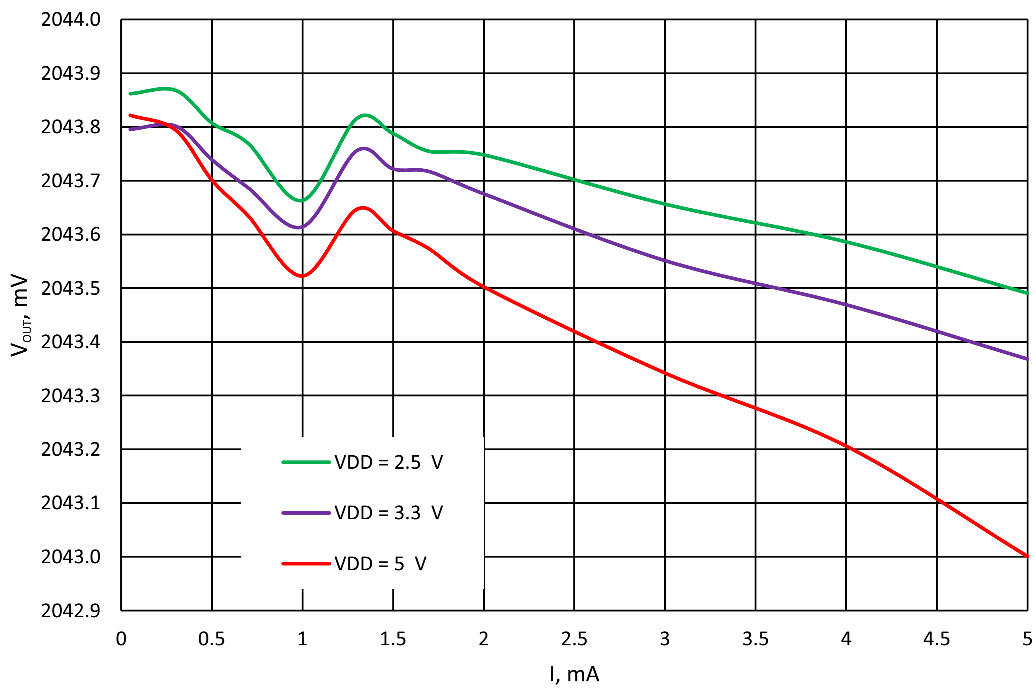


Figure 206: HD Buffer Typical Load Regulation, Vref = 2048 mV, T = -40 °C to +85 °C

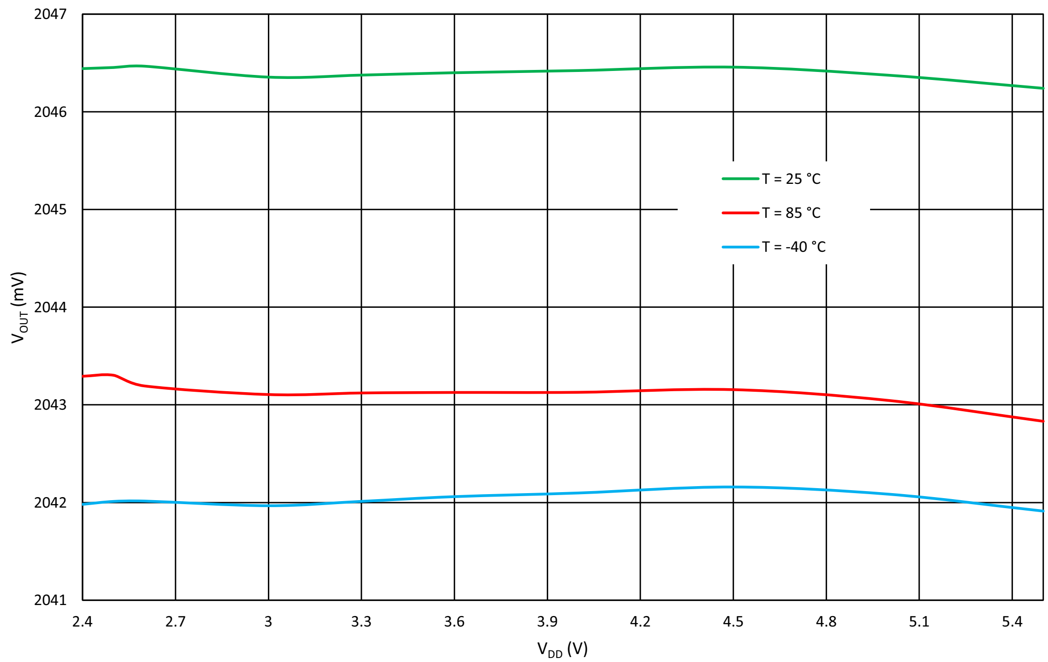


Figure 207: HD Buffer Typical Line Regulation, I_{LOAD} = 5 mA

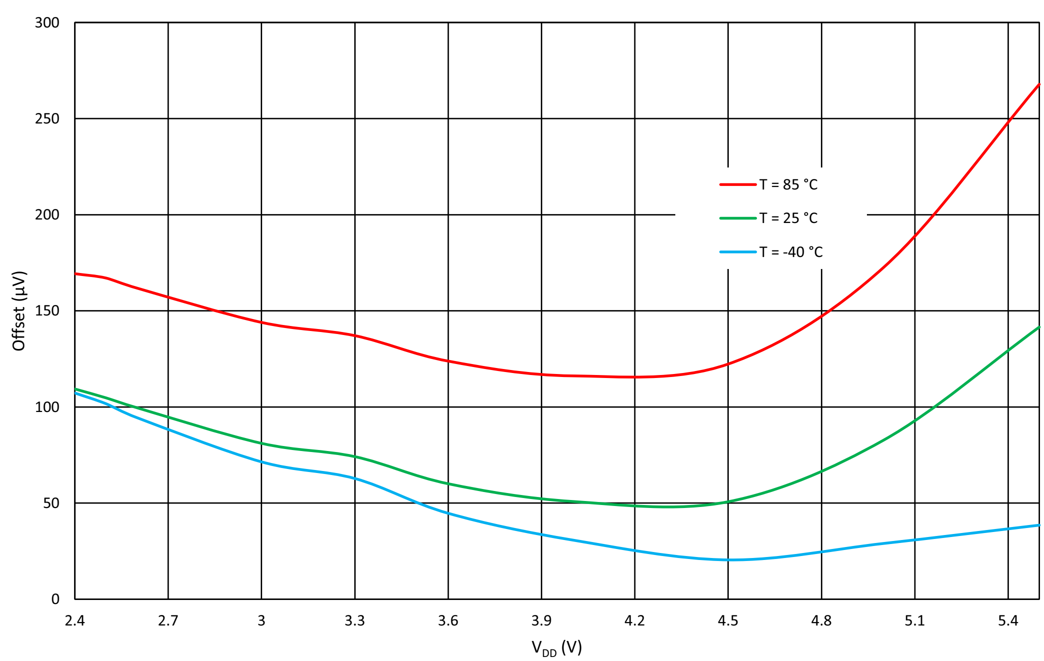


Figure 208: HD Buffer Offset vs. V_{DD}

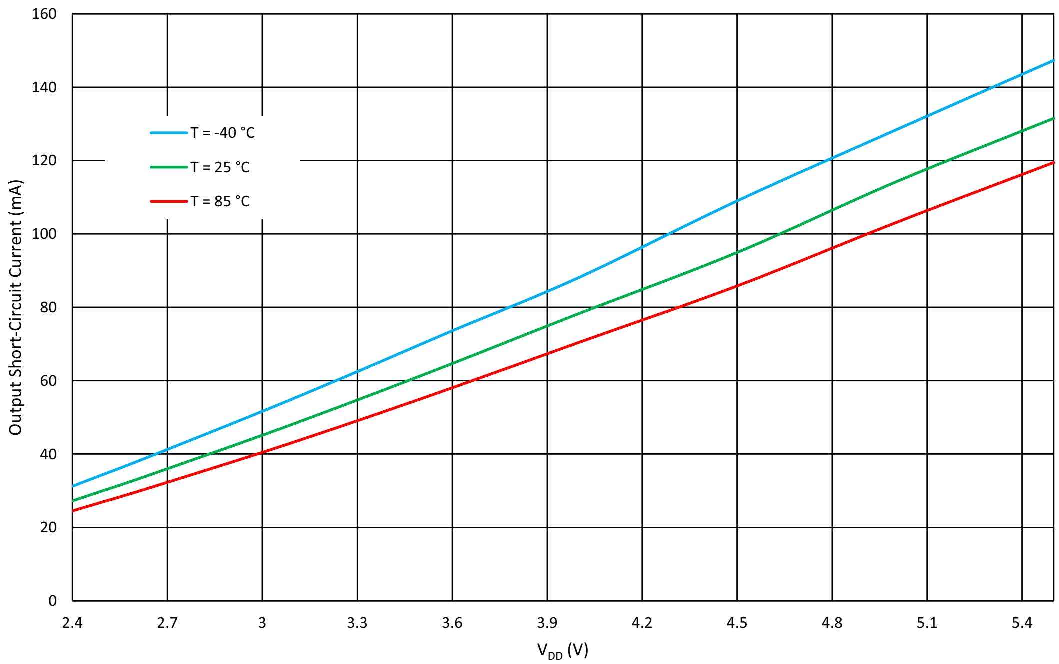


Figure 209: HD Buffer Output Short-Circuit Current vs. V_{DD}

16 Clocking

16.1 OSC GENERAL DESCRIPTION

The SLG47004 has three internal oscillators to support a variety of applications:

- Oscillator0 (2.048 kHz)
- Oscillator1 (2.048 MHz)
- Oscillator2 (25 MHz)

There are two divider stages for each oscillator that give the user flexibility for introducing clock signals to connection matrix, as well as various other Macrocells. The pre-divider (first stage) for Oscillator allows the selection of /1, /2, /4, or /8 to divide down frequency from the fundamental. The second stage divider has an input of frequency from the pre-divider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24, or /64 on Connection Matrix Input lines [52], [53], and [54]. Please see Figure 213 for more details on the SLG47004 clock scheme.

Oscillator2 (25 MHz) has an additional function of 100 ns delayed startup, which can be enabled/disabled by register [713]. This function is recommended to use when analog blocks are used along with the Oscillator.

The Matrix Power-down/Force On function allows switching off or force on the oscillator using an external pin. The Matrix Power-down/Force On (Connection Matrix Output [91], [92], [93]) signal has the highest priority. The OSC operates according to the Table 59

It is highly recommended to force the bandgap on when OSC1 or OSC2 are used in the project.

Table 59: Oscillator Operation Mode Configuration Settings

POR	External Clock Selection	Signal From Connection Matrix	Register: Power-Down or Force On by Matrix Input	Register: Auto Power-On or Force On	OSC Enable Signal from CNT/DLY Macrocells	OSC Operation Mode
0	X	X	X	X	X	OFF
1	1	X	X	X	X	Internal OSC is OFF, logic is ON
1	0	1	0	X	X	OFF
1	0	1	1	X	X	ON
1	0	0	X	1	X	ON
1	0	0	X	0	CNT/DLY requires OSC	ON
1	0	0	X	0	CNT/DLY does not require OSC	OFF
Note 1 The OSC will run only when any macrocell that uses OSC is powered on.						

16.2 OSCILLATOR0 (2.048 KHZ)

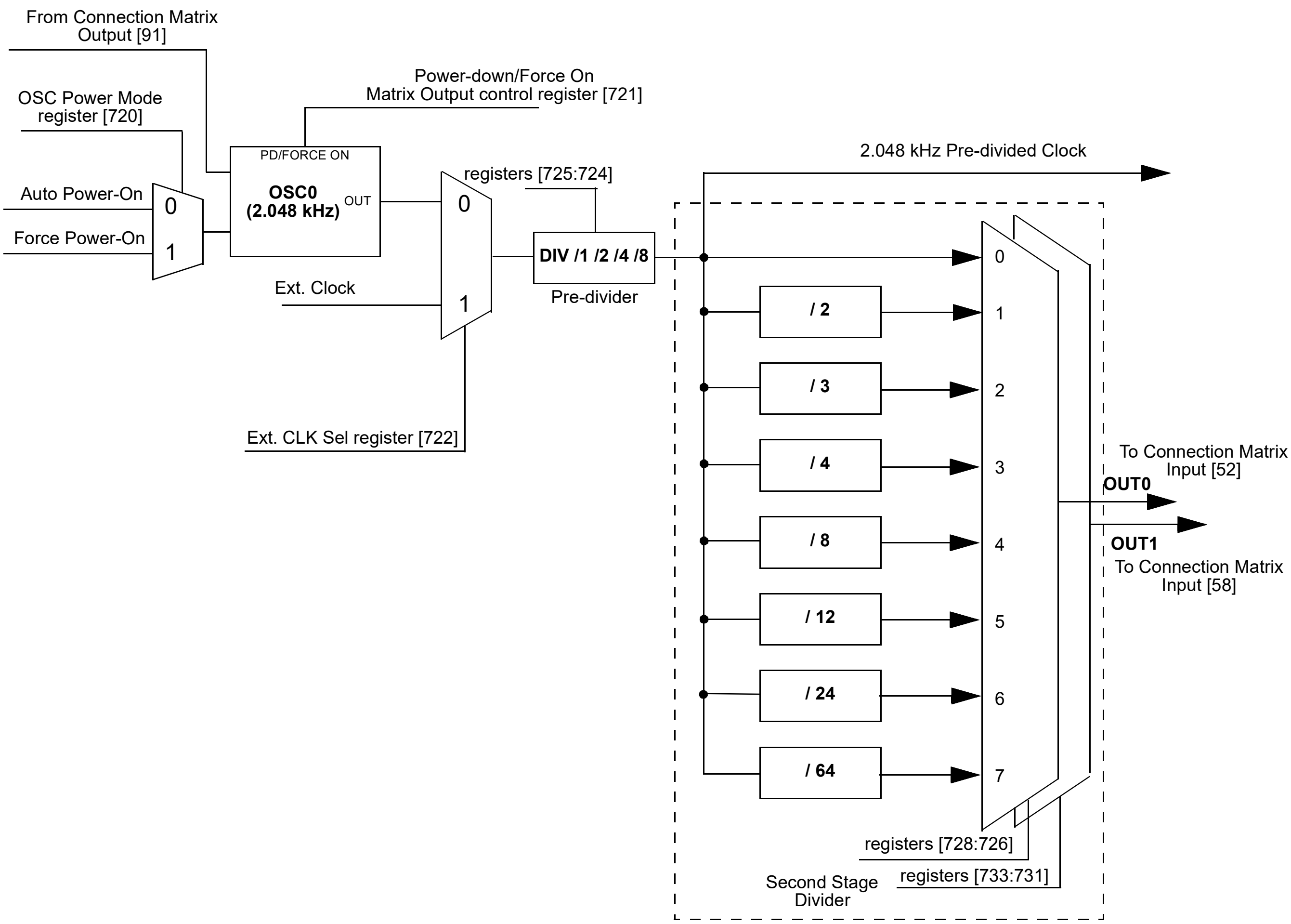


Figure 210: Oscillator0 Block Diagram

16.3 OSCILLATOR1 (2.048 MHZ)

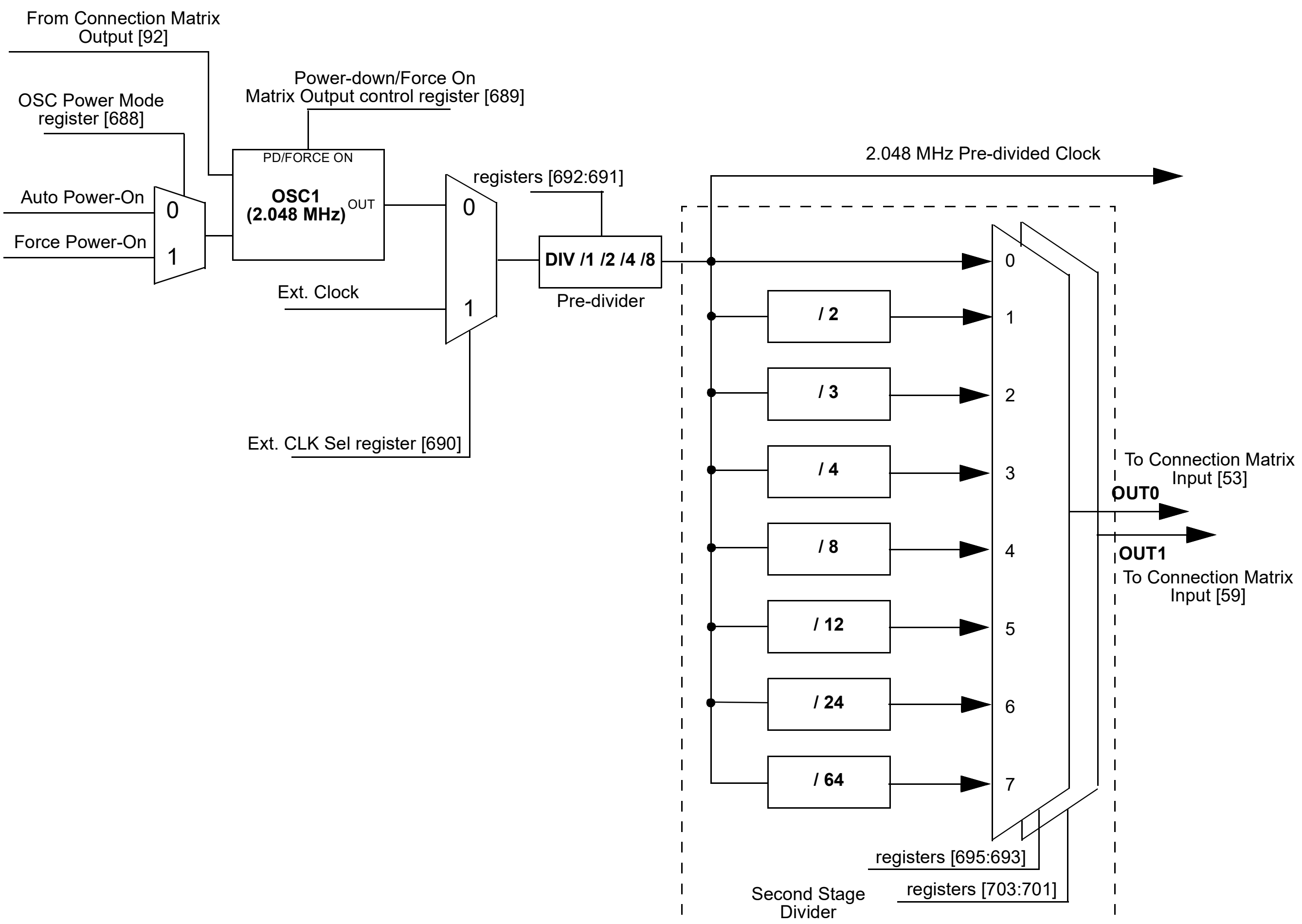


Figure 211: Oscillator1 Block Diagram

16.4 OSCILLATOR2 (25 MHZ)

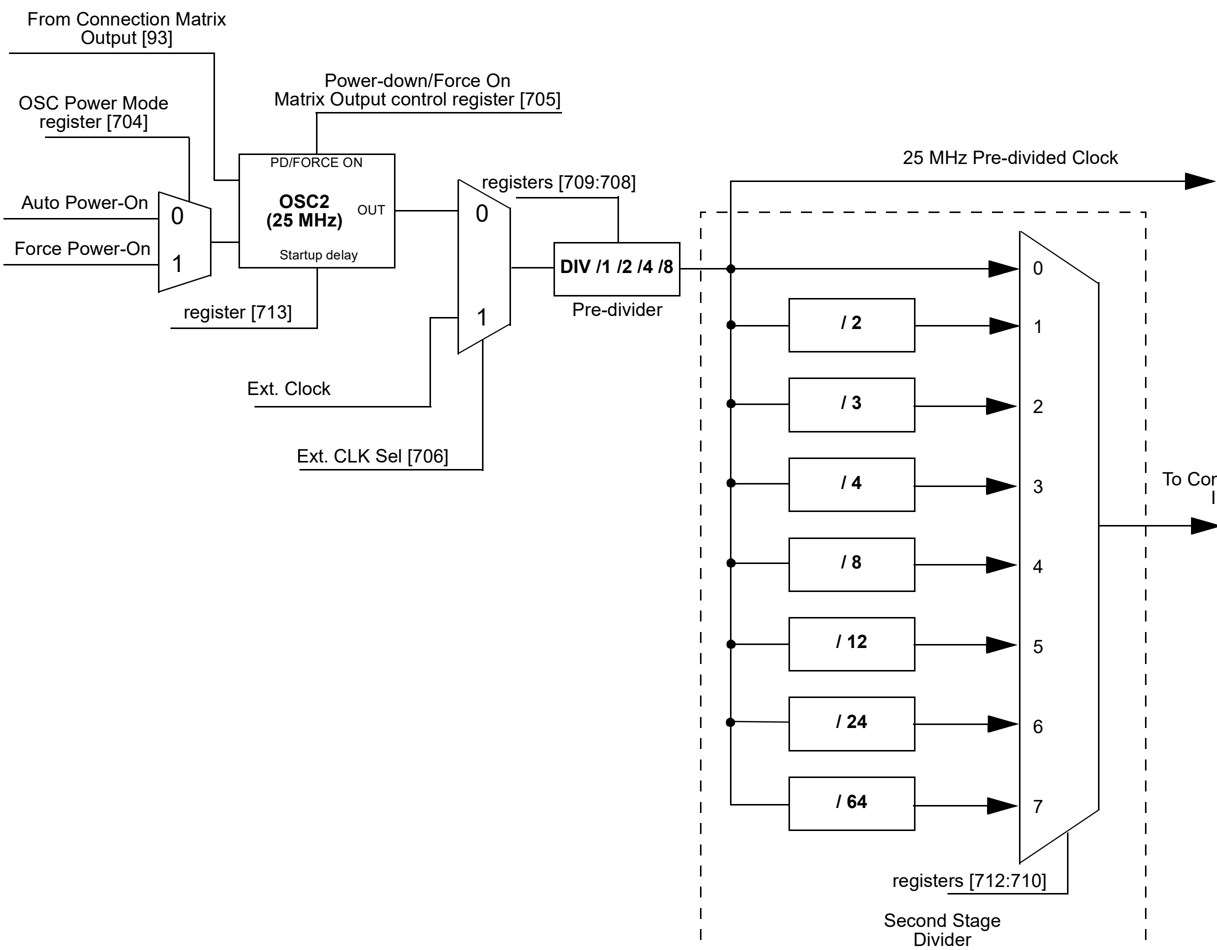


Figure 212: Oscillator2 Block Diagram

16.5 CNT/DLY CLOCK SCHEME

Each CNT/DLY within Multi-Function macrocell has its own additional clock divider connected to oscillators pre-divider. Available dividers are:

- OSC0/1, OSC0/8, OSC0/64, OSC0/512, OSC0/4096, OSC0/32768, OSC0/262144
- OSC1/1, OSC1/8, OSC1/64, OSC1/512
- OSC2/1, OSC2/4

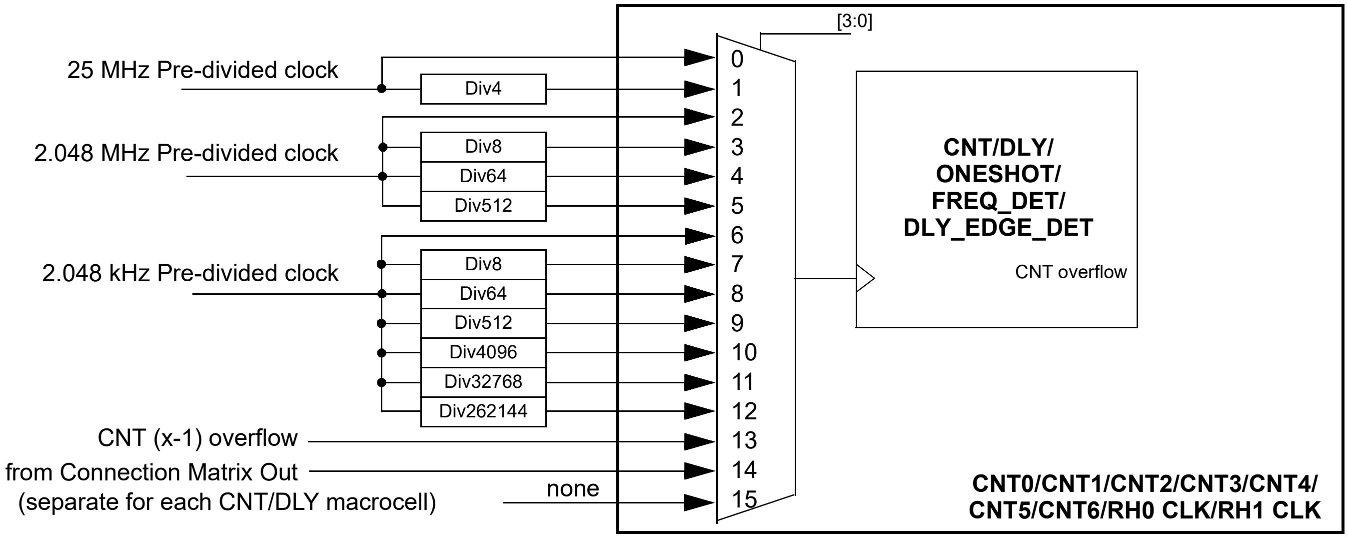


Figure 213: Clock Scheme

16.6 EXTERNAL CLOCKING

The SLG47004 supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

16.6.1 IO10 Source for Oscillator0 (2.048 kHz)

When register [722] is set to 1, an external clocking signal on IO0 will be routed in place of the internal oscillator derived 2.048 kHz clock source. See Figure 210. The high and low limits for frequency that can be selected are 0 MHz and 10 MHz.

16.6.2 IO1 Source for Oscillator1 (2.048 MHz)

When register [690] is set to 1, an external clocking signal on IO1 will be routed in place of the internal oscillator derived 2.048 MHz clock source. See Figure 211. The high and low limits for frequency that can be selected are 0 MHz and 10 MHz.

16.6.3 IO2 Source for Oscillator2 (25 MHz)

When register [706] is set to 1, an external clocking signal on IO2 will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 212. The external frequency range is 0 MHz to 20 MHz at V_{DD} = 2.4 V, 0 MHz to 30 MHz at V_{DD} = 3.3 V, 0 MHz to 50 MHz at V_{DD} = 5.0 V. When an external clock is selected for OSC2, the oscillator's output signal will be inverted with respect to the IO2 input signal.

16.7 OSCILLATORS POWER-ON DELAY

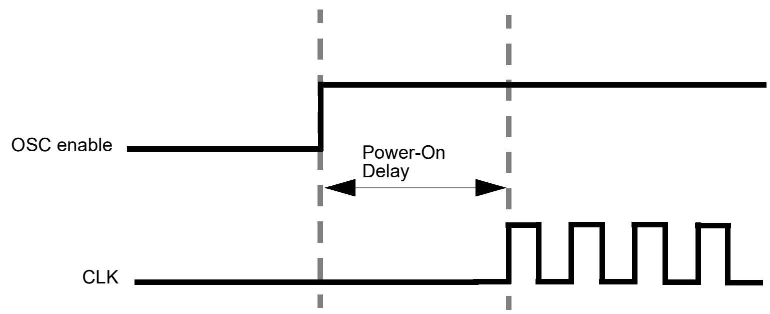


Figure 214: Oscillator Startup Diagram

Note 1 OSC power mode: “Auto Power-On”.

Note 2 “OSC enable” signal appears when any macrocell that uses OSC is powered on

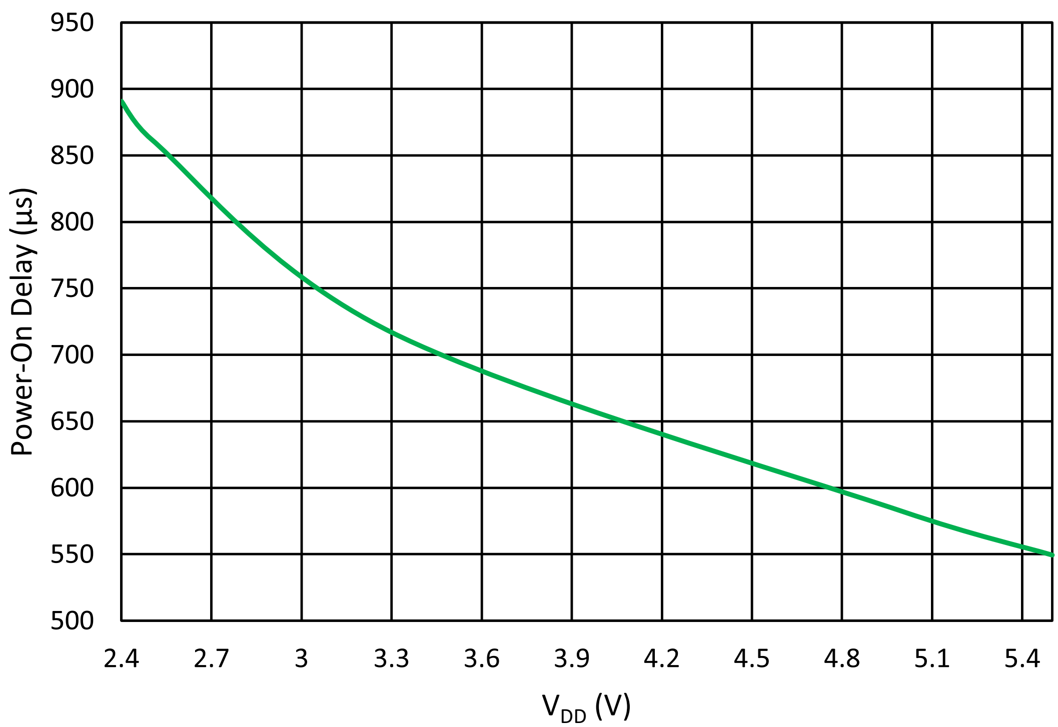


Figure 215: OSC0 Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC0 = 2.048 kHz

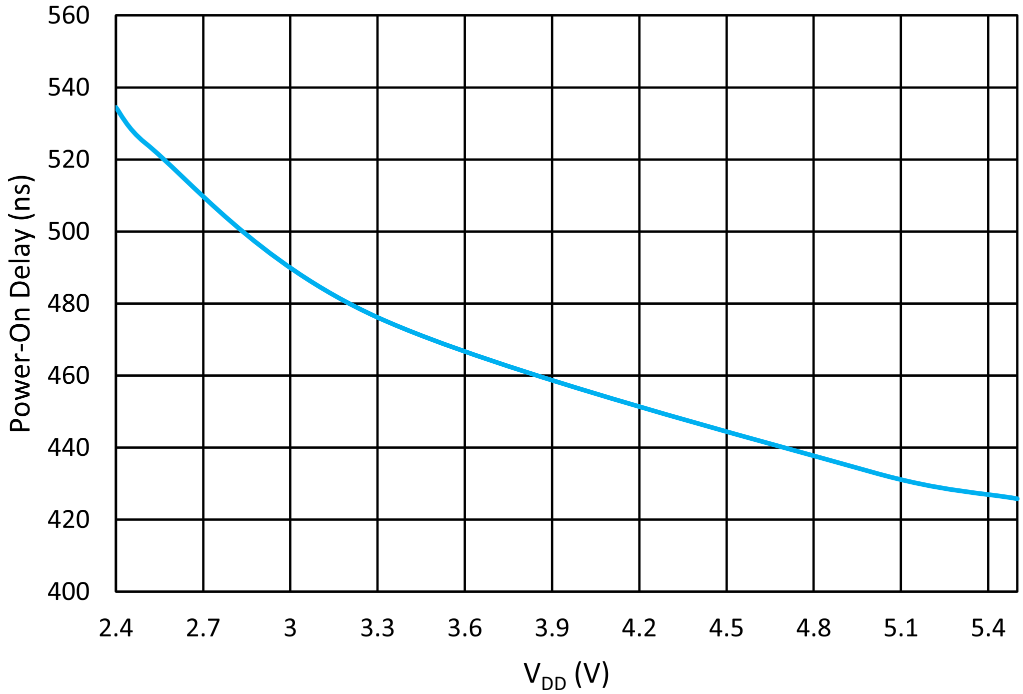


Figure 216: OSC1 Oscillator Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC1 = 2.048 MHz

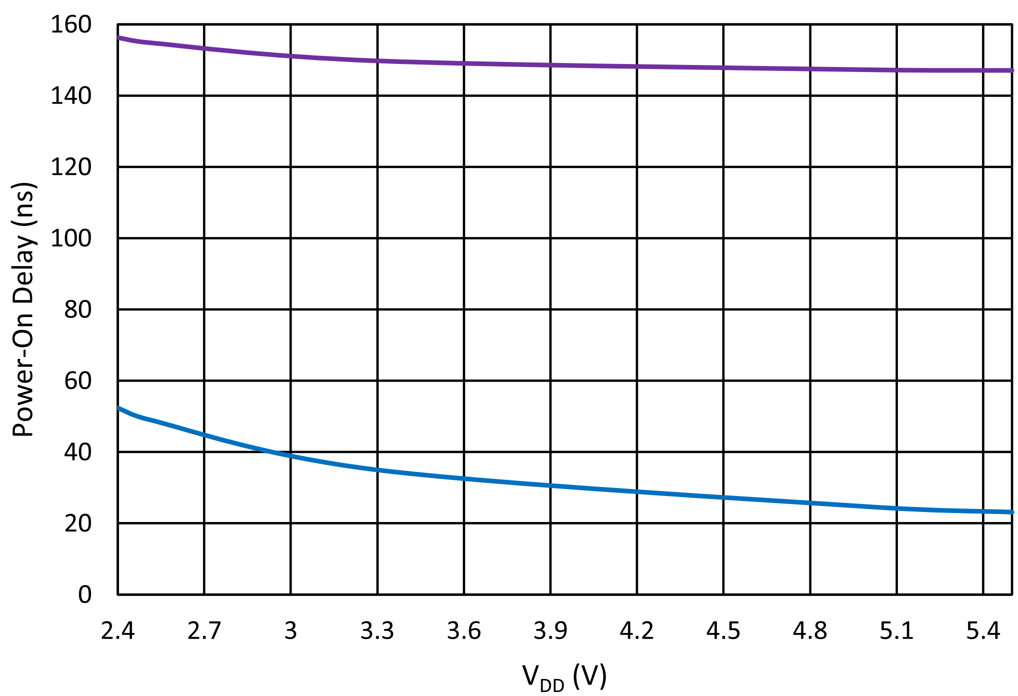


Figure 217: OSC2 Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC2 = 25 MHz

16.8 OSCILLATORS ACCURACY

Note: OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

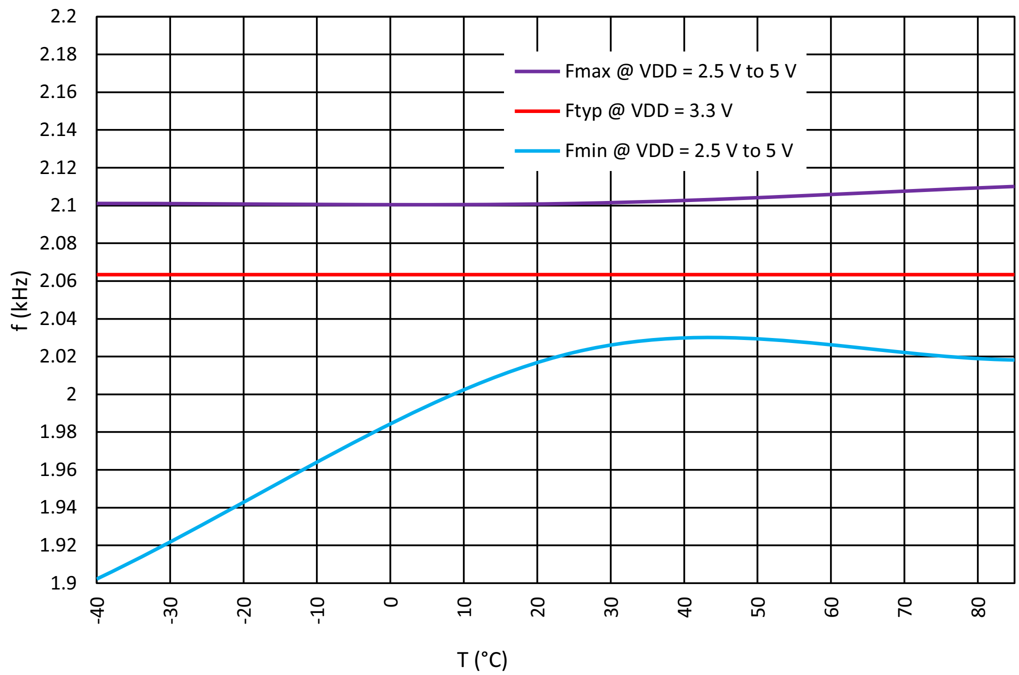


Figure 218: OSC0 Frequency vs. Temperature, OSC0 = 2.048 kHz

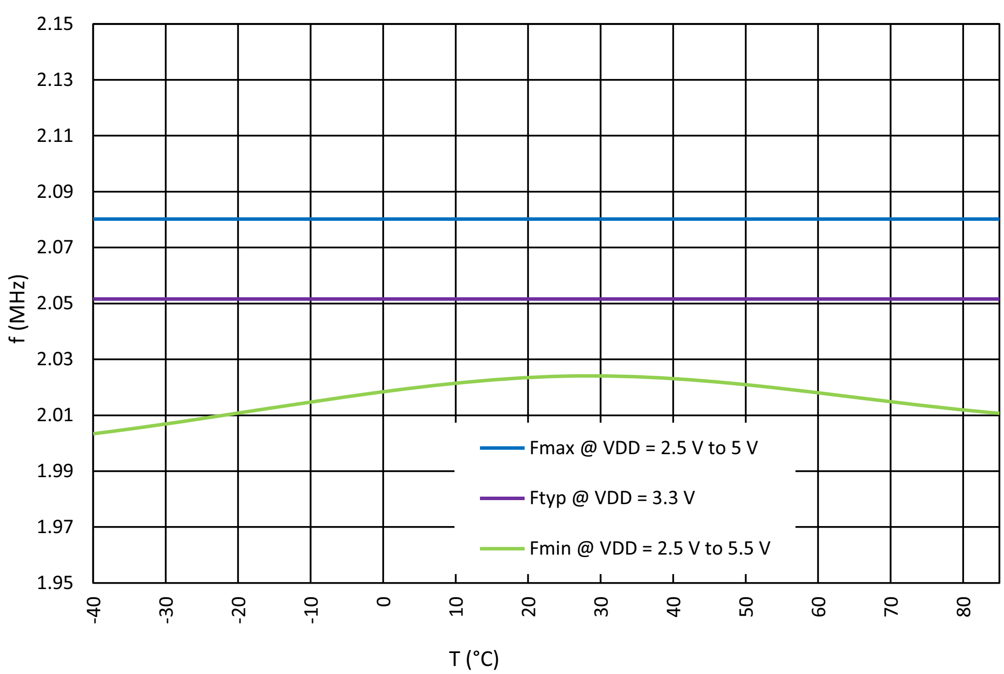


Figure 219: OSC1 Frequency vs. Temperature, OSC1 = 2.048 MHz

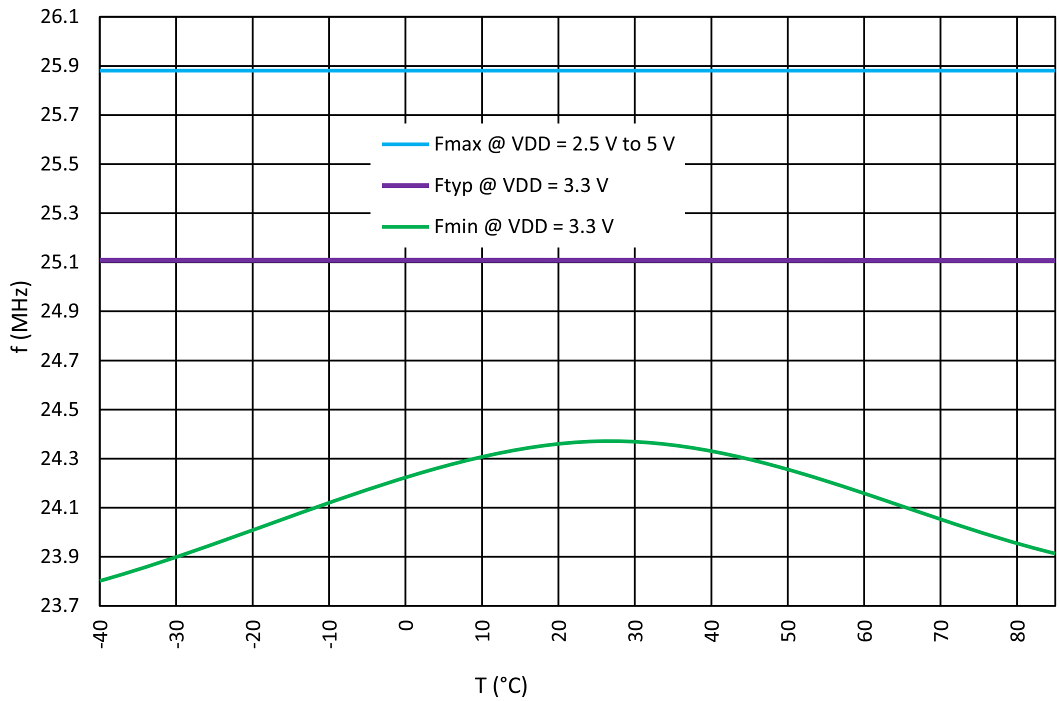


Figure 220: OSC2 Frequency vs. Temperature, OSC2 = 25 MHz

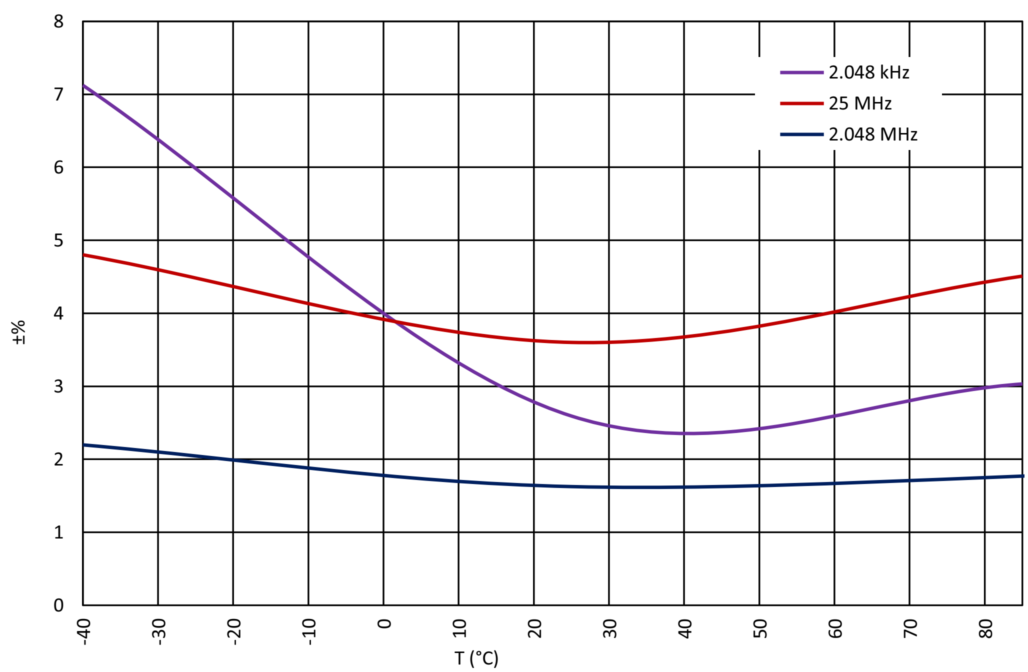


Figure 221: Oscillators Total Error vs. Temperature at V_{DD} = 2.4 V to 5.5 V

Note: For more information see Section 3.8.

16.9 OSCILLATORS SETTLING TIME

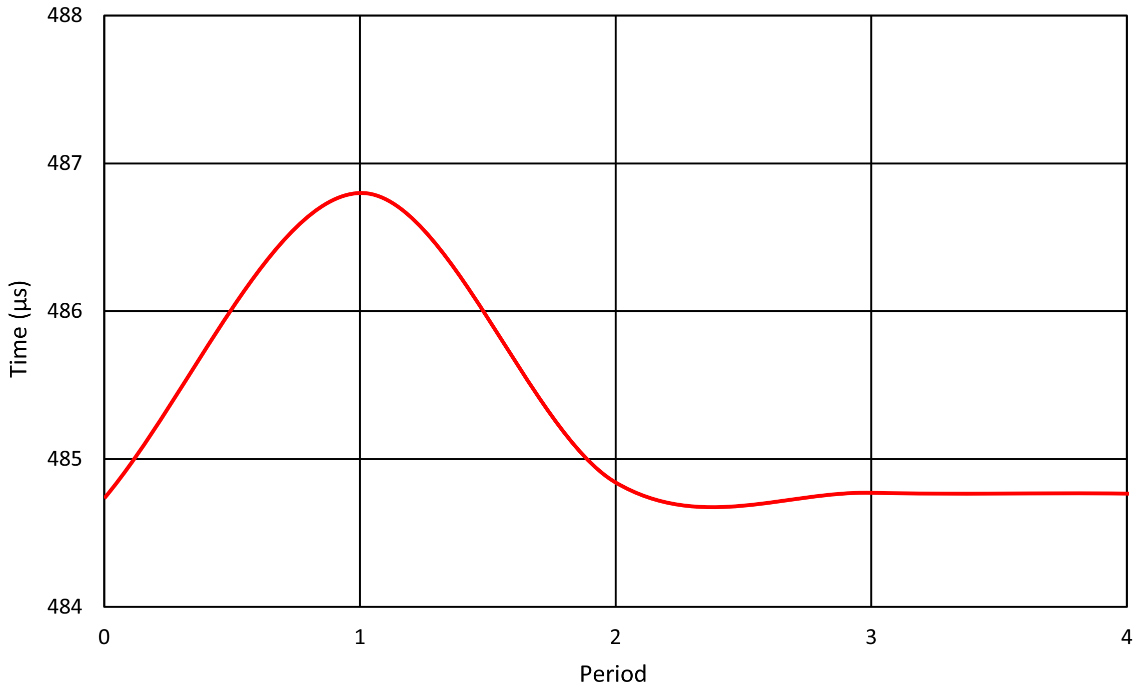


Figure 222: Oscillator0 Settling Time, V_{DD} = 3.3 V, T = 25 °C, OSC0 = 2 kHz

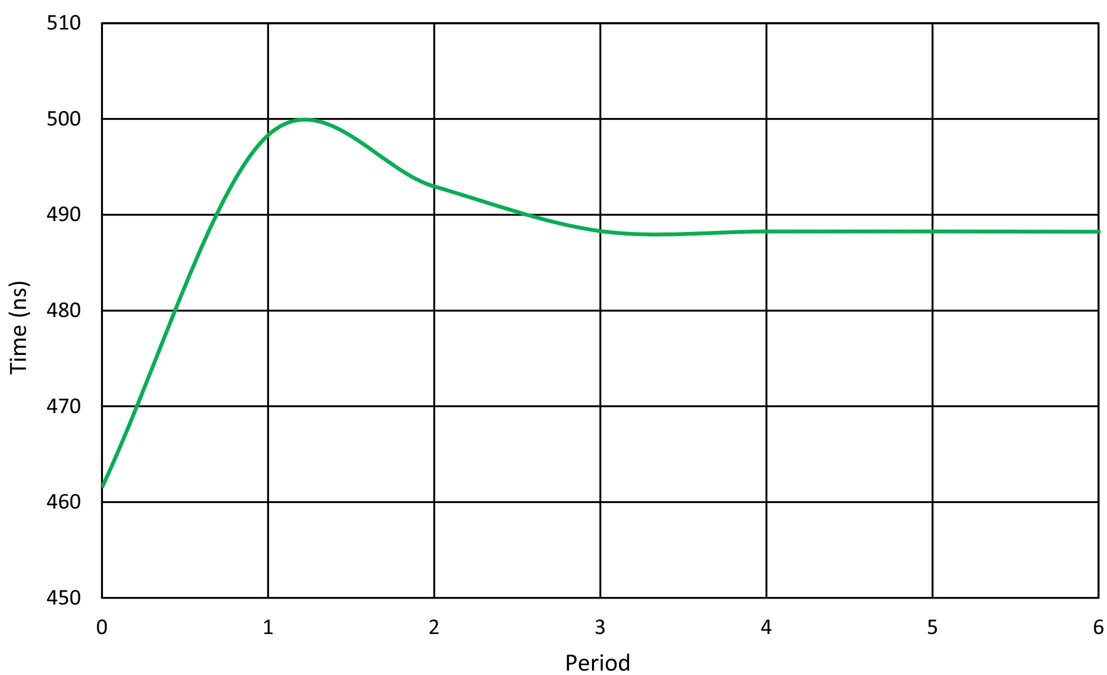


Figure 223: Oscillator1 Settling Time, V_{DD} = 3.3 V, T = 25 °C, OSC1 = 2 MHz

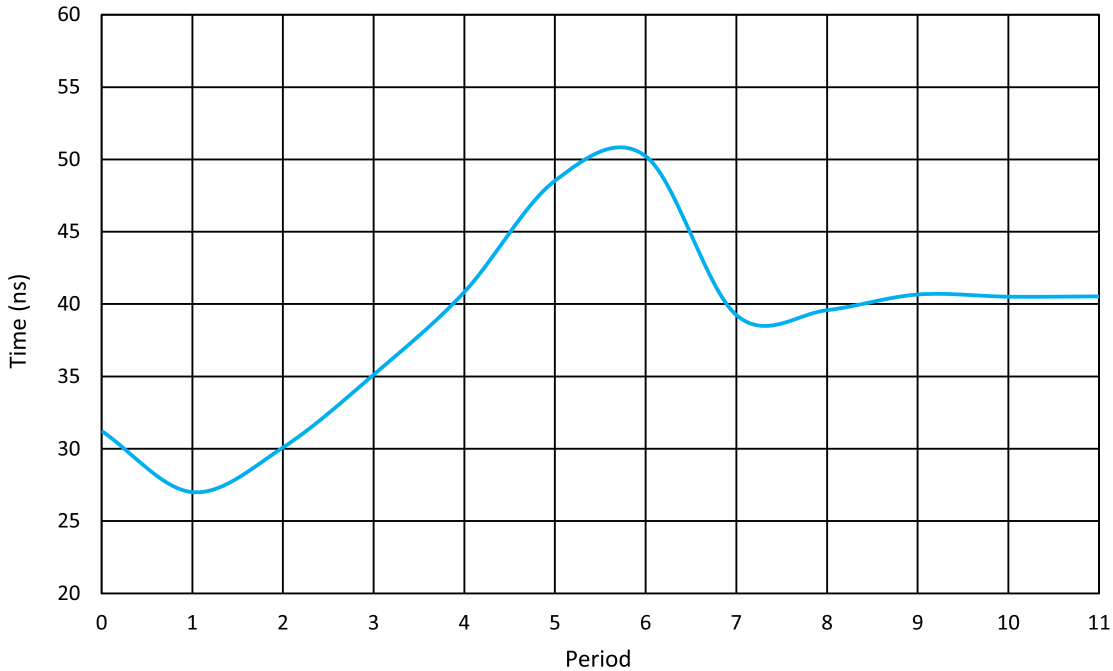


Figure 224: Oscillator2 Settling Time, V_{DD} = 3.3 V, T = 25 °C, OSC2 = 25 MHz (Normal Start)

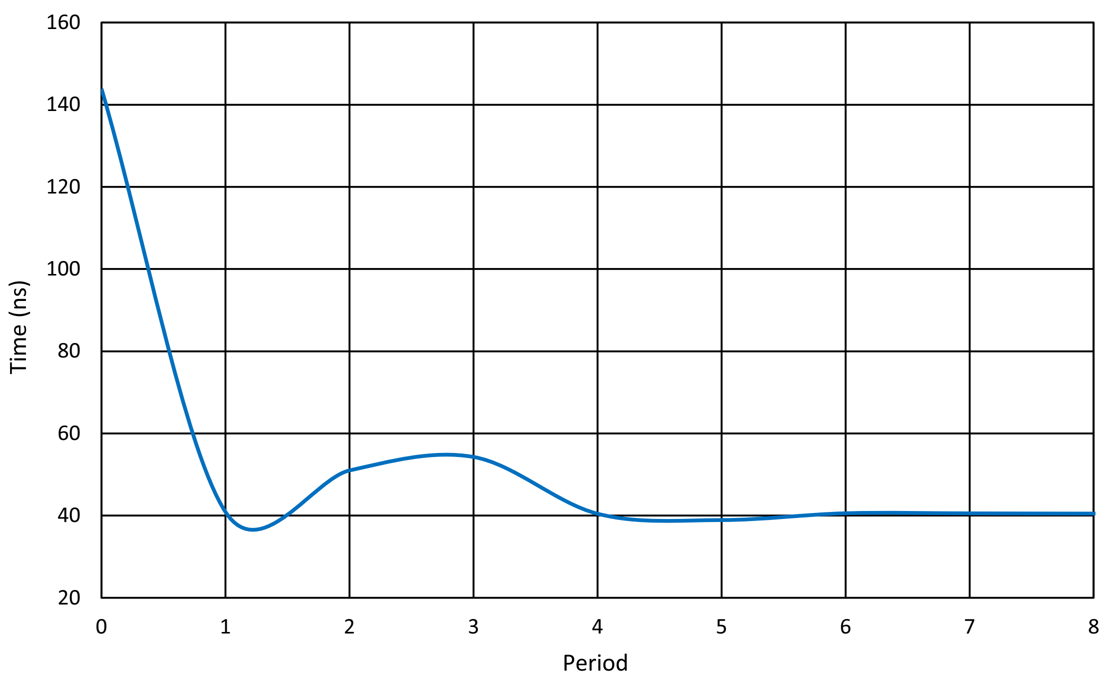


Figure 225: Oscillator2 Settling Time, V_{DD} = 3.3 V, T = 25 °C, OSC2 = 25 MHz (Start with Delay)

16.10 OSCILLATORS CURRENT CONSUMPTION

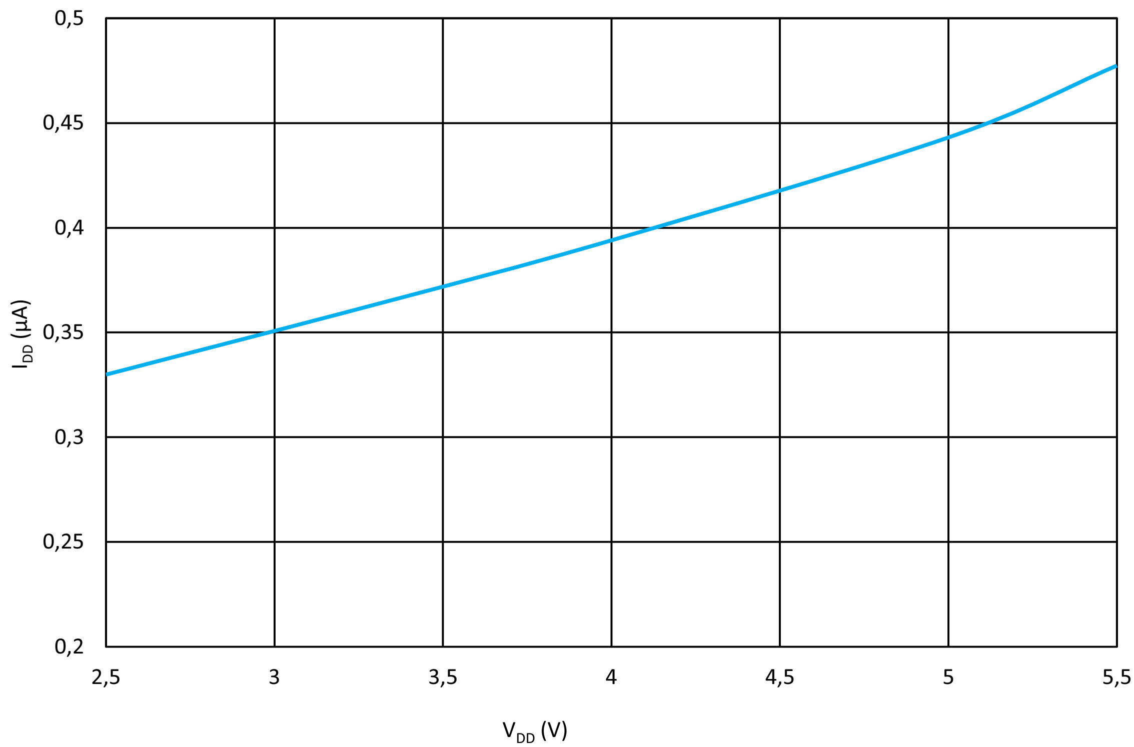


Figure 226: OSC0 Current Consumption vs. V_{DD} at T = -40 °C to +85 °C (All Pre-Dividers)

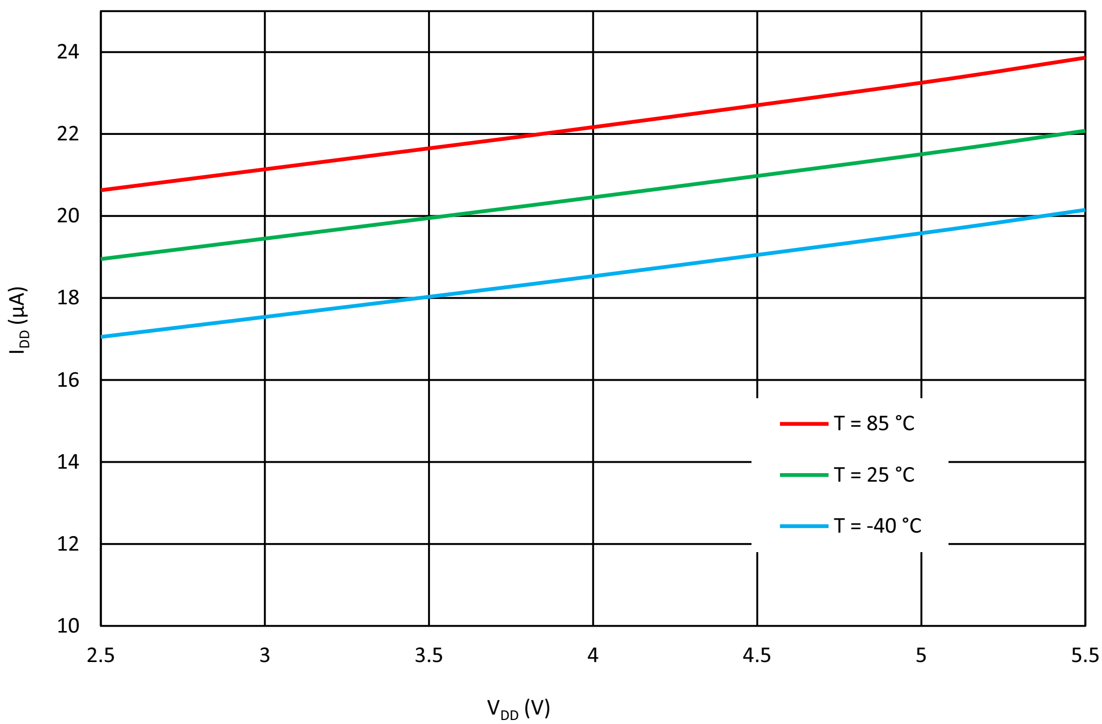


Figure 227: OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 1)

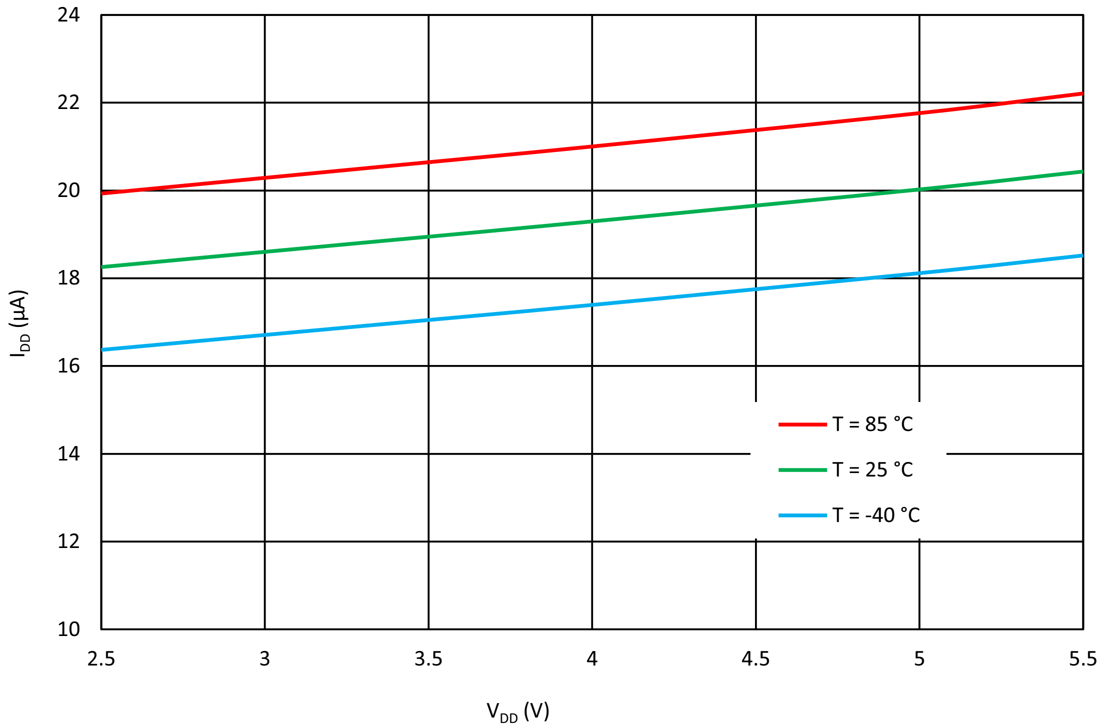


Figure 228: OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 4)

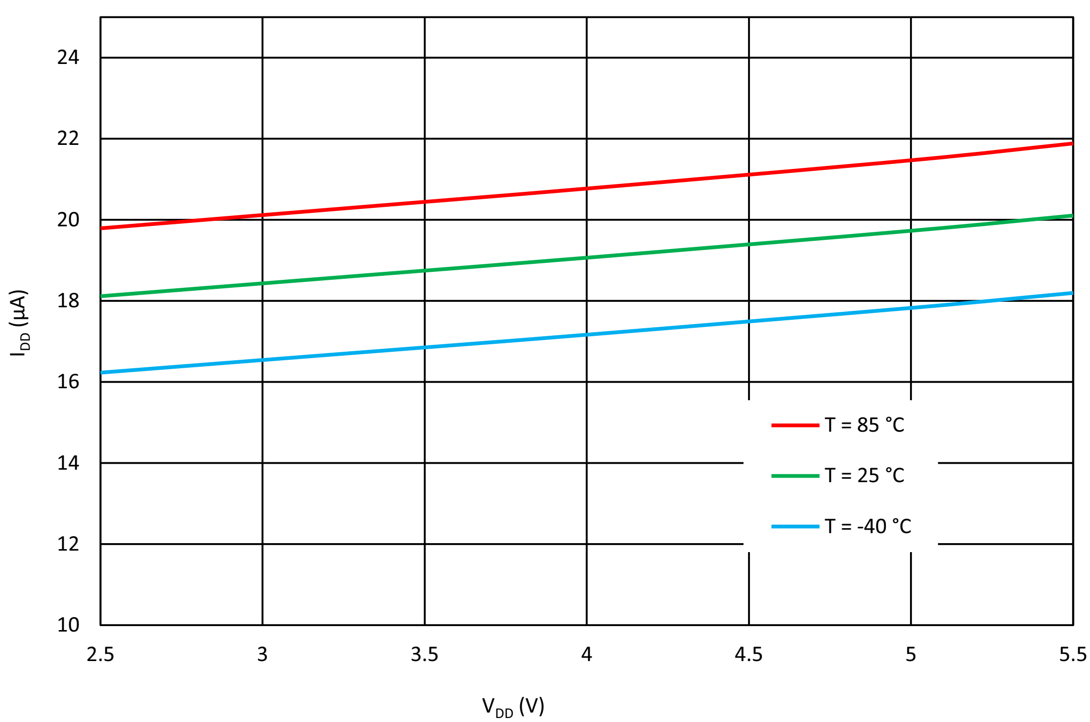


Figure 229: OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 8)

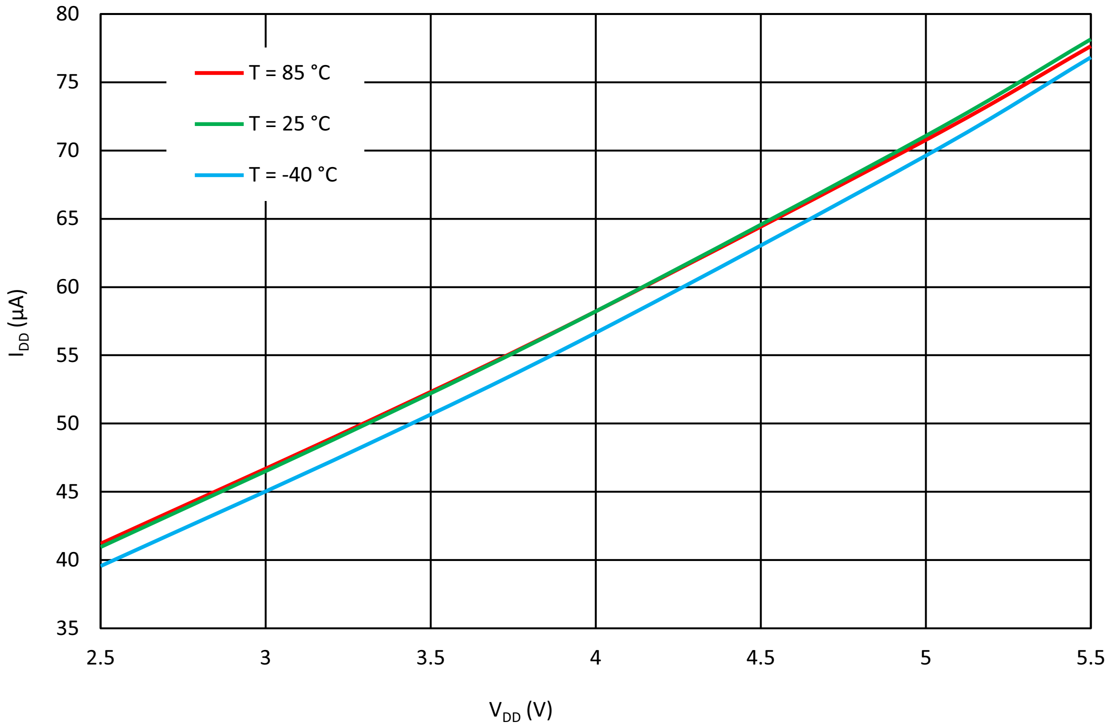


Figure 230: OSC2 Current Consumption vs. V_{DD} (Pre-Divider = 1)

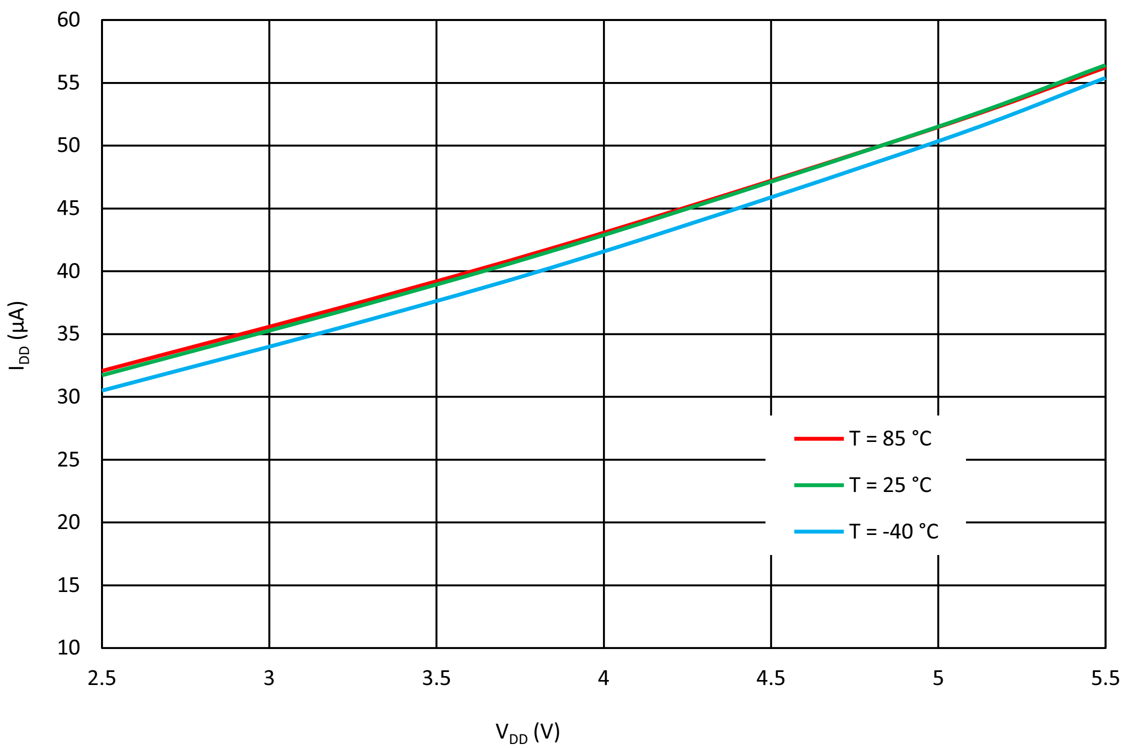


Figure 231: OSC2 Current Consumption vs. V_{DD} (Pre-Divider = 4)

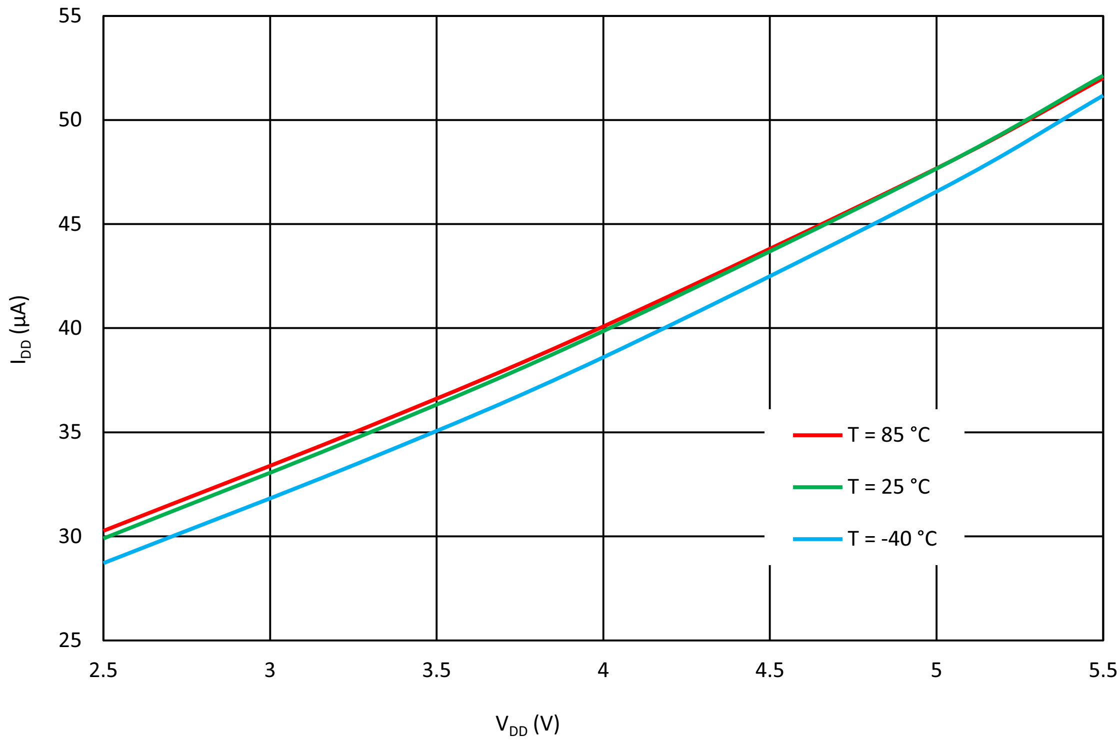


Figure 232: OSC2 Current Consumption vs. V_{DD} (Pre-Divider = 8)

17 Power-On Reset

The SLG47004 has a Power-On Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during Power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IOs.

17.1 GENERAL OPERATION

The SLG47004 is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on PIN13) is less than Power-Off Threshold (see in Table 6), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (Note) than the V_{DD} voltage is applied to any other PIN. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG47004, the voltage applied on the V_{DD} should be higher than the Power-On Threshold (Note). The full operational V_{DD} range for the SLG47004 is 2.4 V to 5.5 V. This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-On Threshold. After the POR sequence has started, the SLG47004 will have a typical Startup Time (see in Table 6) to go through all the steps in the sequence, and will be ready and completely operational after the POR sequence is complete.

Note: The Power-On Threshold is defined in Table 6.

To power down the chip, the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down, it should be less than Power-Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before, the voltage on PINs can't be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

17.2 POR SEQUENCE

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 233.

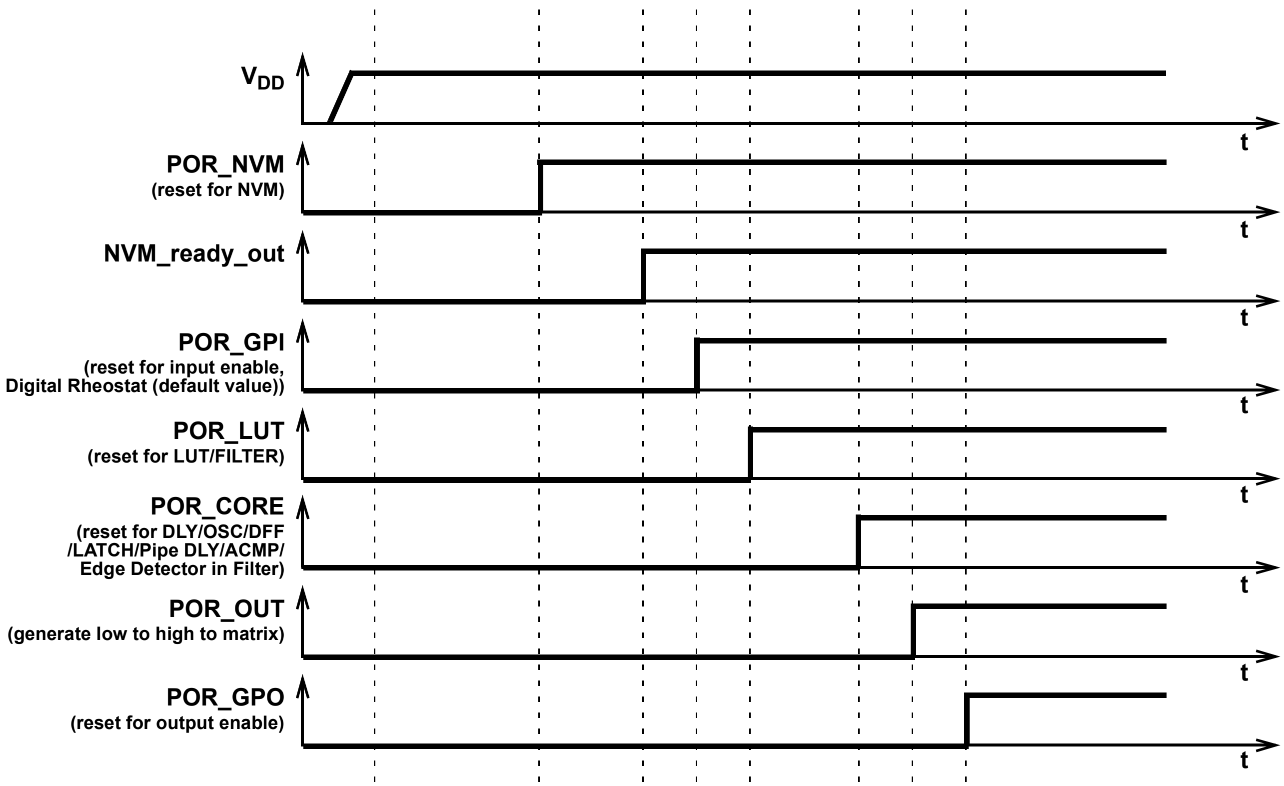


Figure 233: POR Sequence

As can be seen from Figure 233 after the V_{DD} has started ramping up and crossed the Power-On Threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM and transfers this information to a CMOS LATCH, that serves to configure each macrocell, and the Connection Matrix, which routes signals between macrocells. The third stage causes the reset of the input pins, and then enables them. At that time Digital Rheostats value is set to its default value. After that, the LUTs are reset and become active. After LUTs, the Delay cells, OSCs, DFFs, LATCHES, and Pipe Delay are initialized. Only after all macrocells are initialized, internal POR signal (POR macrocell output) goes from LOW to HIGH (POR_OUT in Figure 233). The last portion of the device to be initialized is the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature, and even will vary from chip to chip (process influence).

17.3 MACROCELLS OUTPUT STATES DURING POR SEQUENCE

To have a full picture of SLG47004 operation during powering and POR sequence refer to Figure 234, which describes the macrocell output states during the POR sequence.

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in high impedance state). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; Digital Rheostats value is set to its default value; LUTs also output LOW. After that input pins are enabled. Next, only LUTs are configured. Then, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output pins that become active and determined by the input signals.

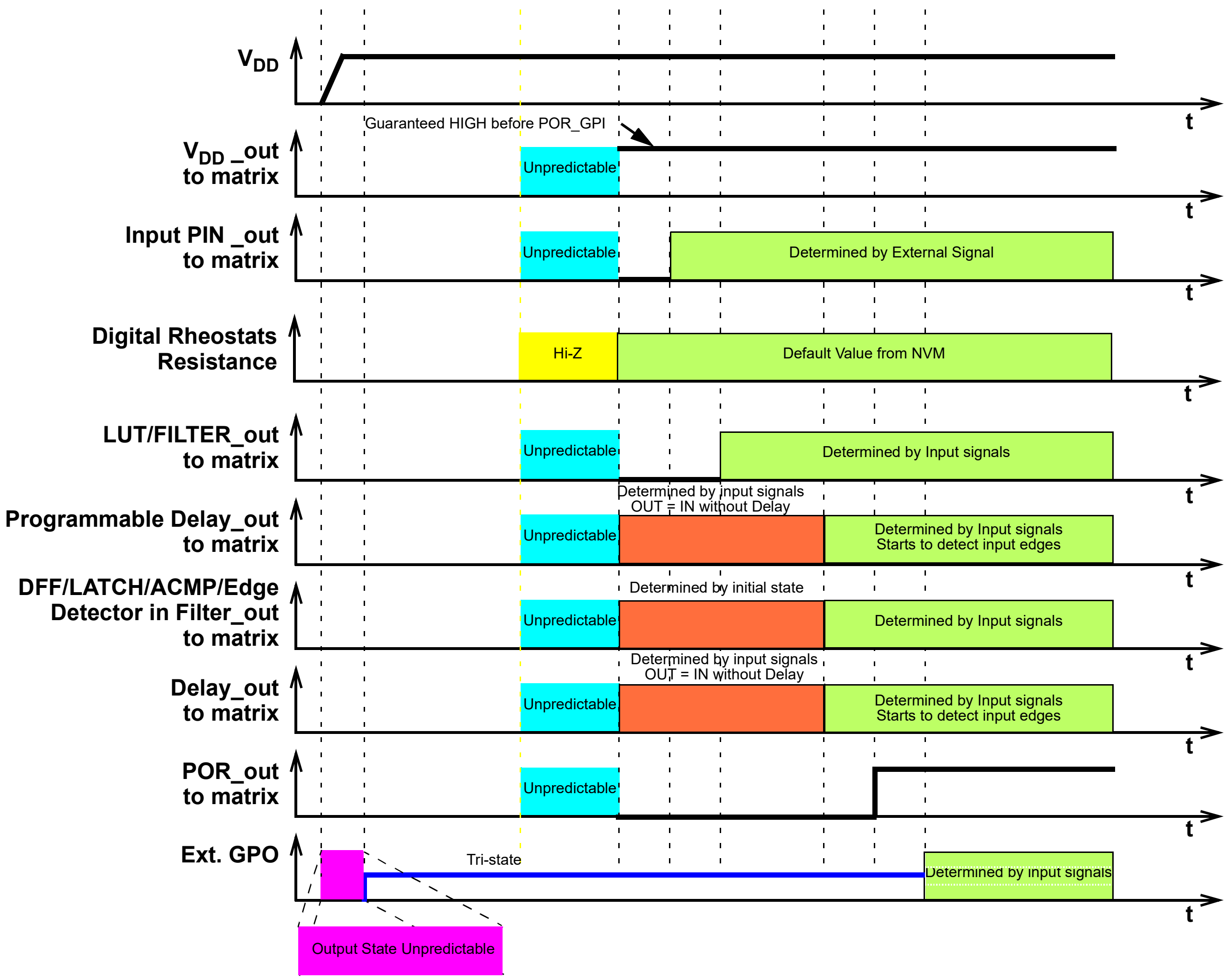


Figure 234: Internal Macrocell States During POR Sequence

17.3.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated power-up time of 1.63 V to 2.04 V, macrocells in SLG47004 are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input pins, Pull-up/down, Digital Rheostats, Op Amps.
2. LUTs.
3. DFFs, Delays/Counters, Pipe Delay, OSCs, ACMPs.
4. POR output to matrix.
5. Output pin corresponds to the internal logic.

The Vref output pin driving signal can precede POR output signal going high by 3 µs to 5 µs. The POR signal going high indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any pin should not be higher than the V_{DD} level. There are ESD Diodes between pin →

V_{DD} and pin → GND on each pin. Exceeding V_{DD} results in leakage current on the input pin, and V_{DD} will be pulled up, following the voltage on the input pin.

17.3.2 Power-Down

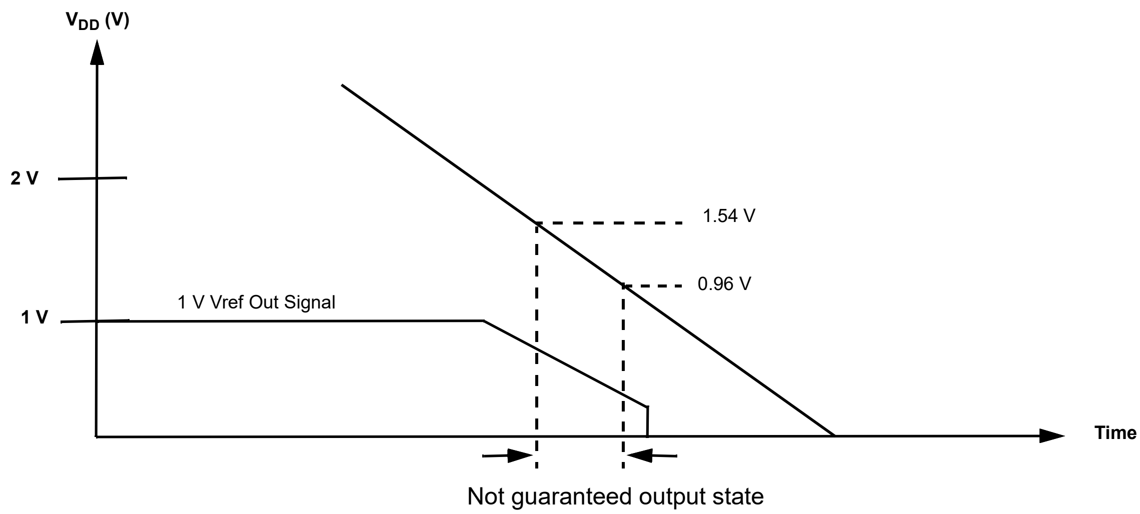


Figure 235: Power-Down

During Power-down macrocells in SLG47004 are powered off after V_{DD} falling down below Power-Off Threshold. Please note, that during a slow rampdown outputs can possibly switch state.

18 I²C Serial Communications Macrocell

18.1 I²C SERIAL COMMUNICATIONS MACROCELL OVERVIEW

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

The I²C bus Master is also able to read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving the I²C bus Master the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits registers [1795:1792]. See Section 19 for more details on I²C read/write memory protection.

18.2 I²C SERIAL COMMUNICATIONS DEVICE ADDRESSING

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 236. After the Start bit, the first four bits are a control code. Each bit in a control code can be sourced independently from the register or by value defined externally by IO1, IO2, IO3, and IO4. The LSB of the control code is defined by the value of IO1, while the MSB is defined by the value of IO4. The address source (either register bit or PIN) for each bit in the control code is defined by registers [1019:1016]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus.The default control code is 0001. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either "1111" or "0000" in a system with other slave device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to ensure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. The valid addresses are shown in the memory map in Figure 246.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address.

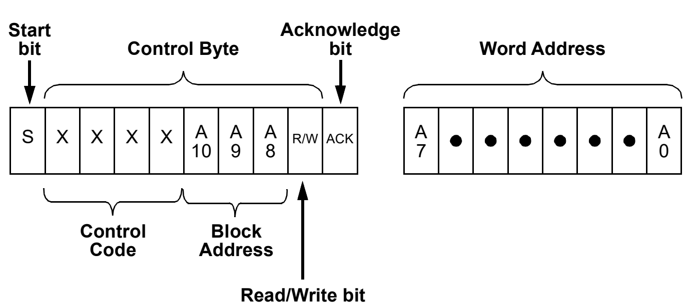


Figure 236: Basic Command Structure

18.3 I²C SERIAL GENERAL TIMING

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 237. Timing specifications can be found in the AC Characteristics, section 3.4.

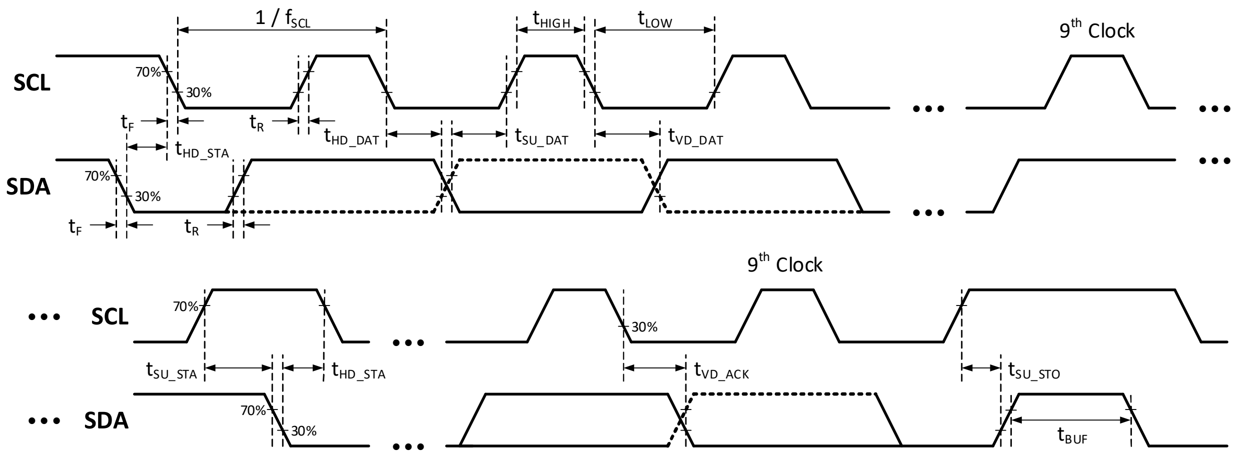


Figure 237: I²C General Timing Characteristics

18.4 I²C SERIAL COMMUNICATIONS COMMANDS

18.4.1 Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits], and the R/W bit (set to "0") are placed onto the I²C bus by the Master. After the SLG47004 sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG47004, where the data byte is to be written. After the SLG47004 sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG47004 again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG47004 generates the Acknowledge bit.

It is possible to latch all IOs during I²C write command to the register configuration data (block address A10, A9, A8 = 000), register [985] = 1 - Enable. It means that IOs will remain their state until the write command is done.

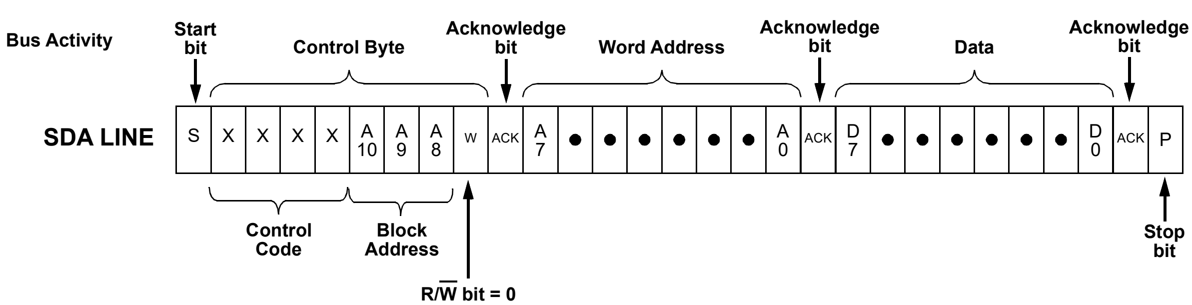


Figure 238: Byte Write Command, R/W = 0

18.4.2 Sequential Write Command

The write Control Byte, Word Address, and the first data byte are transmitted to the SLG47004 in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Bus Master continues to transmit data bytes to the SLG47004. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG47004 generates the Acknowledge bit.

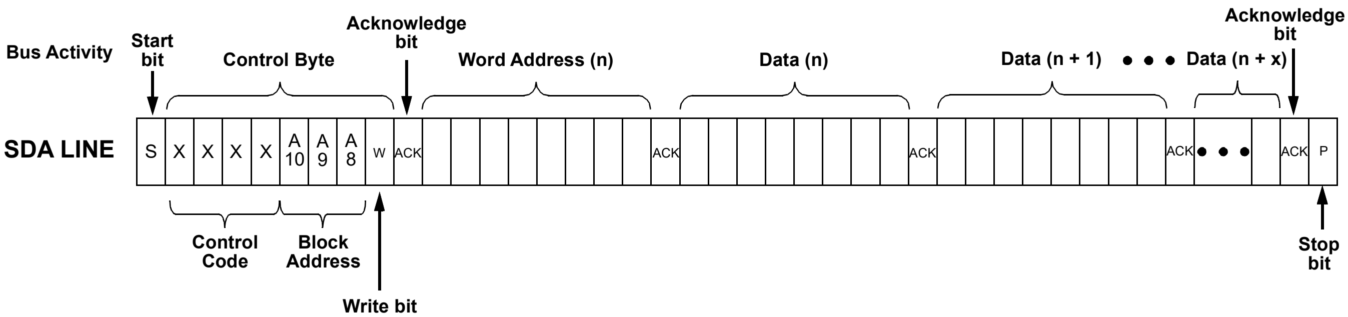


Figure 239: Sequential Write Command

18.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Sequential Read command (which contains a write control byte) reads data up to address n, the address pointer would get incremented to n + 1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n + 1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/$\overline{W}$ bit = “1”. The SLG47004 will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit, and follow immediately with a Stop condition

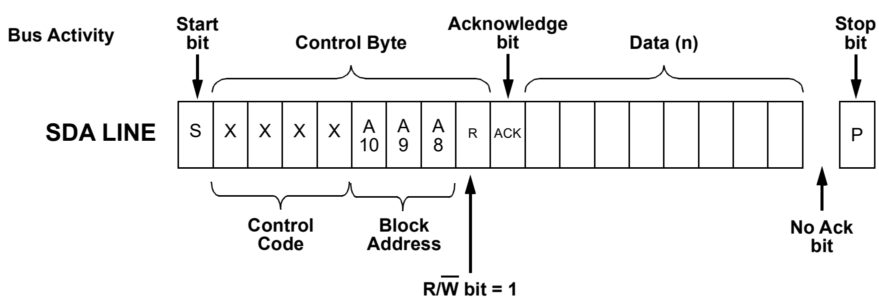


Figure 240: Current Address Read Command, R/$\overline{W}$ = 1

18.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/W bit set to “1”, after which the SLG47004 issues an Acknowledge bit followed by the requested eight data bits.

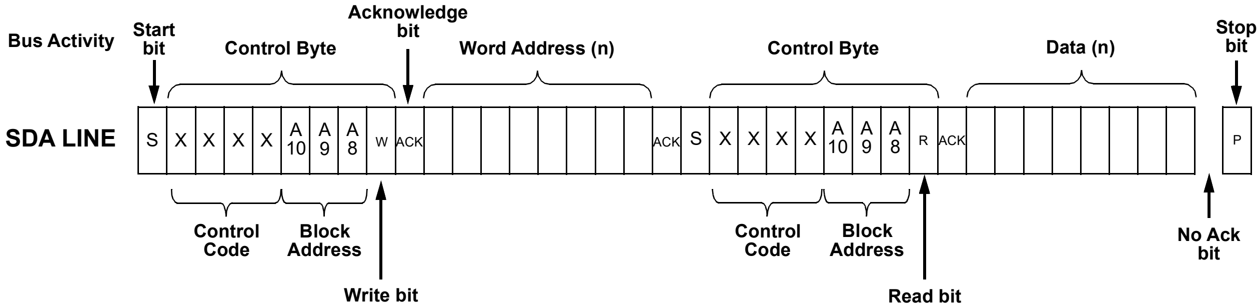


Figure 241: Random Read Command

18.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Random Read command, except that once the SLG47004 transmits the first data byte, the Bus Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Bus Master can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

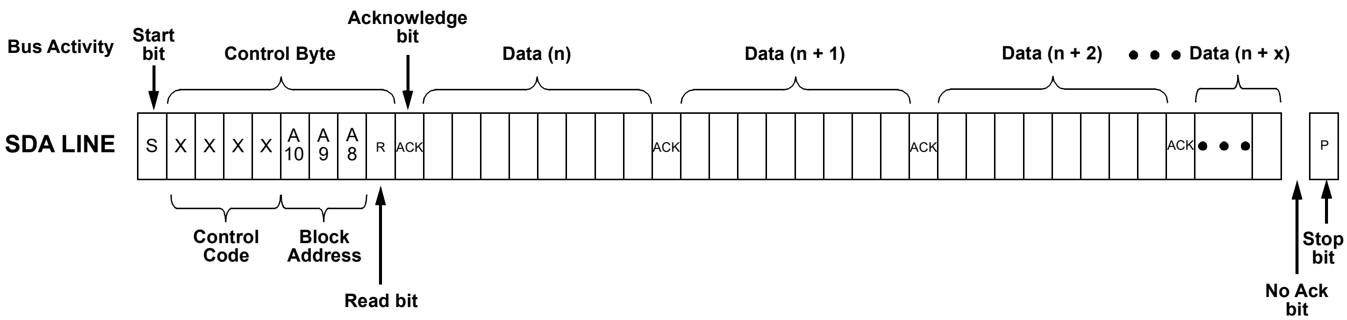


Figure 242: Sequential Read Command

18.4.6 I^{2}C Serial Reset Command

If I^{2}C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells and all connections provided by the Connection Matrix. This is implemented by setting register [984] I^{2}C reset bit to “1”, which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [984] will be set to “0” automatically. The Figure 243 illustrates the sequence of events for this reset function.

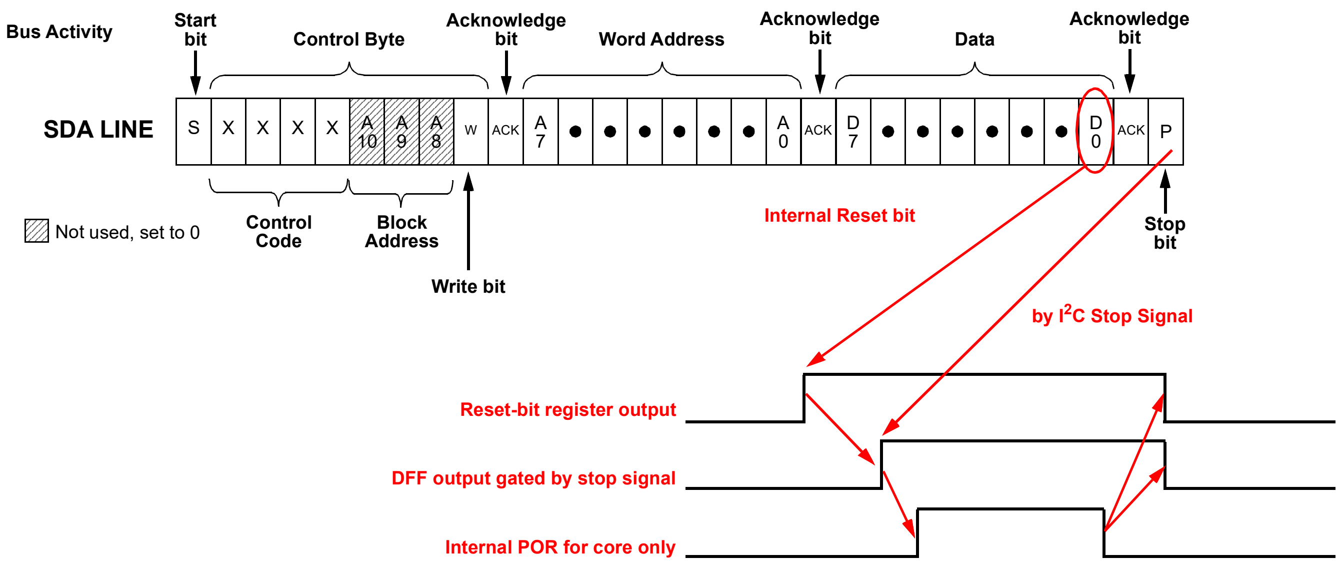


Figure 243: Reset Command Timing

18.5 CHIP CONFIGURATION DATA PROTECTION

The SLG47004 utilizes a scheme that allows a portion or the entire Register and NVM to be inhibited from being read or written/erased. There are two bytes that define the register and NVM access or change. The second byte NPR defines the chip NVM data configuration read and write protection. The first byte RPR defines the register read and write protection. If desired, the protection lock bit (PRL) can be set so that protection may no longer be modified, thereby making the current protection scheme permanent. The status of the RPR and NPR can be determined by following a Random Read sequence. Changing the state of the RPR and NPR is accomplished with a Byte Write sequence with the requirements outlined in this section.

Special care must be taken when NVM page 14 is rewritten (registers [1919:1792]). This page contains rheostats tolerance data that can be permanently lost during write/erase operation.

The RPR register is located on H’E0 address, while NPR is located on H’E1 address.

The RPR format is shown in Table 60, and the RPR bit functions are included in Table 61.

Table 60: RPR Format

	b7	b6	b5	b4	b3	b2	b1	b0
RPR				RH_PRB	RPRB3	RPRB2	RPRB1	RPRB0

* Becomes read only after PRL is high. The content is permanently locked for write and erase after PRL is high.

Table 61: RPR Bit Function Description

Bit	Name		Type	Description
4	RH_PRB	--	R/W*	0: Program signal from connection matrix is enabled 1: Program signal from connection matrix is disabled
3:2	RPRB3	2k Register Write Selection Bits	R/W*	00: 2k register data is unprotected for write; 01: 2k register data is partly protected for write; Please refer to the Table 64. 10: 2k register data is fully protected for write.
	RPRB2		R/W*	

Table 61: RPR Bit Function Description(Continued)

Bit	Name		Type	Description
1:0	RPRB1	2k Register Read Selection Bits	R/W*	00: 2k register data is unprotected for read; 01: 2k register data is partly protected for read; Please refer to the Table 64. 10: 2k register data is fully protected for read.
	RPRB0		R/W*	

The NPR format is shown in Table 62, and the NPR bit functions are included in Table 63.

Table 62: NPR Format

	b7	b6	b5	b4	b3	b2	b1	b0
NPR							NPRB1	NPRB0

Table 63: NPR Bit Function Description

Bit	Name		Type	Description
1:0	NPRB1	2k NVM Configuration Selection Bits	R/W*	00: 2k NVM Configuration data is unprotected for read and write/erase; 01: 2k NVM Configuration data is fully protected for read; 10: 2k NVM Configuration data is fully protected for write/erase; 11: 2k NVM Configuration data is fully protected for read and write/erase.
	NPRB0		R/W*	

* Becomes read only after PRL is high. The content is permanently locked for write and erase after PRL is high.

The protection selection bits allow different levels of protection of the register and NVM Memory Array.

There is a dedicated bit RH_PRB, that enables/disables "Program" signal of PT block to change NVM rheostats resistance values. If RH_PRB [1796] = 0, "Program" signal is enabled. If RH_PRB [1796] = 1, "Program" signal is disabled. Note that RH_PRB bit has no effect on I^{2}C access to NVM. To enable/disable I^{2}C access to rheostat resistance value, stored in NVM, user must change NPRB0, NPRB1 bits.

The Protect Lock Bit (PRL) is used to permanently lock (for write and erase) the current state of the RPR and NPR,as well as EEPROM protection. A Logic 0 indicates that the protection byte can be modified, whereas a Logic 1 indicates the byte has been locked and can no longer be modified.

In this case it is impossible to erase the whole page E with protection bytes. The PRL is located at E4 address (register [1824]).

18.6 I^{2}C SERIAL COMMAND REGISTER MAP

There are nine read/write protect modes for the design sequence from being corrupted or copied. See Table 64 for details.

Table 64: Read/Write Register Protection Options

Configurations	Protection Modes Configuration									Test Mode	Register Address
	Unlock	Partly Lock Read	Partly Lock Write	Partly Lock Read/ Write	Partly Lock Read & Lock Write	Lock Read & Partly Lock Write	Lock Read	Lock Write	Lock Read/ Write		
RPR[1:0]	00	01	00	01	01	10	10	00	10		
RPR[3:2]	00	00	01	01	10	01	00	10	10		
I^{2}C Byte Write Bit Masking (section 18.7.2)	R/W	R/W	R/W	R/W	R	W	W	R	-	-	F6
I^{2}C Serial Reset Command (section 18.4.6)	R/W	R/W	R/W	R/W	R	W	W	R	-	-	7Bb'0

Table 64: Read/Write Register Protection Options(Continued)

Configurations	Protection Modes Configuration									Test Mode	Register Address
	Unlock	Partly Lock Read	Partly Lock Write	Partly Lock Read/ Write	Partly Lock Read & Lock Write	Lock Read & Partly Lock Write	Lock Read	Lock Write	Lock Read/ Write		
RPR[1:0]	**00**	**01**	**00**	**01**	**01**	**10**	**10**	**00**	**10**		
RPR[3:2]	**00**	**00**	**01**	**01**	**10**	**01**	**00**	**10**	**10**		
Outputs Latching During I^{2}C Write (section18.7)	R/W	R/W	R/W	R/W	R	W	W	R	-	-	7Bb'1
Connection Matrix Virtual Inputs (section 6.3)	R/W	R/W	R/W	R/W	R	W	W	R	-	-	7C
RH0_CNT Data	R/W	R/W	R/W	R/W	R	W	W	R	-	R/W	C0,C1
RH1_CNT Data	R/W	R/W	R/W	R/W	R	W	W	R	-	R/W	D0,D1
Macrocells Output Values (Connection Matrix Inputs, section	R	R	R	R	R	-	-	R	-	R	C4~CA
Counter Current Value	R	R	R	R	R	-	-	R	-	R	CB~CE
RH0_CNT Value	R	R	R	R	R	R	R	R	R	R	C2,C3
RH1_CNT Value	R	R	R	R	R	R	R	R	R	R	D2,D3
Protection Mode Selection (sections 18.6, 19.6)	R/W	R/W	R	R	R	R	R/W	R	R7	R	E4'b0
I^{2}C Slave Address	R/W	R/W	R	R	R	R	R/W	R	R	R	7Fb'3~7F b'0
Pin slave address select	R/W	R/W					R/W				7Fb'7~7F b'4
Service page lock	R	R	R	R	R	R	R	R	R	R	F3b'0
RH0 Tolerance Data	R	R	R	R	R	R	R	R	R	R	E6,E7
RH1 Tolerance Data	R	R	R	R	R	R	R	R	R	R	E8,E9
Protect Mode Config (RH_PRB,RPR, NPR,WPR)	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	E0, E1, E2
Page Erase byte	W**	W**	W**	W**	W**	W**	W**	W**	W**	W**	E3
Macrocells Inputs Configuration (Connection Matrix Outputs) (section 6.2)	R/W	W	R	-	-	-	W	R	-	-	00~4A (4B rev)
Configuration Bits for All Macrocells (IOs, ACMPs, Combination Function Macrocells, and others)	R/W	W	R	-	-	-	W	R	-	-	

R/W	Allow Read and Write Data
W	Allow Write Data Only
W**	Pages that can be erased are defined by NVM write protection

R	Allow Read Data Only
-	The Data is protected for Read and Write

Note 1 R/W becomes read only if protection mode selection (lock bit) is set to 1.

Note 2 R/W Readable/writable depend on the "Trim mode enable" bit. If “Trim mode enable” bit value = 1, then trim bits are enable.

It is possible to read some data from macrocells, such as counter current value, connection matrix, and connection matrix virtual inputs. The I^2C write will not have any impact on data in case data comes from macrocell output, except Connection Matrix Virtual Inputs. The silicon identification service bits allow identifying silicon family, its revision, and others.

R/W* - Becomes read only after PRL is high.See Section 21 for detailed information on all registers.

18.7 I^{2}C ADDITIONAL OPTIONS

When Output latching during I^{2}C write to the register configuration data (block address A10, A9, A8 = 000), registers [985] = 1 allows all PINs output value to be latched while register content is changing. It will protect the output change due to configuration process during I^{2}C write in case multiple register bytes are changed. Inputs and internal macrocells retain their status during I^{2}C write.

See Section 21 for detailed information on all registers.

18.7.1 Reading Counter Data via I^{2}C

The current count value in three counters in the device can be read via I^{2}C. The counters that have this additional functionality are 16-bit CNT0, and 8-bit counters CNT2 and CNT4.

18.7.2 I^{2}C Byte Write Bit Masking

The I^{2}C macrocell inside SLG47004 supports masking of individual bits within a byte that is written to the RAM memory space. This function is supported across the entire RAM memory space. To implement this function, the user performs a Byte Write Command (see Section 18.4.1 for details) on the I^{2}C Byte Write Mask Register (address 0F6H) with the desired bit mask pattern. This sets a bit mask pattern for the target memory location that will take effect on the next Byte Write Command to this register byte. Any bit in the mask that is set to "1" in the I^{2}C Byte Write Mask Register will mask the effect of changing that particular bit in the target register, during the next Byte Write Command. The contents of the I^{2}C Byte Write Mask Register are reset (set to 00h) after valid Byte Write Command. If the next command received by the device is not a Byte Write Command, the effect of the bit masking function will be aborted, and the I^{2}C Byte Write Mask Register will be reset with no effect. Figure 244 shows an example of this function.

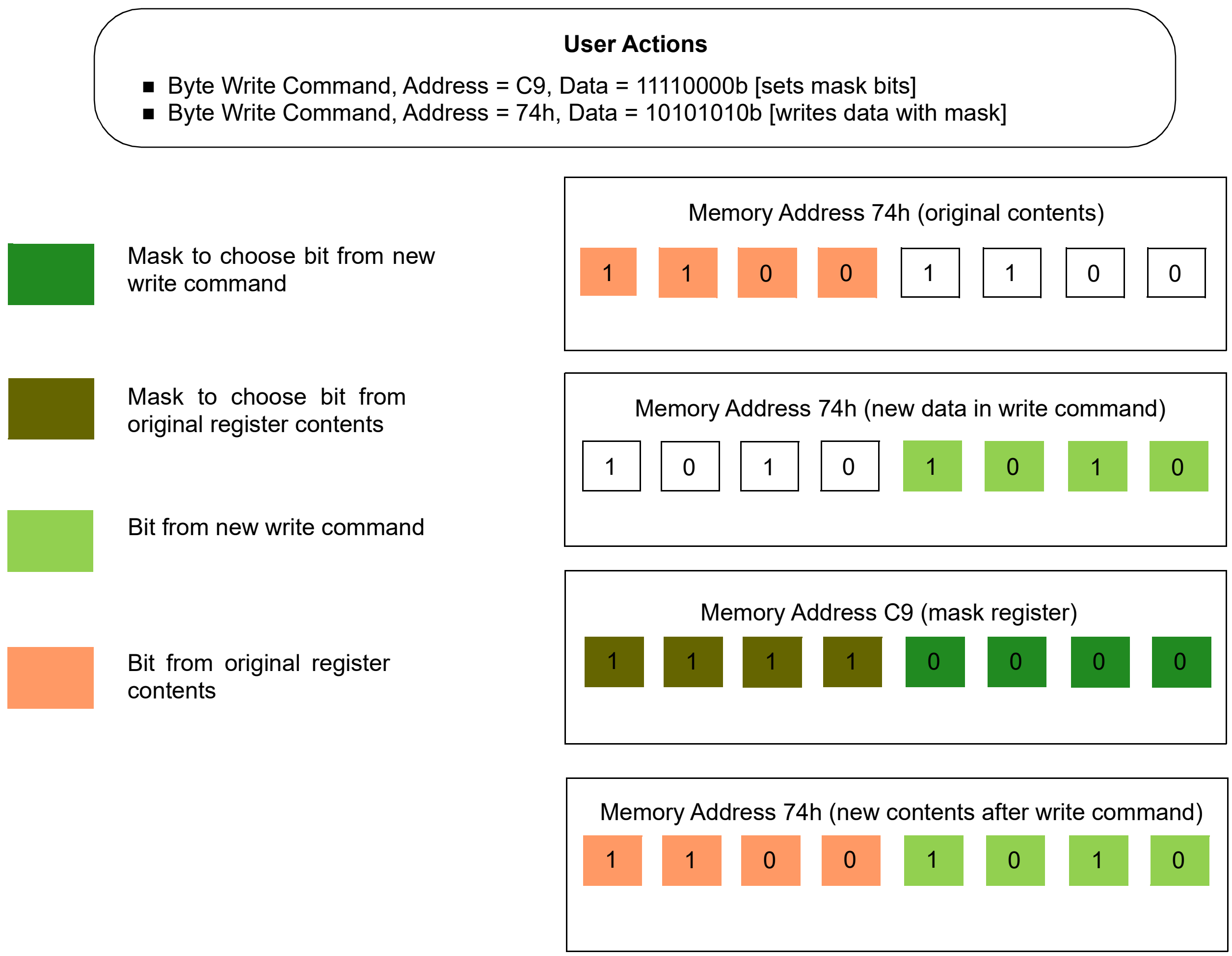


Figure 244: Example of I^{2}C Byte Write Bit Masking

19 Non-Volatile Memory

The SLG47004 provides 2,048 bits of Serial Electrically Erasable Configuration Register memory that is used for device configuration, and 2,048 bits Programmable Read-Only Memory (emulated EEPROM). Each of these memory spaces is internally organized as 16 pages of 16 bytes. The device features a Software Write Protection feature with five different programmable levels of protection for the emulated EEPROM array. The protection settings of the device can be made permanent if desired. The emulated EEPROM memory operates with a supply voltage ranging from 2.4 V to 5.5 V for Read and 2.5 V to 5.5 V for Write.

The emulated EEPROM inside the SLG47004 operates as a slave device and utilizes a simple I^2C compatible 2-wire digital serial interface to communicate with a host controller commonly referred to as the bus Master. The Master initiates and controls all read and write operations to the Slave devices on the serial bus, and both the Master and the Slave devices can transmit and receive data on the bus.

Key features:

- Low-voltage Operation
  - for Read: VCC = 2.4 V to 5.5 V
  - for Write: VCC = 2.5 V to 5.5 V
- I^2C-Compatible (2-Wire) Serial Interface
  - 100 kHz Standard Mode
  - 400 kHz Fast Mode (FM)
- Software Write Protection of the EEPROM Emulation Array
  - Five configuration options
  - Protection settings can be made permanent
- Low Current Consumption
  - Read Current 0.5 mA max
  - Page Write Current 3.0 mA max
  - Chip Erase Current 3.0 mA max
  - Standby Current (1.0 µA max)
- 16-byte Page Write Mode
- Self-timed Write/Erase Cycle (20 ms max)
- Reliability
  - Endurance: 1,000 write cycles
  - Data retention: 10 years at 125 °C

19.1 SERIAL NVM WRITE OPERATIONS

Write access to the NVM is possible by setting A3, A2, A1, A0 to “0000”, which allows serial write data for a single page only. Upon receipt of the proper Control Byte and Word Address bytes, the SLG47004 will send an ACK. The device will then be ready to receive page data, which is 16 sequential writes of 8-bit data words. The SLG47004 will respond with an ACK after each data word is received. The addressing device, such as a bus Master, must then terminate the write operation with a Stop condition after all page data is written. At that time the device will enter an internally self-timed write cycle, which will be completed within t_{WR} (20 ms). While the data is being written into the NVM Memory Array, all inputs, outputs, internal logic, and I^2C access to the Register data will be operational/valid. Please refer to Figure 246 for the SLG47004 Memory Map.

Note: The 16 programmed bytes should be in the same page. Any I^2C command that does not meet specific requirements will be ignored and NVM will remain unprogrammed.

Note: Special care must be taken when NVM page 14 is rewritten (registers [1919:1792]). This page contains rheostats tolerance data that can be permanently lost during write/erase operation.

SLG47004 will ignore the Serial NVM Write command in case the self-programming procedure for programming rheostat value into the NVM is in progress. The SLG47004 will respond with NACK in this case. Please refer to the Acknowledge Polling section for more details.

Data “1” cannot be re-programmed as data “0” without erasure. Each byte can only be programmed one time without erasure.

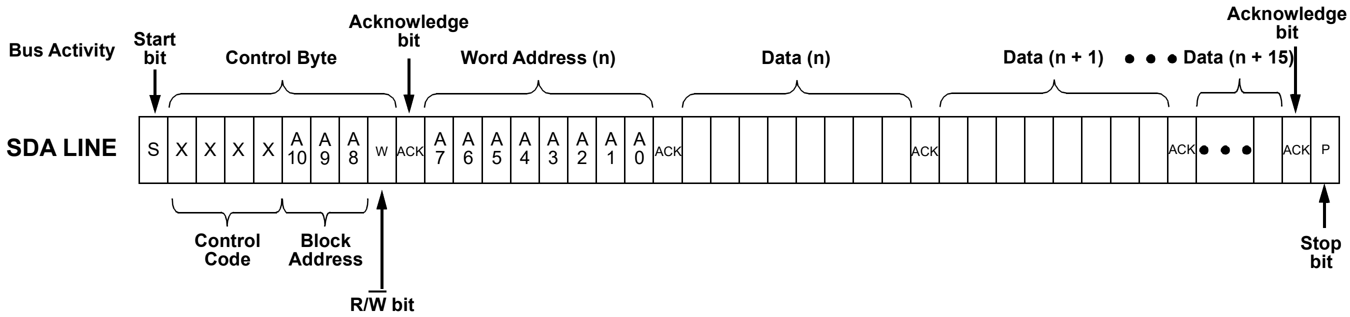


Figure 245: Page Write Command

A10 will be ignored during communication to SLG47004.

A9 = 1 will enable access to the NVM.

A9 = 1 and A8 = 0 corresponds to the 2K bits chip configuration NVM data.

A9 = 1 and A8 = 1 corresponds to the 2K bits of emulated EEPROM data.

A3, A2, A1, and A0 should be 0000 for the page write operation.

In a single page, if the data written to any byte is 00H, the contents of the matching byte in NVM memory will not be altered.

Lowest I^{2}C Address = 000h

I^{2}C Block Address			Memory Space
A10 = 0	A9 = 0	A8 = 0	**2 kbits Register Data Configuration**
A10 = 0	A9 = 0	A8 = 1	**Not Used**
A10 = 0	A9 = 1	A8 = 0	**2 kbits NVM Data Configuration**
A10 = 0	A9 = 1	A8 = 1	**2 kbits EEPROM**
A10 = 1	A9 = X	A8 = X	**Not Used**

Highest I^{2}C Address = 7FFh

Figure 246: I^{2}C Block Addressing

19.2 SERIAL NVM READ OPERATIONS

There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read

Please refer to the Section 18 for more details.

19.3 SERIAL NVM ERASE OPERATIONS

The erase scheme allows a portion or the entire emulated EEPROM including the 2K bits NVM chip configuration to be erased by modifying the contents of the Erase Registers (ERSE <2:0>). Changing the state of the ERSE is accomplished with a Byte Write sequence with the requirements outlined in this section.

The ERSE registers are located on byte E3h.

The ERSE format is shown in Table 65, and the ERSE bit functions are included in Table 66.

Table 65: Erase Register Bit Format

	b7	b6	b5	b4	b3	b2	b1	b0
Page Erase Register	ERSE2	ERSE1	ERSE0	ERSEB4	ERSEB3	ERSEB2	ERSEB1	ERSEB0

Table 66: Erase Register Bit Function Description

Bit	Name		Type	Description
7	ERSE2	Erase Enable	W	000: erase disable 110: cause the NVM erase
6	ERSE1		W	
5	ERSE0		W	
4	ERSEB4	Page Selection for Erase	W	Define the page address, which will be erased: ERSB4 = 0 corresponds to the Upper 2K NVM used for chip configuration; ERSB4 = 1 corresponds to the 2-k emulated EEPROM
3	ERSEB3		W	
2	ERSEB2		W	
1	ERSEB1		W	
0	ERSEB0		W	

Upon receipt of the proper Device Address and Erase Registers Address, the SLG47004 will send an ACK. The device will then be ready to receive Erase Registers data. The SLG47004 will respond with an ACK after Erase Registers data word is received. The addressing device, such as a bus Master, must then terminate the write operation with a Stop condition. At that time the device will enter an internally self-timed erase cycle, which will be completed within t_{ER} ms. While the data is being written into the Memory Array, all inputs, outputs, internal logic, and I^2C access to the Register data will be operational/valid.

After the erase has taken place, the contents of ERSE bits will be set to “0” automatically. The internal erase cycle will be triggered at the time the Stop Bit in the I^2C command is received.

19.4 ACKNOWLEDGE POLLING

An Acknowledge Polling routine can be implemented to optimize time sensitive applications that would prefer not to wait the fixed maximum write cycle time (t_{WR}) or erase maximum cycle time (t_{ER}). This method allows the application to know immediately when the Serial EEPROM emulation write/erase cycle has completed, so a subsequent operation can be started. Once the internally self-timed write/erase cycle has started, an Acknowledge Polling routine can be initiated. This involves repeatedly sending a Start condition followed by a valid Device Address byte (NVM block address) with the R/W bit set at Logic 0. The device will not respond with an ACK while the write cycle is ongoing. Once the internal write/erase cycle has completed, emulated EEPROM will respond with an ACK, allowing a new read, erase, or write operation to be immediately initiated.

The same behavior will happen during the self-programming procedure when the rheostat value is written into the NVM.

The length of the self-timed write cycle (t_{WR}) and self-timed erase cycle (t_{ER}) is defined as the amount of time from the Stop condition that begins the internal write operation to the Start condition of the first Device Address byte that includes NVM address (A9 = 1; A8 = X) sent to the SLG47004, that it subsequently responds to with an ACK.

19.5 LOW POWER STANDBY MODE

Emulated EEPROM inside the SLG47004 has a low power standby mode which is enabled when any one of the following occurs:

- A valid power-up sequence is performed
- A Stop condition is received by the devices unless it initiates an internal write/erase cycle
- At the completion of an internal write/erase cycle
- An unsuccessful match of the device type identifier or hardware address in the Device Address byte occurs

19.6 EMULATED EEPROM WRITE PROTECTION

The SLG47004 utilizes a software scheme that allows a portion or the entire emulated EEPROM to be inhibited from being written or erased by modifying the contents of the Write Protection Register (WPR). If desired, the WPR can be set so that it may no longer be modified/erased, thereby making the current protection scheme permanent. The status of the WPR can be determined by following a Random Read sequence. Changing the state of the WPR is accomplished with a Byte Write sequence with the requirements outlined in this section.

The WPR register is located at E2 Address.

The WPR format is shown in Table 67, and the WPR bit functions are included in Table 68.

Table 67: Write/Erase Protect Register Format

	b7	b6	b5	b4	b3	b2	b1	b0
WPR						WPRE	WPB1	WPB0

Table 68: Write/Erase Protect Register Bit Function Description

Bit	Name		Type	Description
2	WPRE	Write Protect Register Enable	R/W	0: No Software Write Protection enabled (default) 1: Write Protection is set by the state of WPB [1:0] bits
1:0	WPB1	Write Protect Block Bits	R/W	00: Upper quarter of emulated EEPROM is write protected (default) 01: Upper half of emulated EEPROM is write protected 10: Upper 3/4 of emulated EEPROM is write protected. 11: Entire emulated EEPROM is write protected.
	WPB0		R/W	

Write Protect Enable (WPRE): The Write Protect Enable Bit is used to enable or disable the device Software Write/Erase Protect. A Logic 0 in this position will disable Software Write/Erase Protection, and a Logic 1 will enable this function.

Write Protect Block Bits (WPB1:WPB0): The Write Protect Block bits allow four levels of protection of the Memory Array, provided that the WPRE bit is a Logic 1. If the WPRE bit is a Logic 0, the state of the WPB1:0 bits have no impact on device protection.

Protect Lock Bit (PRL): The Protect Lock Bit is used to permanently lock the current state of the WPR, as well as RPR and NPR (see Section 18.5). A Logic 0 indicates that the WPR, RPR, and NPR can be modified, whereas a Logic 1 indicates the WPR, RPR, and NPR has been locked and can no longer be modified. The PRL register bit is located at register [1824] address.

20 Analog Temperature Sensor

The SLG47004 has an Analog Temperature sensor (TS) with an output voltage linearly-proportional to the Centigrade temperature. The TS cell shares buffer with Vref 0, so it is impossible to use both cells simultaneously, its output can be connected directly to the IO0 or IO1 or the ACPM1_L positive input. Using buffer causes low-output impedance, linear output and makes interfacing to readout or control circuitry especially easy. Vref0 and Vref1 share output buffers with Temperature sensor. Note, that user can use any of output buffers, but Temperature sensor is calibrated for Vref1 output buffer. The TS is rated to operate over a -40 °C to 85 °C temperature range. The error in the whole temperature range does not exceed ±1.76 %. For more details refer to Section 3.12.

$$V_{TS1} = -2.4 \times T + 900.2$$

$$V_{TS2} = -2.8 \times T + 1082.7$$

where:

V_{TS1} (mV) - TS Output Voltage, range 1

V_{TS2} (mV) - TS Output Voltage, range 2

T (°C) - Temperature

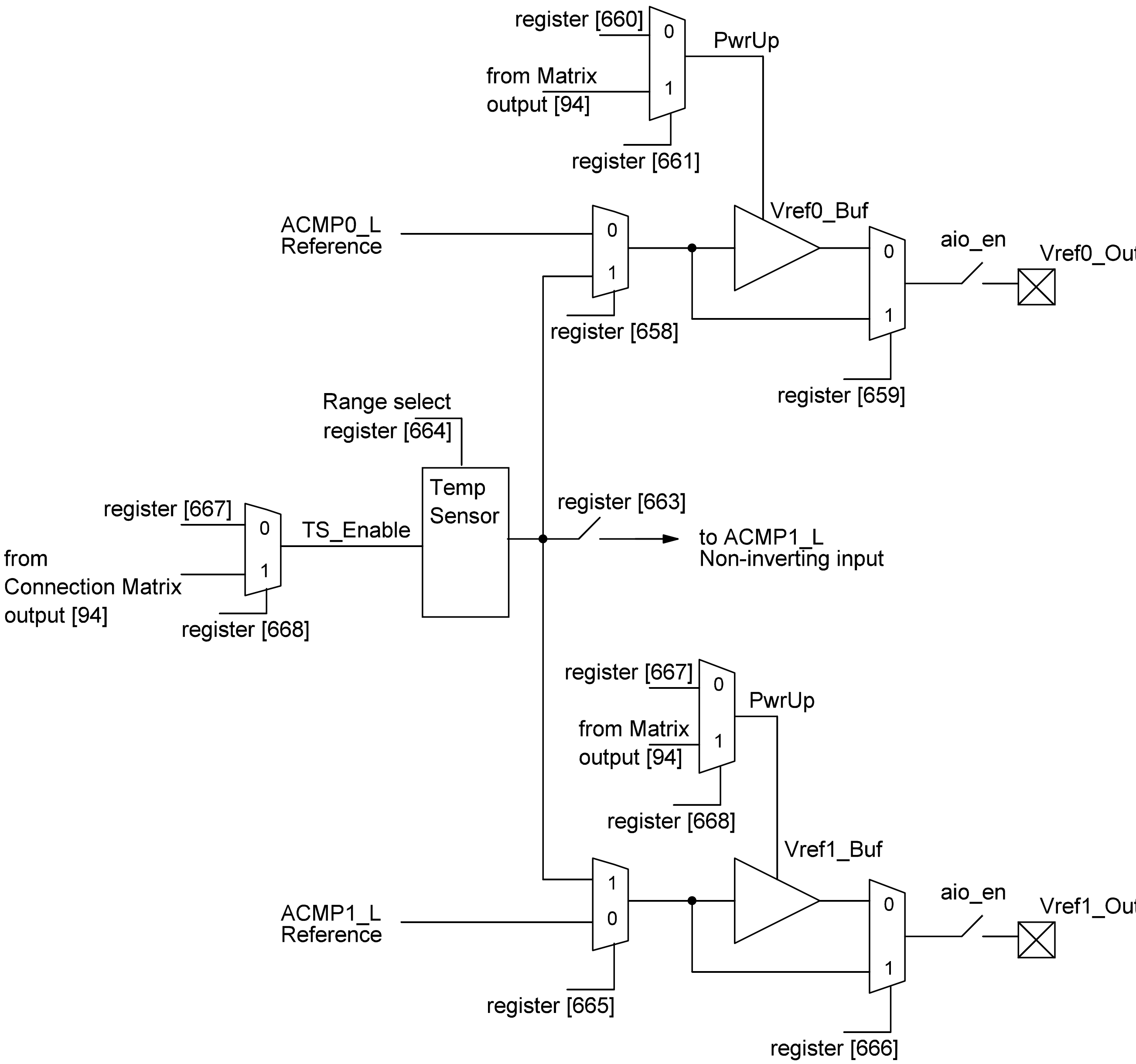


Figure 247: Analog Temperature Sensor Structure Diagram

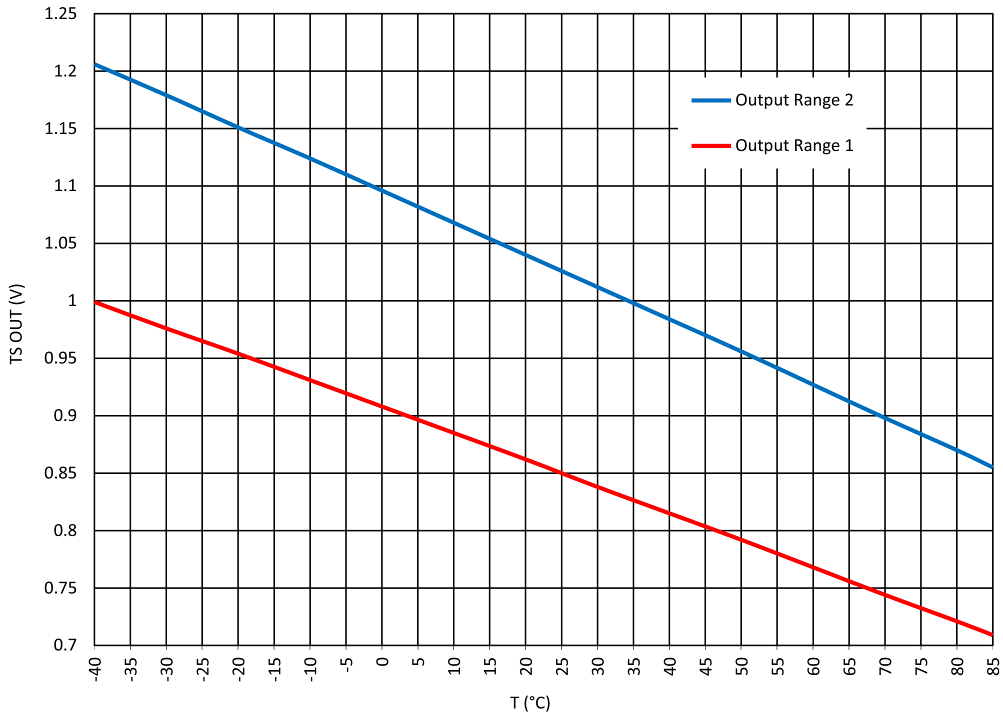


Figure 248: TS Output vs. Temperature, V_{DD} = 3.3 V

21 Register Definitions

21.1 REGISTER MAP

Table 69: Register Map

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
Matrix Output			
0	0	2-bit LUT0 & DFF0	OUT0: IN0 of 2-bit LUT0 or Clock Input of DFF0
	1		
	2		
	3		
	4		
	5		
	6		OUT1: IN1 of 2-bit LUT0 or Data Input of DFF0
	7		
1	8		
	9		
	10		
	11		
	12	2-bit LUT1 & DFF1	OUT2: IN0 of 2-bit LUT1 or Clock Input of DFF1
	13		
	14		
	15		
2	16		
	17		
	18		OUT3: IN1 of 2-bit LUT1 or Data Input of DFF1
	19		
	20		
	21		
	22		
	23		
3	24	2-bit LUT2 & DFF2	OUT4: IN0 of 2-bit LUT2 or Clock Input of DFF2
	25		
	26		
	27		
	28		
	29		
	30		OUT5: IN1 of 2-bit LUT2 or Data Input of DFF2
	31		
4	32		
	33		
	34		
	35		
	36	2-bit LUT3 & PGen	OUT6: IN0 of 2-bit LUT3 or Clock Input of PGen
	37		
	38		
	39		

Table 69: Register Map (Continued)

Address: Byte	Address: Register Bit	Signal Function	Register Bit Definition
5	40	2-bit LUT3 & PGen	OUT6: IN0 of 2-bit LUT3 or Clock Input of PGen
	41		
	42		OUT7: IN1 of 2-bit LUT3 or nRST of PGen
	43		
	44		
	45		
	46		
	47		
6	48	3-bit LUT0 & DFF3	OUT8: IN0 of 3-bit LUT0 or CLK Input of DFF3
	49		
	50		
	51		
	52		
	53		
	54		OUT9: IN1 of 3-bit LUT0 or Data Input of DFF3
	55		
7	56		
	57		
	58		
	59		
	60		OUT10: IN2 of 3-bit LUT0 or nRST (nSET) of DFF3
	61		
	62		
	63		
8	64		
	65		
	66	3-bit LUT1 & DFF4	OUT11: IN0 of 3-bit LUT1 or CLK Input of DFF4
	67		
	68		
	69		
	70		
	71		
9	72		OUT12: IN1 of 3-bit LUT1 or Data Input of DFF4
	73		
	74		
	75		
	76		
	77		
	78		OUT13: IN2 of 3-bit LUT1 or nRST (nSET) of DFF4
	79		
A	80		
	81		
	82		
	83		

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
A	84	3-bit LUT2 & DFF5	OUT14: IN0 of 3-bit LUT2 or CLK Input of DFF5
	85		
	86		
	87		
B	88		
	89		
	90		OUT15: IN1 of 3-bit LUT2 or Data Input of DFF5
	91		
	92		
	93		
	94		
	95		
C	96		OUT16: IN2 of 3-bit LUT2 or nRST (nSET) of DFF5
	97		
	98		
	99		
	100		
	101		
	102	3-bit LUT3 & DFF6	OUT17: IN0 of 3-bit LUT3 or CLK Input of DFF6
	103		
D	104		
	105		
	106		
	107		
	108		OUT18: IN1 of 3-bit LUT3 or Data Input of DFF6
	109		
	110		
	111		
E	112		
	113		
	114		OUT19: IN2 of 3-bit LUT3 or nRST (nSET) of DFF6
	115		
	116		
	117		
	118		
	119		
F	120	3-bit LUT4 & DFF7	OUT20: IN0 of 3-bit LUT4 or CLK Input of DFF7
	121		
	122		
	123		
	124		
	125		
	126		OUT21: IN1 of 3-bit LUT4 or Data Input of DFF7
	127		

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
10	128	3-bit LUT4 & DFF7	OUT21: IN1 of 3-bit LUT4 or Data Input of DFF7
	129		
	130		
	131		
	132		OUT22: IN2 of 3-bit LUT4 or nRST (nSET) of DFF7
	133		
	134		
	135		
11	136		
	137		
	138	3-bit LUT5 & DFF8	OUT23: IN0 of 3-bit LUT5 or CLK Input of DFF8
	139		
	140		
	141		
	142		
	143		
12	144		OUT24: IN1 of 3-bit LUT5 or Data Input of DFF8
	145		
	146		
	147		
	148		
	149		
	150		OUT25: IN2 of 3-bit LUT5 or nRST (nSET) of DFF8
	151		
13	152		
	153		
	154		
	155		
	156	3-bit LUT6 & DFF9	OUT26: IN0 of 3-bit LUT6 or CLK Input of DFF9
	157		
	158		
	159		
14	160		
	161		
	162		OUT27: IN1 of 3-bit LUT6 or Data Input of DFF9
	163		
	164		
	165		
	166		
	167		
15	168		OUT28: IN2 of 3-bit LUT6 or nRST (nSET) of DFF9
	169		
	170		
	171		
	172		
	173		

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
15	174	Multi_function1	OUT29: IN0 of 3-bit LUT7 or CLK Input of DFF11 Delay1 Input (or Counter1 nRST Input)
	175		
16	176		
	177		
	178		
	179		
	180		OUT30: IN1 of 3-bit LUT7 or nRST (nSET) of DFF11 Delay1 Input (or Counter1 nRST Input)
	181		
	182		
	183		
17	184		
	185		
	186		OUT31: IN2 of 3-bit LUT7 or Data of DFF11 Delay1 Input (or Counter1 nRST Input)
	187		
	188		
	189		
	190		
	191		
18	192	Multi_function2	OUT32: IN0 of 3-bit LUT8 or CLK Input of DFF12 Delay2 Input (or Counter2 nRST Input)
	193		
	194		
	195		
	196		
	197		
	198		OUT33: IN1 of 3-bit LUT8 or nRST (nSET) of DFF12 Delay2 Input (or Counter2 nRST Input)
	199		
19	200		
	201		
	202		
	203		
	204		OUT34: IN2 of 3-bit LUT8 or Data of DFF12 Delay2 Input (or Counter2 nRST Input)
	205		
	206		
	207		
1A	208		
	209		
	210	Multi_function3	OUT35: IN0 of 3-bit LUT9 or CLK Input of DFF13 Delay3 Input (or Counter3 nRST Input)
	211		
	212		
	213		
	214		
	215		

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
1B	216	Multi_function3	OUT36: IN1 of 3-bit LUT9 or nRST (nSET) of DFF13 Delay3 Input (or Counter3 nRST Input)
	217		
	218		
	219		
	220		
	221		
	222		
	223		
1C	224		OUT37: IN2 of 3-bit LUT9 or Data of DFF13 Delay3 Input (or Counter3 nRST Input)
	225		
	226		
	227		
	228	Multi_function4	OUT38: IN0 of 3-bit LUT10 or CLK Input of DFF14 Delay4 Input (or Counter4 nRST Input)
	229		
	230		
	231		
1D	232		
	233		
	234		
	235		
	236		OUT39: IN1 of 3-bit LUT10 or nRST (nSET) of DFF14 Delay4 Input (or Counter4 nRST Input)
	237		
	238		
	239		
1E	240		OUT40: IN2 of 3-bit LUT10 or Data of DFF14 Delay4 Input (or Counter4 nRST Input)
	241		
	242		
	243		
	244		
	245		
	246	Multi_function5	OUT41: IN0 of 3-bit LUT11 or CLK Input of DFF15 Delay5 Input (or Counter5 nRST Input)
	247		
1F	248		
	249		
	250		
	251		
	252		OUT42: IN1 of 3-bit LUT11 or nRST (nSET) of DFF15 Delay5 Input (or Counter5 nRST Input)
	253		
	254		
	255		
20	256		
	257		
	258		OUT43: IN2 of 3-bit LUT11 or Data of DFF15 Delay5 Input (or Counter5 nRST Input)
	259		
	260		
	261		
	262		
	263		

Table 69: Register Map (Continued)

Address: Byte	Address: Register Bit	Signal Function	Register Bit Definition
21	264	Multi_function6	OUT44: IN0 of 3-bit LUT12 or CLK Input of DFF16 Delay6 Input (or Counter6 nRST Input)
	265		
	266		
	267		
	268		
	269		
	270		
	271		
22	272		OUT45: IN1 of 3-bit LUT12 or nRST (nSET) of DFF16 Delay6 Input (or Counter6 nRST Input)
	273		
	274		
	275		
	276		
	277		
	278		OUT46: IN2 of 3-bit LUT12 or Data of DFF16 Delay6 Input (or Counter6 nRST Input)
	279		
23	280		
	281		
	282	3-bit LUT13 & Pipe Delay (RIPP CNT)	OUT47: IN0 of 3-bit LUT13 or Input of Pipe Delay or UP signal of RIPP CNT
	283		
	284		
	285		
	286		
	287		
24	288		OUT48: IN1 of 3-bit LUT13 or nRST of Pipe Delay or nSET of RIPP CNT
	289		
	290		
	291		
	292		
	293		
	294		OUT49: IN2 of 3-bit LUT13 or Clock of Pipe Delay_RIPP CNT
	295		
25	296		
	297		
	298		
	299		
	300	4-bit LUT_DFF10	OUT50: IN0 of 4-bit LUT0 or CLK Input of DFF10
	301		
	302		
	303		
26	304		
	305		
	306		OUT51: IN1 of 4-bit LUT0 or Data of DFF10
	307		
	308		
	309		
	310		
	311		

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
27	312	4-bit LUT_DFF10	OUT52: IN2 of 4-bit LUT0 or nRST (nSET) of DFF10
	313		
	314		
	315		
	316		
	317		
	318		OUT53: IN3 of 3-bit LUT0
	319		
28	320		
	321		
	322		
	323		
	324	Multi_function0	OUT54: IN0 of 4-bit LUT1 or CLK Input of DFF17 Delay0 Input (or Counter0 nRST Input)
	325		
	326		
	327		
29	328		
	329		
	330		OUT55: IN1 of 4-bit LUT1 or nRST of DFF17 Delay0 Input (or Counter0 nRST Input) Delay/Counter0 External CLK source
	331		
	332		
	333		
	334		
	335		
2A	336		OUT56: IN2 of 4-bit LUT1 or nSET of DFF17 Delay0 Input (or Counter0 nRST Input) Delay/Counter0 External CLK source KEEP Input of FSM0
	337		
	338		
	339		
	340		
	341		
	342		OUT57: IN3 of 4-bit LUT1 or Data of DFF17 Delay0 Input (or Counter0 nRST Input) UP Input of FSM
	343		
2B	344		
	345		
	346		
	347		
	348	Programmable delay	OUT58: Programmable delay/edge detect input
	349		
	350		
	351		
2C	352		
	353		
	354	Filter/Edge detector	OUT59: Filter/Edge detect input
	355		
	356		
	357		
	358		
	359		

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
2D	360	IO0	OUT60: IO0 DOUT
	361		
	362		
	363		
	364		
	365		
	366		
	367		
2E	368		OUT61: IO0 DOUT OE
	369		
	370		
	371		
	372		
	373		
	374		
	375		
2F	376	IO1	OUT62: IO1 DOUT
	377		
	378		
	379		
	380		
	381		
	382		
	383		
30	384		OUT63: IO1 DOUT OE
	385		
	386		
	387		
	388		
	389		
	390		
	391		
31	392	IO2	OUT64: IO2 DOUT
	393		
	394		
	395		
	396		
	397		
	398		
	399		
32	400		OUT65: IO2 DOUT OE
	401		
	402		
	403		
	404		
	405		
	406		
	407		

Table 69: Register Map (Continued)

Address: Byte	Address: Register Bit	Signal Function	Register Bit Definition
33	408	IO4	OUT68: IO4 DOUT
	409		
	410		
	411		
	412		
	413		
	414		
	415		
34	416		OUT69: IO4 DOUT OE
	417		
	418		
	419		
	420	IO5	OUT70: IO5 DOUT
	421		
	422		
	423		
35	424		
	425		
	426		
	427		
	428		OUT71: IO5 DOUT OE
	429		
	430		
	431		
36	432	IO6	OUT72: IO6 DOUT
	433		
	434		
	435		
	436		
	437		
	438		
	439		
37	440		OUT73: IO6 DOUT OE
	441		
	442		
	443		
	444	Programmable Trim Block0	OUT74: set0 of Auto Calibration
	445		
	446		
	447		
38	448		
	449		
	450		
	451		
	452		OUT75: clock0 of Auto Calibration
	453		
	454		
	455		

Table 69: Register Map (Continued)

Address: Byte	Address: Register Bit	Signal Function	Register Bit Definition
39	456	Programmable Trim Block0	OUT76: reload0 of Auto Calibration
	457		
	458		
	459		
	460		
	461		
	462		OUT77: program0 of Auto Calibration
	463		
3A	464		
	465		
	466		
	467		
	468	Digital Rheostat	OUT78: Rheostat Counter0 up/down 0: down, 1: up. (register [920] = 0) 0: up, 1: down. (register [920] = 1)
	469		
	470		
	471		
3B	472		
	473		
	474	Programmable Trim Block1	OUT79: set1 of Auto Calibration
	475		
	476		
	477		
	478		
	479		
3C	480		OUT80: clock1 of Auto Calibration
	481		
	482		
	483		
	484		
	485		
	486		OUT81: reload1 of Auto Calibration
	487		
3D	488		
	489		
	490		
	491		
	492		OUT82: program1 of Auto Calibration
	493		
	494		
	495		
3E	496		
	497		
	498	Digital Rheostat	OUT83: Rheostat Counter1 up/down 0: down, 1: up. (register [923] = 0) 0: up, 1: down. (register [923] = 1)
	499		
	500		
	501		
	502		
	503		

Table 69: Register Map (Continued)

Address: Byte	Address: Register Bit	Signal Function	Register Bit Definition
3F	504	FIFO Reset of PT blocks	OUT84: FIFO nRST of the control logic of reload0/reload1/auto program0/auto program1
	505		
	506		
	507		
	508		
	509		
	510	Chopper ACMP	OUT85: Chopper ACMP Power Up
	511		
40	512		
	513		
	514		
	515		
	516	Digital Rheostat	OUT86: Rheostat Charge pump enable
	517		
	518		
	519		
41	520		
	521		
	522	Analog Switch0	OUT87: ASW0 enable/Half bridge enable
	523		
	524		
	525		
	526		
	527		
42	528	Analog Switch1	OUT88: ASW1 enable/Half bridge data
	529		
	530		
	531		
	532		
	533		
	534	ACMP0	OUT89: ACMP0 Power Up
	535		
43	536		
	537		
	538		
	539		
	540	ACMP1	OUT90: ACMP1 Power Up
	541		
	542		
	543		
44	544		
	545		
	546	OSC0	OUT91: OSC0 ENABLE
	547		
	548		
	549		
	550		
	551		

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
45	552	OSC1	OUT92: OSC1 ENABLE
	553		
	554		
	555		
	556		
	557		
	558	OSC2	OUT93: OSC2 ENABLE
	559		
46	560		
	561		
	562		
	563		
	564	Temperature Sensor	OUT94: VREFO TEMPSEN/VREFO Power Up
	565		
	566		
	567		
47	568		
	569		
	570	HDBUF	OUT95: HDBUF ENABLE
	571		
	572		
	573		
	574		
	575		
48	576	Op Amp0	OUT96: OP0(Op Amp ACMP0) Power Up
	577		
	578		
	579		
	580		
	581		
	582	Op Amp1	OUT97: OP1(Op Amp ACMP1) Power Up
	583		
49	584		
	585		
	586		
	587		
	588	Op Amp2	OUT98: OP2 Power Up (In Amp Mode)
	589		
	590		
	591		
4A	592		
	593		
	594	Op amps	OUT99: OP VREF ENABLE
	595		
	596		
	597		
	598		
	599		

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
4B	600	Reserved	
	601	Reserved	
	602	Reserved	
	603	Reserved	
	604	Reserved	
	605	Reserved	
	606	Reserved	
	607	Reserved	
ACMP0			
4C	608	ACMP Low Energy Power Up enable (ACMP power after bg_ok)	1: enable
	609	ACMP input path LPF enable	1: enable
	610	ACMP sampling mode enable	1: enable
	611	ACMP short time wake sleep mode disable	0: short time wake sleep enable 1: short time wake sleep disable
	612	ACMP wake sleep function enable	1: enable
	613	ACMP Vref path LPF enable (when ACMP hysteresis > 196 mV)	1: enable
	614 615	ACMP input divider selection	00: 1 01: 0.5 10: 1/3 11: 1/4
4D	616 617	ACMP input mux selection	00: OP0 output 01: from Pin 10: tie VDD
	618 619 620 621 622 623	ACMP Low to High Vref selection	000000-111111: 32 mV ~2.048 V/step = 32 mV
4E	624 625 626 627 628 629	ACMP High to Low Vref selection	000000-111111: 32 mV ~2.048 V/step = 32 mV
ACMP1			
4E	630	ACMP Low Energy Power Up enable (ACMP power after bg_ok)	1: enable
	631	ACMP input path LPF enable	1: enable
4F	632	ACMP sampling mode enable	1: enable
	633	ACMP short time wake sleep mode disable	0: short time wake sleep enable 1: short time wake sleep disable
	634	ACMP wake sleep function enable	1: enable
	635	ACMP Vref path LPF enable (when ACMP hysteresis > 196 mV)	1: enable
	636 637	ACMP input divider selection	00: 1 01: 0.5 10: 1/3 11: 1/4

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
4F	638	ACMP input mux selection	00: OP1 output 01: from Pin 10: ACMP0 input mux output 11: VrefO1 Temp sensor output
	639		
50	640	ACMP Low to High Vref selection	000000-111111: 32 mV ~2.048 V/step = 32 mV
	641		
	642		
	643		
	644		
	645		
	646	ACMP High to Low Vref selection	000000-111111: 32 mV ~2.048 V/step = 32 mV
	647		
51	648		
	649		
	650		
	651		
Vref			
51	652	Reserved	
	653	Reserved	
	654	Reserved	
	655	Reserved	
52	656	Reserved	
	657	Reserved	
	658	VREFO0 input source selection	0: ACMP0 VREF 1: Temp Sensor
	659	VREFO0 output buffer enable	1: enable
	660	VREFO0 register Power Up	VREFO0 register power on signal
	661	VREFO0 Power Up selection	0: Power Up from reg 1: from matrix
	662	Reserved	no use
	663	VREFO1's temp sensor to ACMP1 input path enable	Temp Sensor output to ACMP1 enable 1: enable
53	664	VREFO1's temp sensor range selection	0:1V; 1:1.2V
	665	VREFO1 input source selection	0: ACMP1 Vref 1: TS
	666	VREFO1 output buffer enable	1: enable
	667	VREFO1 register Power Up	VrefO1 register power on signal
	668	VREFO1 Power Up selection	0: Power Up from reg 1: from matrix
	669	ACMP Vrefs source selection	ACMP Vref gen source selection (0: VBG, 1: V_{DD})
	670	ACMP0 external Vref enable	1:enable
	671	ACMP1 external Vref enable	1:enable
54	672	Reserved	
54	673	Reserved	
	674	Reserved	

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
54	675	Reserved	
	676		
	677		
	678	Reserved	
	679	Reserved	
55	680	Reserved	
	681	Reserved	
	682	Reserved	
	683	Reserved	
	684	Reserved	
	685	Reserved	
	686	Reserved	
	687	Reserved	
OSC1			
56	688	OSC1 turn on by register	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
	689	OSC1 matrix power down or on select	0: matrix down 1: matrix on
	690	OSC1 external clock source enable	0: internal OSC1 1: external clock from Pin15
	691	OSC1 post divider ratio control	00: div 1 01: div 2 10: div 4 11: div8
	692		
	693	OSC1 matrix divider ratio control	000: /1 001:/2 010:/4 011: /3 100: /8 101: /12 110: /24 111: /64
	694		
	695		
57	696	OSC1 matrix out enable	0: disable 1: enable
	697	Reserved	
	698	Reserved	
	699	Reserved	
	700	OSC1 2nd output to matrix enable	0: disable 1: enable
	701	OSC1 2nd matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
	702		
	703		
OSC2			

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
58	704	OSC2 turn on by register	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
58	705	OSC2 matrix power down or on select	0: matrix down 1: matrix on
58	706	OSC2 external clock source enable	0: internal OSC2 1: external clock from IO2
58	707	OSC2 matrix out enable	0: disable 1: enable
58	708 709	OSC2 post divider ratio control	00: div 1 01: div 2 10: div 4 11: div8
58 59	710 711 712	OSC2 matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
59	713	OSC2 startup delay with 100ns	0: enable 1: disable
59	714	Reserved	
59	715	Reserved	
59	716	Reserved	
59	717	Op Amp0 sr boost for OP 8 MHz	0: enable, 1: disable
59	718	Op Amp1 sr boost for OP 8 MHz	0: enable, 1: disable
59	719	Op Amp2 sr boost for OP 8 MHz	0: enable, 1: disable
OSC0			
5A	720	OSC0 turn on by register	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
5A	721	OSC0 matrix power down or on select	0: matrix down 1: matrix on
5A	722	OSC0 external clock source enable	0: internal OSC0 1: external clock from IO0
5A	723	OSC0 matrix out enable	0: disable 1: enable
5A	724 725	OSC0 post divider ratio control	00: div 1 01: div 2 10: div 4 11: div8
5A 5B	726 727 728	OSC0 matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
5B	729	enable OSC0 output gating by wake_sleep signal (note: the wake_sleep clock is separated path, so it is not gated)	0: no gating 1: enable
	730	OSC0 2nd output to matrix enable	0: disable 1: enable
	731 732 733	OSC0 2nd matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
	734	Reserved	
	735	Reserved	
Analog Switch			
5C	736	ASW0 small NMOS enable selection	0: small NMOS disable 1: small NMOS enable by matrix87
	737	ASW1 small PMOS enable selection	0: small PMOS disable 1: small PMOS enable by matrix88
	738	ASW0 big PMOS control selection	0: control by matrix87 1:control by Op Amp0
	739	ASW1 big NMOS control selection	0: control by matrix88 1:control by Op Amp1
	740	ASW half bridge mode enable	0: analog switch mode 1: half bridge (enable from matrix87; data from matrix88)
	741 742	ASW half bridge dead time select	00: bypass 01: 20ns 10: 100ns 11: 500ns
	743	Reserved	
Op Amp0/1/2			
5D	744 745	Op Amp0 bandwidth selection	00: 128 kHz 01: 512 kHz 10: 2 MHz 11: 8 MHz
	746 747	Op Amp1 bandwidth selection	00: 128 kHz 01: 512 kHz 10: 2 MHz 11: 8 MHz
	748 749	Op Amp2 bandwidth selection	00: 128 kHz 01: 512 kHz 10: 2 MHz 11: 8 MHz
	750	ACMP/Op Amp0 mode	0: Op amp mode 1: ACMP mode
	751	ACMP/Op Amp1 mode	0: Op amp mode 1: ACMP mode
5E	752	Op Amp0 charge pump disable	0: Op amp input common voltage higher than V_{DD}-1.5V, enable CP 1: Op amp input common voltage lower than V_{DD}-1.5V, disable CP

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
5E	753	Op Amp1 charge pump disable	0: Op amp input common voltage higher than V_{DD}-1.5V, enable CP; 1: Op amp input common voltage lower than V_{DD}-1.5V, disable CP
	754	Op Amp2 charge pump disable	0: Op amp input common voltage higher than V_{DD}-1.5V, enable CP 1: Op amp input common voltage lower than V_{DD}-1.5V, disable CP
	755	Path between Op Amp0/1 and Op Amp2	0: path on (for normal function) 1: path off (for trim function)
	756	Op Amp2's Vref buffer bypass control	0: without buffer 1: with buffer
	757	Supporting blocks for Op Amp0 on/off	0: on/off follows op amp 1: always on except input common voltage of op amp lower than V_{DD}-1.5 V
	758	Supporting blocks for Op Amp1 on/off	0: on/off follows op amp 1: always on except input common voltage of op amp lower than V_{DD}-1.5V
	759	Supporting blocks for Op Amp2 on/off	0: on/off follows op amp 1: always on except input common voltage of op amp lower than V_{DD}-1.5V
5F	760	Op amp ACMP Vref0 output selection[0]	000000-111111: 32 mV ~2.048 V/step = 32 mV
	761	Op amp ACMP Vref0 output selection[1]	
	762	Op amp ACMP Vref0 output selection[2]	
	763	Op amp ACMP Vref0 output selection[3]	
	764	Op amp ACMP Vref0 output selection[4]	
	765	Op amp ACMP Vref0 output selection[5]	
	766	Op amp ACMP Vref0 register enable (select by register [782])	0: dynamic on/off 1: Vref enable
	767	Vref0 to op amp/ACMP input enable	0:disable; 1: enable
60	768	Op amp ACMP Vref1 output selection[0]	000000-111111: 32 mV ~2.048 V/step = 32 mV
	769	Op amp ACMP Vref1 output selection[1]	
	770	Op amp ACMP Vref1 output selection[2]	
	771	Op amp ACMP Vref1 output selection[3]	
	772	Op amp ACMP Vref1 output selection[4]	
	773	Op amp ACMP Vref1 output selection[5]	
	774	Op amp ACMP Vref1 register enable (select by register [783])	0: dynamic on/off 1: Vref enable
	775	Vref1 to op amp/ACMP input enable	0:disable; 1: enable
61	776	Op amp ACMP Vref0 output selection	0: Vref to ACMP negative input 1: Vref to ACMP positive input
	777	Op amp ACMP Vref1 output selection	0: Vref to ACMP negative input 1: Vref to ACMP positive input
	778	Reserved	
	779	Reserved	
	780	Op amp ACMP Vref0 input voltage selection	0: 2.048 V 1: V_{DD}
	781	Op amp ACMP Vref1 input voltage selection	0: 2.048 V 1: V_{DD}
	782	Op amp ACMP vref0 enable selection	0: from register [766] 1: from matrix99
61	783	Op amp ACMP vref1 enable selection	0: from register [774] 1: from matrix99

Table 69: Register Map (Continued)

Address: Byte	Address: Register Bit	Signal Function	Register Bit Definition
3-bit LUT2/DFF5			
62	784	3-bit LUT2_DFF5 setting	<2:0>: 3-bit LUT2 <2:0>
	785		
	786		
	787		<3>:3-bit LUT2 <3>/DFF5 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	788		<4>:3-bit LUT2<4>/DFF5 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	789		<5>:3-bit LUT2 <5>/DFF5 Initial Polarity Select 0: Low, 1: High
	790		<6>:3-bit LUT2 <6>/DFF5 Output Select 0: Q output, 1: QB output
	791		<7>:3-bit LUT2 <7>/DFF5 or Latch Select 0: DFF function, 1: Latch function
3-bit LUT3/DFF6			
63	792	3-bit LUT3_DFF6 setting	<2:0>: 3-bit LUT3 <2:0>
	793		
	794		
	795		<3>:3-bit LUT3 <3>/DFF6 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	796		<4>:3-bit LUT3<4>/DFF6 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	797		<5>:3-bit LUT3 <5>/DFF6 Initial Polarity Select 0: Low, 1: High
	798		<6>:3-bit LUT3 <6>/DFF6 Output Select 0: Q output, 1: QB output
	799		<7>:3-bit LUT3 <7>/DFF6 or Latch Select 0: DFF function, 1: Latch function
3-bit LUT4/DFF7			
64	800	3-bit LUT4_DFF7 setting	<2:0>: 3-bit LUT4 <2:0>
	801		
	802		
	803		<3>:3-bit LUT4 <3>/DFF7 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	804		<4>:3-bit LUT4<4>/DFF7 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	805		<5>:3-bit LUT4 <5>/DFF7 Initial Polarity Select 0: Low, 1: High
	806		<6>:3-bit LUT4 <6>/DFF7 Output Select 0: Q output, 1: QB output
64	807	3-bit LUT4_DFF7 setting	<7>:3-bit LUT4 <7>/DFF7 or Latch Select 0: DFF function, 1: Latch function
3-bit LUT5/DFF8			

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
65	808	3-bit LUT5_DFF8 setting	<2:0>: 3-bit LUT5 <2:0>
	809		
	810		
	811		<3>:3-bit LUT5 <3>/DFF8 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	812		<4>:3-bit LUT5<4>/DFF8 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	813		<5>:3-bit LUT5 <5>/DFF8 Initial Polarity Select 0: Low, 1: High
	814		<6>:3-bit LUT5 <6>/DFF8 Output Select 0: Q output, 1: QB output
	815		<7>:3-bit LUT5 <7>/DFF8 or Latch Select 0: DFF function, 1: Latch function
3-bit LUT6/DFF9			
66	816	3-bit LUT6_DFF9 setting	<2:0>: 3-bit LUT6 <2:0>
	817		
	818		
	819		<3>3-bit LUT6 <3>/DFF9 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	820		<4>:3-bit LUT6<4>/DFF9 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	821		<5>:3-bit LUT6 <5>/DFF9 Initial Polarity Select 0: Low, 1: High
	822		<6>:3-bit LUT6 <6>/DFF9 Output Select 0: Q output, 1: QB output
	823		<7>:3-bit LUT6 <7>/DFF9 or Latch Select 0: DFF function, 1: Latch function
67	824	3-bit LUT2 or DFF5 Select	0: 3-bit LUT2 1: DFF5
	825	3-bit LUT3 or DFF6 Select	0: 3-bit LUT3 1: DFF6
	826	3-bit LUT4 or DFF7 Select	0: 3-bit LUT4 1: DFF7
	827	3-bit LUT5 or DFF8 Select	0: 3-bit LUT5 1: DFF8
	828	3-bit LUT6 or DFF9 Select	0: 3-bit LUT6 1: DFF8
	829	4-bit LUT0 or DFF10 Select	0: 4-bit LUT0 1: DFF10
	830	Reserved	
	831	Reserved	
4-bit LUT0/DFF10			

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
68	832	4-bit LUT0_DFF10 setting	<9:0>: 4-bit LUT0 <9:0>
	833		
	834		
	835		
	836		
	837		
	838		
	839		
69	840		
	841		
	842		<10>:4-bit LUT0 <10>/DFF10 stage selection 0: Q of first DFF; 1 Q of second DFF
	843		<11>:4-bit LUT0 <11>/DFF10 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	844		<12>:4-bit LUT0 <12>/DFF10 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	845		<13>:4-bit LUT0 <13> /DFF10 Initial Polarity Select 0: Low, 1: High
	846		<14>:4-bit LUT0 <14>/DFF10 Output Select 0: Q output, 1: QB output
	847		<15>:4-bit LUT0 <15>/DFF10 or Latch Select 0: DFF function, 1: Latch function
3-bit LUT13/Pipe Delay (RIPP CNT)			
6A	848	LUT value or pipe delay out sel or nSET/END value	at LUT/pipe delay mode bit<7:4>: 3-bit LUT13 <7:4> / REG_S1<3:0> pipe delay out1 sel bit<3:0>: 3-bit LUT13 <3:0> / REG_S0<3:0> pipe delay out0 sel at RIPP CNT mode bit<2:0> is the nSET value. bit<5:3> is the END value bit<6> is the range control: 0: full cycle, 1: range cycle bit<7> No used
	849		
	850		
	851		
	852		
	853		
	854		
	855		
6B	856	Active level selection for RST/SET	0: Active low level reset/set 1: Active high level reset/set
	857	Out of 3-bit LUT13 or Out0 of Pipe Delay/RIPP CNT Select	0: 3-bit LUT13 1: OUT0 of Pipe Delay or RIPP CNT
	858	PIPE_RIPP_CNT_S	0: Pipe delay mode selection 1: Ripple Counter mode selection
	859	Pipe Delay OUT1 Polarity Select	0: Non-inverted 1: Inverted
	860	Reserved	
	861	Reserved	
	862	Reserved	
	863	Reserved	
Programmable Delay			

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
6C	864	Delay Value Select for Programmable Delay & Edge Detector	00: 125ns 01: 250ns 10: 375ns 11: 500ns
	865		
	866	Select the Edge Mode of Programmable Delay & Edge Detector	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
	867		
Filter/Edge Detector			
6C	868	Filter or Edge Detector selection	0: filter 1: edge detect
	869	Output Polarity Select	0: output non-invert 1: output invert
	870	Select the edge mode	00: Rising Edge Detect 01: Falling Edge Detect 10: Both Edge Detect 11: Both Edge DLY
	871		
Chopper ACMP			
6D	872	Chopper ACMP positive input selection for calibration channel0	00: from In Amp out 01: from Op Amp0 out 10: from Op Amp1 out 11: IO1
	873		
	874	Chopper ACMP positive input selection for calibration channel1	00: from In Amp out 01: from Op Amp0 out 10: from Op Amp1 out 11: IO1
	875		
	876	Reserved	
	877	Reserved	
	878	Reserved	
	879	Reserved	
6E	880	Reserved	
	881	Reserved	
	882	Output Polarity Select	0: output non-invert 1: output invert
	883	Reserved	
	884		
	885		
	886		
	887		
6F	888	Reserved	
	889		
	890	Reserved	
	891	Reserved	
Calibration			

Table 69: Register Map (Continued)

Address Byte	Register Bit	Signal Function	Register Bit Definition
6F	892	auto calibration channel selection by register	0: calibration channel0 1: calibration channel1
	893	auto calibration channel selection source selection	0:calibration channel auto selection 1: from register [892]
	894	RH_CNT1 clock source selection	0: From Chopper ACMP (Chopper ACMP changes one time per rheostat clock) 1: from matrix directly
	895	RH_CNT0 clock source selection	0: From Chopper ACMP (Chopper ACMP changes one time per rheostat clock) 1: from matrix directly
70	896 897 898 899	Calibration0 clock divider	0000: Reserved 0001: Reserved 0010: OSC1/64 0011: OSC1/512 0100: OSC0 0101:OSC0/8 0110: OSC0/64 0111: OSC0/512 1000: OSC0/4096 1001: OSC0/32768 1010: OSC0/262144 1011/1100/1101/1110: GND 1111: EXTCLK
	900	Up/down selection	0: chopper ACMP 1: matrix83
	901	auto_calibration disable	0: auto calibration enable 1: disable
	902	Reserved	
	903	Reserved	
71	904 905 906 907	Calibration1 clock divider	0000: Reserved 0001: Reserved 0010: OSC1/64 0011: OSC1/512 0100: OSC0 0101: OSC0/8 0110: OSC0/64 0111: OSC0/512 1000: OSC0/4096 1001: OSC0/32768 1010: OSC0/262144 1011/1100/1101/1110: GND 1111: EXTCLK
	908	Up/down selection	0: chopper ACMP 1: matrix83
	909	auto_calibration disable	0: auto calibration enable 1: disable
	910	Reserved	
	911	Reserved	
Digital Rheostats			

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
72	912	POTCP0 turn on by register	0: control by matrix86 1: on
	913	POTCP1 turn on by register	0: control by matrix86 1: on
	914	POTCP0/1 clock source selection	0: from LPBG chopper OSC 1: from OSC1
	915	POTCP0/1 clock source select from register	0: by register [914] 1: calibration auto on
	916	Reserved	
	917	Reserved	
	918	Reserved	
	919	Reserved	
73	920	Polarity selection of RH_CNT0 UP signal	0: default (up = 0 down mode, up = 1 up mode) 1: (up = 0 up mode, up = 1 down mode)
	921	Reserved	
	922	Reserved	
	923	Polarity selection of RH_CNT1 UP signal	0: default (up = 0 down mode, up = 1 up mode) 1: (up = 0 up mode, up = 1 down mode)
	924	Reserved	
	925	Reserved	
	926	Reserved	
	927	Reserved	
HD Buffer			
74	928 929 930 931 932 933	Chop ACMP Vref selection for calibration channel 0	000000-111111: 1/64 ~ 64/64 (divider input select by register [946])
	934	Chop ACMP calibration channel0 external Vref selection	0: external Vref (pin18) 1: internal Vref
	935	Reserved	
75	936 937 938 939 940 941	Chop ACMP Vref selection for calibration channel 1	000000-111111: 1/64 ~ 64/64 (divider input select by register [946])
	942	Chop ACMP calibration channel1 external Vref selection	0: external Vref (pin18) 1: internal Vref
	943	Reserved	

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
76	944	HD buffer register enable (select by register [945])	0: disable 1: enable
	945	HD buffer enable selection	0: from register [944] 1: from matrix95
	946	Chop ACMP Vref divider input selection	0: from HD buffer output 1: from op amp Vref voltage (2.048/V_{DD} selection register in Vref block)
	947	Reserved	
	948	Reserved	
	949	Reserved	
	950	Reserved	
	951	Reserved	
CP OSC/Regulator			
77	952	CPOSC single or multiple mode select	0: multiple OSC mode 1: single OSC mode
	953	Reserved	
	954	CPOSC0 frequency select	00: 250 kHz 01: 1 MHz 10: 4 MHz 11: 8 MHz
	955		
	956	Reserved	
	957	Reserved	
	958		
	959	Reserved	
78	960	Reserved	
	961	Reserved	
	962	CPOSC1 frequency select	00: 250 kHz 01: 1 MHz 10: 4 MHz 11: 8 MHz
	963		
	964	Reserved	
	965	Reserved	
	966		
	967	Reserved	
79	968	Reserved	
	969	Reserved	
	970	CPOSC2 frequency select	00: 250 kHz 01: 1 MHz 10: 4 MHz 11: 8 MHz
	971		
	972	Reserved	
	973	Reserved	
	974		
	975	Reserved	

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
7A	976	Buffer Vref select	00: none 01: internal Vref 10: Rheostat Vref 11: external Vref
	977		
	978	Reserved	
	979	Reserved	
	980	Reserved	
	981	Reserved	
	982	Reserved	
	983	Reserved	
7B	984	I^2C soft reset	0: Keep existing condition 1: Reset execution, reload NVM to registers
	985	IO latch enable during I^2C write	0: disable 1: enable
	986	Reserved	
	987	Reserved	
	988	Reserved	
	989	Reserved	
	990	Reserved	
	991	Reserved	
7C	992	Matrix Input 32	I^2C_virtual_0 Input
	993	Matrix Input 33	I^2C_virtual_1 Input
	994	Matrix Input 34	I^2C_virtual_2 Input
	995	Matrix Input 35	I^2C_virtual_3 Input
	996	Matrix Input 36	I^2C_virtual_4 Input
	997	Matrix Input 37	I^2C_virtual_5 Input
	998	Matrix Input 38	I^2C_virtual_6 Input
	999	Matrix Input 39	I^2C_virtual_7 Input
7D	1000	8-bit Pattern ID Byte 0 (from NVM): ID [23:16]	
	1001		
	1002		
	1003		
	1004		
	1005		
	1006		
	1007		
7E	1008	Reserved	
	1009		
	1010		
	1011		
	1012		
	1013		
	1014		
	1015		

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
7F	1016	I^2C slave address	
	1017		
	1018		
	1019		
	1020	slave address selection bit0	0: from register [1016] 1: from Pin15
	1021	slave address selection bit1	0: from register [1017] 1: from Pin16
	1022	slave address selection bit2	0: from register [1018] 1: from Pin17
	1023	slave address selection bit3	0: from register [1019] 1: from Pin18
80	1024	Reserved	
	1025		
	1026		
	1027		
	1028		
	1029		
	1030		
	1031		
81	1032	Reserved	
	1033		
	1034		
	1035		
	1036		
	1037		
	1038	Reserved	
	1039	Reserved	
82	1040	Reserved	
	1041		
	1042		
	1043		
	1044		
	1045		
	1046	Reserved	
	1047	Reserved	
83	1048	Reserved	
	1049		
	1050		
	1051		
	1052		
	1053		
	1054	Reserved	
	1055	Reserved	

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
84	1056	Reserved	
	1057		
	1058		
	1059		
	1060		
	1061	Reserved	
	1062		
	1063		
85	1064		
	1065		
	1066	Reserved	
	1067		
	1068		
	1069		
	1070		
	1071	Reserved	
86	1072		
	1073		
	1074		
	1075		
	1076	Reserved	
	1077		
	1078		
	1079		
87	1080		
	1081	Reserved	
	1082		
	1083		
	1084		
	1085		
	1086	Reserved	
	1087		
88	1088		
	1089		
	1090		
	1091	Reserved	
	1092		
	1093		
	1094		
	1095		

Table 69: Register Map (Continued)

Address Byte	Register Bit	Signal Function	Register Bit Definition
89	1096	Reserved	
	1097		
	1098		
	1099		
	1100		
	1101	Reserved	
	1102		
	1103		
8A	1104		
	1105		
	1106	Reserved	
	1107		
	1108		
	1109		
	1110		
	1111	Reserved	
8B	1112		
	1113		
	1114		
	1115		
	1116	Reserved	
	1117	Reserved	
	1118	Reserved	
	1119	Reserved	
8C	1120		
	1121		
	1122		
	1123		
	1124	Reserved	
	1125		
	1126		
	1127		
8D	1128		
	1129	Reserved	
	1130	Reserved	
	1131		
	1132		
	1133		
	1134		
	1135	Reserved	
8E	1136		
	1137		
	1138		
	1139		
	1140	Reserved	

Table 69: Register Map (Continued)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Signal Function</th><th rowspan="2">Register Bit Definition</th></tr>
<tr><th>Byte</th><th>Register Bit</th></tr>
<tr><td rowspan="3">8E</td><td>1141</td><td rowspan="5">Reserved</td><td></td></tr>
<tr><td>1142</td><td></td></tr>
<tr><td>1143</td><td></td></tr>
<tr><td rowspan="8">8F</td><td>1144</td><td></td></tr>
<tr><td>1145</td><td></td></tr>
<tr><td>1146</td><td rowspan="5">Reserved</td><td></td></tr>
<tr><td>1147</td><td></td></tr>
<tr><td>1148</td><td></td></tr>
<tr><td>1149</td><td></td></tr>
<tr><td>1150</td><td></td></tr>
<tr><td>1151</td><td>Reserved</td><td></td></tr>
<tr><td colspan="4">SCL/SDA</td></tr>
<tr><td rowspan="4">90</td><td>1152</td><td rowspan="2">I^{2}C SCL/SDA input mode select bits
(for low voltage in purpose)</td><td rowspan="2">00: digital without Schmitt trigger
01: digital with Schmitt trigger
10: low voltage digital in
11: analog IO</td></tr>
<tr><td>1153</td></tr>
<tr><td>1154</td><td>Reserved</td><td></td></tr>
<tr><td>1155</td><td>I^{2}C mode selection</td><td>0: I^{2}C fast mode +
1: I^{2}C standard/fast mode</td></tr>
<tr><td colspan="4">IO0</td></tr>
<tr><td rowspan="4">90</td><td>1156</td><td rowspan="2">input mode configuration</td><td rowspan="2">00: digital without Schmitt Trigger
01: digital with Schmitt Trigger
10: low voltage digital in
11: analog IO</td></tr>
<tr><td>1157</td></tr>
<tr><td>1158</td><td rowspan="2">output mode configuration</td><td rowspan="2">00: Push-Pull 1x
01: Push-Pull 2x
10: 1x Open-Drain
11: 2x Open-Drain</td></tr>
<tr><td>1159</td></tr>
<tr><td rowspan="3">91</td><td>1160</td><td rowspan="2">Pull-up/down resistance selection</td><td rowspan="2">00: floating
01: 10k
10: 100k
11: 1M</td></tr>
<tr><td>1161</td></tr>
<tr><td>1162</td><td>Pull-up/down selection</td><td>0: Pull-down
1: Pull-up</td></tr>
<tr><td colspan="4">IO1</td></tr>
<tr><td rowspan="5">91</td><td>1163</td><td rowspan="2">input mode configuration</td><td rowspan="2">00: digital without Schmitt Trigger
01: digital with Schmitt Trigger
10: low voltage digital in
11: analog IO</td></tr>
<tr><td>1164</td></tr>
<tr><td>1165</td><td rowspan="2">output mode configuration</td><td rowspan="2">00: Push-Pull 1x
01: Push-Pull 2x
10: 1x Open-Drain
11: 2x Open-Drain</td></tr>
<tr><td>1166</td></tr>
<tr><td>1167</td><td rowspan="2">Pull-up/down resistance selection</td><td rowspan="2">00: floating
01: 10K
10: 100K
11: 1M</td></tr>
<tr><td rowspan="2">92</td><td>1168</td></tr>
<tr><td>1169</td><td>Pull-up/down selection</td><td>0: Pull-down
1: Pull-up</td></tr>
<tr><td colspan="4">IO2</td></tr>
</table>

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
92	1170 1171	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
92	1172 1173	output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
92	1174 1175	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
93	1176	Pull-up/down selection	0: Pull-down 1: Pull-up
IO3			
93	1177 1178	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
93	1179 1180	output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
93	1181 1182	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
93	1183	Pull-up/down selection	0: Pull-down 1: Pull-up
IO4			
94	1184 1185	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
94	1186 1187	output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
94	1188 1189	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
94	1190	Pull-up/down selection	0: Pull-down 1: Pull-up
IO5			

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
94	1191	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
95	1192		
95	1193	output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
95	1194		
95	1195	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
95	1196		
95	1197	Pull-up/down selection	0: Pull-down 1: Pull-up
IO6			
95	1198	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
95	1199		
96	1200	output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
96	1201		
96	1202	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
96	1203		
96	1204	Pull-up/down selection	0: Pull-down 1: Pull-up
I0			
96	1205	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
96	1206		
96	1207	IO fast Pull-up/down enable	0: disable 1: enable
97	1208	Reserved	
97	1209	Reserved	
97	1210	Reserved	
97	1211	Reserved	
97	1212	Reserved	
97	1213	Reserved	
97	1214	Reserved	
97	1215	Reserved	

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
98	1216	Multi0 register configure	mulit_function selection
	1217		
	1218		dly2lut selection
	1219		
	1220		output selection of 4-bit LUT1/DFF17: 0: 4-bit LUT1 1: DFF17
	1221		external clock selection
	1222		
	1223	DLY/CNT0 Mode Selection	00: DLY 01: one shoot 10: frequency detect 11: CNT register [1238] = 0
99	1224		
	1225	DLY/CNT0 edge Mode Selection	00: both edge 01: falling edge 10: rising edge 11: High Level Reset (only in CNT mode)
	1226		
	1227	DLY/CNT0 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2) 0001: 25M/4 0010: 2M(OSC1) 0011: 2M/8 0100: 2M/64 0101: 2M/512 0110: 2K(OSC0) 0111: 2K/8 1000: 2K/64 1001: 2K/512 1010: 2K/4096 1011: 2K/32768 1100: 2K/262144 1101: CNT6_END 1110: External 1111: Not used
	1228		
	1229		
	1230		
	1231	FSM0 SET/RST Selection	0: Reset to 0 1: Set to data
9A	1232	wake sleep mode selection	0: Default Mode, 1: Wake Sleep Mode (registers [1224:1223] = 11)
	1233	Wake sleep power down state selection	0: low 1: high
	1234	Keep signal sync selection	0: bypass 1: after two DFF
	1235	UP signal sync selection	0: bypass 1: after two DFF
	1236	CNT0 CNT mode SYNC selection	0: bypass 1: after two DFF
	1237	CNT0 output pol selection	0: Default Output 1: Inverted Output
	1238	CNT0 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers [1224:1223] = 00)
	1239	Reserved	

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
9B	1240	Multi1 register configure	mulit_function selection
	1241		
	1242		dly2lut selection
	1243		
	1244		output selection of 3-bit LUT7/DFF11: 0: 3-bit LUT7 1: DFF11
	1245	CNT1 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers [1251:1248] = 0000/0001/0010)
	1246	CNT1 CNT mode SYNC selection	0: bypass 1: after two DFF
	1247	CNT1 output pol selection	0: Default Output 1: Inverted Output
9C	1248	CNT1 function and edge mode selection	0000: both edge Delay 0001: falling edge delay 0010: rising edge delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1249		
	1250		
	1251		
	1252	DLY/CNT1 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2) 0001: 25M/4 0010: 2M(OSC1) 0011: 2M/8 0100: 2M/64 0101: 2M/512 0110: 2K(OSC0) 0111: 2K/8 1000: 2K/64 1001: 2K/512 1010: 2K/4096 1011: 2K/32768 1100: 2K/262144 1101: CNT0_END 1110: External 1111: Not used
	1253		
	1254		
	1255		

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
9D	1256	Multi2 register configure	mulit_function selection
	1257		
	1258		dly2lut selection
	1259		
	1260		output selection of 3-bit LUT8/DFF12: 0: 3-bit LUT8 1: DFF12
	1261	CNT2 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers [1267:1264] = 0000/0001/0010)
	1262	CNT2 CNT mode SYNC selection	0: bypass 1: after two DFF
	1263	CNT2 output pol selection	0: Default Output 1: Inverted Output
9E	1264	CNT2 function and edge mode selection	0000: both edge Delay 0001: falling edge delay 0010: rising edge delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 111: high level reset CNT
	1265		
	1266		
	1267		
9E	1268	DLY/CNT2 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2) 0001: 25M/4 0010: 2M(OSC1) 0011: 2M/8 0100: 2M/64 0101: 2M/512 0110: 2K(OSC0) 0111: 2K/8 1000: 2K/64 1001: 2K/512 1010: 2K/4096 1011: 2K/32768 1100: 2K/262144 1101: CNT1_END 1110: External 1111: Not used
	1269		
	1270		
	1271		

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
9F	1272	Multi3 register configure	mulit_function selection
	1273		
	1274		dly2lut selection
	1275		
	1276		output selection of 3-bit LUT9/DFF13: 0: 3-bit LUT9 1: DFF13
	1277	CNT3 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection(registers [1283:1280] = 0000/0001/0010)
	1278	CNT3 CNT mode SYNC selection	0: bypass; 1: after two DFF
	1279	CNT3 output pol selection	0: Default Output, 1: Inverted Output
A0	1280	CNT3 function and edge mode selection	0000: both edge Delay 0001: falling edge delay 0010: rising edge delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1281		
	1282		
	1283		
	1284	DLY/CNT3 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2) 0001: 25M/4 0010: 2M(OSC1) 0011: 2M/8 0100: 2M/64 0101: 2M/512 0110: 2K(OSC0) 0111: 2K/8 1000: 2K/64 1001: 2K/512 1010: 2K/4096 1011: 2K/32768 1100: 2K/262144 1101: CNT2_END 1110: External 1111: Not used
	1285		
	1286		
	1287		

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
A1	1288	Multi4 register configure	mulit_function selection
	1289		
	1290		dly2lut selection
	1291		
	1292		output selection of 3-bit LUT10/DFF14: 0: 3-bit LUT10 1: DFF14
	1293	CNT4 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers [1299:1296] = 0000/0001/0010)
	1294	CNT4 CNT mode SYNC selection	0: bypass 1: after two DFF
	1295	CNT4 output pol selection	0: Default Output 1: Inverted Output
A2	1296	CNT4 function and edge mode selection	0000: both edge Delay 0001: falling edge delay 0010: rising edge delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect; 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1297		
	1298		
	1299		
	1300	DLY/CNT4 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2) 0001: 25M/4 0010: 2M(OSC1) 0011: 2M/8 0100: 2M/64 0101: 2M/512 0110: 2K(OSC0) 0111: 2K/8 1000: 2K/64 1001: 2K/512 1010: 2K/4096 1011: 2K/32768 1100: 2K/262144 1101: CNT3_END 1110: External 1111: Not used
	1301		
	1302		
	1303		

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
A3	1304	Multi5 register configure	mulit_function selection
	1305		
	1306		dly2lut selection
	1307		
	1308		output selection of 3-bit LUT11/DFF15: 0: 3-bit LUT11 1: DFF15
	1309	CNT5 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers [1315:1312] = 0000/0001/0010)
	1310	CNT5 CNT mode SYNC selection	0: bypass 1: after two DFF
	1311	CNT5 output pol selection	0: Default Output 1: Inverted Output
A4	1312	CNT5 function and edge mode selection	0000: both edge Delay 0001: falling edge delay 0010: rising edge delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1313		
	1314		
	1315		
	1316	DLY/CNT5 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2) 0001: 25M/4 0010: 2M(OSC1) 0011: 2M/8 0100: 2M/64 0101: 2M/512 0110: 2K(OSC0) 0111: 2K/8 1000: 2K/64 1001: 2K/512 1010: 2K/4096 1011: 2K/32768 1100: 2K/262144 1101: CNT4_END 1110: External 1111: Not used
	1317		
	1318		
	1319		

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
A5	1320	Multi6 register configure	mulit_function selection
	1321		
	1322		dly2lut selection
	1323		
	1324		output selection of 3-bit LUT12/DFF16: 0: 3-bit LUT12 1: DFF16
	1325	CNT6 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers [1331:1328] = 0000/0001/0010)
	1326	CNT6 CNT mode SYNC selection	0: bypass 1: after two DFF
	1327	CNT6 output pol selection	0: Default Output 1: Inverted Output
A6	1328	CNT6 function and edge mode selection	0000: both edge Delay 0001: falling edge delay 0010: rising edge delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1329		
	1330		
	1331		
	1332	DLY/CNT6 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2) 0001: 25M/4 0010: 2M(OSC1) 0011: 2M/8 0100: 2M/64 0101: 2M/512 0110: 2K(OSC0) 0111: 2K/8 1000: 2K/64 1001: 2K/512 1010: 2K/4096 1011: 2K/32768 1100: 2K/262144 1101: CNT5_END 1110: External 1111: Not used
	1333		
	1334		
	1335		

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
A7	1336	CNT0 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1337		
	1338	CNT1 initial value selection	00:bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1339		
	1340	CNT6 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1341		
	1342	Reserved	
	1343	Reserved	
A8	1344	CNT2 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1345		
	1346	CNT3 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1347		
	1348	CNT4 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1349		
	1350	CNT5 initial value selection	00:bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1351		
A9	1352	Multi0 4-bit LUT_DFF setting	<12:0>:4-bit LUT1 <12:0>
	1353		
	1354		
	1355		
	1356		
	1357		
	1358		
	1359		
AA	1360		
	1361		
	1362		
	1363		
	1364		
	1365		<13>:4-bit LUT1 <13>/DFF17 Initial Polarity Select 0: Low, 1: High
	1366		<14>:4-bit LUT1 <14>/DFF17 Output Select 0: Q output, 1: QB output
	1367		<15>:4-bit LUT1 <15>/DFF17 or Latch Select 0: DFF function, 1: Latch function

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
AB	1368	REG_CNT0_D<15:0>	Data[15:0]
	1369		
	1370		
	1371		
	1372		
	1373		
	1374		
	1375		
AC	1376		
	1377		
	1378		
	1379		
	1380		
	1381		
	1382		
	1383		
AD	1384	Multi1_3-bit_LUT_DFF setting	<3:0>:3-bit LUT7 <3:0>
	1385		
	1386		
	1387		
	1388		<4>:3-bit LUT7 <4>/DFF11 Initial Polarity Select 0: Low, 1: High
	1389		<5>:3-bit LUT7 <5>/DFF11 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1390		<6>:3-bit LUT7 <6>/DFF11 Output Select 0: Q output, 1: QB output
	1391		<7>:3-bit LUT7 <7>/DFF11 or Latch Select 0: DFF function, 1: Latch function
Multi1_CNT1			
AE	1392	REG_CNT1_D<7:0>	Data[7:0]
	1393		
	1394		
	1395		
	1396		
	1397		
	1398		
	1399		
AF	1400	Multi2 3-bit LUT_DFF setting	<3:0>:3-bit LUT8 <3:0>
	1401		
	1402		
	1403		
	1404		<4>:3-bit LUT8 <4>/DFF12 Initial Polarity Select 0: Low, 1: High
	1405		<5>:3-bit LUT8 <5>/DFF12 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1406		<6>:3-bit LUT8 <6>/DFF12 Output Select 0: Q output, 1: QB output
	1407		<7>:3-bit LUT8 <7>/DFF12 or Latch Select 0: DFF function, 1: Latch function

Table 69: Register Map (Continued)

Address: Byte	Address: Register Bit	Signal Function	Register Bit Definition
B0	1408	REG_CNT2_D<7:0>	Data[7:0]
	1409		
	1410		
	1411		
	1412		
	1413		
	1414		
	1415		
B1	1416	Multi3_3-bit_LUT_DFF setting	<3:0>:3-bit LUT9 <3:0>
	1417		
	1418		
	1419		
	1420		<4>:3-bit LUT9 <4>/DFF13 Initial Polarity Select 0: Low, 1: High
	1421		<5>:3-bit LUT9 <5>/DFF13 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1422		<6>:3-bit LUT9 <6>/DFF13 Output Select 0: Q output, 1: QB output
	1423		<7>:3-bit LUT9 <7>/DFF13 or Latch Select 0: DFF function, 1: Latch function
B2	1424	REG_CNT3_D<7:0>	Data[7:0]
	1425		
	1426		
	1427		
	1428		
	1429		
	1430		
	1431		
B3	1432	Multi4_3-bit_LUT_DFF setting	<3:0>:3-bit LUT10 <3:0>
	1433		
	1434		
	1435		
	1436		<4>:3-bit LUT10 <4>/DFF14 Initial Polarity Select 0: Low, 1: High
	1437		<5>:3-bit LUT10 <5>/DFF14 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1438		<6>:3-bit LUT10 <6>/DFF14 Output Select 0: Q output, 1: QB output
	1439		<7>:3-bit LUT10 <7>/DFF14 or Latch Select 0: DFF function, 1: Latch function
B4	1440	REG_CNT4_D<7:0>	Data[7:0]
	1441		
	1442		
	1443		
	1444		
	1445		
	1446		
	1447		

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
B5	1448	Multi5_3-bit LUT_DFF setting	<3:0>:3-bit LUT11<3:0>
	1449		
	1450		
	1451		
	1452		<4>:3-bit LUT11<4>/DFF15 Initial Polarity Select 0: Low, 1: High
	1453		<5>:3-bit LUT11 <5>/DFF15 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1454		<6>:3-bit LUT11 <6>/DFF15 Output Select 0: Q output, 1: QB output
	1455		<7>:3-bit LUT11 <7>/DFF15 or Latch Select 0: DFF function, 1: Latch function
B6	1456	REG_CNT5_D<7:0>	Data[7:0]
	1457		
	1458		
	1459		
	1460		
	1461		
	1462		
	1463		
B7	1464	Multi6_3-bit_LUT_DFF setting	<3:0>:3-bit LUT12 <3:0>
	1465		
	1466		
	1467		
	1468		<4>:3-bit LUT12 <4>/DFF16 Initial Polarity Select 0: Low, 1: High
	1469		<5>:3-bit LUT12 <5>/DFF16 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1470		<6>:3-bit LUT12 <6>/DFF16 Output Select 0: Q output, 1: QB output
	1471		<7>:3-bit LUT12 <7>/DFF16 or Latch Select 0: DFF function, 1: Latch function
B8	1472	REG_CNT6_D<7:0>	Data[7:0]
	1473		
	1474		
	1475		
	1476		
	1477		
	1478		
	1479		

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
B9	1480	2-bit LUT0/DFF0 setting	<0>:2-bit LUT0 <0>
	1481		<1>:2-bit LUT0 <1>/DFF0 Initial Polarity Select 0: Low, 1: High
	1482		<2>:2-bit LUT0 <2>/DFF0 Output Select 0: Q output, 1: QB output
	1483		<3>:2-bit LUT0 <3>/DFF0 or Latch Select 0: DFF function, 1: Latch function
	1484	2-bit LUT1/DFF1 setting	<0>:2-bit LUT0 <0>
	1485		<1>:2-bit LUT0 <1>/DFF0 Initial Polarity Select 0: Low, 1: High
	1486		<2>:2-bit LUT0 <2>/DFF0 Output Select 0: Q output, 1: QB output
	1487		<3>:2-bit LUT0 <3>/DFF0 or Latch Select 0: DFF function, 1: Latch function
BA	1488	2-bit LUT2/DFF2 setting	<0>:2-bit LUT0 <0>
	1489		<1>:2-bit LUT0 <1>/DFF0 Initial Polarity Select 0: Low, 1: High
	1490		<2>:2-bit LUT0 <2>/DFF0 Output Select 0: Q output, 1: QB output
	1491		<3>:2-bit LUT0 <3>/DFF0 or Latch Select 0: DFF function, 1: Latch function
	1492	2-bit LUT0 or DFF0 Select	0: 2-bit LUT0 1: DFF0
	1493	2-bit LUT1 or DFF1 Select	0: 2-bit LUT1 1: DFF1
	1494	2-bit LUT2 or DFF2 Select	0: 2-bit LUT2 1: DFF2
	1495	Reserved	
BB	1496	PGen data	PGen Data[15:0]
	1497		
	1498		
	1499		
	1500		
	1501		
	1502		
	1503		
BC	1504		
	1505		
	1506		
	1507		
	1508		
	1509		
	1510		
	1511		

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
BD	1512	2-bit LUT3_VAL or PGen_data	2-bit LUT3<3:0> or PGen 4bit counter data<3:0>
	1513		
	1514		
	1515		
	1516	2-bit LUT3 or PGen Select	0: 3-bit LUT3 1: PGen
	1517	Active level selection for RST/SET	0: Active low level reset/set 1: Active high level reset/set
	1518	3-bit LUT0 or DFF3 Select	0: 3-bit LUT0 1: DFF3
	1519	3-bit LUT1 or DFF4 Select	0: 3-bit LUT1 1: DFF4
BE	1520	3-bit LUT0_DFF3 setting	<1:0>: 3-bit LUT0 <1:0>
	1521		
	1522		<2>: 3-bit LUT0 <2>/DFF3 stage selection 0: Q of first DFF; 1 Q of second DFF
	1523		<3>:3-bit LUT0 <3>/DFF3 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	1524		<4>:3-bit LUT0 <4>/DFF3 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1525		<5>:3-bit LUT0 <5>/DFF3 Initial Polarity Select 0: Low, 1: High
	1526		<6>:3-bit LUT0 <6>/DFF3 Output Select 0: Q output, 1: QB output
	1527		<7>:3-bit LUT0 <7>/DFF3 or Latch Select 0: DFF function, 1: Latch function
BF	1528	3-bit LUT1_DFF4 setting	<2:0>: 3-bit LUT1 <2:0>
	1529		
	1530		
	1531		<3>:3-bit LUT1 <3>/DFF4 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	1532		<4>:3-bit LUT1 <4>/DFF4 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1533		<5>:3-bit LUT1 <5>/DFF4 Initial Polarity Select 0: Low, 1: High
	1534		<6>:3-bit LUT1 <6>/DFF4 Output Select 0: Q output, 1: QB output
	1535		<7>:3-bit LUT1 <7>/DFF4 or Latch Select 0: DFF function, 1: Latch function

Table 69: Register Map (Continued)

Address Byte	Register Bit	Signal Function	Register Bit Definition
C0	1536	Rheostat0 data selection	0000000000: 0 ~ 1111111111:100k
	1537		
	1538		
	1539		
	1540		
	1541		
	1542		
	1543		
C1	1544		
	1545		
	1546	Reserved	
	1547	Reserved	
	1548	Reserved	
	1549	Reserved	
	1550	Reserved	
	1551	Reserved	
C2	1552	Rheostat0 current value (read only)	
	1553		
	1554		
	1555		
	1556		
	1557		
	1558		
	1559		
C3	1560		
	1561		
	1562	Reserved	
	1563	Reserved	
	1564	Reserved	
	1565	Reserved	
	1566	Reserved	
	1567	Reserved	
C4	1568	Matrix Input 0	GND
	1569	Matrix Input 1	2-bit LUT0/DFF0 output
	1570	Matrix Input 2	2-bit LUT1/DFF1 output
	1571	Matrix Input 3	2-bit LUT2/DFF2 output
	1572	Matrix Input 4	2-bit LUT3/PGen output
	1573	Matrix Input 5	3-bit LUT0/DFF3 output
	1574	Matrix Input 6	3-bit LUT1/DFF4 output
	1575	Matrix Input 7	3-bit LUT2/DFF5 output
C5	1576	Matrix Input 8	3-bit LUT3/DFF6 output
	1577	Matrix Input 9	3-bit LUT4/DFF7 output
	1578	Matrix Input 10	3-bit LUT5/DFF8 output
	1579	Matrix Input 11	3-bit LUT6/DFF9 output
	1580	Matrix Input 12	CNT_DLY0 output
	1581	Matrix Input 13	MLT0 4-bit LUT1/DFF17_OUT
	1582	Matrix Input 14	CNT_DLY1 output
	1583	Matrix Input 15	MLT1 3-bit LUT7/DFF11_OUT

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
C6	1584	Matrix Input 16	CNT_DLY2 output
	1585	Matrix Input 17	MLT2 3-bit LUT8/DFF12_OUT
	1586	Matrix Input 18	CNT_DLY3 output
	1587	Matrix Input 19	MLT3 3-bit LUT9/DFF13_OUT
	1588	Matrix Input 20	CNT_DLY4 output
	1589	Matrix Input 21	MLT4 3-bit LUT10/DFF14_OUT
	1590	Matrix Input 22	CNT_DLY5 output
	1591	Matrix Input 23	MLT5 3-bit LUT11/DFF15_OUT
C7	1592	Matrix Input 24	CNT_DLY6 output
	1593	Matrix Input 25	MLT6 3-bit LUT12/DFF16_OUT
	1594	Matrix Input 26	3-bit LUT13/Pipe Delay/RippleCNT_out0
	1595	Matrix Input 27	Pipe Delay/RippleCNT_out1
	1596	Matrix Input 28	Pipe Delay/RippleCNT_out2
	1597	Matrix Input 29	4-bit LUT0/DFF10 output
	1598	Matrix Input 30	Programmable Delay Edge Detect Output
	1599	Matrix Input 31	Edge Detect Filter Output
C8	1600	Matrix Input 40	RH0 Idle/Active
	1601	Matrix Input 41	RH1 Idle/Active
	1602	Matrix Input 42	Output of Op Amp0 in ACMP mode
	1603	Matrix Input 43	Output of Op Amp1 in ACMP mode
	1604	Matrix Input 44	IO0 Digital Input
	1605	Matrix Input 45	IO1 Digital Input
	1606	Matrix Input 46	IO2 Digital Input
	1607	Matrix Input 47	IO3 Digital Input
C9	1608	Matrix Input 48	IO4 Digital Input
	1609	Matrix Input 49	IO5 Digital Input
	1610	Matrix Input 50	IO6 Digital Input
	1611	Matrix Input 51	I0 Digital Input
	1612	Matrix Input 52	Oscillator0 output 0
	1613	Matrix Input 53	Oscillator1 output 0
	1614	Matrix Input 54	Oscillator2 output
	1615	Matrix Input 55	Chopper ACMP Out
CA	1616	Matrix Input 56	ACMP0 Output (low speed)
	1617	Matrix Input 57	ACMP1 Output (low speed)
	1618	Matrix Input 58	Oscillator0 output 1
	1619	Matrix Input 59	Oscillator1 output 1
	1620	Matrix Input 60	POR OUT
	1621	Matrix Input 61	V_{DD}
	1622	Matrix Input 62	V_{DD}
	1623	Matrix Input 63	V_{DD}

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
CB	1624	CNT0_Q	
	1625		
	1626		
	1627		
	1628		
	1629		
	1630		
	1631		
CC	1632		
	1633		
	1634		
	1635		
	1636		
	1637		
	1638		
	1639		
CD	1640	CNT5_Q	
	1641		
	1642		
	1643		
	1644		
	1645		
	1646		
	1647		
CE	1648	CNT6_Q	
	1649		
	1650		
	1651		
	1652		
	1653		
	1654		
	1655		
CF	1656	Reserved	
	1657	Reserved	
	1658	Reserved	
	1659	Reserved	
	1660	Reserved	
	1661	Reserved	
	1662	Reserved	
	1663	Reserved	

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
D0	1664	Rheostat1 data selection	0000000000: 0 ~ 1111111111:100k
	1665		
	1666		
	1667		
	1668		
	1669		
	1670		
	1671		
D1	1672		
	1673		
	1674	Reserved	
	1675	Reserved	
	1676	Reserved	
	1677	Reserved	
	1678	Reserved	
	1679	Reserved	
D2	1680	Rheostat1 current value (read only)	
	1681		
	1682		
	1683		
	1684		
	1685		
	1686		
	1687		
D3	1688		
	1689		
	1690	Reserved	
	1691	Reserved	
	1692	Reserved	
	1693	Reserved	
	1694	Reserved	
	1695	Reserved	
D4	1696	Reserved	
	1697	Reserved	
	1698	Reserved	
	1699	Reserved	
	1700	Reserved	
	1701	Reserved	
	1702	Reserved	
	1703	Reserved	
D5	1704	Reserved	
	1705	Reserved	
	1706	Reserved	
	1707	Reserved	
	1708	Reserved	
	1709	Reserved	
	1710	Reserved	
	1711	Reserved	

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
D6	1712	Reserved	
	1713	Reserved	
	1714	Reserved	
	1715	Reserved	
	1716	Reserved	
	1717	Reserved	
	1718	Reserved	
	1719	Reserved	
D7	1720	Reserved	
	1721	Reserved	
	1722	Reserved	
	1723	Reserved	
	1724	Reserved	
	1725	Reserved	
	1726	Reserved	
	1727	Reserved	
D8	1728	Reserved	
	1729	Reserved	
	1730	Reserved	
	1731	Reserved	
	1732	Reserved	
	1733	Reserved	
	1734	Reserved	
	1735	Reserved	
D9	1736	Reserved	
	1737	Reserved	
	1738	Reserved	
	1739	Reserved	
	1740	Reserved	
	1741	Reserved	
	1742	Reserved	
	1743	Reserved	
DA	1744	Reserved	
	1745	Reserved	
	1746	Reserved	
	1747	Reserved	
	1748	Reserved	
	1749	Reserved	
	1750	Reserved	
	1751	Reserved	
DB	1752	Reserved	
	1753	Reserved	
	1754	Reserved	
	1755	Reserved	
	1756	Reserved	
	1757	Reserved	
	1758	Reserved	
	1759	Reserved	

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
DC	1760	Reserved	
	1761	Reserved	
	1762	Reserved	
	1763	Reserved	
	1764	Reserved	
	1765	Reserved	
	1766	Reserved	
	1767	Reserved	
DD	1768	ID[24]: Reserved	
	1769	ID[25]: Reserved	Reserved for NVM Power-Up Check Pattern Status (A55A match from Flag)
	1770	ID[27:26]: Reserved for Silicon Identification Service Bits (metal hard code)	
	1771		
	1772	Reserved	
	1773		
	1774		
	1775		
DE	1776	Reserved	
	1777		
	1778		
	1779		
	1780		
	1781		
	1782		
	1783		
DF	1784	Reserved	
	1785		
	1786		
	1787		
	1788		
	1789		
	1790		
	1791		
E0	1792	RPR<1:0> (2k register read selection bits)	00: 2k register data is unprotected for read 01: 2k register data is partly protected for read 10: 2k register data is fully protected for read 11: reserved
	1793		
	1794	RPR<3:2> (2k register write selection bits)	00: 2k register data is unprotected for write 01: 2k register data is partly protected for write 10: 2k register data is fully protected for write 11: reserved
	1795		
	1796	RH_PRB	0: Rheostat Program Input from matrix enabled 1: Rheostat Program Input from matrix disabled
	1797	Reserved	
	1798	Reserved	
	1799	Reserved	

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
E1	1800	NPR<1:0> (2k NVM configuration selection bits)	00: 2k NVM Configuration data is unprotected for read and write/erase 01: 2k NVM Configuration data is fully protected for read 10: 2k NVM Configuration data is fully protected for write/erase 11: 2k NVM Configuration data is fully protected for read and write/erase
	1801		
	1802	NPR<3:2> (Rheostat0 NVM configuration selection bits)	00: Rheosta0 NVM Configuration data is unprotected for read and write/erase 01: Rheosta0 NVM Configuration data is fully protected for read 10: Rheosta0 NVM Configuration data is fully protected for write/erase 11: Rheosta0 NVM Configuration data is fully protected for read and write/erase
	1803		
	1804	NPR<5:4> (Rheostat1 NVM configuration selection bits)	00: Rheosta1 NVM Configuration data is unprotected for read and write/erase 01: Rheosta1 NVM Configuration data is fully protected for read 10: Rheosta1 NVM Configuration data is fully protected for write/erase 11: Rheosta1 NVM Configuration data is fully protected for read and write/erase
	1805		
	1806	Reserved	
	1807	Reserved	
E2	1808	WPR<1:0> (EEPROM Write protect block bits range: page31~16)	00: Upper 1/4 (page16~19) of EEPROM is write protected (default) 01: Upper 2/4 (page16~23) of EEPROM is write protected 10: Upper 3/4 (page16~27) of EEPROM is write protected 11: Entire (page16~31) EEPROM is write protected
	1809		
	1810	WPRE (EEPROM Write protect register enable)	0: No Software Write Protection enabled (default) 1: Write Protection is set by the state of the WPR<1:0> bits
	1811	Reserved	
	1812	Reserved	
	1813	Reserved	
	1814	Reserved	
	1815	Reserved	
E3	1816	ERSE<4:0> (Page selection for erase)	Define the page address which will be erased ERSE<4> = 0 corresponds to the upper 2k NVM used for chip configuration ERSE<4> = 1 corresponds to the 2k EEPROM
	1817		
	1818		
	1819		
	1820		
	1821	ERSE <2:0> (Erase enable)	000/001/010/011/100/101/111: erase disable 110: cause the NVM erase: full NVM (4k bits) erase for ERSCHIP = 1 if DIS_ERSCHIP=0 or page erase for ERSCHIP=0.
	1822		
	1823		
E4	1824	PRL (Protection lock)	0: RPR/WPR/NPR setting can be changed 1: RPR/WPR/NPR setting cannot be changed
	1825	Reserved	
	1826	Reserved	
	1827	Reserved	
	1828	Reserved	
	1829	Reserved	
	1830	Reserved	
	1831	Reserved	

Table 69: Register Map (Continued)

Address: Byte	Address: Register Bit	Signal Function	Register Bit Definition
E5	1832	Reserved	
	1833		
	1834		
	1835		
	1836		
	1837		
	1838		
	1839		
E6	1840	Rheostat0 tolerance data <0>	
	1841	Rheostat0 tolerance data <1>	
	1842	Rheostat0 tolerance data <2>	
	1843	Rheostat0 tolerance data <3>	
	1844	Rheostat0 tolerance data <4>	
	1845	Rheostat0 tolerance data <5>	
	1846	Rheostat0 tolerance data <6>	
	1847	Rheostat0 tolerance data <7>	
E7	1848	Rheostat0 tolerance data <8>	
	1849	Rheostat0 tolerance data <9>	
	1850	Rheostat0 tolerance data <10>	
	1851	Rheostat0 tolerance data <11>	
	1852	Rheostat0 tolerance data <12>	
	1853	Rheostat0 tolerance data <13>	
	1854	Rheostat0 tolerance data <14>	
	1855	Sign of Rheostat0 tolerance data	0: “+” 1: "-"
E8	1856	Rheostat1 tolerance data <0>	
	1857	Rheostat1 tolerance data <1>	
	1858	Rheostat1 tolerance data <2>	
	1859	Rheostat1 tolerance data <3>	
	1860	Rheostat1 tolerance data <4>	
	1861	Rheostat1 tolerance data <5>	
	1862	Rheostat1 tolerance data <6>	
	1863	Rheostat1 tolerance data <7>	
E9	1864	Rheostat1 tolerance data <8>	
	1865	Rheostat1 tolerance data <9>	
	1866	Rheostat1 tolerance data <10>	
	1867	Rheostat1 tolerance data <11>	
	1868	Rheostat1 tolerance data <12>	
	1869	Rheostat1 tolerance data <13>	
	1870	Rheostat1 tolerance data <14>	
	1871	Sign of Rheostat1 tolerance data	0: "+"; 1: "-"
EA	1872	Reserved	
	1873		
	1874		
	1875		

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
EA	1876	Reserved	
	1877		
	1878		
	1879		
EB	1880	Reserved	
	1881		
	1882		
	1883		
	1884	Reserved	
	1885	Reserved	
	1886	Reserved	
	1887	Reserved	
EC	1888	Reserved	
	1889	Reserved	
	1890	Reserved	
	1891	Reserved	
	1892	Reserved	
	1893	Reserved	
	1894	Reserved	
	1895	Reserved	
ED	1896	Reserved	
	1897	Reserved	
	1898	Reserved	
	1899	Reserved	
	1900	Reserved	
	1901	Reserved	
	1902	Reserved	
	1903	Reserved	
EE	1904	Reserved	
	1905	Reserved	
	1906	Reserved	
	1907	Reserved	
	1908	Reserved	
	1909	Reserved	
	1910	Reserved	
	1911	Reserved	
EF	1912	Reserved	
	1913	Reserved	
	1914	Reserved	
	1915	Reserved	
	1916	Reserved	
	1917	Reserved	
	1918	Reserved	
	1919	Reserved	

Table 69: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
F0	1920	Reserved	
	1921		
	1922		
	1923		
	1924		
	1925		
	1926		
	1927		
F1	1928	Reserved	
	1929		
	1930		
	1931		
	1932		
	1933		
	1934		
	1935		
F2	1936	Reserved	
	1937		
	1938		
	1939		
	1940		
	1941		
	1942		
	1943		
F3	1944	Service page lock bit	0: Service page can be changed 1: Service page is locked
	1945	BG Chopper off	0: chopper enable 1: chopper off
	1946	Reserved	
	1947	Reserved	
	1948	BG register power down	0: power on 1: power off
	1949	Reserved	
	1950	Reserved	
	1951	Reserved	
F4	1952	Reserved	
	1953	Reserved	
	1954	Reserved	
	1955	Reserved	
	1956	Reserved	
	1957	Reserved	
	1958	Reserved	
	1959	Reserved	

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
F5	1960	Reserved	
	1961	Reserved	
	1962	Reserved	
	1963	Reserved	
	1964	Reserved	
	1965	Reserved	
	1966	Reserved	
	1967	Reserved	
F6	1968	I^2C write mask bits	0: overwrite; 1: mask the bit which set to high
	1969		
	1970		
	1971		
	1972		
	1973		
	1974		
	1975		
F7	1976	Reserved	
	1977		
	1978		
	1979		
	1980		
	1981		
	1982		
	1983		
F8	1984	Reserved	
	1985		
	1986		
	1987		
	1988		
	1989		
	1990		
	1991		
F9	1992	Reserved	
	1993		
	1994		
	1995		
	1996		
	1997		
	1998		
	1999	Reserved	

Table 69: Register Map (Continued)

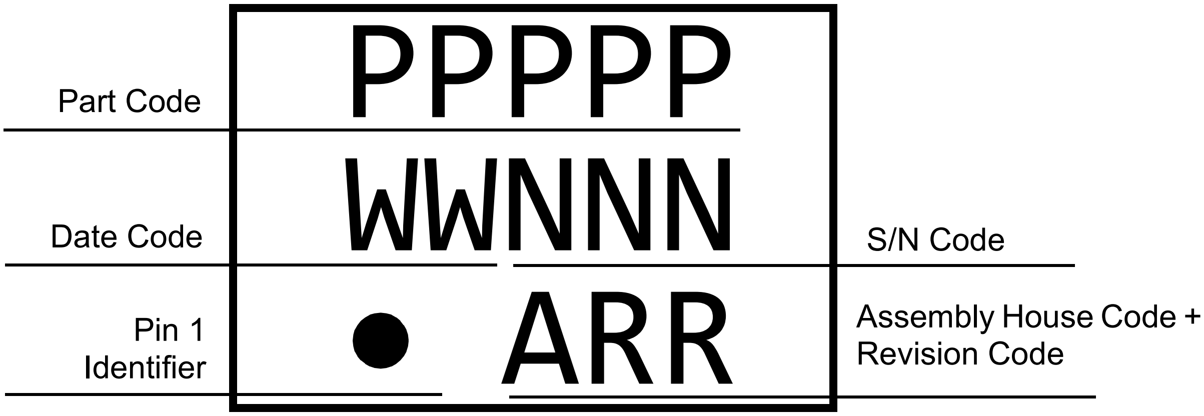
Address		Signal Function	Register Bit Definition
Byte	Register Bit		
FA	2000	Reserved	
	2001		
	2002		
	2003		
	2004		
	2005	Reserved	
	2006	Reserved	
	2007	Reserved	
FB	2008	Reserved	
	2009		
	2010		
	2011		
	2012		
	2013	Reserved	
	2014	Reserved	
	2015	Reserved	
FC	2016	Reserved	
	2017		
	2018		
	2019		
	2020		
	2021	Reserved	
	2022	Reserved	
	2023	Reserved	
FD	2024	Reserved	
	2025		
	2026		
	2027		
	2028		
	2029	Reserved	
	2030	Reserved	
	2031	Reserved	
FE	2032	Reserved	
	2033		
	2034		
	2035		
	2036		
	2037	Reserved	
	2038	Reserved	
	2039	Reserved	

Table 69: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
FF	2040	Reserved	
	2041	Reserved	
	2042	Reserved	
	2043	Reserved	
	2044	Reserved	
	2045	Reserved	
	2046	Reserved	
	2047	Reserved	

22 Package Top Marking System Definition

22.1 STQFN-24L 3 MM X 3 MM X 0.55 MM, 0.4P FCD PACKAGE

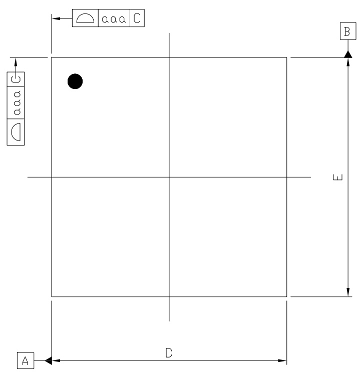


23 Package Information

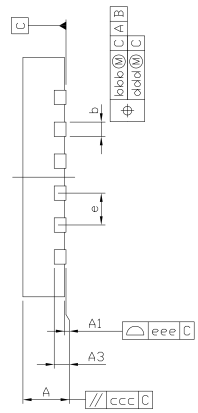
23.1 PACKAGE OUTLINES FOR STQFN 24L 3 MM X 3 MM X 0.55 MM 0.4P GREEN PACKAGE

JEDEC MO-220

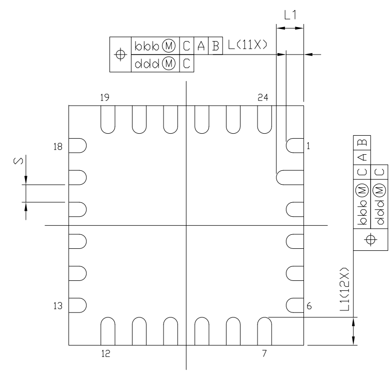
IC Net Weight: 0.0116 g



Top View



Side View



Bottom View

PKG CODE	UQFN					
SYMBOLS	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.10	0.15	0.20	0.004	0.006	0.008
b	0.13	0.18	0.23	0.005	0.007	0.009
D	2.95	3.00	3.05	0.116	0.118	0.120
E	2.95	3.00	3.05	0.116	0.118	0.120
e	0.40 BSC			0.016 BSC		
L	0.175	0.225	0.275	0.007	0.009	0.011
L1	0.30	0.35	0.40	0.012	0.014	0.016
S	0.22 REF.			0.009 REF.		
aaa	0.07			0.003		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		

"A1" MAX LEAD COPLANARITY 0.05mm

STANDARD TOLERANCE : ±0.05

PAD SIZE	LEAD FINISH		JEDEC CODE
	Pure Tin	PPF	
	V	X	N/A

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

23.2 STQFN HANDLING

Be sure to handle STQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle STQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

23.3 SOLDERING INFORMATION

Please see IPC/JEDEC J-STD-020: for relevant soldering information. More information can be found at www.jedec.org.

24 Ordering Information

Part Number	Type
SLG47004V	24-pin STQFN
SLG47004VTR	24-pin STQFN - Tape and Reel (5k units)

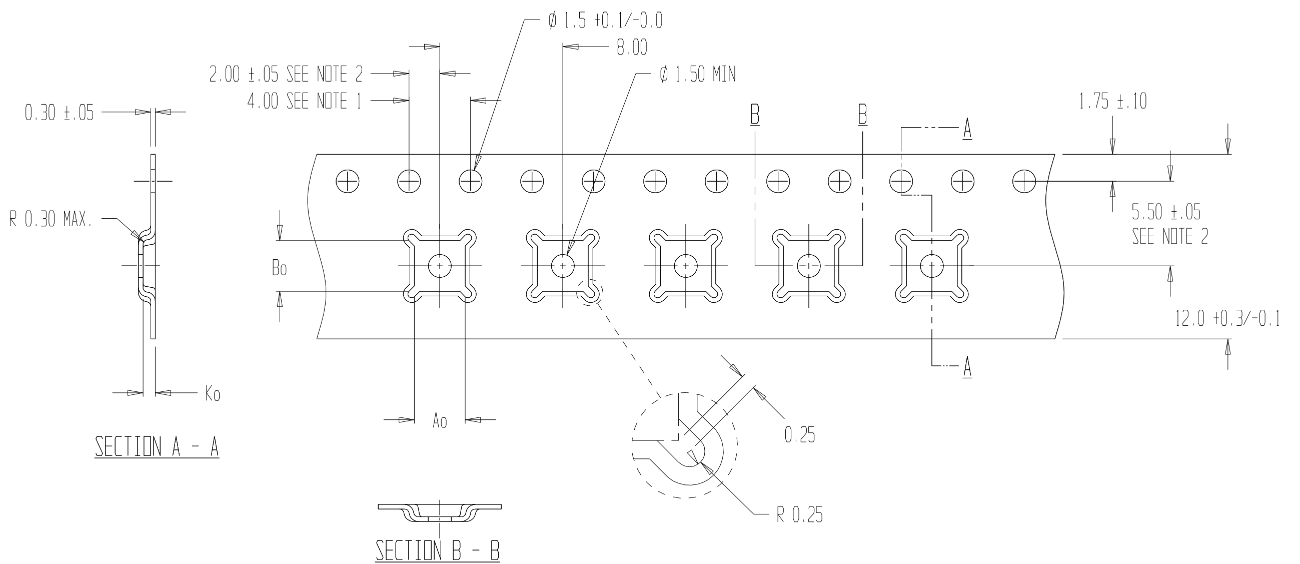
Note 1 Use SLG47004V to order. Shipments are automatically in Tape and Reel.
Note 2 "TR" suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

24.1 TAPE AND REEL SPECIFICATIONS

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
STQFN 24L 3 mm x3 mm 0.4P FC Green	24	3 x 3 x 0.55	5.000	10.000	330 / 100	42	336	42	336	12	8

24.2 CARRIER TAPE DRAWING AND DIMENSIONS

Package Type	PocketBTM Length (mm)	PocketBTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 24L 3 mm x3 mm 0.4P FC Green	3.3	3.3	0.8	4	8	1.55	1.75	5.5	12



Notes:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
3. A0 AND B0 ARE CALCULATED ON A PLANE AT A DISTANCE “R” ABOVE THE BOTTOM OF THE POCKET.

Note: Orientation in carrier: Pin1 is at upper left corner (Quadrant1).

25 Layout Guidelines

SLG47004 has two analog supply pins and two ground pins: V_{DD}, V_{DDA}, GND and AGND. Separating analog supply voltage from digital one helps to minimize noise generated by the digital part of IC.

Analog supply voltage domain: operational amplifiers, charge pumps for op amps, charge pumps for Oscillators, bias generators and regulators for op amps, digital rheostats, Chopper ACMP, HD Buffer, Vref of op amp and HD Buffer, Low Power Bandgap.

Digital supply voltage domain: ACMPs, Vref of ACMPs, Vref output buffers, Oscillator 0, Oscillator 1, Oscillator 2, I^2C macrocell, NVM logic, Multi-function and Combination Function macrocells.

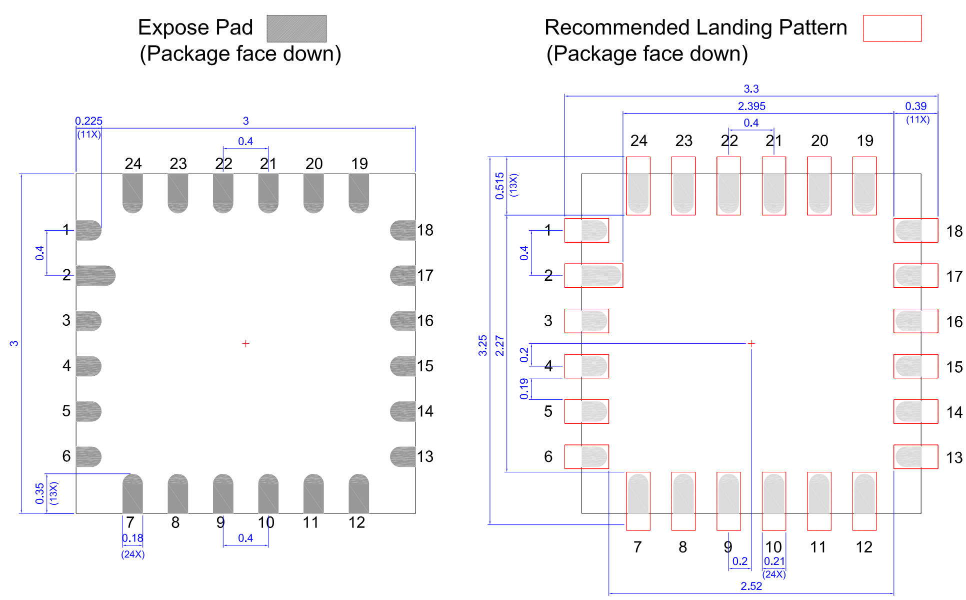
Analog and digital grounds must be connected together on the PCB board. The place of connection depends on users schematic. For application cases with low digital current of SLG47004, both AGND and GND should be connected to analog ground plane.

It is strongly recommended to connect I0 (Pin21) to the ground if it is not used in the project.

The following suggestions allow to minimize the impact of digital blocks operation on the analog macrocells:

- decrease the slew rate of input digital signals
- use proper grounding. If possible, use grounding polygons along the input/output digital traces
- to interface digital signals first use IO1, IO2, IO3, IO4, then use other GPIOs.

25.1 STQFN 24L 3 MM X 3 MM X 0.55 MM 0.4P GREEN PACKAGE



Glossary

A

ACK	Acknowledge bit
ACMP	Analog Comparator
ACMPH	Analog Comparator High Speed
ACMPL	Analog Comparator Low Power
AS	Analog Switch

B

BG	Bandgap

C

CLK	Clock
CMO	Connection matrix output
CNT	Counter

D

DFF	D Flip-Flop
DI	Digital Input
DILV	Low Voltage Digital Input
DLY	Delay
DNL	Differential Non-Linearity
DR	Digital Rheostat

E

EC	Electrical Characteristics
ERSE	Erase Enable
ERSR	Erase Register
ESD	Electrostatic discharge
EV	End Value

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

I

IN	Input

In Amp	Instrumentation Amplifier
DNL	Differential Non-Linearity
INL	Integral Non-Linearity
IO	Input/Output

L

LPF	Low Pass Filter
LSB	Least Significant Bit
LUT	Look Up Table
LV	Low Voltage

M

MSB	Most Significant Bit
MTP	Multiple-Time-Programmable
MUX	Multiplexer

N

NPR	Non-Volatile Memory Read/Write/Erase Protection
nRST	Reset
NVM	Non-Volatile Memory

O

OA	Operational Amplifier
OD	Open-Drain
OE	Output Enable
Op Amp	Operational Amplifier
OSC	Oscillator
OUT	Output

P

PD	Power-down
PGen	Pattern Generator
POR	Power-On Reset
PP	Push-Pull
PRL	Protect Lock Bit
PT	Programmable Trim
PWR	Power
P DLY	Programmable Delay

R

RPR	Register Read/Write Protection

RPRB	Register Read/Write Protection Bit
RPRL	Register Protection Read/Write/Erase Lock
R/W	Read/Write

S

SCL	I^2C Clock Input
SDA	I^2C Data Input/Output
SLA	Slave Address
SMT	With Schmitt Trigger
SPST	Single-pole/Single throw
SV	nSET Value

T

TS	Temperature Sensor

V

Vref	Voltage Reference

W

WOSMT	Without Schmitt Trigger
WPB	Write Protect Bit
WPR	Write Protection Register
WPRE	Write Protect Enable
WS	Wake and Sleep Controller

Revision History

Revision	Date	Description
3.9	19-Nov-2024	Corrected LUTs naming Corrected Programmable Trim Blocks and Digital Rheostat's Internal Circuit Corrected I^2C General Timing Characteristics figure Corrected I^2C Pins Timing Characteristics Replaced graph OA1 Open Loop Gain and Phase vs. Frequency for BW = 8 MHz
3.8	10-Oct-2024	Corrected Input Voltage Noise value in table EC of OA
3.7	1-Jul-2024	Updated subsection Changing Rheostat Value Directly via I^2C Fixed typos
3.6	6-Feb-2024	Updated registers [1007:1000] Updated figure Typical Implementation of Voltage Regulator (A) and Current Sources (B, C) Fixed typos
3.5	27-Sep-2023	Added Note 3 to section Wake and Sleep Controller Updated table Erase Register Bit Function Description Updated TS equations Fixed typos
3.4	3-Apr-2023	Updated R_{PULL} in section Electrical Characteristics Corrected Figure Reset Command Timing
3.3	1-Mar-2023	Added notes to section Ordering Information
3.2	23-Jan-2023	Corrected $BWDT_{CAP}$ parameter in table 100K Digital Rheostat Characteristics
3.1	21-Sept-2022	Updated parameter V_{OFFSET} in table Programmable Operational Amplifier Characteristics
3.0	8-Sept-2022	Final version

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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