SLG46826

GreenPAK Programmable Mixed-Signal Matrix with In-System Programmability

General Description

The SLG46826 provides a small, low power component for commonly used Mixed-Signal functions. The user creates the circuit design by programming the multiple time Non-Volatile Memory (NVM) to configure the interconnect logic, the IOs, and the macrocells of the SLG46826. Dual power supply allows to flexibly interface two independent voltage domains.This highly versatile device allows a wide variety of Mixed-Signal functions to be designed within a very small, low power single integrated circuit.

Key Features

- Two High Speed General Purpose Rail-to-Rail Analog Comparators (ACMPxH)
- Two Low Power General Purpose Rail-to-Rail Analog Comparators (ACMPxL)
- Two Voltage References
  - Two Vref Outputs
- Eleven Combination Function Macrocells
  - Three Selectable DFF/LATCH or 2-bit LUTs
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Six Selectable DFF/LATCH or 3-bit LUTs
  - One Selectable Pipe Delay or Ripple Counter or 3-bit LUT
- Eight Multi-Function Macrocells
  - Seven Selectable DFF/LATCH or 3-bit LUTs + 8-bit Delay/Counters
  - One Selectable DFF/LATCH or 4-bit LUT + 16-bit Delay/Counter
- Serial Communications
  - I^2C Protocol Interface
- 2-kbit (256 x 8) I^2C-Compatible (2-Wire) Serial EEPROM emulation with Software Write Protection
- Programmable Delay with Edge Detector Output
- Deglitch Filter or Edge Detector
- Three Oscillators
  - 2.048 kHz Oscillator
  - 2.048 MHz Oscillator
  - 25 MHz Oscillator
- Analog Temperature Sensor
- Power-On Reset
- In-System Programmability
- Multiple Time Programmable Memory
- Wide Range Power Supply
  - 2.5 V (±8 %) to 5 V (±10 %) V_{DD}
  - 1.8 V (±5 %) to 5 V (±10 %) V_{DD2} ($V_{DD2} \leq V_{DD}$)
- Operating Temperature Range: -40 °C to +85 °C
- RoHS Compliant/Halogen-Free
- Two Packages Available
  - 20-pin STQFN: 2 mm x 3 mm x 0.55 mm, 0.4 mm pitch
  - 20-pin TSSOP: 6.5 mm x 6.4 mm x 1.2 mm, 0.65 mm pitch

Applications

- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics
- Smartphones and Fitness Bands
- Notebook and Tablet PCs

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Contents

General Description **1**
Key Features **1**
Applications **1**
1 Block Diagram **7**
2 Pinout **8**
2.1 Pin Configuration - STQFN- 20L 8
2.2 Pin Configuration - TSSOP-20L 9
3 Characteristics **13**
3.1 Absolute Maximum Ratings 13
3.2 Electrostatic Discharge Ratings 13
3.3 Recommended Operating Conditions 13
3.4 Electrical Characteristics 14
3.5 Timing Characteristics 23
3.6 OSC Characteristics 26
3.7 ACMP Specifications 27
3.8 Analog Temperature Sensor Characteristics 31
4 User Programmability **33**
5 IO Pins **34**
5.1 IO Pins 34
5.2 GPIO Pins 34
5.3 GPO Pins 34
5.4 GPI Pins 34
5.5 Pull-Up/Down Resistors 34
5.6 Fast Pull-up/down during Power-up 34
5.7 I^2C Mode IO Structure (VDD or VDD2) 35
5.8 Matrix OE IO Structure (VDD or VDD2) 36
5.9 Register OE IO Structure (VDD or VDD2) 37
5.10 Register OE IO Structure (VDD or VDD2) 38
5.11 IO Typical Performance 39
6 Connection Matrix **42**
6.1 Matrix Input Table 43
6.2 Matrix Output Table 44
6.3 Connection Matrix Virtual Inputs 47
6.4 Connection Matrix Virtual Outputs 48
7 Combination Function Macrocells **49**
7.1 2-Bit LUT or D Flip-Flop Macrocells 49
7.2 2-bit LUT or Programmable Pattern Generator 52
7.3 3-Bit LUT or D Flip-Flop with Set/Reset Macrocells 54
7.4 3-Bit LUT or Pipe Delay/Ripple Counter Macrocell 61
8 Multi-Function Macrocells **66**
8.1 3-Bit LUT or DFF/LATCH with 8-Bit Counter/Delay Macrocells 66
8.2 CNT/DLY/FSM Timing Diagrams 75
8.3 4-Bit LUT or DFF/LATCH with 16-Bit Counter/Delay Macrocell 83
8.4 Wake and Sleep Controller 86
9 Analog Comparators **90**
9.1 ACMP0H Block Diagram 91
9.2 ACMP1H Block Diagram 92
9.3 ACMP2L Block Diagram 93
9.4 ACMP3L Block Diagram 94
9.5 ACMP Typical Performance 95
10 Programmable Delay/Edge Detector **99**
10.1 Programmable Delay Timing Diagram - Edge Detector Output 99
11 Additional Logic Function. Deglitch Filter **100**
12 Voltage Reference **101**
12.1 Voltage Reference Overview 101
12.2 Vref Selection Table 101

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12.3 Vref Block Diagram 102
12.4 Vref Load Regulation 103
13 Clocking 105
13.1 Oscillator general description 105
13.2 Oscillator0 (2.048 kHz) 106
13.3 Oscillator1 (2.048 MHz) 107
13.4 Oscillator2 (25 MHz) 108
13.5 CNT/DLY Clock Scheme 109
13.6 External Clocking 109
13.7 Oscillators Power-On Delay 110
13.8 Oscillators Accuracy 112
14 Power-On Reset 115
14.1 General Operation 115
14.2 POR Sequence 116
14.3 Macrocells Output States During POR Sequence 116
15 I^2C Serial Communications Macrocell 119
15.1 I^2C Serial Communications Macrocell Overview 119
15.2 I^2C Serial Communications Device Addressing 119
15.3 I^2C Serial General Timing 120
15.4 I^2C Serial Communications Commands 120
15.5 Chip Configuration Data Protection 123
15.6 I^2C Serial Command Register Map 124
15.7 I^2C Additional Options 125
16 Non-Volatile Memory 128
16.1 Serial NVM Write Operations 128
16.2 Serial NVM Read Operations 130
16.3 Serial NVM Erase Operations 130
16.4 Acknowledge Polling 131
16.5 Low power standby mode 131
16.6 Emulated EEPROM Write Protection 131
17 Analog Temperature Sensor 132
18 Register Definitions 135
18.1 Register Map 135
19 Package Top Marking System Definition 174
19.1 STQFN 20L 2 mm x 3 mm 0.4P FCD Package 174
19.2 TSSOP-20 174
20 Package Information 175
20.1 Package outlines for STQFN 20L 2 mm x 3 mm 0.4P FCD 175
20.2 Package outlines for TSSOP 20L 173 MIL Green 176
20.3 STQFN and TSSOP Handling 177
20.4 Soldering Information 177
21 Ordering Information 178
21.1 Tape and Reel Specifications 178
21.2 Carrier Tape Drawing and Dimensions 178
21.3 STQFN-20L 179
21.4 TSSOP-20L 179
22 Layout Guidelines 180
22.1 STQFN 20L 2 mm x 3 mm 0.4P FCD Package 180
22.2 TSSOP-20 180
Glossary 181
Revision History 184

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Figures

Figure 1: Block Diagram 7
Figure 2: Steps to Create a Custom GreenPAK Device 33
Figure 3: IO with I2C Mode IO Structure Diagram 35
Figure 4: Matrix OE IO Structure Diagram 36
Figure 5: GPIO Register OE IO Structure Diagram 37
Figure 6: GPIO Register OE IO Structure Diagram 38
Figure 7: Typical High Level Output Current vs. High Level Output Voltage at T = 25 °C 39
Figure 8: Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T = 25 °C, Full Range 39
Figure 9: Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T = 25 °C 40
Figure 10: Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T = 25 °C, Full Range 40
Figure 11: Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T = 25 °C 41
Figure 12: Connection Matrix 42
Figure 13: Connection Matrix Example 42
Figure 14: 2-bit LUT0 or DFF0 49
Figure 15: 2-bit LUT1 or DFF1 50
Figure 16: 2-bit LUT2 or DFF2 50
Figure 17: DFF Polarity Operations 52
Figure 18: 2-bit LUT3 or PGen 53
Figure 19: PGen Timing Diagram 53
Figure 20: 3-bit LUT0 or DFF3 55
Figure 21: 3-bit LUT1 or DFF4 55
Figure 22: 3-bit LUT2 or DFF5 56
Figure 23: 3-bit LUT3 or DFF6 56
Figure 24: 3-bit LUT4 or DFF7 57
Figure 25: 3-bit LUT5 or DFF8 57
Figure 26: DFF Polarity Operations with nReset 60
Figure 27: DFF Polarity Operations with nSet 61
Figure 28: 3-bit LUT6/Pipe Delay/Ripple Counter 63
Figure 29: Example: Ripple Counter Functionality 64
Figure 30: Possible Connections Inside Multi-Function Macrocell 66
Figure 31: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT7/DFF10, CNT/DLY1) 67
Figure 32: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT8/DFF11, CNT/DLY2) 68
Figure 33: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT9/DFF12, CNT/DLY3) 69
Figure 34: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT10/DFF13, CNT/DLY4) 70
Figure 35: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT11/DFF14, CNT/DLY5) 71
Figure 36: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT12/DFF15, CNT/DLY6) 72
Figure 37: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT13/DFF16, CNT/DLY7) 73
Figure 38: Delay Mode Timing Diagram, Edge Select: Both, Counter Data: 3 75
Figure 39: Delay Mode Timing Diagram for Different Edge Select Modes 76
Figure 40: Counter Mode Timing Diagram without Two DFFs Synced Up 76
Figure 41: Counter Mode Timing Diagram with Two DFFs Synced Up 77
Figure 42: One-Shot Function Timing Diagram 77
Figure 43: Frequency Detection Mode Timing Diagram 78
Figure 44: Edge Detection Mode Timing Diagram 79
Figure 45: Delayed Edge Detection Mode Timing Diagram 80
Figure 46: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3 81
Figure 47: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3 81
Figure 48: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3 82
Figure 49: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3 82
Figure 50: Counter Value, Counter Data = 3 83
Figure 51: 4-bit LUT0 or CNT/DLY0 84
Figure 52: Wake and Sleep Controller 86
Figure 53: Wake and Sleep Timing Diagram, Normal Wake Mode, Counter Reset is Used 87
Figure 54: Wake and Sleep Timing Diagram, Short Wake Mode, Counter Reset is Used 87
Figure 55: Wake and Sleep Timing Diagram, Normal Wake Mode, Counter Set is Used 88
Figure 56: Wake and Sleep Timing Diagram, Short Wake Mode, Counter Set is Used 88

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Figure 57: ACMP0H Block Diagram 91
Figure 58: ACMP1H Block Diagram 92
Figure 59: ACMP2L Block Diagram 93
Figure 60: ACMP3L Block Diagram 94
Figure 61: Typical Propagation Delay vs. Vref for ACMPxH at T = 25 °C, Gain = 1, Buffer - Disabled, Hysteresis = 0 95
Figure 62: Typical Propagation Delay vs. Vref for ACMPxL at T = 25 °C, Gain = 1, Buffer - Disabled, Hysteresis = 0 95
Figure 63: ACMPxH Power-On Delay vs. V_{DD} 96
Figure 64: ACMPxL Power-On Delay vs. V_{DD} 96
Figure 65: ACMPxH Input Offset Voltage vs. Vref at T = -40 °C to 85 °C, Input Buffer Disabled 97
Figure 66: ACMPxH Input Offset Voltage vs. Vref at T = -40 °C to 85 °C, Input Buffer Enabled 97
Figure 67: ACMPxL Input Offset Voltage vs. Vref at T = -40 °C to 85 °C 98
Figure 68: ACMP Input Current Source vs. Input Voltage at T = -40 °C to 85 °C, V_{DD} = 3.3 V 98
Figure 69: Programmable Delay 99
Figure 70: Edge Detector Output 99
Figure 71: Deglitch Filter or Edge Detector 100
Figure 72: Voltage Reference Block Diagram 102
Figure 73: Typical Load Regulation, Vref = 320 mV, T = -40 °C to +85 °C, Buffer - Enable 103
Figure 74: Typical Load Regulation, Vref = 640 mV, T = -40 °C to +85 °C, Buffer - Enable 103
Figure 75: Typical Load Regulation, Vref = 1280 mV, T = -40 °C to +85 °C, Buffer - Enable 104
Figure 76: Typical Load Regulation, Vref = 2016 mV, T = -40 °C to +85 °C, Buffer - Enable 104
Figure 77: Oscillator0 Block Diagram 106
Figure 78: Oscillator1 Block Diagram 107
Figure 79: Oscillator2 Block Diagram 108
Figure 80: Clock Scheme 109
Figure 81: Oscillator Startup Diagram 110
Figure 82: Oscillator0 Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC0 = 2.048 kHz 110
Figure 83: Oscillator1 Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC1 = 2.048 MHz 111
Figure 84: Oscillator2 Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC2 = 25 MHz 111
Figure 85: Oscillator0 Frequency vs. Temperature, OSC0 = 2.048 kHz 112
Figure 86: Oscillator1 Frequency vs. Temperature, OSC1 = 2.048 MHz 112
Figure 87: Oscillator2 Frequency vs. Temperature, OSC2 = 25 MHz 113
Figure 88: Oscillators Total Error vs. Temperature 113
Figure 89: POR Sequence 116
Figure 90: Internal Macrocell States during POR Sequence 117
Figure 91: Power-Down 118
Figure 92: Basic Command Structure 119
Figure 93: I^2C General Timing Characteristics 120
Figure 94: Byte Write Command, R/W = 0 120
Figure 95: Sequential Write Command 121
Figure 96: Current Address Read Command, R/W = 1 121
Figure 97: Random Read Command 122
Figure 98: Sequential Read Command 122
Figure 99: Reset Command Timing 123
Figure 100: Example of I^2C Byte Write Bit Masking 127
Figure 101: Page Write Command 129
Figure 102: I^2C Block Addressing 129
Figure 103: Analog Temperature Sensor Structure Diagram 133
Figure 104: TS Output vs Temperature, V_{DD} = 2.3 V to 5.5 V 134

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Tables

Table 1: Functional Pin Description 9
Table 2: Pin Type Definitions 12
Table 3: Absolute Maximum Ratings 13
Table 4: Electrostatic Discharge Ratings 13
Table 5: Recommended Operating Conditions 13
Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted 14
Table 7: EC of the I^2C Pins at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted 19
Table 8: I^2C Pins Timing Characteristics at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted 20
Table 9: Typical Current Estimated for Each Macrocell at T = -40 °C to +85 °C 21
Table 10: Typical Delay Estimated for Each Macrocell at T = 25 °C 23
Table 11: Programmable Delay Expected Delays and Widths (Typical) at T = 25 °C 25
Table 12: Typical Filter Rejection Pulse Width at T = 25 °C 25
Table 13: Typical Counter/Delay Offset Measurements at T = 25 °C 25
Table 14: Oscillators Frequency Limits, V_{DD} = 2.3 V to 5.5 V 26
Table 15: Oscillators Power-On Delay at T = 25 °C, OSC Power Mode: "Auto Power-On" 26
Table 16: ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted 27
Table 17: TS Output vs Temperature (Output Range 1) 31
Table 18: TS Output vs Temperature (Output Range 2) 31
Table 19: TS Output Error (Output Range 1) 31
Table 20: TS Output Error (Output Range 2) 32
Table 21: Matrix Input Table 43
Table 22: Matrix Output Table 44
Table 23: Connection Matrix Virtual Inputs 48
Table 24: 2-bit LUT0 Truth Table 51
Table 25: 2-bit LUT1 Truth Table 51
Table 26: 2-bit LUT2 Truth Table 51
Table 27: 2-bit LUT Standard Digital Functions 51
Table 28: 2-bit LUT1 Truth Table 54
Table 29: 2-bit LUT Standard Digital Functions 54
Table 30: 3-bit LUT0 Truth Table 58
Table 31: 3-bit LUT1 Truth Table 58
Table 32: 3-bit LUT2 Truth Table 58
Table 33: 3-bit LUT3 Truth Table 58
Table 34: 3-bit LUT4 Truth Table 58
Table 35: 3-bit LUT5 Truth Table 58
Table 36: 3-bit LUT Standard Digital Functions 59
Table 37: 3-bit LUT6 Truth Table 64
Table 38: 3-bit LUT7 Truth Table 74
Table 39: 3-bit LUT8 Truth Table 74
Table 40: 3-bit LUT9 Truth Table 74
Table 41: 3-bit LUT10 Truth Table 74
Table 42: 3-bit LUT11 Truth Table 74
Table 43: 3-bit LUT12 Truth Table 74
Table 44: 3-bit LUT13 Truth Table 74
Table 45: 4-bit LUT0 Truth Table 85
Table 46: 4-bit LUT Standard Digital Functions 85
Table 47: Vref Selection Table 101
Table 48: Oscillator Operation Mode Configuration Settings 105
Table 49: Oscillator Output Duty Cycle 114
Table 50: RPR Format 123
Table 51: RPR Bit Function Description 123
Table 52: NPR Format 124
Table 53: NPR Bit Function Description 124
Table 54: Read/Write Register Protection Options 124
Table 55: Erase Register Bit format 130
Table 56: Erase Register Bit Function Description 130
Table 57: Write/Erase Protect Register Format 131
Table 58: Write/Erase Protect Register Bit Function Description 131
Table 59: Register Map 135

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1 Block Diagram

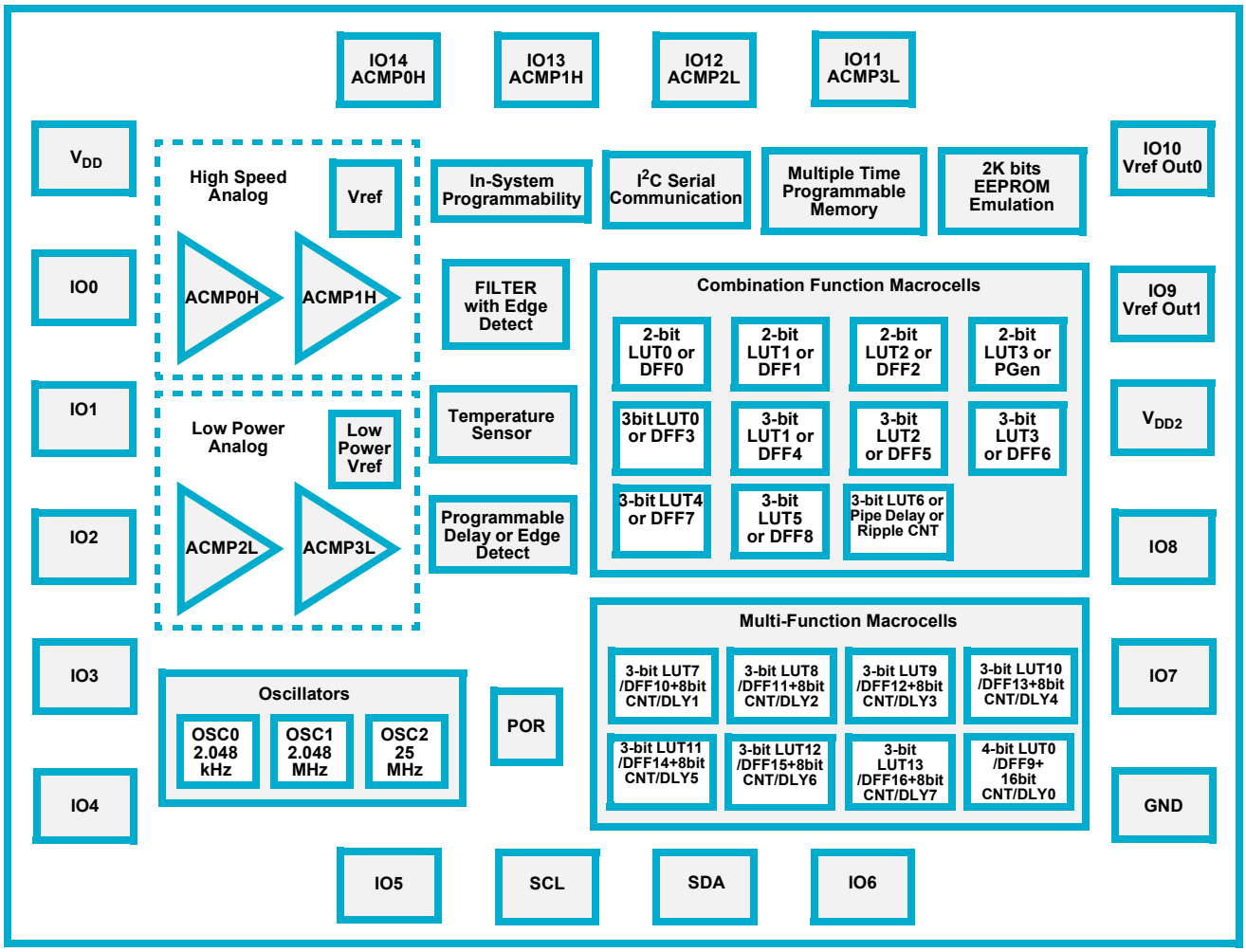

Figure 1: Block Diagram

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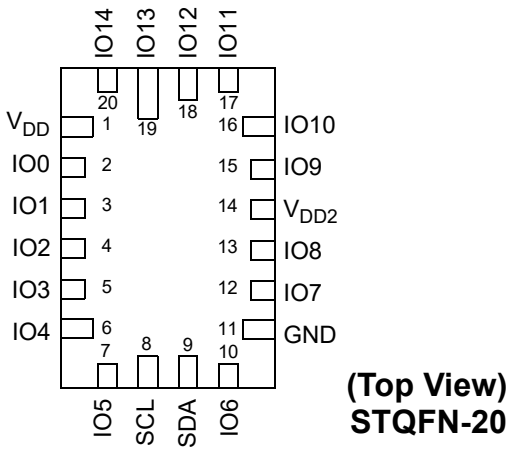
2 Pinout

2.1 PIN CONFIGURATION - STQFN- 20L



(Top View)
STQFN-20

Pin #	Pin Name	Pin Functions
1	V_{DD}	Power Supply
2	IO0	GPIO
3	IO1	GPIO or Vref IN
4	IO2	GPIO, SLA_0
5	IO3	GPIO, SLA_1
6	IO4	GPIO, SLA_2
7	IO5	GPIO, SLA_3
8	SCL	I^2C_SCL
9	SDA	I^2C_SDA
10	IO6	GPO
11	GND	Ground
12	IO7	GPO
13	IO8	GPIO
14	V_{DD2}	Power Supply
15	IO9	GPIO or Vref_OUT1
16	IO10	GPIO or Vref_OUT0
17	IO11	GPIO or ACMP3L_IN
18	IO12	GPIO or ACMP2L_IN
19	IO13	GPIO or ACMP1H_IN
20	IO14	GPIO or ACMP0H_IN

Legend:

ACMPx+: ACMPx Positive Input
ACMPx-: ACMPx Negative Input
SCL: I^2C Clock Input
SDA: I^2C Data Input/Output
Vrefx: Voltage Reference Output
SLA: Target (Slave) Address

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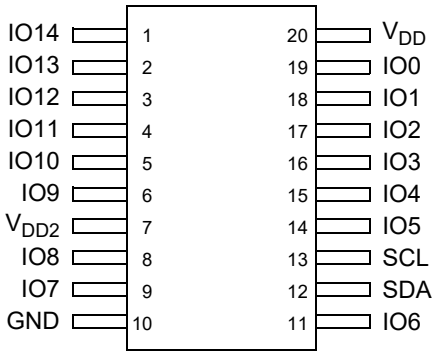
2.2 PIN CONFIGURATION - TSSOP-20L



TSSOP-20
(Top View)

Pin #	Pin Name	Pin Functions
1	IO14	GPIO or ACMP0H_IN
2	IO13	GPIO or ACMP1H_IN
3	IO12	GPIO or ACMP2L_IN
4	IO11	GPIO or ACMP3L_IN
5	IO10	GPIO or Vref_OUT0
6	IO9	GPIO or Vref_OUT1
7	V_{DD2}	Power Supply
8	IO8	GPIO
9	IO7	GPO
10	GND	Ground
11	IO6	GPO
12	SDA	I^2C_SDA
13	SCL	I^2C_SCL
14	IO5	GPIO, SLA_3
15	IO4	GPIO, SLA_2
16	IO3	GPIO, SLA_1
17	IO2	GPIO, SLA_0
18	IO1	GPIO or Vref IN
19	IO0	GPIO
20	V_{DD}	Power Supply

Legend:
ACMPx+: ACMPx Positive Input
ACMPx-: ACMPx Negative Input
SCL: I^2C Clock Input
SDA: I^2C Data Input/Output
Vrefx: Voltage Reference Output
SLA: Target Address

Table 1: Functional Pin Description

Pin No.		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN 20L	TSSOP 20L					
1	20	V_{DD}	VDD	Power Supply	--	--
			ACMP0H+	Analog Comparator 0 Positive Input	Analog	--
			ACMP1H+	Analog Comparator 1 Positive Input	Analog	--
			ACMP2L+	Analog Comparator 2 Positive Input	Analog	--
			ACMP3L+	Analog Comparator 3 Positive Input	Analog	--

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Table 1: Functional Pin Description(Continued)

Pin No.		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN 20L	TSSOP 20L					
2	19	IO0	IO0	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			I^2C_EXPAND_0	--	--	--
			EXT_OSC0_IN	External Clock Connection	--	--
3	18	IO1	IO1	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			EXT_Vref	Analog Comparator Negative Input	Analog	--
4	17	IO2	IO2	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
			EXT_SLA_0		Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
5	16	IO3	IO3	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
			EXT_SLA_1		Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
6	15	IO4	IO4	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
			EXT_SLA_2		Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
7	14	IO5	IO5	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
			EXT_SLA_3		Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			I^2C_EXPAND_1	--	--	--
8	13	SCL	SCL	I^2C Serial Clock	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
9	12	SDA	SDA	I^2C Serial Data	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--

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Table 1: Functional Pin Description(Continued)

Pin No.		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN 20L	TSSOP 20L					
10	11	IO6	IO6	General Purpose Output	--	Push-Pull (1x) (2x)
					--	Open-Drain NMOS (1x) (2x)
					--	--
			I^2C_EXPAND_2	--	--	--
11	10	GND	GND	Ground	--	--
12	9	IO7	IO7	General Purpose Output	--	Push-Pull (1x) (2x)
					--	Open-Drain NMOS (1x) (2x)
					--	--
13	8	IO8	IO8	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			EXT_OSC2_IN	--	--	--
14	7	V_{DD2}	V_{DD2}	Power Supply	--	--
15	6	IO9	IO9	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			Vref1_OUT	Voltage Reference 1 Output	--	Analog
			I^2C_EXPAND_3	--	--	--
16	5	IO10	IO10	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			Vref0_OUT	Voltage Reference 0 Output	--	Analog
			EXT_OSC1_IN	--	--	--
17	4	IO11	IO11	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			ACMP3L+	Analog Comparator 3 Positive Input	Analog	--
18	3	IO12	IO12	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			ACMP2L+	Analog Comparator 2 Positive Input	Analog	--

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Table 1: Functional Pin Description(Continued)

Pin No.		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN 20L	TSSOP 20L					
19	2	IO13	IO13	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			ACMP1H+	Analog Comparator 1 Positive Input	Analog	--
20	1	IO14	IO14	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			ACMP0H+	Analog Comparator 0 Positive Input	Analog	--

Note 1 General Purpose IO's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in IO structure.

Table 2: Pin Type Definitions

Pin Type	Description
V_{DD}	Power Supply
IO	Input/Output
SCL	I^2C Serial Clock
SDA	I^2C Serial Data
GND	Ground
V_{DD2}	Power Supply 2

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3 Characteristics

3.1 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Voltage on V_{DD} relative to GND		-0.3	7	V
DC Input Voltage		GND - 0.5 V	V_{DD} + 0.5 V	V
Maximum Average or DC Current Through V_{DD} Pin		--	90	mA
Maximum Average or DC Current Through V_{DD2} Pin		--	90	mA
Maximum Average or DC Current Through GND Pin (Per chip side, **(Note 1)**)		--	100	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	15.3	mA
	Push-Pull 2x	--	22.1	
	OD 1x	--	15.5	
	OD 2x	--	23	
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
Moisture Sensitivity Level		1		

Note 1 The GreenPAK's GND rail is divided in two sides. IOs 0 to 6, SCL, SDA are connected to one side and IOs 7 to 14 are connected to another side.

3.2 ELECTROSTATIC DISCHARGE RATINGS

Table 4: Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V

3.3 RECOMMENDED OPERATING CONDITIONS

Table 5: Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DD})		2.3	5.5	V
	During NVM Write and Erase commands	2.5	5.5	V
Supply Voltage 2 (V_{DD2})	$V_{DD2} \leq V_{DD}$	1.71	5.5	V
Operating Temperature		-40	85	°C
Maximal Voltage Applied to any PIN in High Impedance State		--	V_{DD} + 0.3 **(Note 1)**	V
Capacitor Value at V_{DD}		0.1	--	µF
Analog Input Common Mode Range	Allowable Input Voltage at Analog Pins	0	V_{DD} or V_{DD2} **(Note 2)**	V

Note 1 IOs 0 to 6, SCL, SDA are powered from V_{DD} and IOs 7 to 14 are powered from V_{DD2}.
Note 2 V_{DD} for IO1 and V_{DD2} for IO11 to IO14

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3.4 ELECTRICAL CHARACTERISTICS

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IH}	HIGH-Level Input Voltage	Logic Input **(Note 1)**	0.7x V_{DD} **(Note 2)**	--	V_{DD}+ 0.3 **(Note 2)**	V
		Logic Input with Schmitt Trigger	0.8x V_{DD} **(Note 2)**	--	V_{DD}+ 0.3 **(Note 2)**	V
		Low-Level Logic Input **(Note 1)**	1.25	--	V_{DD}+ 0.3 **(Note 2)**	V
V_{IL}	LOW-Level Input Voltage	Logic Input **(Note 1)**	GND-0.3	--	0.3x V_{DD} **(Note 2)**	V
		Logic Input with Schmitt Trigger	GND-0.3	--	0.2x V_{DD} **(Note 2)**	V
		Low-Level Logic Input **(Note 1)**	GND-0.3	--	0.5	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	V_{DD2} = 1.8 V ± 5 %	0.1	0.4	0.7	V
		V_{DD} = 2.5 V ± 8 % **(Note 2)**	0.29	0.41	0.56	V
		V_{DD} = 3.3 V ± 10 % **(Note 2)**	0.33	0.45	0.57	V
		V_{DD} = 5 V ± 10 % **(Note 2)**	0.42	0.57	0.74	V
V_O	Maximal Voltage Applied to any PIN in High Impedance State		--	--	V_{DD}+ 0.3 **(Note 2)**	V
V_{OH}	HIGH-Level Output Voltage **(Note 2)**	Push-Pull, 1x Drive, I_{OH} = 1 mA, V_{DD} = V_{DD2} = 2.3 V	2.178	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 1 mA, V_{DD} = V_{DD2} = 2.5 V	2.389	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 1 mA, V_{DD} = V_{DD2} = 2.7 V	2.598	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = V_{DD2} = 3.0 V	2.712	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = V_{DD2} = 3.3 V	3.039	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = V_{DD2} = 3.6 V	3.36	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = V_{DD2} = 4.5 V	4.157	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = V_{DD2} = 5.0 V	4.678	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = V_{DD2} = 5.5 V	5.201	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 1 mA, V_{DD} = V_{DD2} = 2.3 V	2.239	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 1 mA, V_{DD} = V_{DD2} = 2.5 V	2.443	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 1 mA, V_{DD} = V_{DD2} = 2.7 V	2.648	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = V_{DD2} = 3.0 V	2.854	--	--	V

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Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OH}	HIGH-Level Output Voltage **(Note 2)**	Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = V_{DD2} = 3.3 V	3.165	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = V_{DD2} = 3.6 V	3.474	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = V_{DD2} = 4.5 V	4.314	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = V_{DD2} = 5.0 V	4.821	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = V_{DD2} = 5.5 V	5.329	--	--	V
V_{OL}	LOW-Level Output Voltage **(Note 2)**	Push-Pull, 1x Drive, I_{OL}= 1 mA, V_{DD} = V_{DD2} = 2.3 V	--	--	0.085	V
		Push-Pull, 1x Drive, I_{OL}= 1 mA, V_{DD} = V_{DD2} = 2.5 V	--	--	0.079	V
		Push-Pull, 1x Drive, I_{OL}= 1 mA, V_{DD} = V_{DD2} = 2.7 V	--	--	0.074	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = V_{DD2} = 3.0 V	--	--	0.210	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = V_{DD2} = 3.3 V	--	--	0.195	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = V_{DD2} = 3.6 V	--	--	0.183	V
		Push-Pull, 1x Drive, I_{OL}= 5 mA, V_{DD} = V_{DD2} = 4.5 V	--	--	0.271	V
		Push-Pull, 1x Drive, I_{OL}= 5 mA, V_{DD} = V_{DD2} = 5.0 V	--	--	0.256	V
		Push-Pull, 1x Drive, I_{OL}= 5 mA, V_{DD} = V_{DD2} = 5.5 V	--	--	0.246	V
		Push-Pull, 2x Drive, I_{OL}= 1 mA, V_{DD} = V_{DD2} = 2.3 V	--	--	0.046	V
		Push-Pull, 2x Drive, I_{OL} = 1 mA, V_{DD} = V_{DD2} = 2.5 V	--	--	0.043	V
		Push-Pull, 2x Drive, I_{OL} = 1 mA, V_{DD} = V_{DD2} = 2.7 V	--	--	0.040	V
		Push-Pull, 2x Drive, I_{OL}= 3 mA, V_{DD} = V_{DD2} = 3.0 V	--	--	0.114	V
		Push-Pull, 2x Drive, I_{OL}= 3 mA, V_{DD} = V_{DD2} = 3.3 V	--	--	0.107	V
		Push-Pull, 2x Drive, I_{OL}= 3 mA, V_{DD} = V_{DD2} = 3.6 V	--	--	0.102	V
		Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = V_{DD2} = 4.5 V	--	--	0.152	V
		Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = V_{DD2} = 5.0 V	--	--	0.145	V
		Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = V_{DD2} = 5.5 V	--	--	0.140	V
		NMOS OD, 1x Drive, I_{OL}= 1 mA, V_{DD} = V_{DD2} = 2.3 V	--	--	0.038	V
		NMOS OD, 1x Drive, I_{OL} = 1 mA, V_{DD} = V_{DD2} = 2.5 V	--	--	0.035	V

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Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OL}	LOW-Level Output Voltage **(Note 2)**	NMOS OD, 1x Drive, I_{OL} = 1 mA, V_{DD} = V_{DD2} = 2.7 V	--	--	0.033	V
		NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = V_{DD2} = 3.0 V	--	--	0.094	V
		NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = V_{DD2} = 3.3 V	--	--	0.088	V
		NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = V_{DD2} = 3.6 V	--	--	0.084	V
		NMOS OD, 1x Drive, I_{OL} = 5 mA, V_{DD} = V_{DD2} = 4.5 V	--	--	0.127	V
		NMOS OD, 1x Drive, I_{OL} = 5 mA, V_{DD} = V_{DD2} = 5.0 V	--	--	0.121	V
		NMOS OD, 1x Drive, I_{OL} = 5 mA, V_{DD} = V_{DD2} = 5.5 V	--	--	0.117	V
		NMOS OD, 2x Drive, I_{OL}= 1 mA, V_{DD} = V_{DD2} = 2.3 V	--	--	0.032	V
		NMOS OD, 2x Drive, I_{OL} = 1 mA, V_{DD} = V_{DD2} = 2.5 V	--	--	0.03	V
		NMOS OD, 2x Drive, I_{OL} = 1 mA, V_{DD} = V_{DD2} = 2.7 V	--	--	0.029	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = V_{DD2} = 3.0 V	--	--	0.064	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = V_{DD2} = 3.3 V	--	--	0.062	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = V_{DD2} = 3.6 V	--	--	0.059	V
		NMOS OD, 2x Drive, I_{OL} = 5 mA, V_{DD} = V_{DD2} = 4.5 V	--	--	0.085	V
		NMOS OD, 2x Drive, I_{OL} = 5 mA, V_{DD} = V_{DD2} = 5.0 V	--	--	0.081	V
		NMOS OD, 2x Drive, I_{OL} = 5 mA, V_{DD} = V_{DD2} = 5.5 V	--	--	0.08	V
I_{OH}	HIGH-Level Output Current **(Note 2) (Note 3)**	Push-Pull, 1x Drive, V_{OH} = V_{DD} - 0.2 = V_{DD2} - 0.2 V_{DD} = V_{DD2} = 2.3 V	1.60	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = V_{DD} - 0.2 = V_{DD2} - 0.2 V_{DD} = V_{DD2} = 2.5 V	1.76	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = V_{DD} - 0.2 = V_{DD2} - 0.2 V_{DD} = V_{DD2} = 2.7 V	1.92	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = V_{DD2} = 3.0 V	5.64	--	--	mA

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Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OH}	HIGH-Level Output Current **(Note 2) (Note 3)**	Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = V_{DD2} = 3.3 V	8.56	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = V_{DD2} = 3.6 V	11.51	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = V_{DD2} = 4.5 V	20.46	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.5 V, V_{DD} = V_{DD2} = 5.0 V	25.12	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.75 V, V_{DD} = V_{DD2} = 5.5 V	29.34	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = V_{DD} - 0.2 = V_{DD2} - 0.2 V_{DD} = V_{DD2} = 2.3 V	3.10	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = V_{DD} - 0.2 = V_{DD2} - 0.2 V_{DD} = V_{DD2} = 2.5 V	3.40	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = V_{DD} - 0.2 = V_{DD2} - 0.2 V_{DD} = V_{DD2} = 2.7 V	3.69	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = V_{DD2} = 3.0 V	10.89	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = V_{DD2} = 3.3 V	16.54	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = V_{DD2} = 3.6 V	22.28	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = V_{DD2} = 4.5 V	39.61	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.5 V, V_{DD} = V_{DD2} = 5.0 V	48.49	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.75 V, V_{DD} = V_{DD2} = 5.5 V	56.39	--	--	mA
I_{OL}	LOW-Level Output Current **(Note 2) (Note 3)**	Push-Pull, 1x Drive, V_{OL} = 0.15 V, V_{DD} = V_{DD2} = 2.3 V	1.73	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.15 V, V_{DD} = V_{DD2} = 2.5 V	1.87	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.15 V, V_{DD} = V_{DD2} = 2.7 V	2.00	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 3.0 V	5.45	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 3.3 V	5.90	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 3.6 V	6.29	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 4.5 V	7.25	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 5.0 V	7.67	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 5.5 V	8.01	--	--	mA

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Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OL}	LOW-Level Output Current **(Note 2) (Note 3)**	Push-Pull, 2x Drive, V_{OL} = 0.15 V, V_{DD} = V_{DD2} = 2.3 V	3.20	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.15 V, V_{DD} = V_{DD2} = 2.5 V	3.44	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.15 V, V_{DD} = V_{DD2} = 2.7 V	3.65	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 3.0 V	10.01	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 3.3 V	10.73	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 3.6 V	11.36	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 4.5 V	12.85	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 5.0 V	13.52	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 5.5 V	14.05	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.15 V, V_{DD} = V_{DD2} = 2.3 V	3.91	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.15 V, V_{DD} = V_{DD2}= 2.5 V	4.19	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.15 V, V_{DD} = V_{DD2} = 2.7 V	4.44	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 3.0 V	12.18	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 3.3 V	13.02	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 3.6 V	13.75	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 4.5 V	15.47	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 5.0 V	16.19	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 5.5 V	16.80	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V, V_{DD} = V_{DD2} = 2.3 V	6.28	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V, V_{DD} = V_{DD2} = 2.5 V	6.68	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V, V_{DD} = V_{DD2} = 2.7 V	7.02	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 3.0 V	20.14	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 3.3 V	21.23	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 3.6 V	22.12	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 4.5 V	24.84	--	--	mA

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Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OL}	LOW-Level Output Current **(Note 2) (Note 3)**	NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 5.0 V	26.08	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = V_{DD2} = 5.5 V	26.72	--	--	mA
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	1.66	2.59	ms
T_{WR}	NVM Page Write Time	V_{DD} = 2.5 V to 5.5 V	--	--	20	ms
T_{ER}	NVM Page Erase Time	V_{DD} = 2.5 V to 5.5 V	--	--	20	ms
PON_{THR}	Power-On Threshold	V_{DD} Level Required to Start Up the Chip	1.60	1.85	2.07	V
$POFF_{THR}$	Power-Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.97	1.23	1.46	V
R_{PULL}	Pull-up or Pull-down Resistance	1 M for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD} **(Note 2)**	--	1	--	MΩ
		100 k for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD} **(Note 2)**	--	100	--	kΩ
		10 k For Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD} **(Note 2)**	--	10	--	kΩ
C_{IN}	Input Capacitance			4		pF

Note 1 No hysteresis.
Note 2 The GreenPAK's power rails are divided in two sides. IOs 0 to 6, SCL, SDA are powered from V_{DD} (one side) and IOs 7 to 14 are powered from V_{DD2} (another side).
Note 3 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

Table 7: EC of the I^2C Pins at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
V_{IL}	LOW-level Input Voltage		-0.5	0.3xV_{DD}	-0.5	0.3xV_{DD}	V
V_{IH}	HIGH-level Input Voltage		0.7xV_{DD}	5.5	0.7xV_{DD}	5.5	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		0.05xV_{DD}	--	0.05xV_{DD}	--	V
V_{OL1}	LOW-Level Output Voltage 1	(Open-Drain) at 3mA sink current V_{DD} > 2 V	0	0.4	0	0.4	V
V_{OL2}	LOW-Level Output Voltage 2	(Open-Drain) at 2 mA sink current V_{DD} ≤ 2 V	0	0.2xV_{DD}	0	0.2xV_{DD}	V
I_{OL}	LOW-Level Output Current **(Note 1)**	V_{OL} = 0.4 V, V_{DD} = 2.3 V	3	--	16.75	--	mA
		V_{OL} = 0.4 V, V_{DD} = 3.0 V	3	--	20	--	mA
		V_{OL} = 0.4 V, V_{DD} = 4.5 V	3	--	20	--	mA
		V_{OL} = 0.6 V	6	--	--	--	mA
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax} **(Note 1)**		14x (V_{DD}/5.5 V)	250	10x (V_{DD}/5.5 V)	120	ns

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Table 7: EC of the I^2C Pins at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Continued)

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
t_{SP}	Pulse Width of Spikes that must be suppressed by the Input Filter		0	50	0	50	ns
I_i	Input Current each IO Pin	$0.1xV_{DD} < V_I < 0.9xV_{DDmax}$	-10	+10	-10	+10	µA
C_i	Capacitance for each IO Pin		--	10	--	10	pF

Note 1 Does not meet standard I^2C specifications: t_{of} = 20x(V_{DD}/5.5 V) (min); For Fast-mode Plus I_{OL} = 20 mA (min) at V_{OL} = 0.4 V.
Note 2 For Fast-mode Plus SDA pin must be configured as NMOS 2x Open-Drain, see register [769] in Section 18.

Table 8: I^2C Pins Timing Characteristics at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
F_{SCL}	Clock Frequency, SCL		--	400	--	1000	kHz
t_{LOW}	Clock Pulse Width Low		1300	--	500	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	260	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA) **(Note 2)**	V_{DD} = 2.5 V ± 8 %	--	95	--	168	ns
		V_{DD} = 3.3 V ± 10 %	--	95	--	157	
		V_{DD} = 5.0 V ± 10 %	--	111	--	156	
t_{AA}	Clock Low to Data Out Valid		--	900	--	450	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	500	--	ns
t_{HD_STA}	Start Hold Time		600	--	260	--	ns
t_{SU_STA}	Start Set-up Time		600	--	260	--	ns
t_{HD_DAT}	Data Hold Time		0	--	0	--	ns
t_{SU_DAT}	Data Set-up Time		100	--	50	--	ns
t_R	Inputs Rise Time		--	300	--	120	ns
t_F	Inputs Fall Time		--	300	--	120	ns
t_{SU_STO}	Stop Set-up Time		600	--	260	--	ns
t_{DH}	Data Out Hold Time		50	--	50	--	ns

Note 1 Timing diagram can be found in the Figure 93.
Note 2 Does not meet standard I^2C specifications: 50 ns.

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Table 9: Typical Current Estimated for Each Macrocell at T = -40 °C to +85 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I	Current	Chip Quiescent	0.39	0.43	0.53	µA
		Vref OUT0 (Source none, Source Temp Sensor, Buffer On)	12.79	12.95	13.57	µA
		Vref OUT0 (Source none, Source Temp Sensor, Buffer Off)	7.62	7.67	7.87	µA
		Vref OUT1 (Source none, Buffer On)	6.53	6.61	7.02	µA
		Vref OUT1 (Source none, Buffer Off)	1.40	1.44	1.54	µA
		Vref (ACMPxH, 0.32 mV, Buffer On)	12.24	12.59	12.21	µA
		Vref (ACMPxL, 0.32 mV, Buffer On)	6.93	7.01	7.43	µA
		ACMP0H, 1H, 2L, 3L,hysteresis disabled, gain = 1, +IN - IO11, 12, 13, 14 Pull-up 1M, Vref = 32 mV	65.86	67.12	70.77	µA
		ACMP0H, 1H, 2L, 3L,hysteresis disabled, gain = 1, +IN - IO11, 12, 13, 14 Pull-down 1M, Vref = 32 mV	37.34	38.05	40.29	µA
		ACMP0H, 1H, 100 µA disabled, hysteresis disabled, gain = 1, +IN - IO13, 14 Pull-up 1M	63.85	65.11	68.71	µA
		ACMP0H, 1H, 100 µA disabled, hysteresis disabled, gain = 1, +IN - IO13, 14 Pull-down 1M	35.97	36.68	38.87	µA
		ACMP0H, 100 µA disabled, hysteresis disabled, gain = 1, +IN - V_{DD}, Vref = 32 mV	36.30	36.96	38.85	µA
		ACMP0H, 100 µA enabled, hysteresis disabled, gain = 1, +IN - IO14 Pull-up 1M, Vref = 32 mV	46.77	47.31	49.23	µA
		ACMP0H, 100 µA enabled, hysteresis disabled, gain = 1, +IN - IO14 Pull-down 1M, Vref = 32 mV	49.02	50.29	53.75	µA

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Table 9: Typical Current Estimated for Each Macrocell at T = -40 °C to +85 °C (Continued)

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I	Current	ACMP0H, 100 µA disabled, hysteresis disabled, gain = 1, +IN - IO14 Pull-up 1M, Vref = 32 mV	36.56	37.23	39.15	µA
		ACMP0H, 100 µA disabled, hysteresis disabled, gain = 1, +IN - IO14 Pull-down 1M, Vref = 32 mV	22.35	22.74	23.97	µA
		ACMP0H, 100 µA disabled, hysteresis disabled, gain = 1, +IN Buff - IO14 Pull-up 1M, Vref = 32 mV	42.96	43.67	45.93	µA
		ACMP0H, 100 µA disabled, hysteresis disabled, gain = 1, +IN Buff - IO14 Pull-down 1M, Vref = 32 mV	25.59	25.99	27.30	µA
		ACMP0H, 100 µA disabled, hysteresis disabled, gain = 0.25, +IN Buff - IO14 Pull-up 1M, Vref = 32 mV	28.12	28.98	34.73	µA
		ACMP0H, 100 µA disabled, hysteresis disabled, gain = 0.25, +IN Buff - IO14 Pull-down 1M, Vref = 32 mV	22.09	22.47	23.66	µA
		ACMP2L, 3L, hysteresis disabled, gain = 1, +IN - IO11, 12 Pull-up 1M, Vref = 32 mV	2.54	2.59	2.74	µA
		ACMP2L, 3L, hysteresis disabled, gain = 1, +IN - IO11, 12 Pull-down 1M, Vref = 32 mV	1.92	1.96	2.09	µA
		ACMP2L, hysteresis disabled, gain = 1, +IN - IO12 Pull-up 1M, Vref = 32 mV	1.98	2.02	2.15	µA
		ACMP2L, hysteresis disabled, gain = 0.25, +IN - IO12 Pull-up 1M, Vref = 32 mV	2.53	2.82	3.60	µA
		ACMP2L, hysteresis disabled, gain = 1 or gain = 0.25, +IN - IO12 Pull-down 1M, Vref = 32 mV	1.66	1.70	1.82	µA
		OSC2 25 MHz, pre-divider = 1	48.79	60.45	87.16	µA
		OSC2 25 MHz, pre-divider = 4	33.19	39.57	54.85	µA
		OSC2 25 MHz, pre-divider = 8	30.30	35.70	48.87	µA
		OSC1 2.048 MHz, pre-divider = 1	23.37	25.98	32.00	µA
		OSC1 2.048 MHz, pre-divider = 4	19.13	20.11	22.32	µA
		OSC1 2.048 MHz, pre-divider = 8	18.40	19.10	20.64	µA
		OSC0 2.048 kHz, Force	0.65	0.70	0.83	µA
		Temperature Sensor, range 2, Source Matrix	14.75	14.81	15.17	µA
		Temperature Sensor, range 2, Source Register	14.88	14.94	15.30	µA
		Temperature Sensor, range 1, Source Matrix	14.88	14.94	15.30	µA
		Temperature Sensor, range 1, Source Register	14.75	14.82	15.17	µA

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3.5 TIMING CHARACTERISTICS

Table 10: Typical Delay Estimated for Each Macrocell at T = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Multi-Function DFF Q	23	21	16	15	11	11	ns
tpd	Delay	Multi-Function DFF nQ	23	21	17	15	12	11	ns
tpd	Delay	Multi-Function DFF nRESET Q	--	29	--	21	--	15	ns
tpd	Delay	Multi-Function DFF nRESET nQ	31	--	22	--	16	--	ns
tpd	Delay	Multi-Function DFF nSET Q	31	--	22	--	16	--	ns
tpd	Delay	Multi-Function DFF nSET nQ	--	29	--	21	--	15	ns
tpd	Delay	DFF Q	17	17	12	12	8	8	ns
tpd	Delay	DFF nQ	18	16	13	11	9	8	ns
tpd	Delay	DFF nRESET Q	--	21	--	15	--	11	ns
tpd	Delay	DFF nRESET nQ	23	--	16	--	11	--	ns
tpd	Delay	DFF nSET Q	22	--	16	--	11	--	ns
tpd	Delay	DFF nSET nQ	--	22	--	15	--	11	ns
tpd	Delay	DFF3 First Q	18	17	12	12	9	9	ns
tpd	Delay	DFF3 First nQ	19	17	13	12	9	8	ns
tpd	Delay	DFF3 First nRESET Q	--	22	--	16	--	11	ns
tpd	Delay	DFF3 First nRESET nQ	23	--	17	--	12	--	ns
tpd	Delay	DFF3 First nSET Q	23	--	16	--	12	--	ns
tpd	Delay	DFF3 First nSET nQ	--	22	--	16	--	11	ns
tpd	Delay	DFF3 Second Q	21	20	15	15	10	10	ns
tpd	Delay	DFF3 Second nQ	22	20	15	14	11	10	ns
tpd	Delay	DFF3 Second nRESET Q	--	22	--	16	--	11	ns
tpd	Delay	DFF3 Second nRESET nQ	23	--	16	--	12	--	ns
tpd	Delay	DFF3 Second nSET Q	23	--	16	--	11	--	ns
tpd	Delay	DFF3 Second nSET nQ	--	22	--	16	--	11	ns
tpd	Delay	Multi-Function LATCH Q	22	24	15	18	11	13	ns
tpd	Delay	Multi-Function LATCH nQ	27	20	19	14	14	10	ns
tpd	Delay	Multi-Function LATCH nRESET Q	27	30	19	22	14	16	ns
tpd	Delay	Multi-Function LATCH nRESET nQ	32	26	23	18	16	13	ns
tpd	Delay	Multi-Function LATCH nSET Q	30	23	21	17	15	12	ns
tpd	Delay	Multi-Function LATCH nSET nQ	25	28	18	20	13	15	ns
tpd	Delay	LATCH Q	16	19	11	13	8	9	ns
tpd	Delay	LATCH nQ	20	15	14	11	10	8	ns
tpd	Delay	LATCH nRESET Q	20	22	14	16	10	11	ns
tpd	Delay	LATCH nRESET nQ	24	20	17	14	12	10	ns
tpd	Delay	LATCH nSET Q	21	17	15	12	11	8	ns
tpd	Delay	LATCH nSET nQ	18	20	13	15	9	10	ns

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Table 10: Typical Delay Estimated for Each Macrocell at T = 25 °C(Continued)

Parameter	Description	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	LATCH3 First Q	17	19	12	14	8	10	ns
tpd	Delay	LATCH3 First nQ	21	16	15	11	10	8	ns
tpd	Delay	LATCH3 First nRESET Q	21	23	15	17	11	12	ns
tpd	Delay	LATCH3 First nRESET nQ	24	21	17	15	12	10	ns
tpd	Delay	LATCH3 First nSET Q	22	18	15	13	11	9	ns
tpd	Delay	LATCH3 First nSET nQ	19	21	14	15	10	11	ns
tpd	Delay	LATCH3 Second Q	18	18	13	13	9	9	ns
tpd	Delay	LATCH3 Second nQ	19	17	14	12	9	9	ns
tpd	Delay	LATCH3 Second nRESET Q	--	23	--	16	--	12	ns
tpd	Delay	LATCH3 Second nRESET nQ	24	--	17	--	12	--	ns
tpd	Delay	LATCH3 Second nSET Q	22	--	15	--	11	--	ns
tpd	Delay	LATCH3 Second nSET nQ	--	21	--	15	--	11	ns
tpd	Delay	Multi-Function 3-bit LUT	22	24	16	18	11	13	ns
tpd	Delay	Multi-Function 3-bit LUT, CNT Delay	50	52	36	38	25	27	ns
tpd	Delay	Multi-Function 4-bit LUT	22	25	16	18	11	13	ns
tpd	Delay	Multi-Function 4-bit LUT, CNT Delay	52	50	37	36	25	26	ns
tpd	Delay	2-bit LUT	17	16	12	12	8	8	ns
tpd	Delay	3-bit LUT	17	17	12	12	8	9	ns
tpd	Delay	Digital input to Low Voltage to PP 1x	35	222	24	150	16	96	ns
tpd	Delay	Digital input to with Schmitt Trigger to PP 1x	26	30	19	22	13	16	ns
tpd	Delay	Digital input to PP 1x	27	31	19	22	13	16	ns
tpd	Delay	Digital input to PP 2x	24	29	18	21	12	15	ns
tpd	Delay	Digital input to NMOS 1x	--	27	--	20	--	14	ns
tpd	Delay	Digital input to NMOS 2x	--	26	--	19	--	14	ns
tpd	Delay	Digital input to 1x3-State (Z to 0)	--	24	--	17	--	12	ns
tpd	Delay	Digital input to 2x3-State (Z to 0)	--	23	--	17	--	12	ns
tpd	Delay	Digital input to 1x3-State (Z to 1)	27	--	19	--	14	--	ns
tpd	Delay	Digital input to 2x3-State (Z to 1)	26	--	19	--	13	--	ns
tpd	Delay	Digital input to 1xOE (Z to 0)	--	24	--	17	--	12	ns
tpd	Delay	Digital input to 1xOE (Z to 1)	27	--	19	--	14	--	ns
tpd	Delay	Ripple CNT CLK UP Q0	18	15	13	11	9	8	ns
tpd	Delay	Ripple CNT CLK UP Q1	23	22	17	16	12	12	ns
tpd	Delay	Ripple CNT CLK UP Q2	28	21	20	16	14	12	ns
tpd	Delay	Ripple CNT CLK DOWN Q0	18	15	13	11	9	8	ns
tpd	Delay	Ripple CNT CLK DOWN Q1	27	21	19	15	14	11	ns
tpd	Delay	Ripple CNT CLK DOWN Q2	26	27	19	20	13	14	ns

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Table 10: Typical Delay Estimated for Each Macrocell at T = 25 °C(Continued)

Parameter	Description	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Ripple CNT nSET UP Q0	26	35	19	25	14	18	ns
tpd	Delay	Ripple CNT nSET UP Q1	25	39	18	28	13	20	ns
tpd	Delay	Ripple CNT nSET UP Q2	24	44	17	32	12	23	ns
tpd	Delay	Ripple CNT nSET DOWN Q0	26	34	19	25	14	18	ns
tpd	Delay	Ripple CNT nSET DOWN Q1	25	41	18	30	13	22	ns
tpd	Delay	Ripple CNT nSET DOWN Q2	24	40	17	29	12	21	ns
tpd	Delay	Edge detect	21	20	15	14	11	10	ns
tw	Width	Edge detect	205	206	153	153	113	113	ns
tpd	Delay	Edge detect Delayed	227	229	168	169	123	124	ns
tpd	Delay	Filter nQ	141	154	99	106	67	67	ns
tpd	Delay	Filter Q	158	137	108	97	68	65	ns
tpd	Delay	PGen CLK	16	15	11	11	8	8	ns
tpd	Delay	PGen nRESET (Z to 0)	--	20	--	14	--	10	ns
tpd	Delay	PGen nRESET (Z to 1)	18	--	12	--	8	--	ns
tpd	Delay	Pipe Delay nRESET Out	30	26	22	19	16	14	ns
tpd	Delay	Pipe Delay Out	22	19	16	13	11	10	ns

Table 11: Programmable Delay Expected Delays and Widths (Typical) at T = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
tw	Pulse Width, 1 cell	mode: (any) edge detect, edge detect output	205	153	113	ns
tw	Pulse Width, 2 cell	mode: (any) edge detect, edge detect output	407	303	223	ns
tw	Pulse Width, 3 cell	mode: (any) edge detect, edge detect output	610	453	334	ns
tw	Pulse Width, 4 cell	mode: (any) edge detect, edge detect output	812	603	444	ns
time1	Delay, 1 cell	mode: (any) edge detect, edge detect output	20	14	10	ns
time1	Delay, 2 cell	mode: (any) edge detect, edge detect output	20	14	10	ns
time1	Delay, 3 cell	mode: (any) edge detect, edge detect output	20	14	10	ns
time1	Delay, 4 cell	mode: (any) edge detect, edge detect output	20	14	10	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	226	168	123	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	429	318	234	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	632	468	344	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	834	618	455	ns

Table 12: Typical Filter Rejection Pulse Width at T = 25 °C

Parameter	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered Pulse Width	< 123	< 84	< 52	ns

Table 13: Typical Counter/Delay Offset Measurements at T = 25 °C

Parameter	OSC Freq	OSC Power	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Power-On time	25 MHz	auto	0.14	0.14	0.14	µs

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Table 13: Typical Counter/Delay Offset Measurements at T = 25 °C(Continued)

Parameter	OSC Freq	OSC Power	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Power-On time	2.048 MHz	auto	0.51	0.46	0.41	µs
Power-On time	2.048 kHz	auto	705	604	486	µs
frequency settling time	25 MHz	auto	4	4	8	µs
frequency settling time	2.048 MHz	auto	0.3	0.4	0.4	µs
frequency settling time	2.048 kHz	auto	660	570	480	µs
variable (CLK period)	25 MHz	forced	0-40	0-40	0-40	ns
variable (CLK period)	2.048 MHz	forced	0-0.5	0-0.5	0-0.5	µs
variable (CLK period)	2.048 kHz	forced	0-488	0-488	0-488	µs
tpd (non-delayed edge)	25 MHz/ 2.048 kHz	either	35	14	10	ns

3.6 OSC CHARACTERISTICS

3.6.1 OSC Specifications

Table 14: Oscillators Frequency Limits, V_{DD} = 2.3 V to 5.5 V

OSC	Temperature Range					
	+25 °C			-40 °C to +85 °C		
	Minimum Value, kHz	Maximum Value, kHz	Error, %	Minimum Value, kHz	Maximum Value, kHz	Error, %
2.048 kHz OSC0	2.025	2.071	+1.13	1.900	2.093	+2.19
			-1.11			-7.21
2.048 MHz OSC1	2020.83	2073.33	+1.19	1991.05	2083.90	+1.75
			-1.33			-2.78
25 MHz OSC2	24585.51	25354.98	+1.42	23562.69	25606.32	+2.43
			-1.66			-5.75

3.6.2 OSC Power-On Delay

Table 15: Oscillators Power-On Delay at T = 25 °C, OSC Power Mode: "Auto Power-On"

Power Supply Range (V_{DD}), V	Oscillator2 25 MHz		Oscillator2 25 MHz Start with delay		Oscillator1 2.048 MHz		Oscillator0 2.048 kHz	
	Typical Value, ns	Maximum Value, ns	Typical Value, ns	Maximum Value, ns	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs
2.30	43.41	48.00	142.46	153.00	530.99	549.00	746.66	1011.73
2.50	38.55	42.00	140.90	150.00	508.76	521.00	704.97	939.85
2.70	34.89	38.00	140.22	149.00	491.43	512.00	671.91	884.63
3.00	30.82	34.00	139.81	149.00	473.49	497.00	633.51	819.23
3.30	27.79	30.00	139.66	148.00	460.75	481.00	604.09	768.79
3.60	25.53	27.00	139.70	149.00	450.80	472.00	580.73	730.10
4.00	23.21	26.00	139.84	149.00	439.61	462.00	556.22	690.04
4.20	22.32	25.00	140.03	148.00	435.00	456.00	545.94	673.29
4.50	21.12	25.00	140.16	150.00	428.88	449.00	532.09	649.85
5.00	19.61	20.00	140.34	149.00	419.91	439.00	510.48	616.17
5.50	18.57	19.00	140.51	149.00	412.39	432.00	485.59	579.80

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3.7 ACMP SPECIFICATIONS

Table 16: ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
V_{ACMP}	ACMP0H, ACMP1H, ACMP2L, ACMP3L Input Voltage Range	Positive Input		0	--	V_{DD}	V
		Negative Input		0	--	V_{DD}	V
V_{offset}	ACMP0H, ACMP1H Input Offset Voltage	Vhys = 0 mV, Gain = 1, Vref = 32 mV to 2016 mV	T = 25 °C	-5.9	--	6.2	mV
				-6.0	--	6.2	mV
	ACMP2L, ACMP3L Input Offset Voltage		T = 25 °C	-6.4	--	6.7	mV
				-7.3	--	7.2	mV
t_{start}	ACMP0H, ACMP1H Start Time	ACMP Power-On delay, Minimal required wake time for the “Wake and Sleep function”	T = 25 °C BG Forced On	--	25.0	36.3	µs
				--	26.2	51.4	µs
	ACMP2L, ACMP3L Start Time			--	139.3	233.3	µs
				--	144.6	326.6	µs
V_{HYS}	ACMP0H, ACMP1H Built-in Hysteresis	V_{HYS} = 32 mV	T = 25 °C	24.30	--	41.65	mV
		V_{HYS} = 64 mV	T = 25 °C	56.14	--	74.15	mV
		V_{HYS} = 192 mV	T = 25 °C	186.19	--	203.55	mV
		V_{HYS} = 32 mV		23.36	--	41.69	mV
		V_{HYS} = 64 mV		53.56	--	75.97	mV
		V_{HYS} = 192 mV		184.02	--	205.66	mV
V_{HYS}	ACMP2L, ACMP3L Built-in Hysteresis	V_{HYS} = 32 mV	T = 25 °C	27.23	--	43.27	mV
		V_{HYS} = 64 mV	T = 25 °C	59.43	--	75.81	mV
		V_{HYS} = 192 mV	T = 25 °C	187.14	--	206.30	mV
		V_{HYS} = 32 mV		25.29	--	44.19	mV
		V_{HYS} = 64 mV		56.49	--	77.18	mV
		V_{HYS} = 192 mV		186.73	--	206.30	mV
R_{sin}	Input Resistance	Gain = 1x		--	100.0	--	MΩ
		Gain = 0.5x		--	2.0	--	MΩ
		Gain = 0.33x		--	2.0	--	MΩ
		Gain = 0.25x		--	2.0	--	MΩ

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Table 16: ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
PROP	Propagation Delay, Response Time for ACMP0H, ACMP1H	Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 10 mV	Low to High	--	1.06	1.96	µs
			High to Low	--	0.95	1.71	µs
		Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 100 mV	Low to High	--	0.56	2.46	µs
			High to Low	--	0.47	0.79	µs
		Gain = 1, T = 25 °C, Vref = 32 mV, Overdrive = 10 mV	Low to High	--	1.21	--	µs
			High to Low	--	0.99	--	µs
		Gain = 0.5, T = 25 °C, Vref = 32 mV, Overdrive = 10 mV	Low to High	--	2.88	--	µs
			High to Low	--	2.52	--	µs
		Gain = 0.33, T = 25 °C, Vref = 32 mV, Overdrive = 10 mV	Low to High	--	3.42	--	µs
			High to Low	--	3.02	--	µs
		Gain = 0.25, T = 25 °C, Vref = 32 mV, Overdrive = 10 mV	Low to High	--	3.88	--	µs
			High to Low	--	3.46	--	µs
		Gain = 1, T = 25 °C, Vref = 32 mV, Overdrive = 100 mV	Low to High	--	0.59	--	µs
			High to Low	--	0.46	--	µs
		Gain = 0.5, T = 25 °C, Vref = 32 mV, Overdrive = 100 mV	Low to High	--	1.24	--	µs
			High to Low	--	1.43	--	µs
		Gain = 0.33, T = 25 °C, Vref = 32 mV, Overdrive = 100 mV	Low to High	--	1.31	--	µs
			High to Low	--	1.52	--	µs
		Gain = 0.25, T = 25 °C, Vref = 32 mV, Overdrive = 100 mV	Low to High	--	1.30	--	µs
			High to Low	--	1.28	--	µs

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Table 16: ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
PROP	Propagation Delay, Response Time for ACMP2L, ACMP3L	Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 10 mV	Low to High	--	42.93	114.55	µs
			High to Low	--	38.99	83.66	µs
		Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 100 mV	Low to High	--	21.13	51.24	µs
			High to Low	--	20.34	51.08	µs
		Gain = 1, T = 25 °C, Vref = 32 mV, Overdrive = 10 mV	Low to High	--	58.77	--	µs
			High to Low	--	48.32	--	µs
		Gain = 0.5, T = 25 °C, Vref = 32 mV, Overdrive = 10 mV	Low to High	--	97.01	--	µs
			High to Low	--	82.49	--	µs
		Gain = 0.33, T = 25 °C, Vref = 32 mV, Overdrive = 10 mV	Low to High	--	133.55	--	µs
			High to Low	--	114.56	--	µs
		Gain = 0.25, T = 25 °C, Vref = 32 mV, Overdrive = 10 mV	Low to High	--	167.39	--	µs
			High to Low	--	145.88	--	µs
		Gain = 1, T = 25 °C, Vref = 32 mV, Overdrive = 100 mV	Low to High	--	26.91	--	µs
			High to Low	--	26.22	--	µs
		Gain = 0.5, T = 25 °C, Vref = 32 mV, Overdrive = 100 mV	Low to High	--	35.23	--	µs
			High to Low	--	34.62	--	µs
		Gain = 0.33, T = 25 °C, Vref = 32 mV, Overdrive = 100 mV	Low to High	--	40.06	--	µs
			High to Low	--	39.51	--	µs
		Gain = 0.25, T = 25 °C, Vref = 32 mV, Overdrive = 100 mV	Low to High	--	43.62	--	µs
			High to Low	--	43.10	--	µs
G	Gain error (including threshold and internal Vref error)	G = 1		--	1	--	
		G = 0.5		0.496	--	0.504	
		G = 0.33		0.330	--	0.338	
		G = 0.25		0.246	--	0.255	

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Table 16: ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
Vref	Internal Vref0 error, Vref0 = 32 mV to 2016 mV	V_{DD} = 4.0 V	T = 25 °C	-0.5	--	0.5	%
	Vref0 Output error, Vref0 = 224 mV to 2016 mV, Buffer Enabled		T = 25 °C, Loading = 1 µA	-6.14	--	5.50	%
			Loading = 1 µA	-6.63	--	5.64	%
	Vref0 Output Capacitance Loading		Load Resistance = 1 MΩ	--	--	5	pF
			Load Resistance = 560 kΩ	--	--	10	pF
			Load Resistance = 100 kΩ	--	--	40	pF
			Load Resistance = 10 kΩ	--	--	80	pF
			Load Resistance = 2 kΩ	--	--	120	pF
			Load Resistance = 1 kΩ, Vref = 32 mV to 1024 mV	--	--	150	pF
	Internal Vref1 error, Vref1 = 32 mV to 2016 mV	V_{DD} = 4.0 V	T = 25 °C	-0.5	--	0.5	%
	Vref1 Output error, Vref1 = 224 mV to 2016 mV, Buffer Enabled		T = 25 °C, Loading = 1 µA	-6.04	--	5.59	%
			Loading = 1 µA	-6.11	--	5.72	%
	Vref1 Output Capacitance Loading		Load Resistance = 1 MΩ	--	--	15	pF
			Load Resistance = 560 kΩ	--	--	27	pF
			Load Resistance = 100 kΩ	--	--	64	pF
			Load Resistance = 10 kΩ	--	--	120	pF
			Load Resistance = 2 kΩ	--	--	180	pF
			Load Resistance = 1 kΩ, Vref = 32 mV to 1024 mV	--	--	210	pF
Is	Input Current Source		Vin = V_{DD} - 0.7 V	79.7	93.5	108.1	µA

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3.8 ANALOG TEMPERATURE SENSOR CHARACTERISTICS

Temperature Sensor typical nonlinearity ±0.87 % for output range 1 and ±0.45 % for output range 2 at V_{DD} = 3.3 V.

Table 17: TS Output vs Temperature (Output Range 1)

T, °C	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V	
	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %
-40	998	±0.59	997	±0.60	996	±0.63
-30	975	±0.56	974	±0.56	974	±0.58
-20	952	±0.49	951	±0.50	951	±0.51
-10	930	±0.48	929	±0.48	929	±0.50
0	907	±0.42	906	±0.42	906	±0.45
10	884	±0.36	883	±0.35	883	±0.37
20	861	±0.38	860	±0.36	860	±0.36
30	838	±0.32	837	±0.28	836	±0.31
40	814	±0.31	813	±0.27	813	±0.30
50	791	±0.32	790	±0.28	789	±0.31
60	767	±0.35	766	±0.32	765	±0.35
70	743	±0.41	742	±0.38	741	±0.43
80	719	±0.54	718	±0.51	717	±0.55
90	694	±0.66	693	±0.65	693	±0.67

Table 18: TS Output vs Temperature (Output Range 2)

T, °C	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V	
	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %
-40	1188	±0.54	1187	±0.54	1187	±0.56
-30	1161	±0.56	1160	±0.56	1160	±0.54
-20	1134	±0.46	1133	±0.45	1133	±0.46
-10	1107	±0.44	1106	±0.44	1105	±0.44
0	1079	±0.41	1078	±0.39	1078	±0.39
10	1052	±0.38	1051	±0.36	1050	±0.34
20	1024	±0.36	1023	±0.33	1022	±0.31
30	995	±0.43	995	±0.40	994	±0.40
40	967	±0.40	966	±0.36	966	±0.35
50	939	±0.43	938	±0.41	938	±0.39
60	910	±0.48	909	±0.47	909	±0.46
70	881	±0.55	880	±0.53	880	±0.54
80	852	±0.68	851	±0.67	851	±0.67
90	823	±0.84	822	±0.84	821	±0.83

Table 19: TS Output Error (Output Range 1)

V_{DD}, V	Error at T							
	-40 °C, %	-20 °C, %	0 °C, %	20 °C, %	40 °C, %	60 °C, %	80 °C, %	90 °C, %
2.30	±0.60	±0.49	±0.43	±0.40	±0.33	±0.36	±0.55	±0.68

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Table 19: TS Output Error (Output Range 1)(Continued)

V_{DD}, V	Error at T							
	-40 °C, %	-20 °C, %	0 °C, %	20 °C, %	40 °C, %	60 °C, %	80 °C, %	90 °C, %
2.50	±0.59	±0.49	±0.42	±0.38	±0.31	±0.35	±0.54	±0.66
2.70	±0.60	±0.49	±0.41	±0.37	±0.30	±0.34	±0.53	±0.66
3.00	±0.60	±0.49	±0.42	±0.36	±0.29	±0.32	±0.52	±0.65
3.30	±0.60	±0.50	±0.42	±0.36	±0.27	±0.32	±0.51	±0.65
3.60	±0.60	±0.50	±0.42	±0.36	±0.28	±0.32	±0.52	±0.64
4.00	±0.62	±0.51	±0.43	±0.35	±0.29	±0.33	±0.53	±0.64
4.20	±0.63	±0.50	±0.43	±0.36	±0.29	±0.34	±0.53	±0.65
4.50	±0.62	±0.51	±0.43	±0.36	±0.29	±0.34	±0.54	±0.65
5.00	±0.63	±0.51	±0.45	±0.36	±0.30	±0.35	±0.55	±0.67
5.50	±0.63	±0.52	±0.46	±0.37	±0.31	±0.37	±0.57	±0.72

Table 20: TS Output Error (Output Range 2)

V_{DD}, V	Error at T							
	-40 °C, %	-20 °C, %	0 °C, %	20 °C, %	40 °C, %	60 °C, %	80 °C, %	90 °C, %
2.30	±0.61	±0.50	±0.43	±0.38	±0.42	±0.50	±0.68	±0.85
2.50	±0.54	±0.46	±0.41	±0.36	±0.39	±0.48	±0.68	±0.84
2.70	±0.54	±0.46	±0.40	±0.35	±0.38	±0.48	±0.67	±0.84
3.00	±0.54	±0.45	±0.40	±0.34	±0.38	±0.47	±0.66	±0.83
3.30	±0.54	±0.45	±0.39	±0.33	±0.36	±0.47	±0.67	±0.84
3.60	±0.54	±0.45	±0.40	±0.32	±0.37	±0.46	±0.67	±0.82
4.00	±0.55	±0.46	±0.40	±0.32	±0.36	±0.45	±0.67	±0.83
4.20	±0.54	±0.45	±0.39	±0.31	±0.36	±0.45	±0.67	±0.82
4.50	±0.56	±0.46	±0.39	±0.31	±0.35	±0.45	±0.67	±0.82
5.00	±0.56	±0.46	±0.39	±0.31	±0.35	±0.46	±0.67	±0.83
5.50	±0.56	±0.46	±0.39	±0.30	±0.36	±0.46	±0.69	±0.85

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4 User Programmability

The SLG46826 is a user programmable device with Multiple-Time-Programmable (MTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

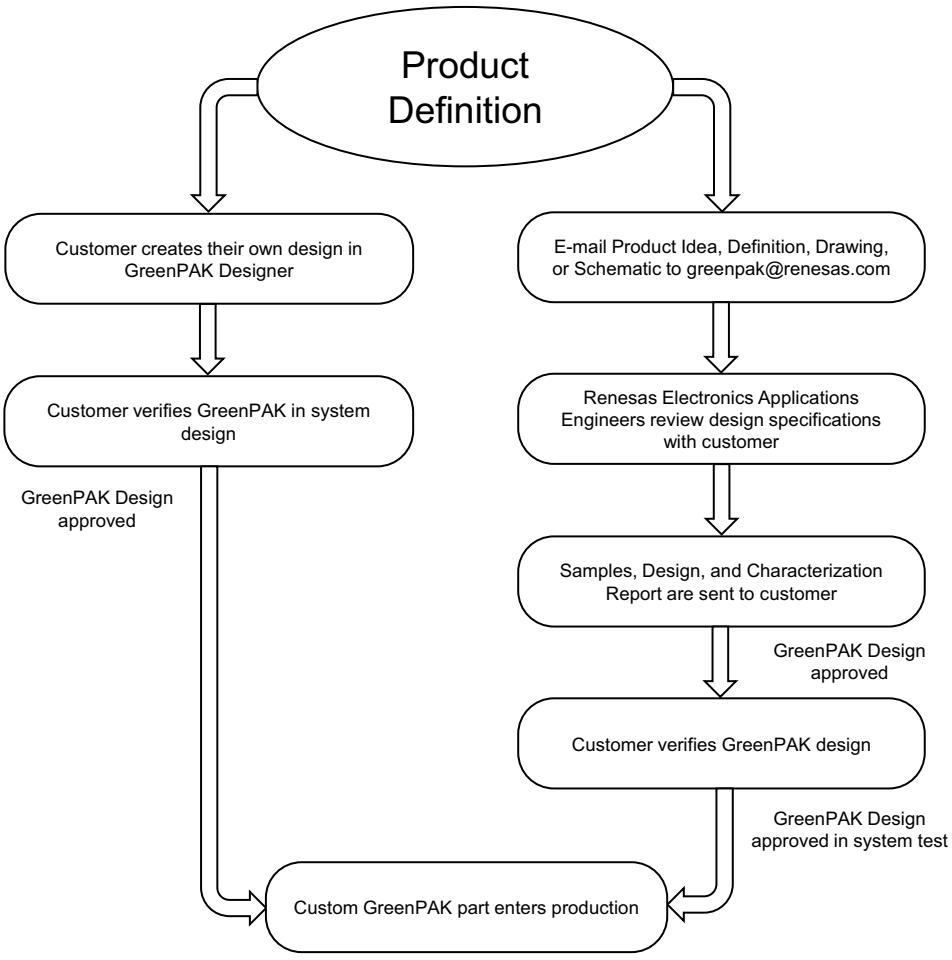

Figure 2: Steps to Create a Custom GreenPAK Device

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5 IO Pins

5.1 IO PINS

The SLG46826 has a total of 13 GPIO, 2 GPO, and 2 GPI Pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference).

IOs 0 to 6, SCL, SDA are powered from V_{DD} and IOs 7 to 14 are powered from $V_{DD2.}$ All internal macrocells are powered from $V_{DD.}$ Voltage on V_{DD2} Pin must be less or equal voltage on V_{DD} Pin.

In case V_{DD2} floating and any Pin powered from V_{DD2} is configured as input, ESD pin protection diodes must be considered when applying an input signal to the pin. This will cause a significant current leakage.

In case V_{DD2} floating and any Pin powered from V_{DD2} is configured as Output, the pin will behave as NMOS Open-Drain.

It is not recommended to connect V_{DD2} to the GND.

5.2 GPIO PINS

IO0, IO1, IO2, IO3, IO4, IO5, IO8, IO9, IO10, IO11, IO12, IO13, IO14 serve as General Purpose IO Pins.

5.3 GPO PINS

IO6 and IO7 serve as General Purpose Output Pins.

5.4 GPI PINS

SCL and SDA serve as General Purpose Input Pins.

5.5 PULL-UP/DOWN RESISTORS

All IO Pins have the option of user-selectable resistors that can be connected to the pin structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. The internal resistors can be configured as either pull-up or pull-downs.

5.6 FAST PULL-UP/DOWN DURING POWER-UP

During power-up, IO Pull-up/down resistance will switch to 2.6 kΩ initially and then it will switch to normal setting value. This function is enabled by register [768].

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5.7 I²C MODE IO STRUCTURE (V_{DD} OR V_{DD2})

5.7.1 I²C Mode Structure (for SCL and SDA)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en = 1
01: Digital In with Schmitt Trigger, smt_en = 1
10: Low Voltage Digital In mode 1, lv_en = 1
11: Reserved

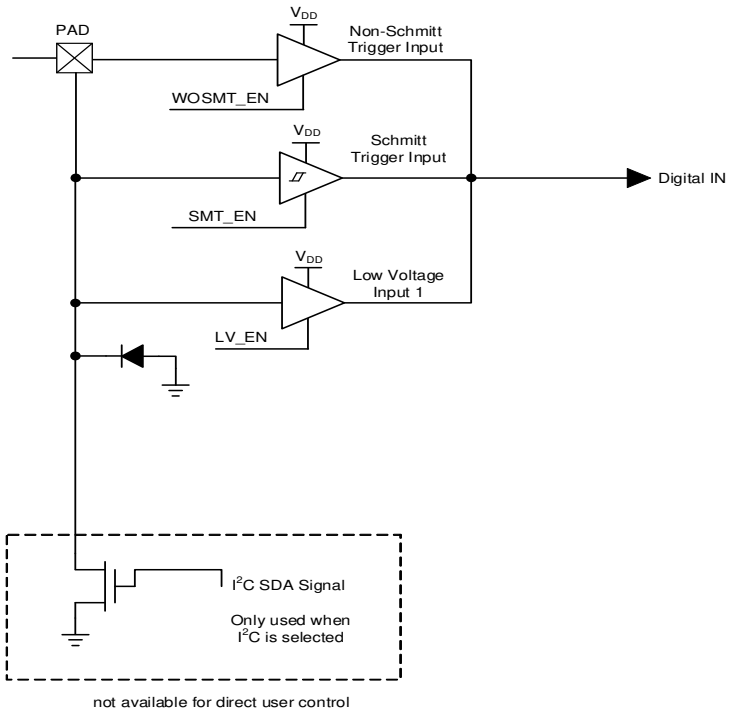

Figure 3: IO with I²C Mode IO Structure Diagram

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5.8 MATRIX OE IO STRUCTURE (V_{DD} OR V_{DD2})

5.8.1 Matrix OE IO Structure (for IOs 1, 4, 5 with V_{DD}, and IOs 8, 9, 10, 11, 12, 13, 14 with V_{DD2})

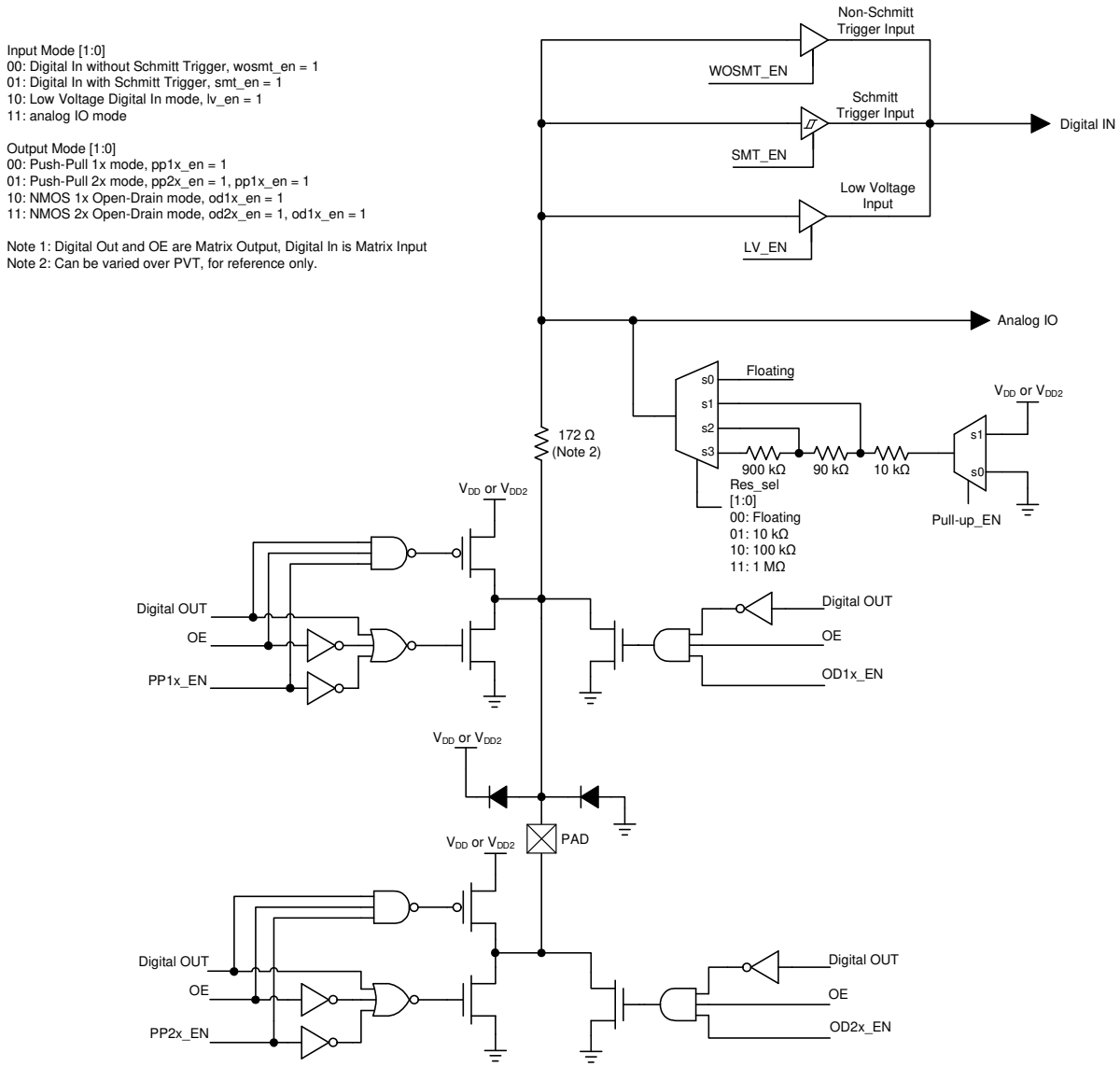

Figure 4: Matrix OE IO Structure Diagram

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5.9 REGISTER OE IO STRUCTURE (V_{DD} OR V_{DD2})

5.9.1 Register OE IO Structure (for IOs 0, 2, 3 with V_{DD})

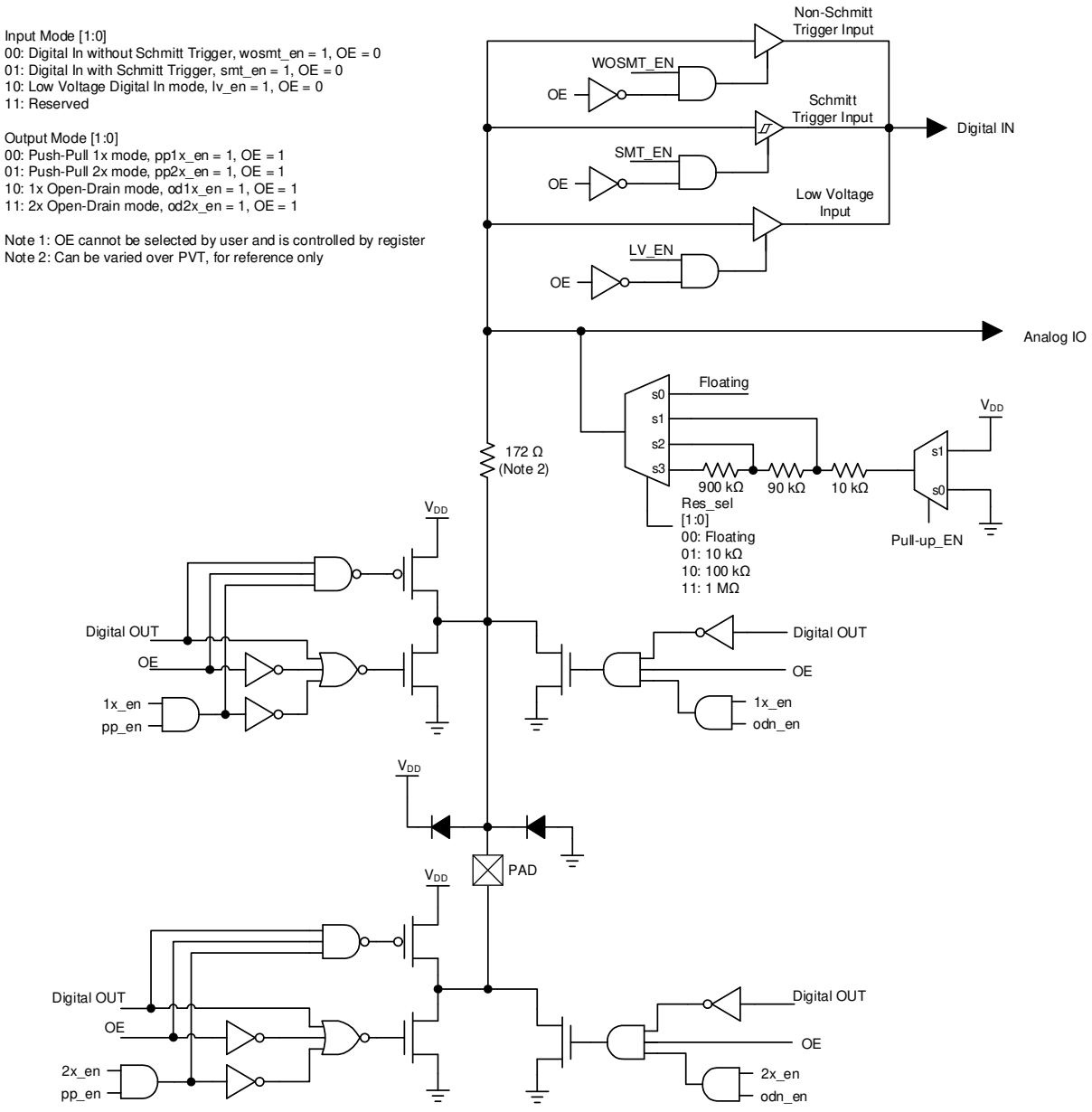

Figure 5: GPIO Register OE IO Structure Diagram

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5.10 REGISTER OE IO STRUCTURE (V_{DD} OR V_{DD2})

5.10.1 Register OE IO Structure (for IO 6 with V_{DD}, and IO 7 with V_{DD2})

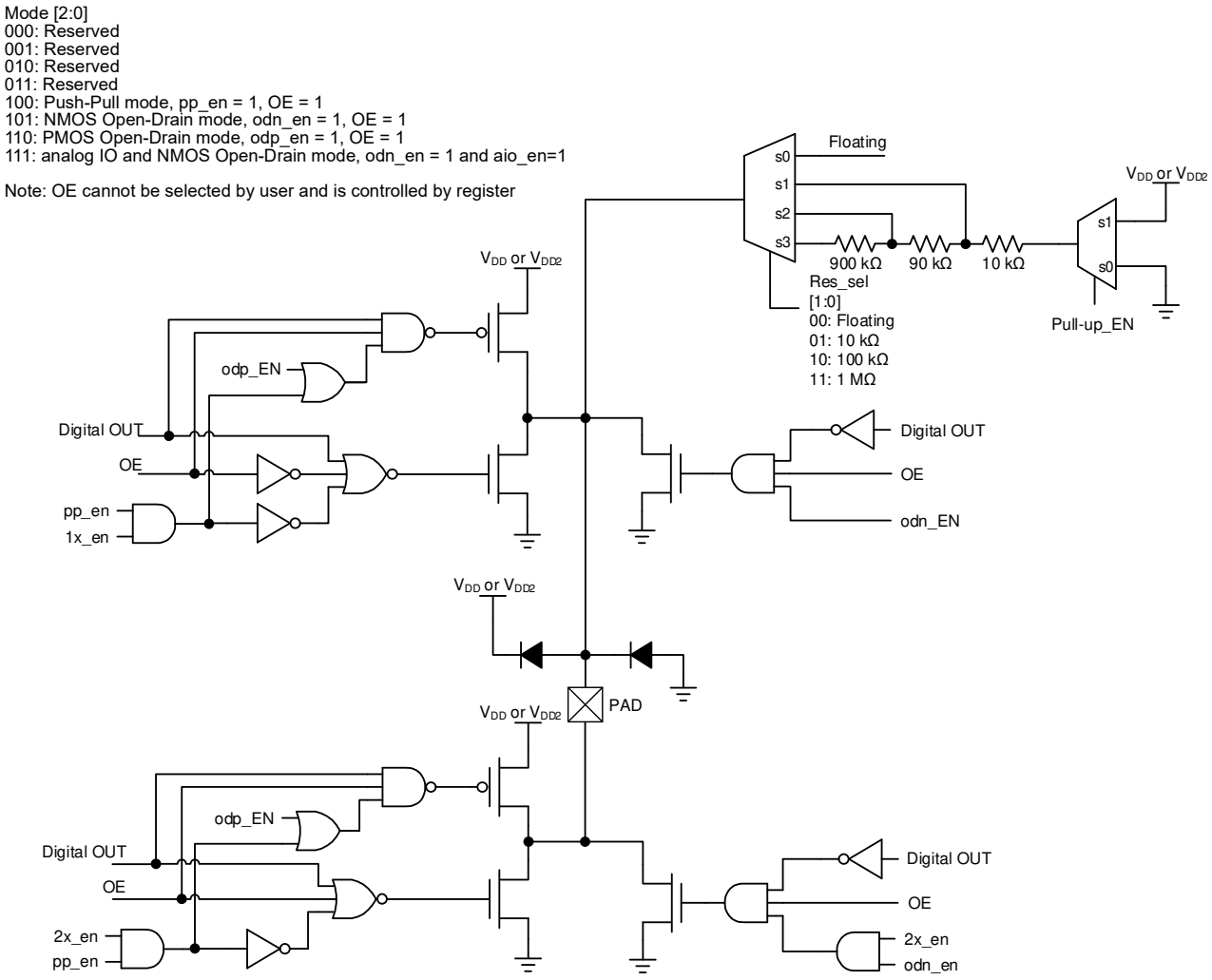

Figure 6: GPIO Register OE IO Structure Diagram

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5.11 IO TYPICAL PERFORMANCE

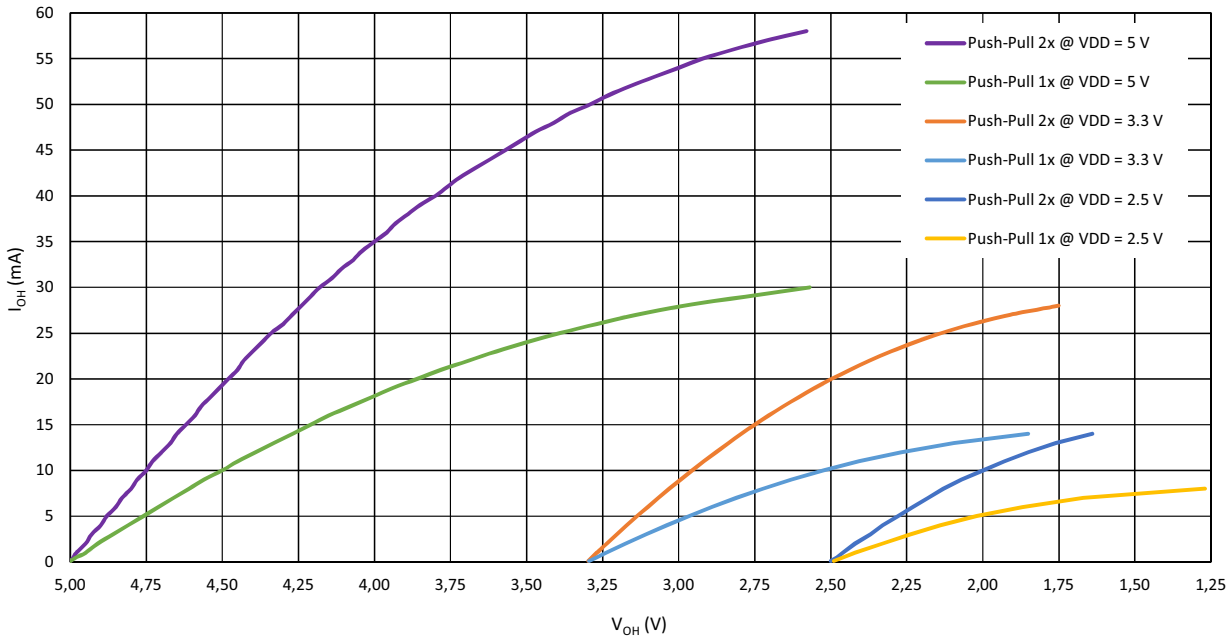

Figure 7: Typical High Level Output Current vs. High Level Output Voltage at T = 25 °C

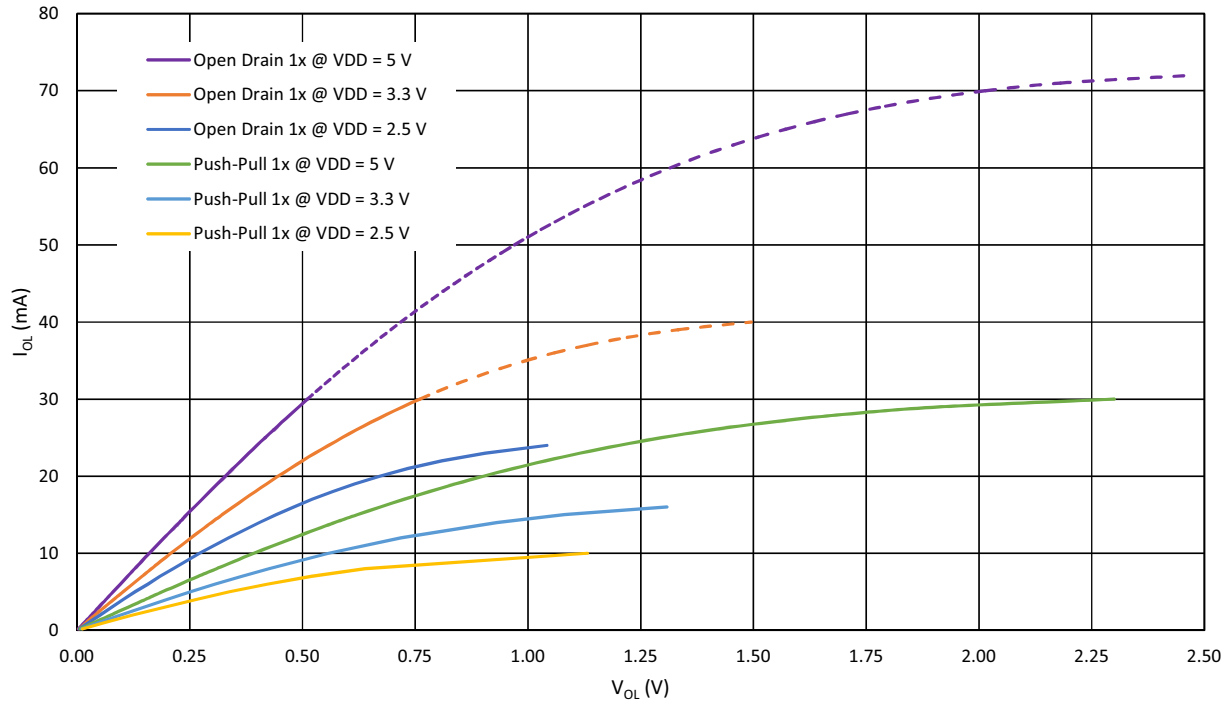

Figure 8: Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T = 25 °C, Full Range

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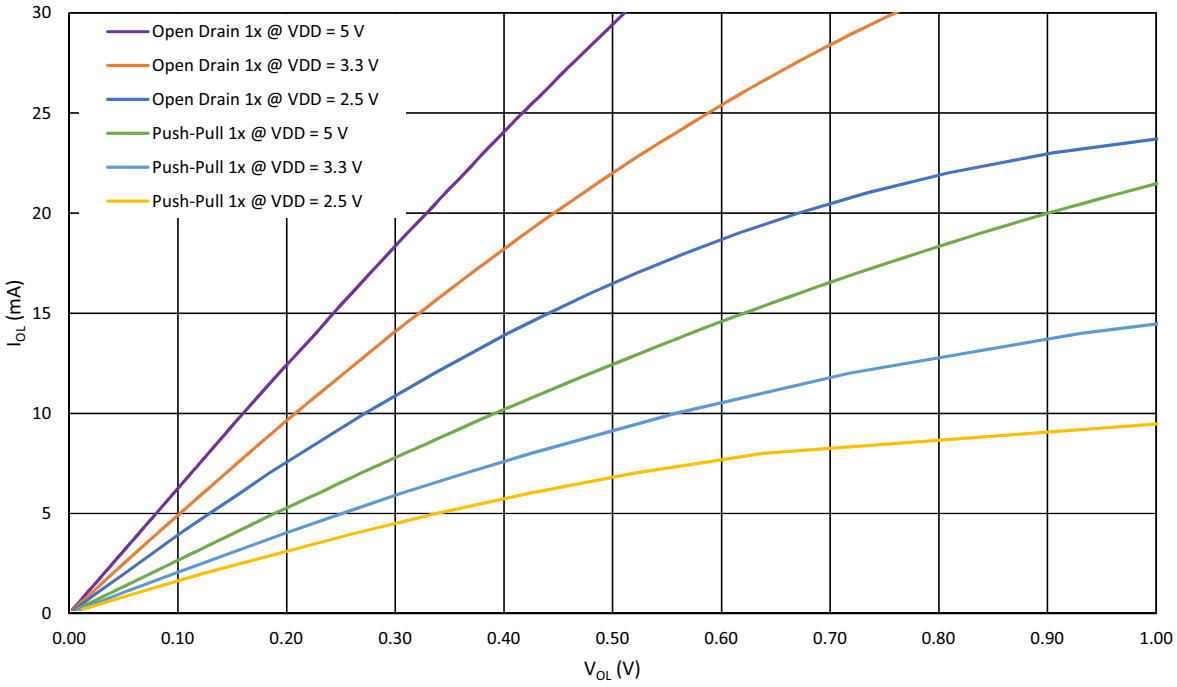

Figure 9: Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T = 25 °C

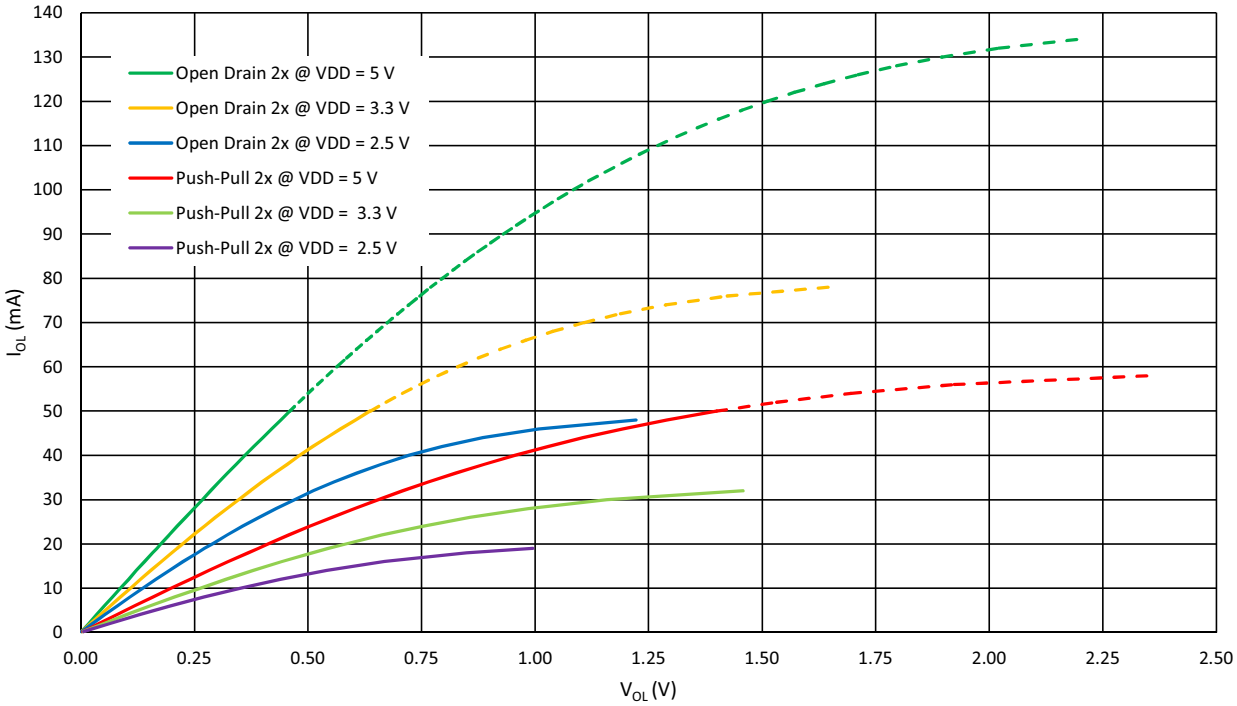

Figure 10: Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T = 25 °C, Full Range

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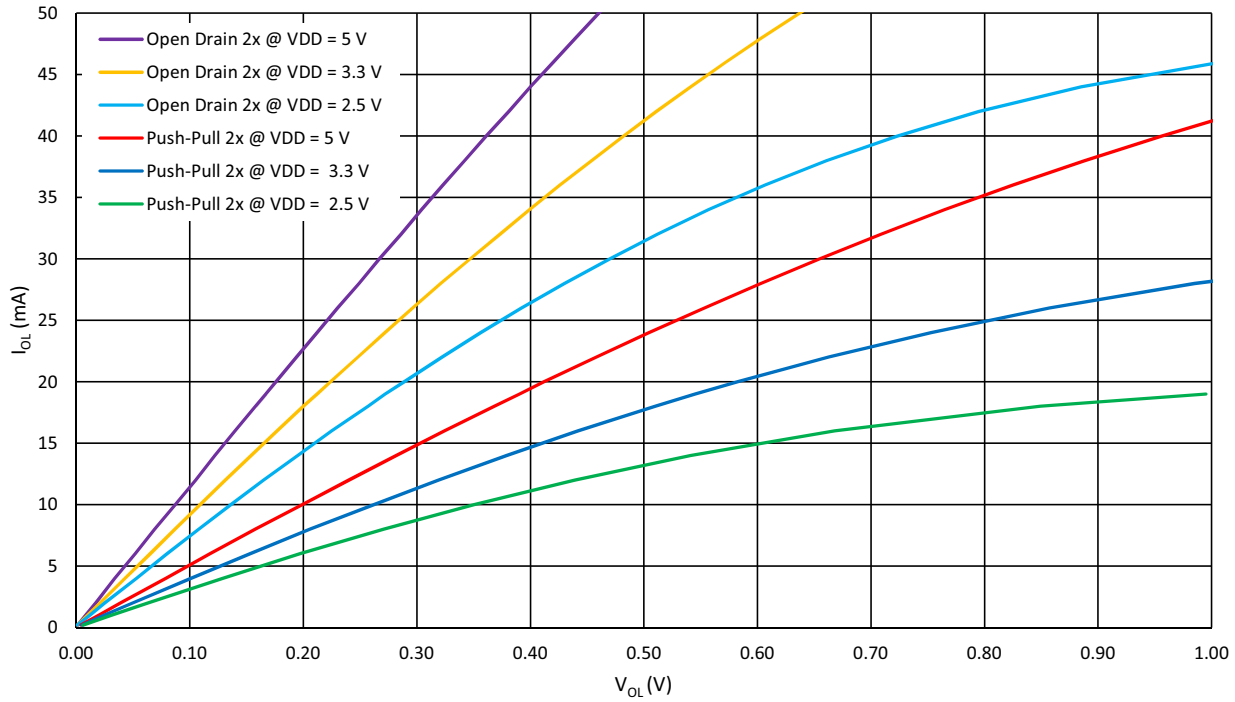

Figure 11: Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T = 25 °C

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6 Connection Matrix

The Connection Matrix in the SLG46826 is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the multiple-time NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG46826 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low”, based on the design that is created. Once the 2048 register bits within the SLG46826 are programmed a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 96 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IOs, LUTs, analog comparators, other digital resources, such as V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG46826’s register table, see Section 18.

Matrix Input Signal Functions	N
GND	0
IO0 Digital In	1
IO1 Digital In	2
IO2 Digital In	3
⋮	⋮
POR OUT	62
V_{DD}	63

Matrix Inputs

Matrix Outputs

N	0	1	2	⋯	95
Registers	registers [5:0]	registers [11:6]	registers [17:12]	⋯	registers [575:570]
Function	Matrix OUT: IN0 of 2-bit LUT0 or Clock Input of DFF0	Matrix OUT: IN1 of 2-bit LUT0 or Data Input of DFF0	Matrix Out: IN0 of 2-bit LUT1 or Clock Input of PGen	⋯	Matrix Output 95

Figure 12: Connection Matrix

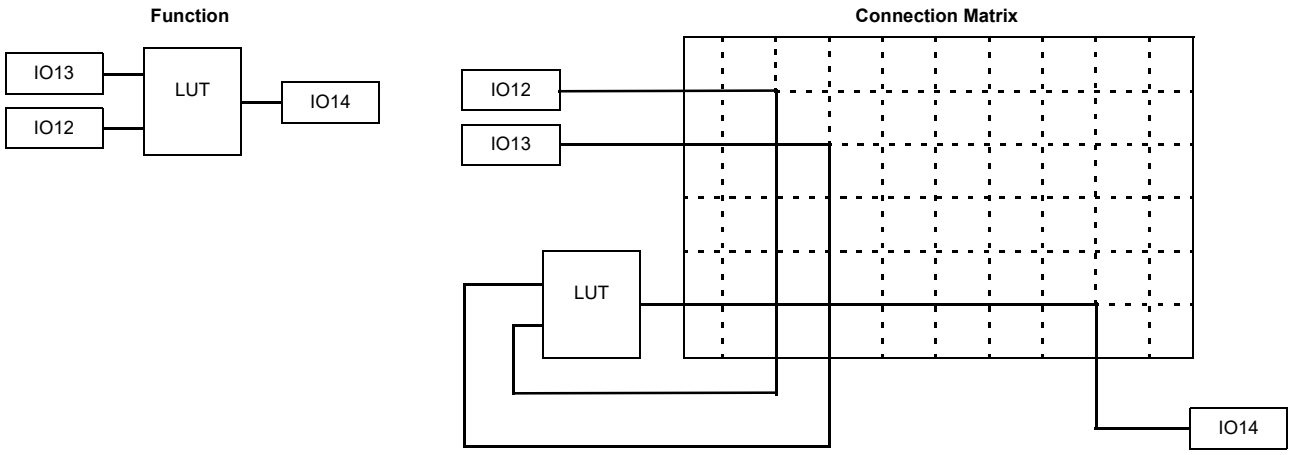

Figure 13: Connection Matrix Example

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6.1 MATRIX INPUT TABLE

Table 21: Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	IO0 Digital Input	0	0	0	0	0	1
2	IO1 Digital Input	0	0	0	0	1	0
3	IO2 Digital Input	0	0	0	0	1	1
4	IO3 Digital Input	0	0	0	1	0	0
5	IO4 Digital Input	0	0	0	1	0	1
6	IO5 Digital Input	0	0	0	1	1	0
7	IO8 Digital Input	0	0	0	1	1	1
8	IO9 Digital Input	0	0	1	0	0	0
9	IO10 Digital Input	0	0	1	0	0	1
10	IO11 Digital Input	0	0	1	0	1	0
11	IO12 Digital Input	0	0	1	0	1	1
12	IO13 Digital Input	0	0	1	1	0	0
13	IO14 Digital Input	0	0	1	1	0	1
14	2-bit LUT0_DFF0_OUT	0	0	1	1	1	0
15	2-bit LUT1_DFF1_OUT	0	0	1	1	1	1
16	2-bit LUT2_DFF2_OUT	0	1	0	0	0	0
17	2-bit LUT3_PGEN_OUT	0	1	0	0	0	1
18	3-bit LUT0_DFF3_OUT	0	1	0	0	1	0
19	3-bit LUT1_DFF4_OUT	0	1	0	0	1	1
20	3-bit LUT2_DFF5_OUT	0	1	0	1	0	0
21	3-bit LUT3_DFF6_OUT	0	1	0	1	0	1
22	3-bit LUT4_DFF7_OUT	0	1	0	1	1	0
23	3-bit LUT5_DFF8_OUT	0	1	0	1	1	1
24	3-bit LUT6_PIPEDLY_RIPP_CNT_OUT0	0	1	1	0	0	0
25	PIPEDLY_RIPP_CNT_OUT1	0	1	1	0	0	1
26	RIPP_CNT_OUT2	0	1	1	0	1	0
27	EDET_FILTER_OUT	0	1	1	0	1	1
28	PROG_DLY_EDET_OUT	0	1	1	1	0	0
29	MULTFUNC_8BIT_1: DLY_CNT_OUT	0	1	1	1	0	1
30	CKOSC1_MATRIX: OSC1 matrix input	0	1	1	1	1	0
31	CKOSC0_MATRIX: OSC0 matrix input	0	1	1	1	1	1
32	CKOSC2_MATRIX: OSC2 matrix input	1	0	0	0	0	0
33	MULTFUNC_8BIT_2: DLY_CNT_OUT	1	0	0	0	0	1
34	MULTFUNC_8BIT_3: DLY_CNT_OUT	1	0	0	0	1	0
35	MULTFUNC_8BIT_4: DLY_CNT_OUT	1	0	0	0	1	1
36	MULTFUNC_8BIT_5: DLY_CNT_OUT	1	0	0	1	0	0
37	MULTFUNC_8BIT_6: DLY_CNT_OUT	1	0	0	1	0	1

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Table 21: Matrix Input Table(Continued)

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
38	MULTFUNC_8BIT_7: DLY_CNT_OUT	1	0	0	1	1	0
39	MULTFUNC_16BIT_0: LUT_DFF_OUT	1	0	0	1	1	1
40	MULTFUNC_8BIT_1: LUT_DFF_OUT	1	0	1	0	0	0
41	MULTFUNC_8BIT_2: LUT_DFF_OUT	1	0	1	0	0	1
42	MULTFUNC_8BIT_3: LUT_DFF_OUT	1	0	1	0	1	0
43	MULTFUNC_8BIT_4: LUT_DFF_OUT	1	0	1	0	1	1
44	MULTFUNC_8BIT_5: LUT_DFF_OUT	1	0	1	1	0	0
45	MULTFUNC_8BIT_6: LUT_DFF_OUT	1	0	1	1	0	1
46	MULTFUNC_8BIT_7: LUT_DFF_OUT	1	0	1	1	1	0
47	MULTFUNC_16BIT_0: DLY_CNT_OUT	1	0	1	1	1	1
48	I^2C_virtual_7 Input: register [976]	1	1	0	0	0	0
49	I^2C_virtual_6 Input: register [977]	1	1	0	0	0	1
50	I^2C_virtual_5 Input: register [978]	1	1	0	0	1	0
51	I^2C_virtual_4 Input: register [979]	1	1	0	0	1	1
52	I^2C_virtual_3 Input: register [980]	1	1	0	1	0	0
53	I^2C_virtual_2 Input: register [981]	1	1	0	1	0	1
54	I^2C_virtual_1 Input: register [982]	1	1	0	1	1	0
55	I^2C_virtual_0 Input: register [983]	1	1	0	1	1	1
56	ACMP0H_OUT	1	1	1	0	0	0
57	ACMP1H_OUT	1	1	1	0	0	1
58	ACMP2L_OUT	1	1	1	0	1	0
59	ACMP3L_OUT	1	1	1	0	1	1
60	2nd CKOSC1_MATRIX	1	1	1	1	0	0
61	2nd CKOSC0_MATRIX	1	1	1	1	0	1
62	POR OUT	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

6.2 MATRIX OUTPUT TABLE

Table 22: Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
5:0	IN0 of 2-bit LUT0 or Clock Input of DFF0	0
11:6	IN1 of 2-bit LUT0 or Data Input of DFF0	1
17:12	IN0 of 2-bit LUT3 or Clock Input of PGen	2
23:18	IN1 of 2-bit LUT3 or nRST of PGen	3
29:24	IN0 of 2-bit LUT1 or Clock Input of DFF1	4
35:30	IN1 of 2-bit LUT1 or Data Input of DFF1	5
41:36	IN0 of 2-bit LUT2 or Clock Input of DFF2	6
47:42	IN1 of 2-bit LUT2 or Data Input of DFF2	7
53:48	IN0 of 3-bit LUT0 or Clock Input of DFF3	8

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Table 22: Matrix Output Table(Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
59:54	IN1 of 3-bit LUT0 or Data Input of DFF3	9
65:60	IN2 of 3-bit LUT0 or nRST(nSET) of DFF3	10
71:66	IN0 of 3-bit LUT1 or Clock Input of DFF4	11
77:72	IN1 of 3-bit LUT1 or Data Input of DFF4	12
83:78	IN2 of 3-bit LUT1 or nRST(nSET) of DFF4	13
89:84	IN0 of 3-bit LUT2 or Clock Input of DFF5	14
95:90	IN1 of 3-bit LUT2 or Data Input of DFF5	15
101:96	IN2 of 3-bit LUT2 or nRST(nSET) of DFF5	16
107:102	IN0 of 3-bit LUT3 or Clock Input of DFF6	17
113:108	IN1 of 3-bit LUT3 or Data Input of DFF6	18
119:114	IN2 of 3-bit LUT3 or nRST(nSET) of DFF6	19
125:120	IN0 of 3-bit LUT4 or Clock Input of DFF7	20
131:126	IN1 of 3-bit LUT4 or Data Input of DFF7	21
137:132	IN2 of 3-bit LUT4 or nRST(nSET) of DFF7	22
143:138	IN0 of 3-bit LUT5 or Clock Input of DFF8	23
149:144	IN1 of 3-bit LUT5 or Data Input of DFF8	24
155:150	IN2 of 3-bit LUT5 or nRST(nSET) of DFF8	25
161:156	IN0 of 3-bit LUT6 or Input of Pipe Delay or UP Signal of RIPP CNT	26
167:162	IN1 of 3-bit LUT6 or nRST of Pipe Delay or STB of RIPP CNT	27
173:168	IN2 of 3-bit LUT6 or Clock of Pipe Delay_RIPP_CNT	28
179:174	Reserved	29
185:180	MULTFUNC_16BIT_0: IN0 of 4-bit LUT0 or Clock Input of DFF9; Delay0 Input (or Counter0 nRST/SET Input)	30
191:186	MULTFUNC_16BIT_0: IN1 of 4-bit LUT0 or nRST of DFF9; Delay0 Input (or Counter0 nRST Input) or Delay/Counter0 External Clock Source	31
197:192	MULTFUNC_16BIT_0: IN2 of 4-bit LUT0 or nSET of DFF9 or KEEP Input of FSM0 or External Clock Input of Delay0 (or Counter0)	32
203:198	MULTFUNC_16BIT_0: IN3 of 4-bit LUT0 or Data Input of DFF9; Delay0 Input (or Counter0 nRST Input) or UP Input of FSM0	33
209:204	MULTFUNC_8BIT_1: IN0 of 3-bit LUT7 or Clock Input of DFF10; Delay1 Input (or Counter1 nRST Input)	34
215:210	MULTFUNC_8BIT_1: IN1 of 3-bit LUT7 or nRST (nSET) of DFF10; Delay1 Input (or Counter1 nRST Input) or Delay/Counter1 External Clock Source	35
221:216	MULTFUNC_8BIT_1: IN2 of 3-bit LUT7 or Data Input of DFF10; Delay1 Input (or Counter1 nRST Input)	36
227:222	MULTFUNC_8BIT_2: IN0 of 3-bit LUT8 or Clock Input of DFF11; Delay2 Input (or Counter2 nRST Input)	37
233:228	MULTFUNC_8BIT_2: IN1 of 3-bit LUT8 or nRST (nSET) of DFF11; Delay2 Input (or Counter2 nRST Input) or Delay/Counter2 External Clock Source	38
239:234	MULTFUNC_8BIT_2: IN2 of 3-bit LUT8 or Data Input of DFF11; Delay2 Input (or Counter2 nRST Input)	39
245:240	MULTFUNC_8BIT_3: IN0 of 3-bit LUT9 or Clock Input of DFF12; Delay3 Input (or Counter3 nRST Input)	40

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Table 22: Matrix Output Table(Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
251:246	MULTFUNC_8BIT_3: IN1 of 3-bit LUT9 or nRST (nSET) of DFF12; Delay3 Input (or Counter3 nRST Input) or Delay/Counter3 External Clock Source	41
257:252	MULTFUNC_8BIT_3: IN2 of 3-bit LUT9 or Data Input of DFF12; Delay3 Input (or Counter3 nRST Input)	42
263:258	MULTFUNC_8BIT_4: IN0 of 3-bit UT10 or Clock Input of DFF13; Delay4 Input (or Counter4 nRST Input)	43
269:264	MULTFUNC_8BIT_4: IN1 of 3-bit LUT10 or nRST (nSET) of DFF13; Delay4 Input (or Counter4 nRST Input) or Delay/Counter4 External Clock Source	44
275:270	MULTFUNC_8BIT_4: IN2 of 3-bit LUT10 or Data Input of DFF13; Delay4 Input (or Counter4 nRST Input)	45
281:276	MULTFUNC_8BIT_5: IN0 of 3-bit LUT11 or Clock Input of DFF14; Delay5 Input (or Counter5 nRST Input)	46
287:282	MULTFUNC_8BIT_5: IN1 of 3-bit LUT11 or nRST (nSET) of DFF14; Delay5 Input (or Counter5 nRST Input) or Delay/Counter5 External Clock Source	47
293:288	MULTFUNC_8BIT_5: IN2 of 3-bit LUT11 or Data Input of DFF14; Delay5 Input (or Counter5 nRST Input)	48
299:294	MULTFUNC_8BIT_6: IN0 of 3-bit LUT12 or Clock Input of DFF15; Delay6 Input (or Counter6 nRST Input)	49
305:300	MULTFUNC_8BIT_6: IN1 of 3-bit LUT12 or nRST (nSET) of DFF15; Delay6 Input (or Counter6 nRST Input) or Delay/Counter6 External Clock Source	50
311:306	MULTFUNC_8BIT_6: IN2 of 3-bit LUT12 or Data Input of DFF15; Delay6 Input (or Counter6 nRST Input)	51
317:312	MULTFUNC_8BIT_7: IN0 of 3-bit LUT13 or Clock Input of DFF16; Delay7 Input (or Counter7 nRST Input)	52
323:318	MULTFUNC_8BIT_7: IN1 of 3-bit LUT13 or nRST (nSET) of DFF16; Delay7 Input (or Counter7 nRST Input) or Delay/Counter7 External Clock Source	53
329:324	MULTFUNC_8BIT_7: IN2 of 3-bit LUT13 or Data Input of DFF16; Delay7 Input (or Counter7 nRST Input)	54
335:330	Filter/Edge detect input	55
341:336	Programmable delay/edge detect input	56
347:342	OSC2 ENABLE from matrix	57
353:348	OSC0 ENABLE from matrix	58
359:354	OSC1 ENABLE matrix	59
365:360	Temp sensor and Vref PD from matrix	60
371:366	BG power-down from matrix	61
377:372	PWR UP of ACMP0H from matrix	62
383:378	PWR UP of ACMP1H from matrix	63
389:384	PWR UP of ACMP2L from matrix	64
395:390	PWR UP of ACMP3L from matrix	65
401:396	Reserved	66
407:402	IO0 Digital Output	67
413:408	IO1 Digital Output	68
419:414	IO1 Digital Output OE	69
425:420	IO2 Digital Output	70

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Table 22: Matrix Output Table(Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
431:426	IO3 Digital Output	71
437:432	IO4 Digital Output	72
443:438	IO4 Digital Output OE	73
449:444	IO5 Digital Output	74
455:450	IO5 Digital Output OE	75
461:456	IO6 Digital Output	76
467:462	IO7 Digital Output	77
473:468	IO8 Digital Output	78
479:474	IO8 Digital Output OE	79
485:480	IO9 Digital Output	80
491:486	IO9 Digital Output OE	81
497:492	IO10 Digital Output	82
503:498	IO10 Digital Output OE	83
509:504	IO11 Digital Output	84
515:510	IO11 Digital Output OE	85
521:516	IO12 Digital Output	86
527:522	IO12 Digital Output OE	87
533:528	IO13 Digital Output	88
539:534	IO13 Digital Output OE	89
545:540	IO14 Digital Output	90
551:546	IO14 Digital Output OE	91
557:552	Reserved	92
563:558	Reserved	93
569:564	Matrix OUT 94	94
575:570	Matrix OUT 95	95
Note 1 For each Address, the two most significant bits are unused.		

6.3 CONNECTION MATRIX VIRTUAL INPUTS

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at 0x7A (0122).

An I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

See Table 23.

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Table 23: Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
55	I^2C_virtual_0 Input	[983]
54	I^2C_virtual_1 Input	[982]
53	I^2C_virtual_2 Input	[981]
52	I^2C_virtual_3 Input	[980]
51	I^2C_virtual_4 Input	[979]
50	I^2C_virtual_5 Input	[978]
49	I^2C_virtual_6 Input	[977]
48	I^2C_virtual_7 Input	[976]

6.4 CONNECTION MATRIX VIRTUAL OUTPUTS

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via I^2C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I^2C addresses for reading these register values are 0x74 (0116) to 0x7B (0123). Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at 0x7A (0122)).

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7 Combination Function Macrocells

The SLG46826 has 11 combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells.

- Three macrocells that can serve as either 2-bit LUT or as D Flip-Flop
- Six macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay/Ripple Counter
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGen)

Inputs/Outputs for the 11 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

7.1 2-BIT LUT OR D FLIP-FLOP MACROCELLS

There are three macrocells that can serve as either 2-bit LUT or as D Flip-Flop. When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change

LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

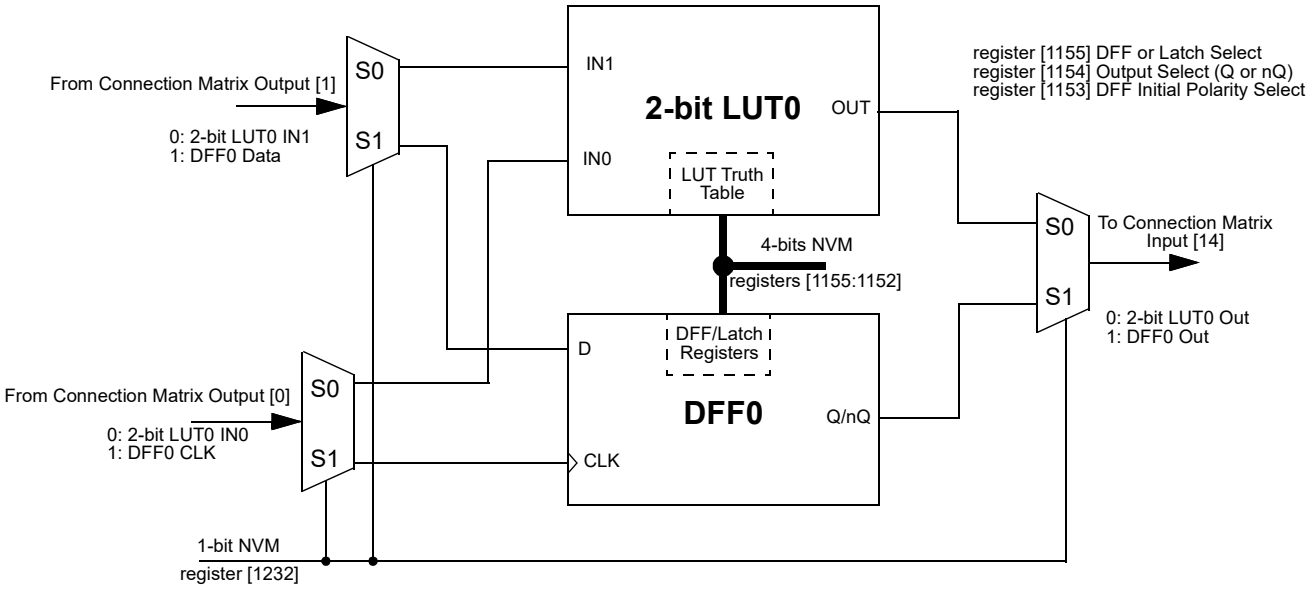

Figure 14: 2-bit LUT0 or DFF0

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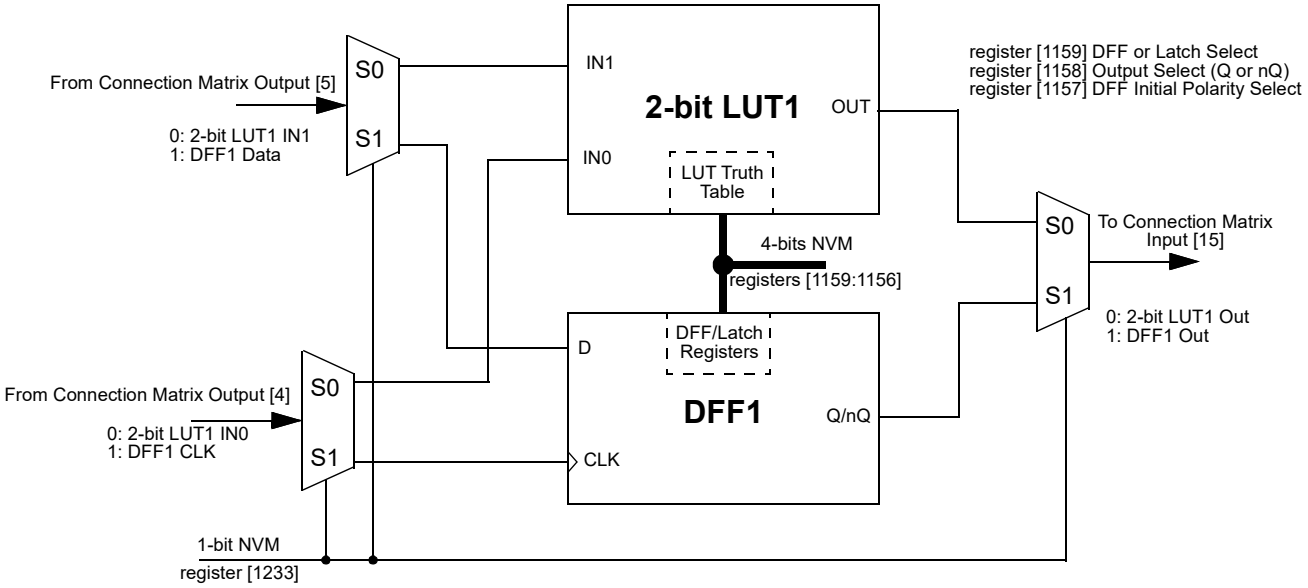

Figure 15: 2-bit LUT1 or DFF1

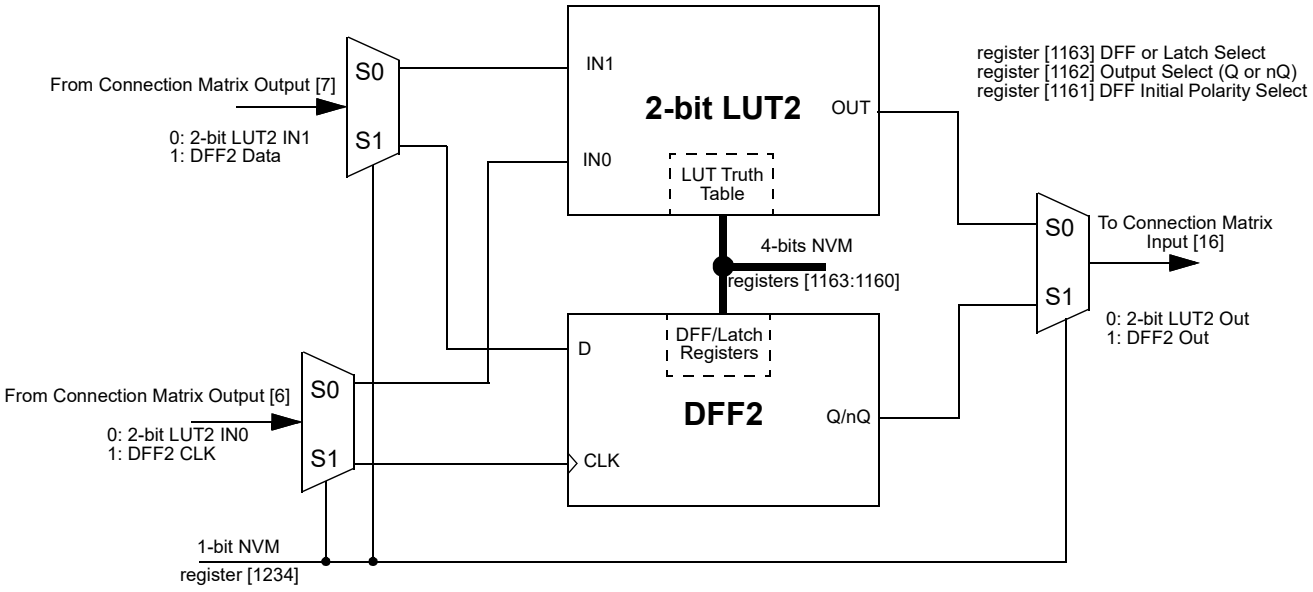

Figure 16: 2-bit LUT2 or DFF2

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7.1.1 2-Bit LUT or D Flip-Flop Macrocell Used as 2-Bit LUT

Table 24: 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	register [1152]	LSB
0	1	register [1153]	
1	0	register [1154]	
1	1	register [1155]	MSB

Table 25: 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1156]	LSB
0	1	register [1157]	
1	0	register [1158]	
1	1	register [1159]	MSB

Table 26: 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	register [1160]	LSB
0	1	register [1161]	
1	0	register [1162]	
1	1	register [1163]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by registers [1155:1152]

2-Bit LUT1 is defined by registers [1159:1156]

2-Bit LUT2 is defined by registers [1163:1160]

Table 27 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 27: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

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7.1.2 Initial Polarity Operations

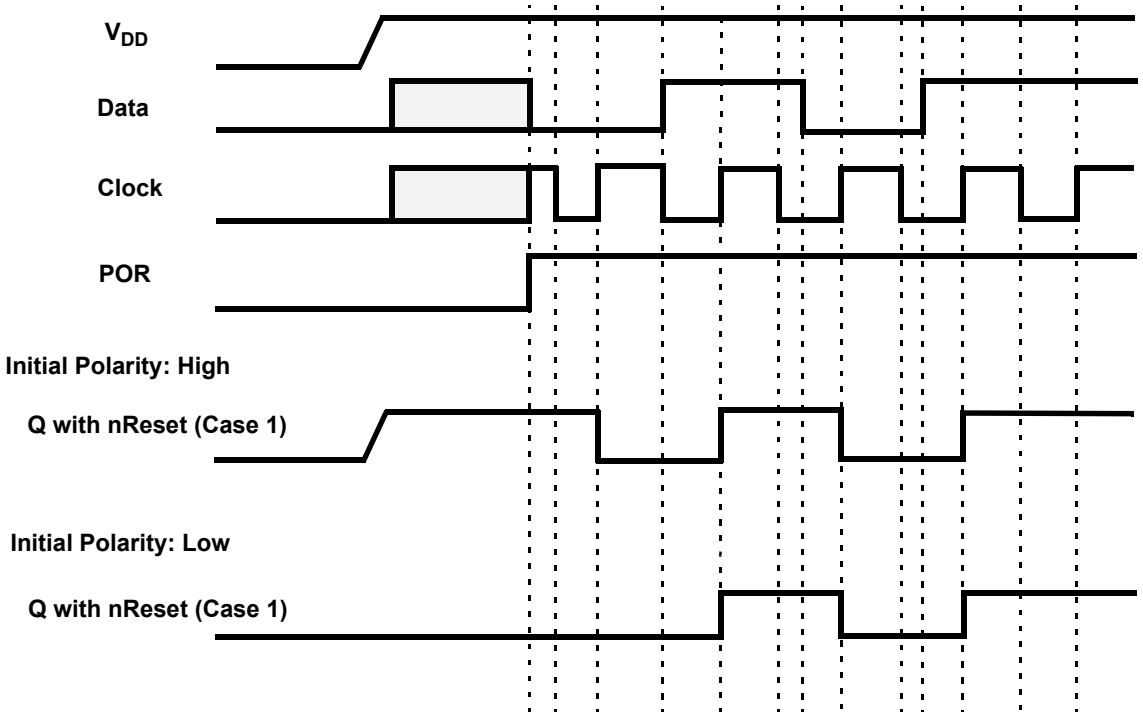

Figure 17: DFF Polarity Operations

7.2 2-BIT LUT OR PROGRAMMABLE PATTERN GENERATOR

The SLG46826 has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or Programmable Pattern Generator (PGen).

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUT can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

When operating as a Programmable Pattern Generator, the output of the macrocell with clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.

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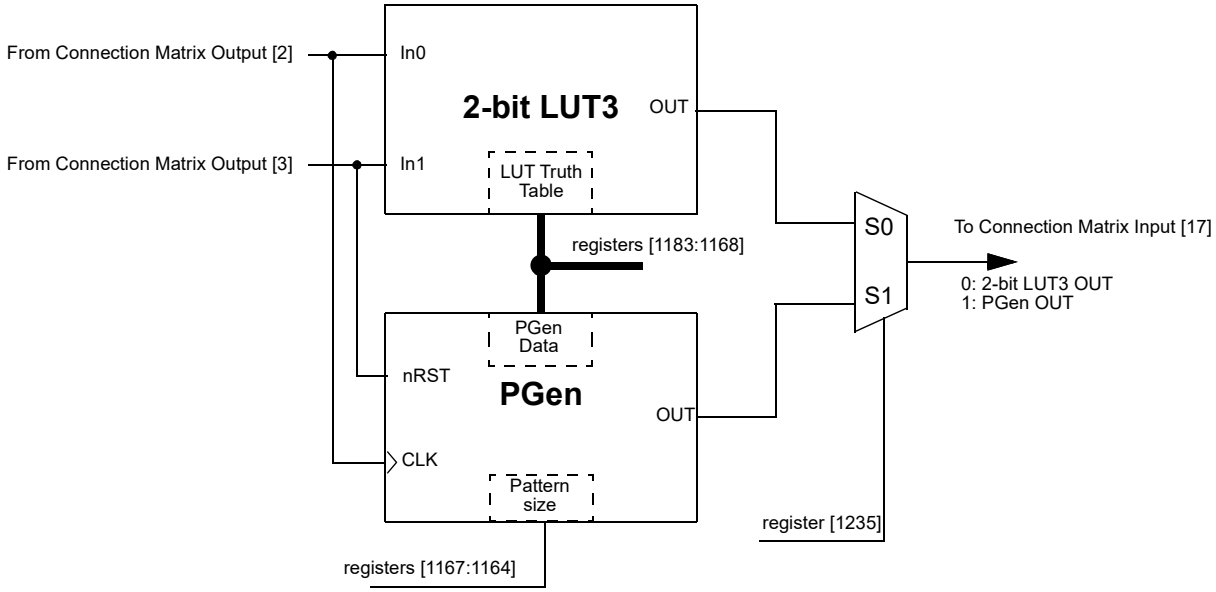

Figure 18: 2-bit LUT3 or PGen

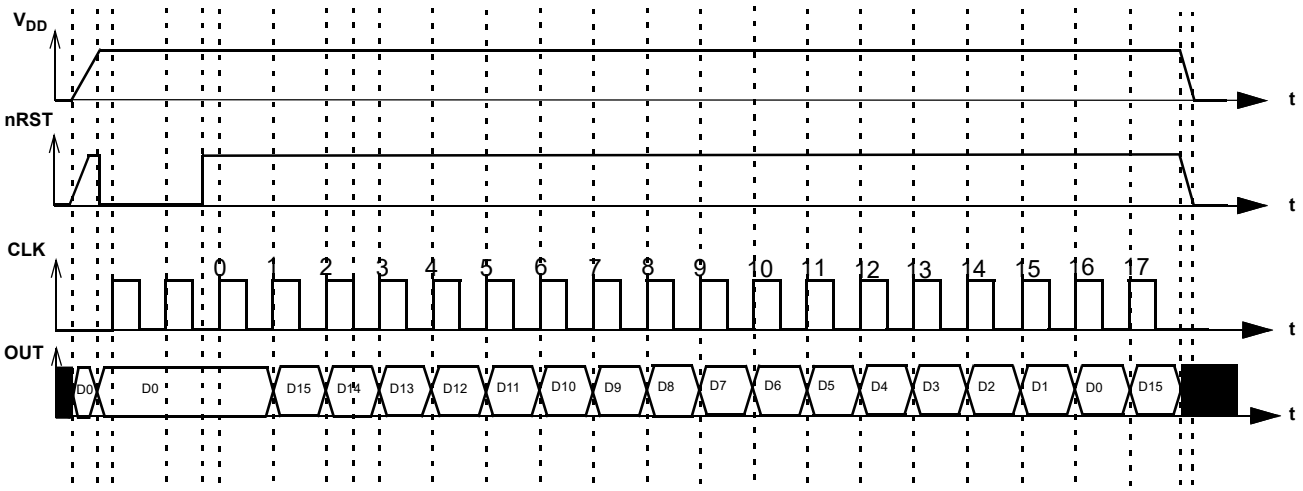

Figure 19: PGen Timing Diagram

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7.2.1 2-Bit LUT or PGen Macrocell Used as 2-Bit LUT

Table 28: 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1164]	LSB
0	1	register [1165]	
1	0	register [1166]	
1	1	register [1167]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

*2-Bit LUT3 is defined by [*1167*:*1164*]*

Table 29 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 29: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.3 3-BIT LUT OR D FLIP-FLOP WITH SET/RESET MACROCELLS

There are six macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix.

DFF3 operation is described below:

- If register [1237] = 0, and the CLK is rising edge triggered, then Q=D, otherwise Q will not change
- If register [1237] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

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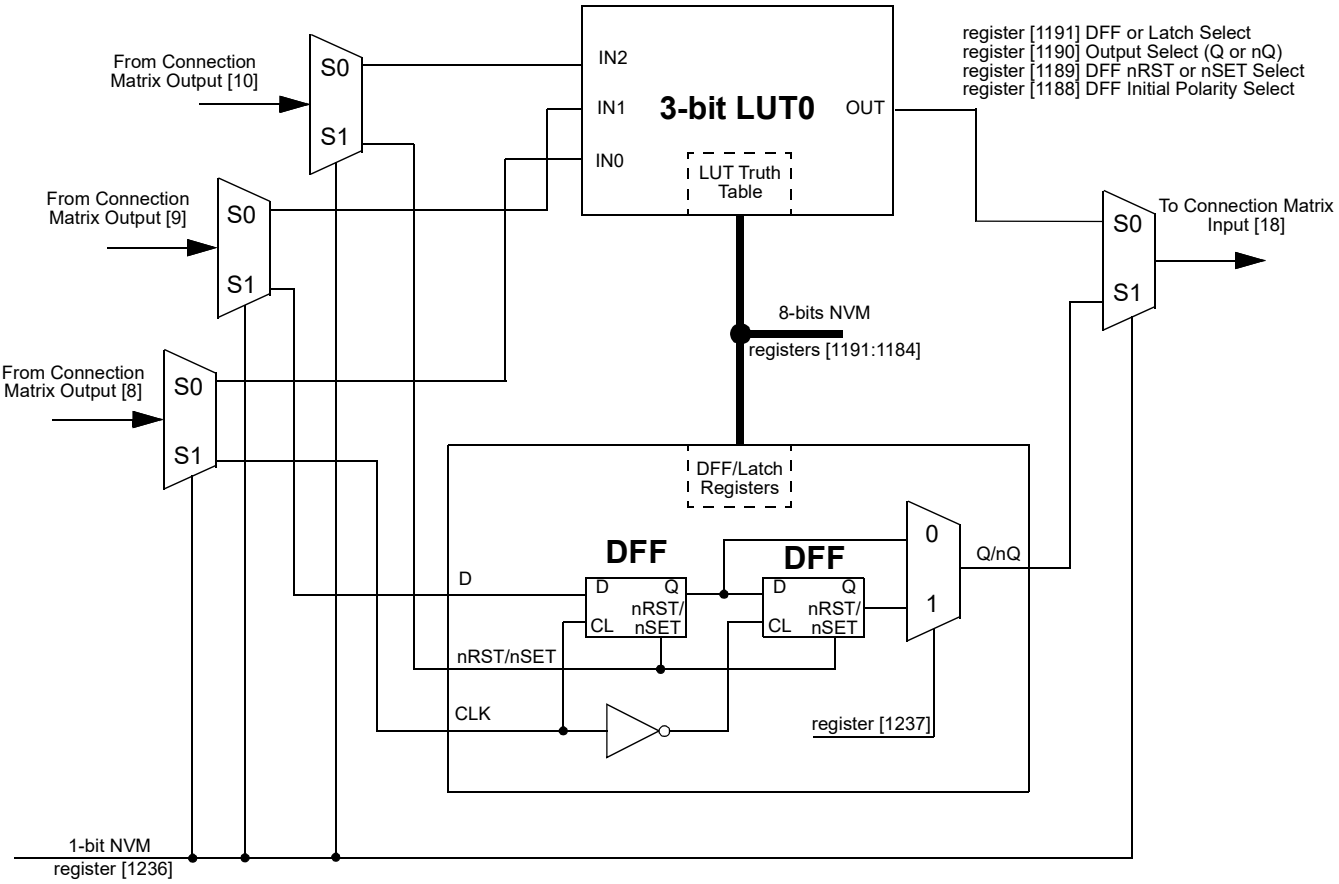

Figure 20: 3-bit LUT0 or DFF3

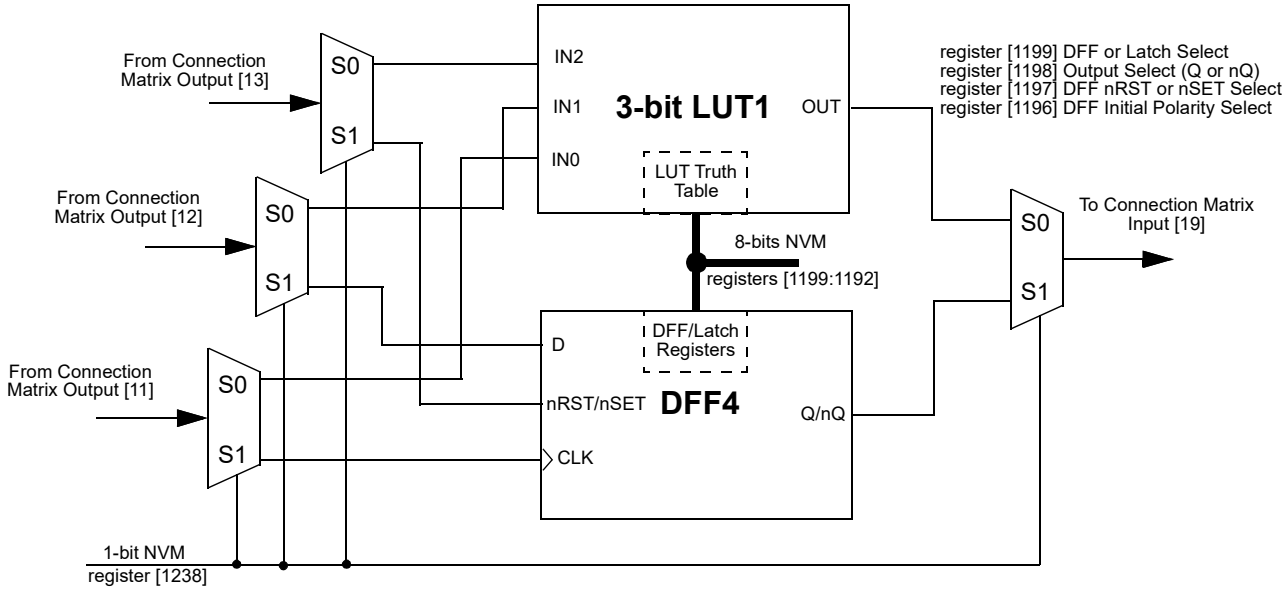

Figure 21: 3-bit LUT1 or DFF4

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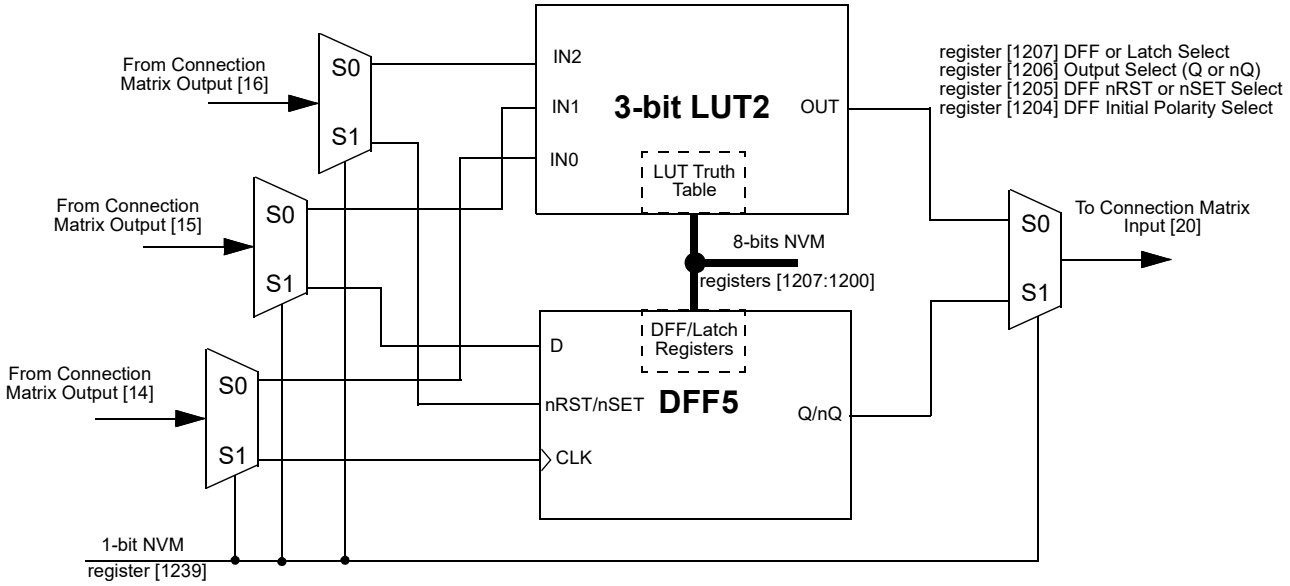

Figure 22: 3-bit LUT2 or DFF5

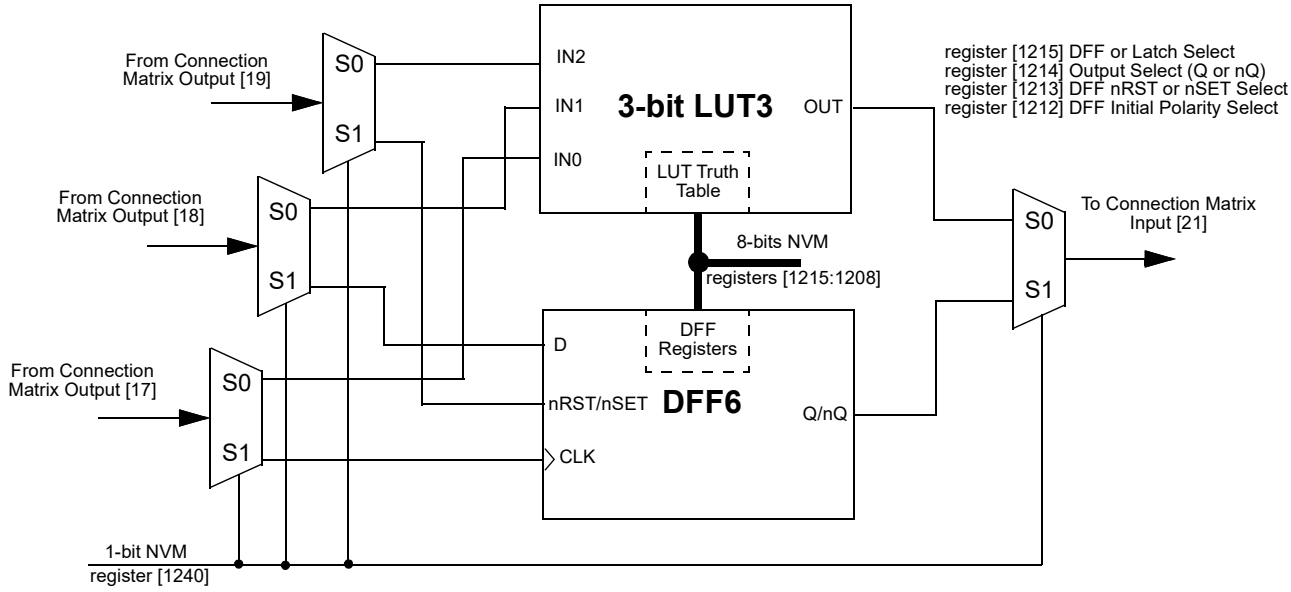

Figure 23: 3-bit LUT3 or DFF6

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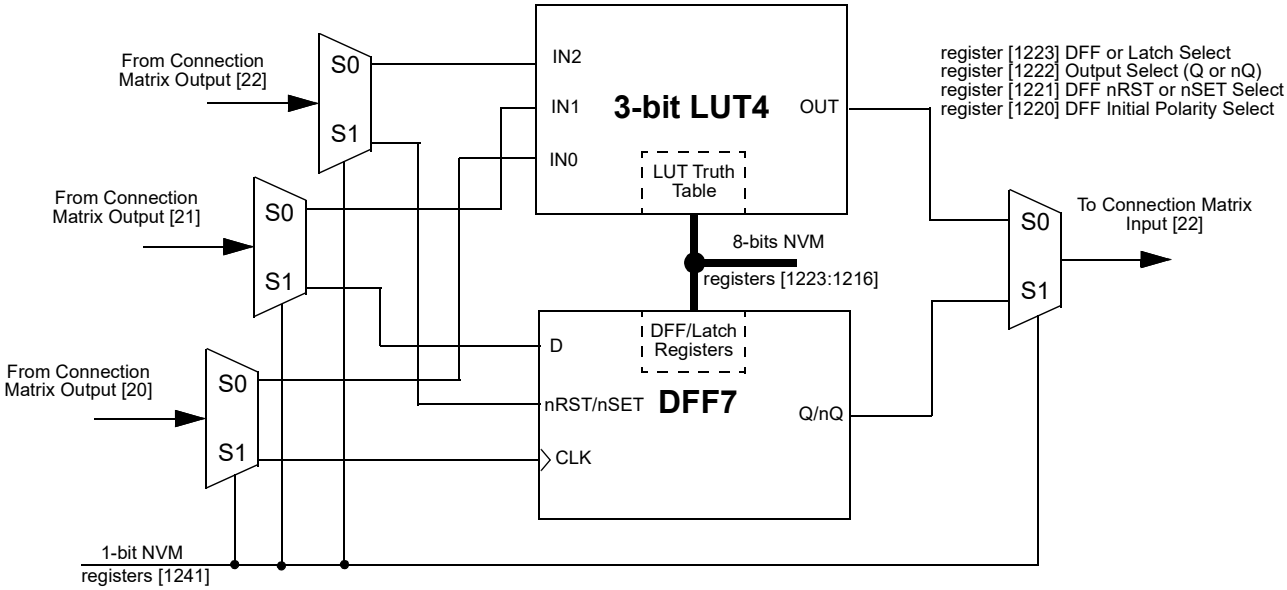

Figure 24: 3-bit LUT4 or DFF7

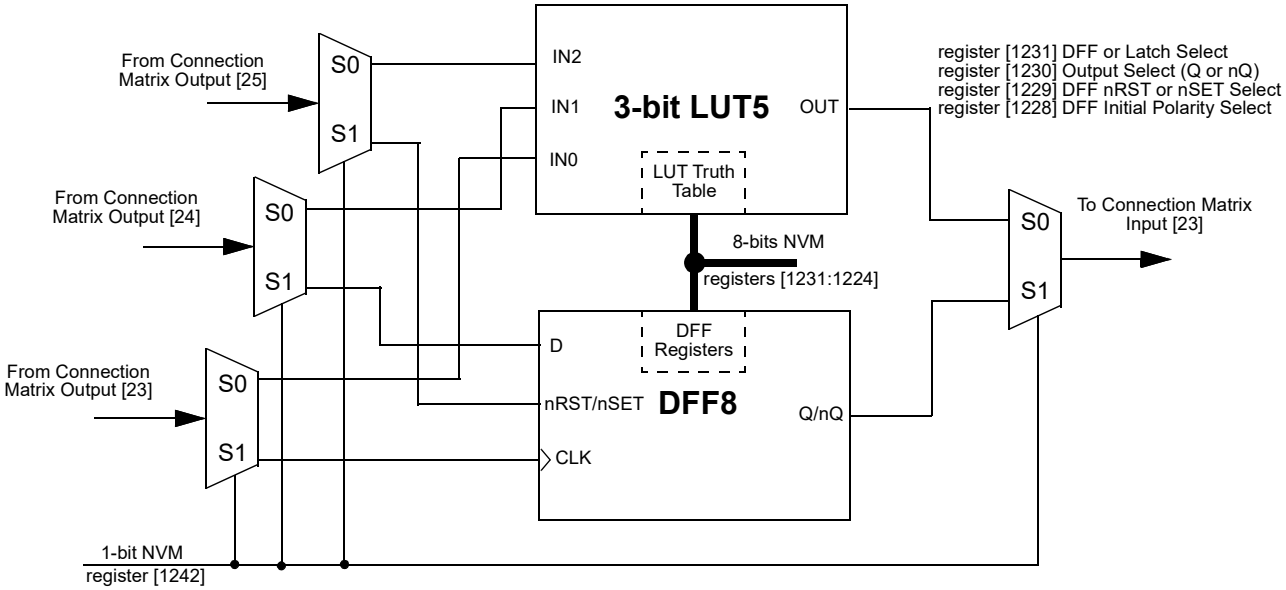

Figure 25: 3-bit LUT5 or DFF8

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7.3.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Table 30: 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1184]	LSB
0	0	1	register [1185]	
0	1	0	register [1186]	
0	1	1	register [1187]	
1	0	0	register [1188]	
1	0	1	register [1189]	
1	1	0	register [1190]	
1	1	1	register [1191]	MSB

Table 31: 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1192]	LSB
0	0	1	register [1193]	
0	1	0	register [1194]	
0	1	1	register [1195]	
1	0	0	register [1196]	
1	0	1	register [1197]	
1	1	0	register [1198]	
1	1	1	register [1199]	MSB

Table 32: 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1200]	LSB
0	0	1	register [1201]	
0	1	0	register [1202]	
0	1	1	register [1203]	
1	0	0	register [1204]	
1	0	1	register [1205]	
1	1	0	register [1206]	
1	1	1	register [1207]	MSB

Table 33: 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1208]	LSB
0	0	1	register [1209]	
0	1	0	register [1210]	
0	1	1	register [1211]	
1	0	0	register [1212]	
1	0	1	register [1213]	
1	1	0	register [1214]	
1	1	1	register [1215]	MSB

Table 34: 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1216]	LSB
0	0	1	register [1217]	
0	1	0	register [1218]	
0	1	1	register [1219]	
1	0	0	register [1220]	
1	0	1	register [1221]	
1	1	0	register [1222]	
1	1	1	register [1223]	MSB

Table 35: 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1224]	LSB
0	0	1	register [1225]	
0	1	0	register [1226]	
0	1	1	register [1227]	
1	0	0	register [1228]	
1	0	1	register [1229]	
1	1	0	register [1230]	
1	1	1	register [1231]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT0 is defined by registers [1191:1184]

3-Bit LUT1 is defined by registers [1199:1192]

3-Bit LUT2 is defined by registers [1207:1200]

3-Bit LUT3 is defined by registers [1215:1208]

3-Bit LUT4 is defined by registers [1223:1216]

3-Bit LUT5 is defined by registers [1231:1224]

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Table 36 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 36: 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

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7.3.2 Initial Polarity Operations

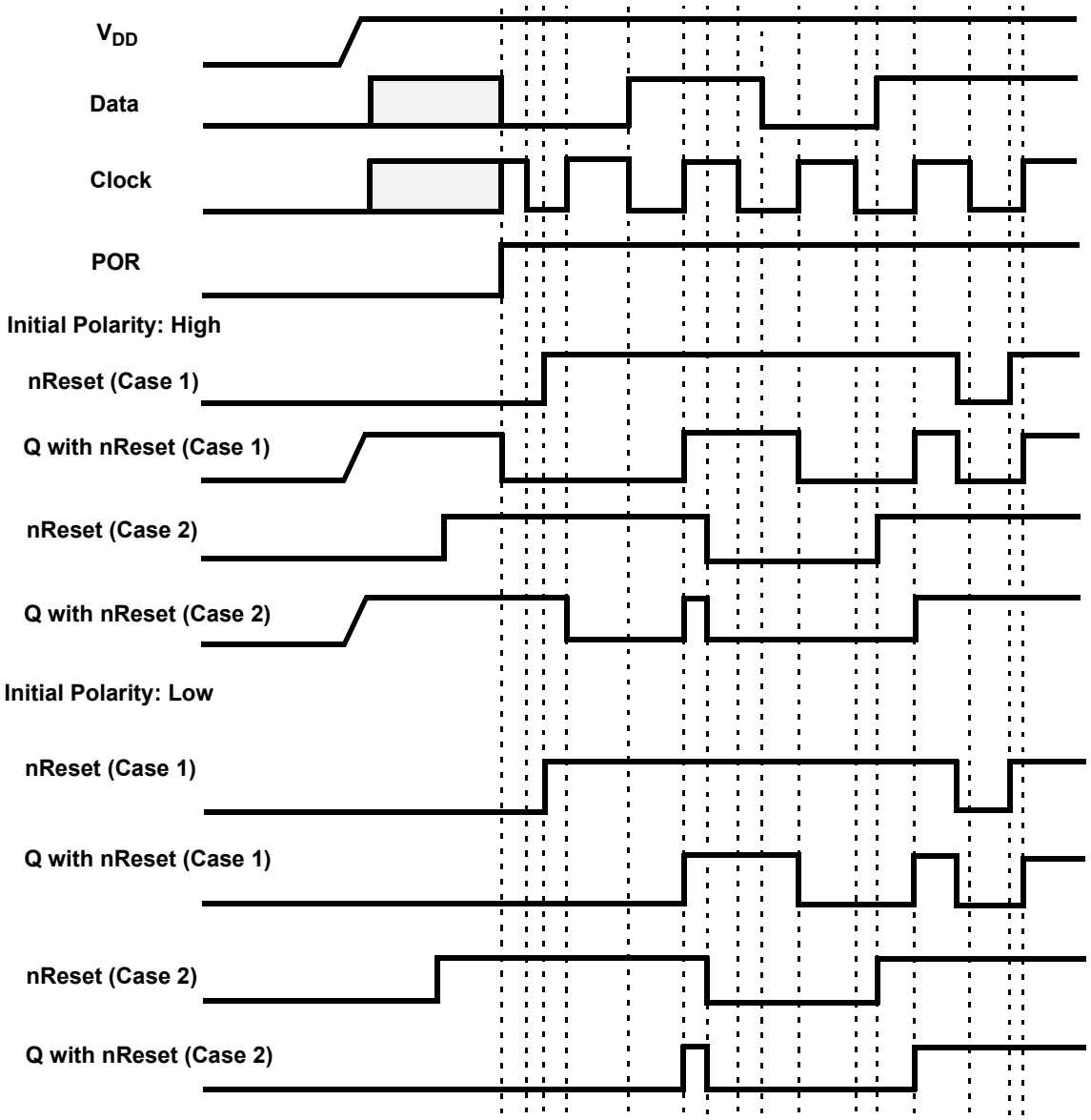

Figure 26: DFF Polarity Operations with nReset

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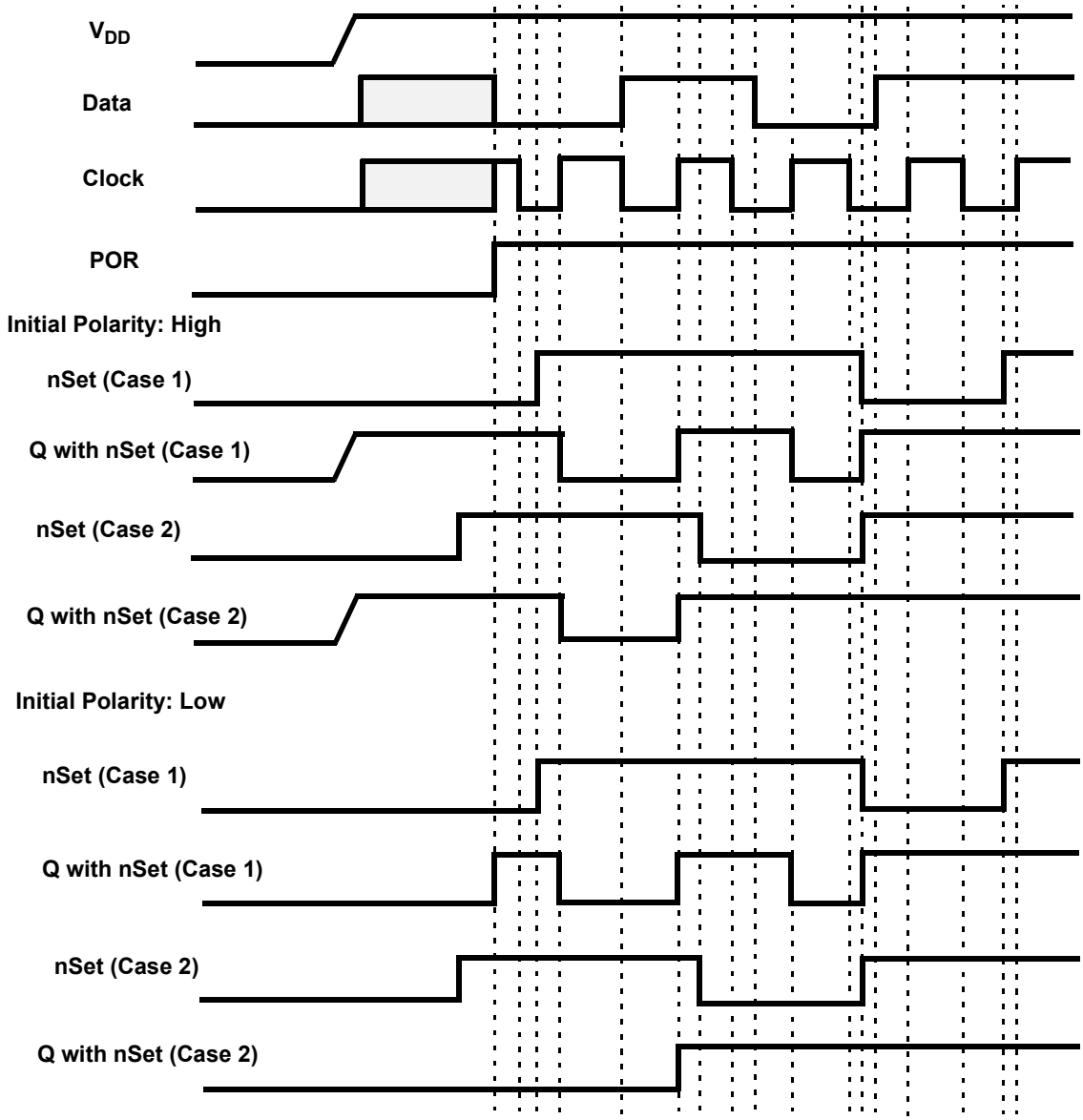

Figure 27: DFF Polarity Operations with nSet

7.4 3-BIT LUT OR PIPE DELAY/RIPPLE COUNTER MACROCELL

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay/Ripple Counter.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a Pipe Delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK), and Reset (nRST). The Pipe Delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell input (IN). Both of the two outputs (OUT0 and OUT1) provide user selectable options for 1 to 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by registers [1251:1248] for OUT0 and registers [1255:1252] for OUT1. The 4-input mux is used to control the selection of the amount of delay.

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The overall time of the delay is based on the clock used in the SLG46826 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the internal Oscillator within the SLG46826). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell. OUT1 Output can be inverted (as selected by register [1256]).

In the Ripple Counter mode, there are 3 options for setting, which use 7 bits. There are 3 bits to set **nSET value (SV)** in range from 0 to 7. It is a value, which will be set into the Ripple Counter outputs when nSET input goes LOW. **End value (EV)** will use 3 bits for setting outputs code, which will be last code in the cycle. After reaching the EV, the Ripple Counter goes to the first code by the rising edge on CLK input. The **Functionality mode** option uses 1 bit. This setting defines how exactly Ripple Counter will operate.

The user can select one of the functionality modes by register: RANGE or FULL. If the RANGE option is selected, the count starts from SV. If UP input is LOW the count goes down: SV→EV→EV-1 to SV+1→SV and others (if SV is smaller than EV), or SV→SV-1 to EV+1→EV→SV (if SV is bigger than EV). If UP input is HIGH, count starts from SV up to EV, and others.

In the FULL range configuration the Ripple Counter functions as follows. If UP input is LOW, the count starts from SV and goes down to 0. Then current counter value jumps to EV and goes down to 0 etc.

If UP input is HIGH, count goes up starting from SV. Then current counter value jumps to 0 and counts up to EV, and others. See Ripple Counter functionality example in Figure 29.

Every step is executed by the rising edge on CLK input.

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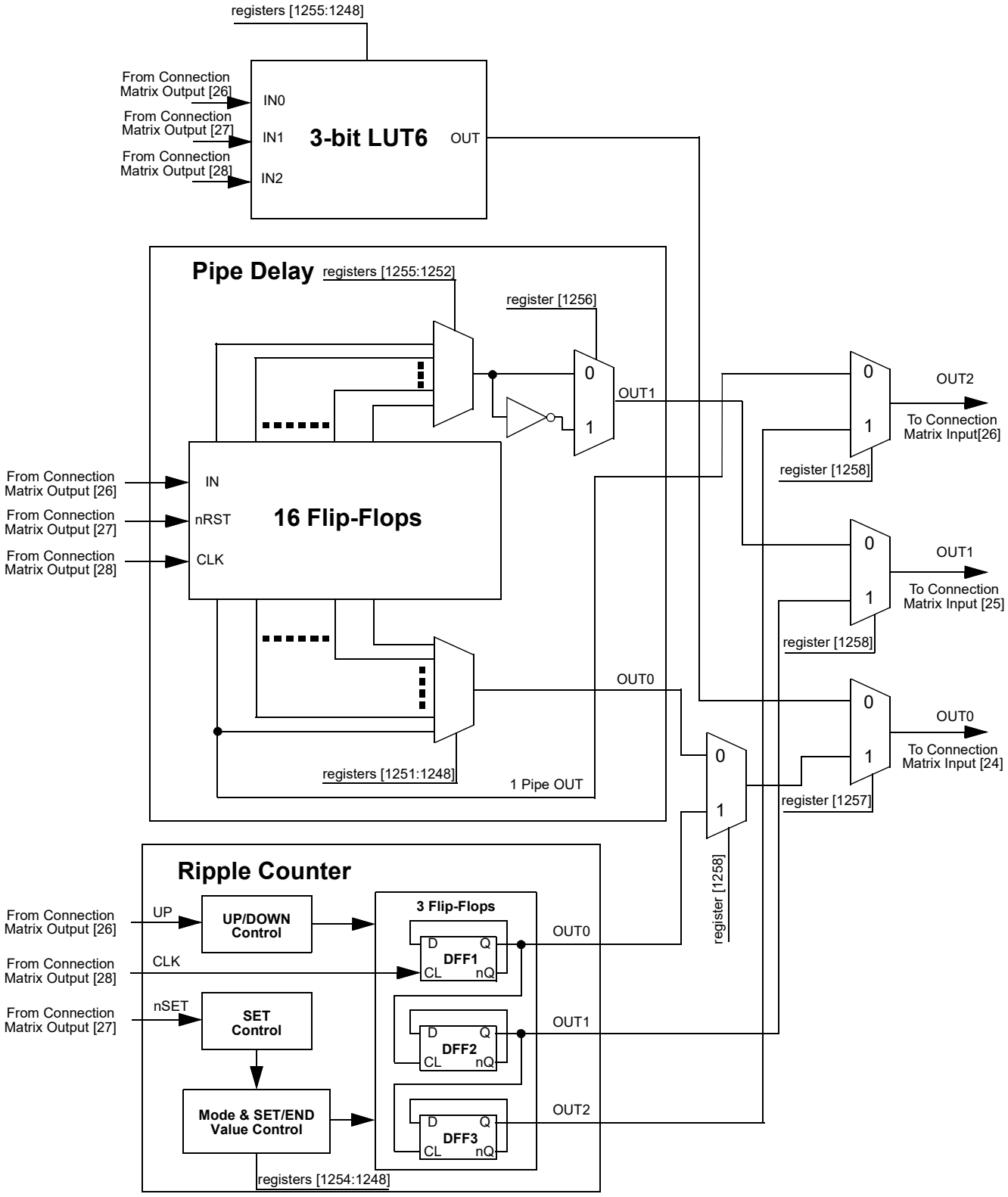

Figure 28: 3-bit LUT6/Pipe Delay/Ripple Counter

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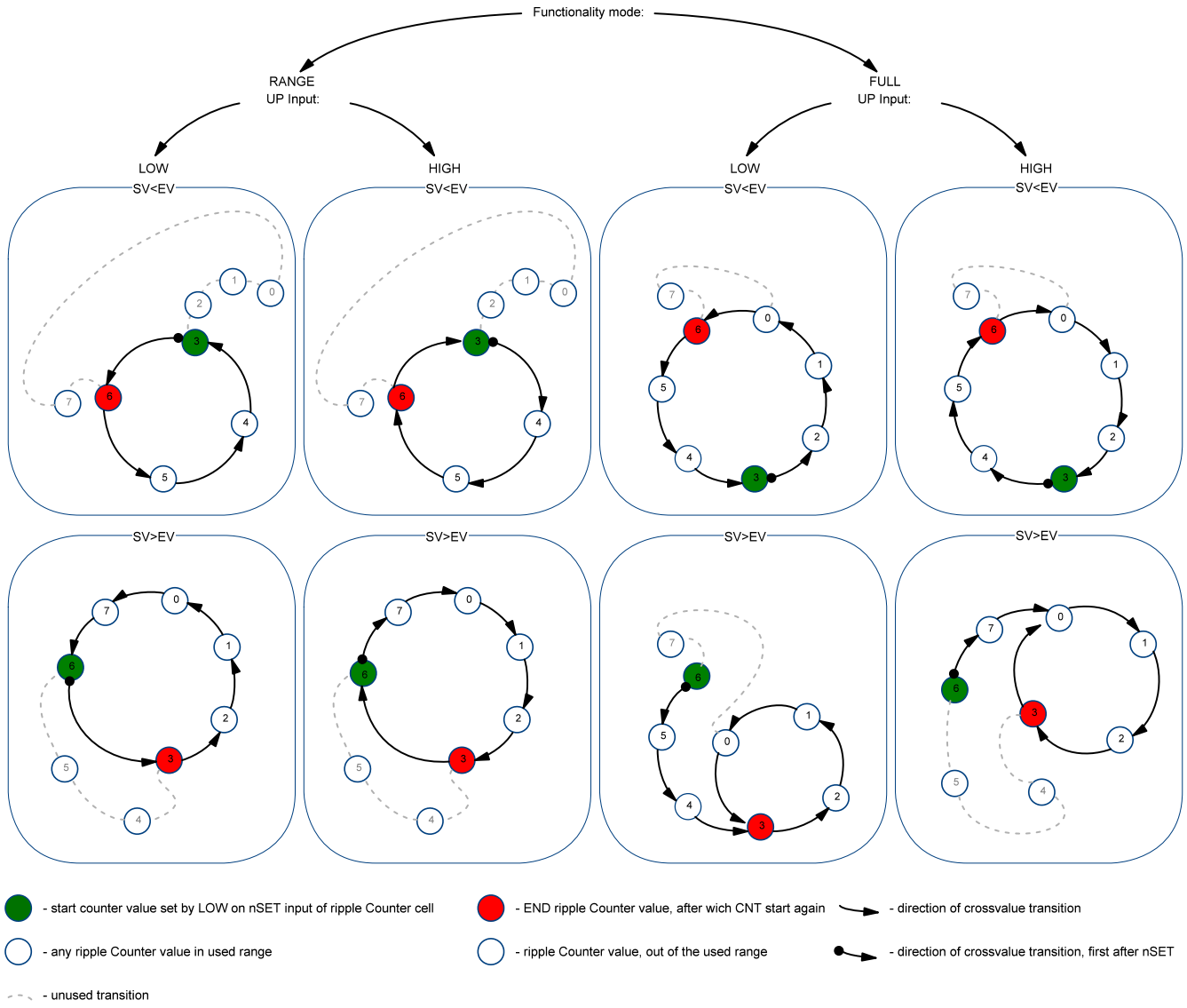

Figure 29: Example: Ripple Counter Functionality

7.4.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUT

Table 37: 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [1248]
0	0	1	register [1249]
0	1	0	register [1250]
0	1	1	register [1251]
1	0	0	register [1252]
1	0	1	register [1253]
1	1	0	register [1254]
1	1	1	register [1255]

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Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT6 is defined by registers [1255:1248]

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8 Multi-Function Macrocells

The SLG46826 has 8 Multi-Function macrocells that can serve more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes such as One Shot, Frequency Detect, Edge Detect, and others. Also, the macrocell is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF, see Figure 30.

See the list below for the functions that can be implemented in these macrocells:

- Seven macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays
- One macrocell that can serve as a 4-bit LUT/D Flip-Flop and as 16-Bit Counter/Delay/FSM

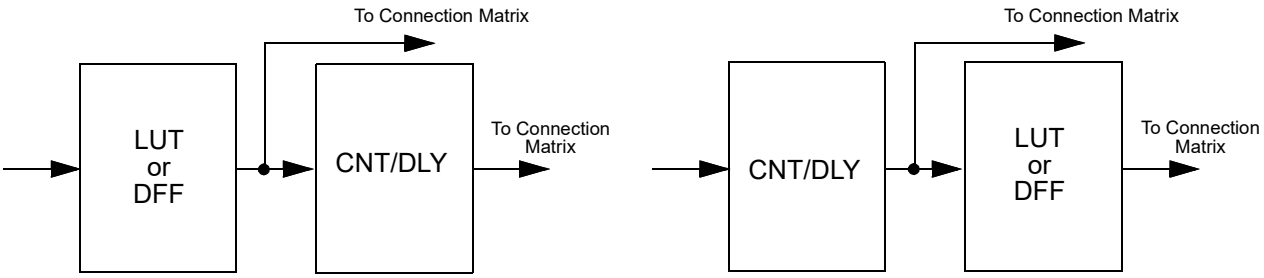

Figure 30: Possible Connections Inside Multi-Function Macrocell

Inputs/Outputs for the 8 Multi-Function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

8.1 3-BIT LUT OR DFF/LATCH WITH 8-BIT COUNTER/DELAY MACROCELLS

There are seven macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays.

When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix or can be connected to CNT/DLY's input.

When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D), clock (CLK), and Reset/Set (nRST/nSET) inputs of the Flip-Flop, with the output going back to the connection matrix or to the CNT/DLY's input.

When used to implement Counter/Delays, each macrocell has a dedicated matrix input connection. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count/delay circuits. These macrocells can also operate in a One-Shot mode, which will generate an output pulse of user-defined width. They can also operate in a Frequency Detection or Edge Detection mode.

Counter/Delay macrocell has an initial value, which define its initial value after GPAK is powered up. It is possible to select initial Low or initial High, as well as initial value defined by a Delay In signal.

For example, in case initial LOW option is used, the rising edge delay will start operation.

For timing diagrams refer to Section 8.2.

Note: After two DFF – counters initialize with counter data = 0 after POR.
Initial state = 1 – counters initialize with counter data = 0 after POR.
Initial state = 0 And After two DFF is bypass – counters initialize with counter data after POR.

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Three of eight macrocells can have their current count value read via I^2C (CNT0, CNT2, and CNT4). However, it is possible to change the counter data (value counter starts operating from) for any macrocell using I^2C write commands. In this mode, it is possible to load count data immediately (after two DFF) or after counter ends counting. See Section 15.7.1 for further details.

8.1.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

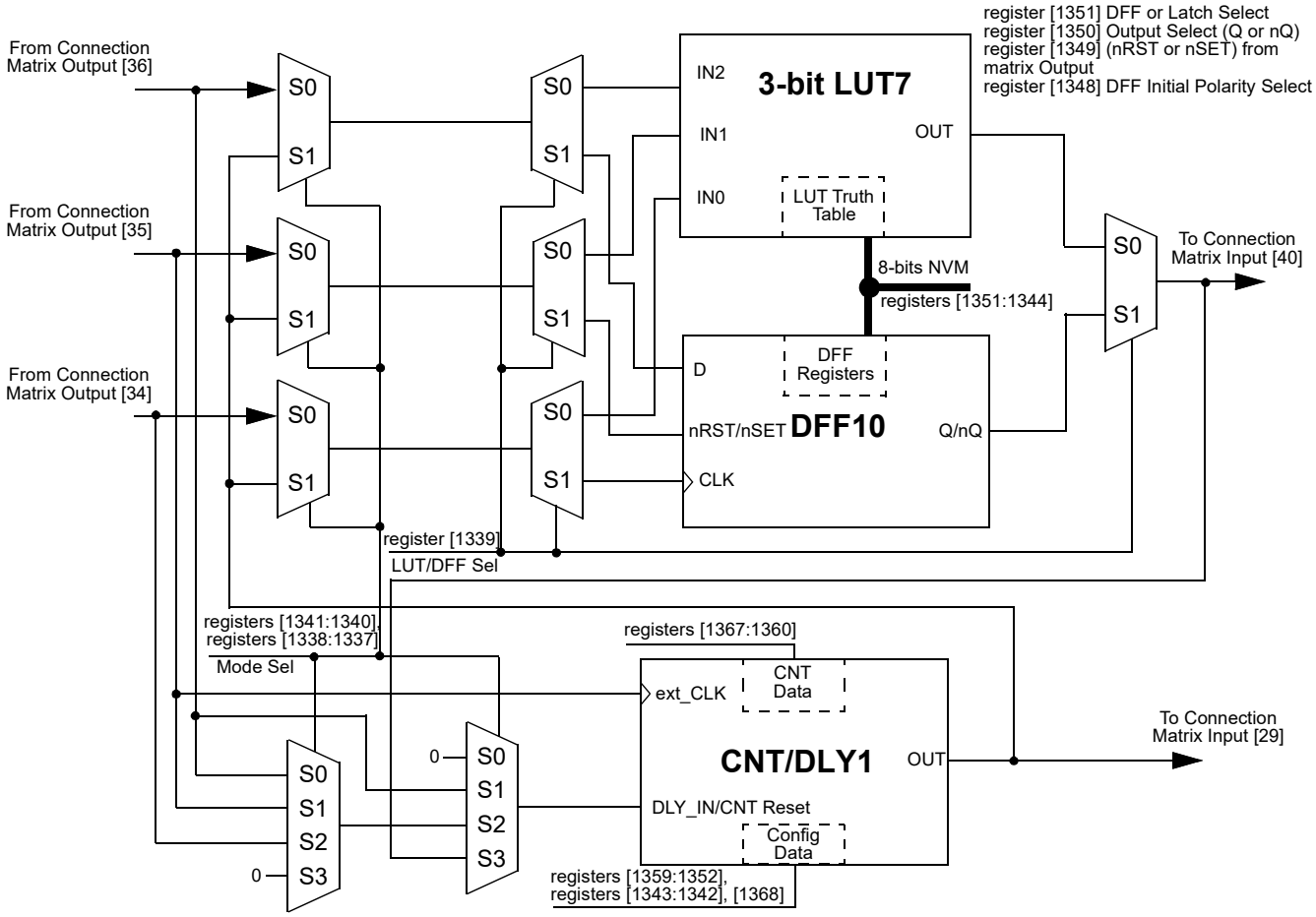

Figure 31: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT7/DFF10, CNT/DLY1)

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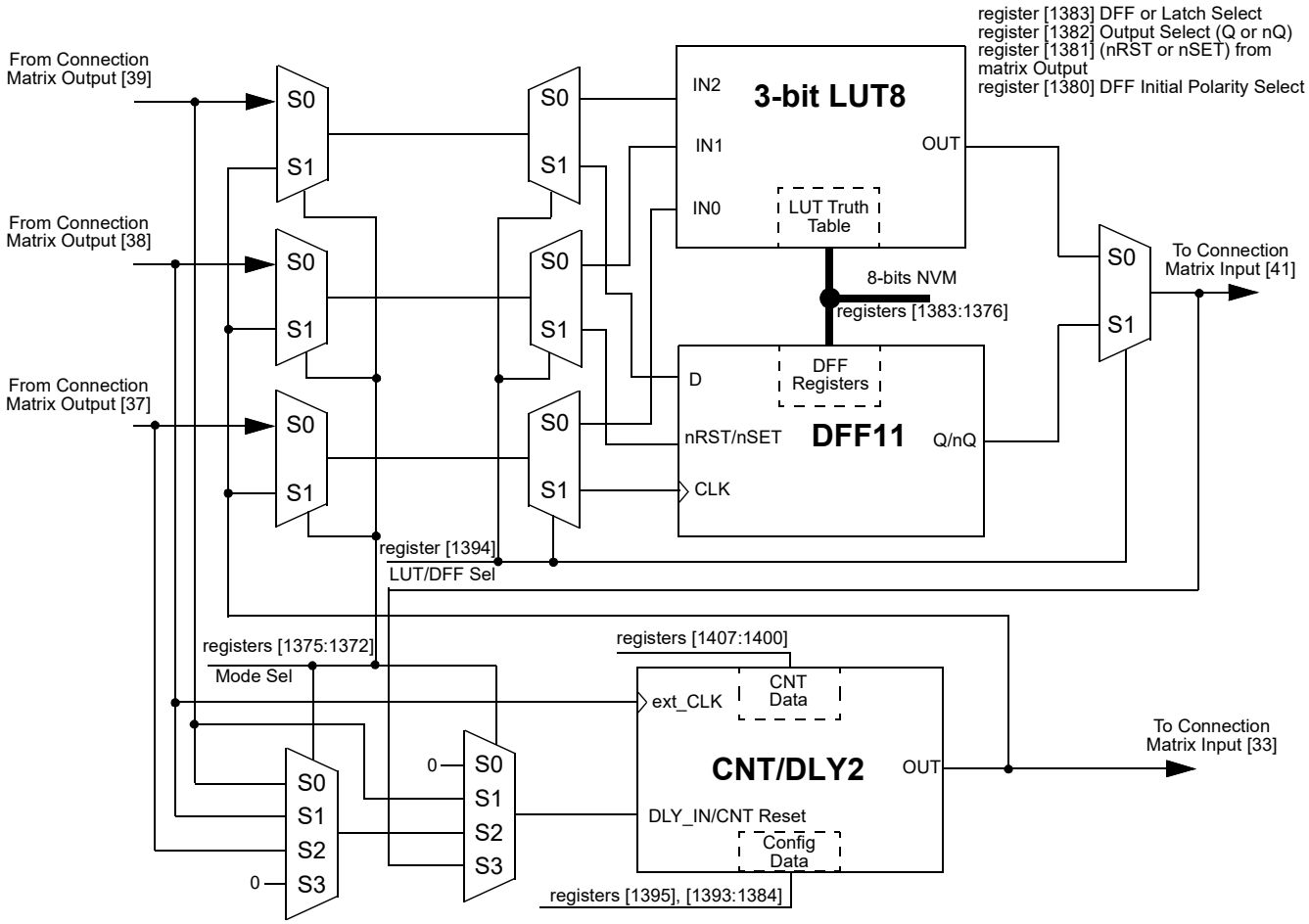

Figure 32: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT8/DFF11, CNT/DLY2)

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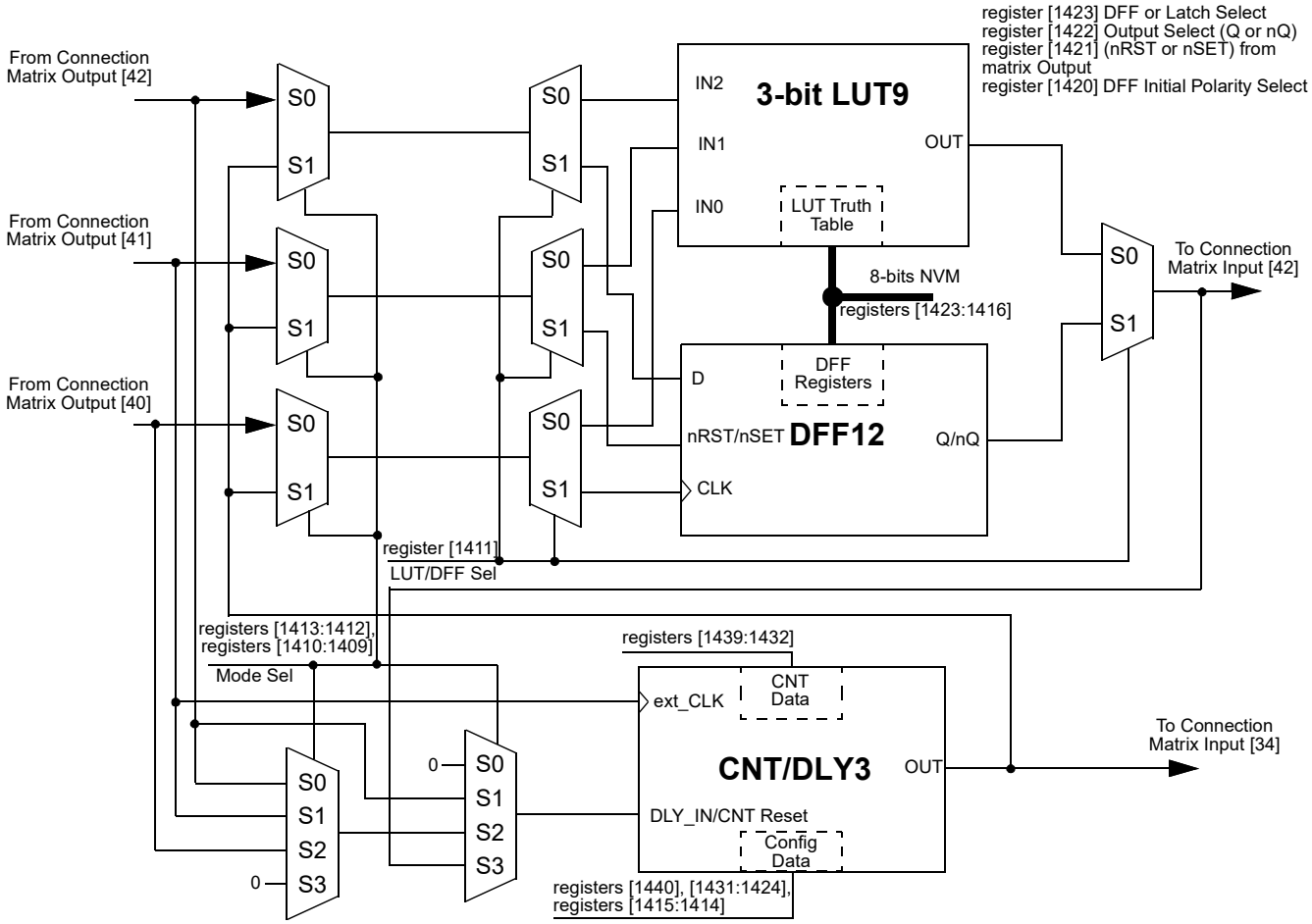

Figure 33: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT9/DFF12, CNT/DLY3)

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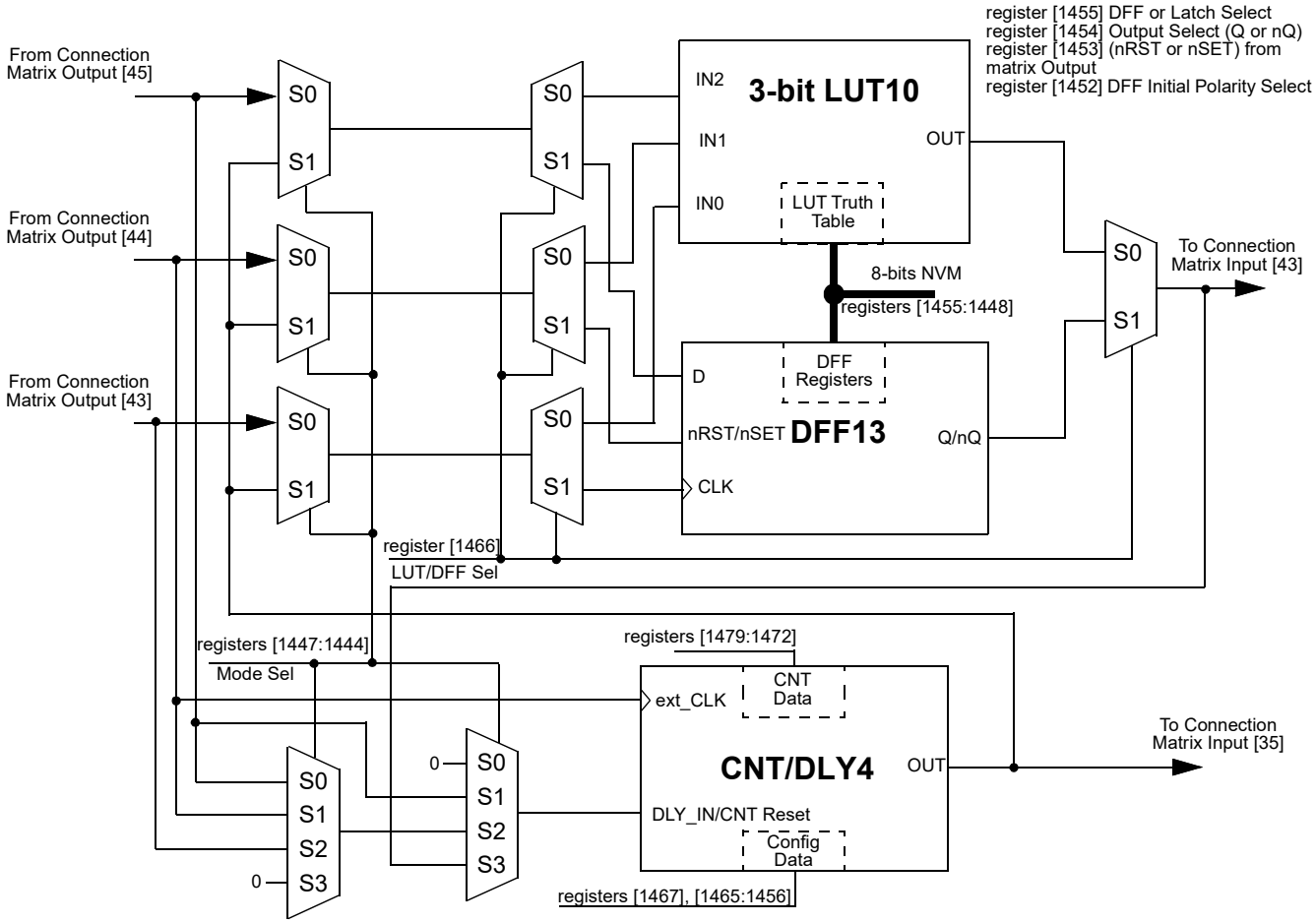

Figure 34: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT10/DFF13, CNT/DLY4)

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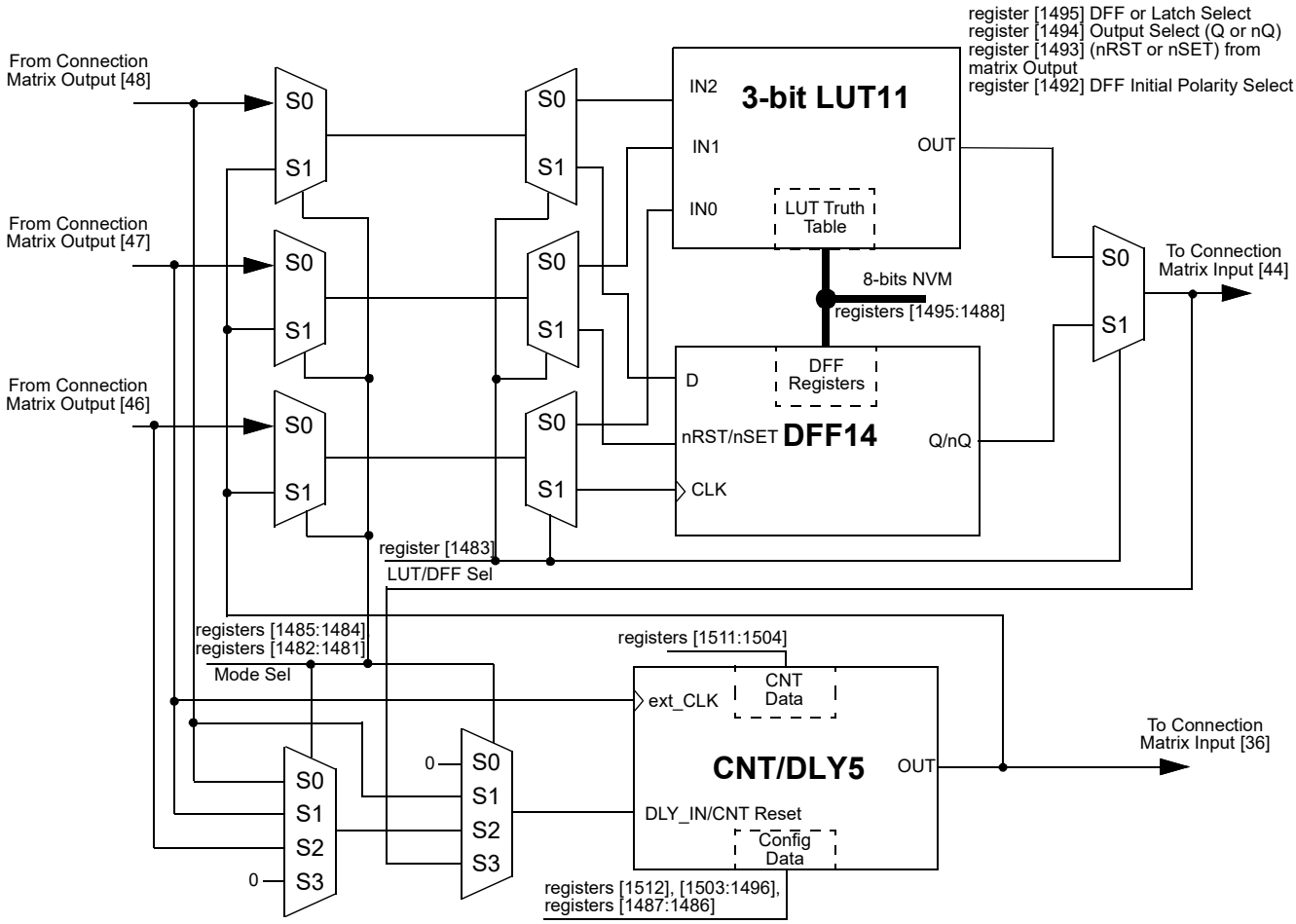

Figure 35: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT11/DFF14, CNT/DLY5)

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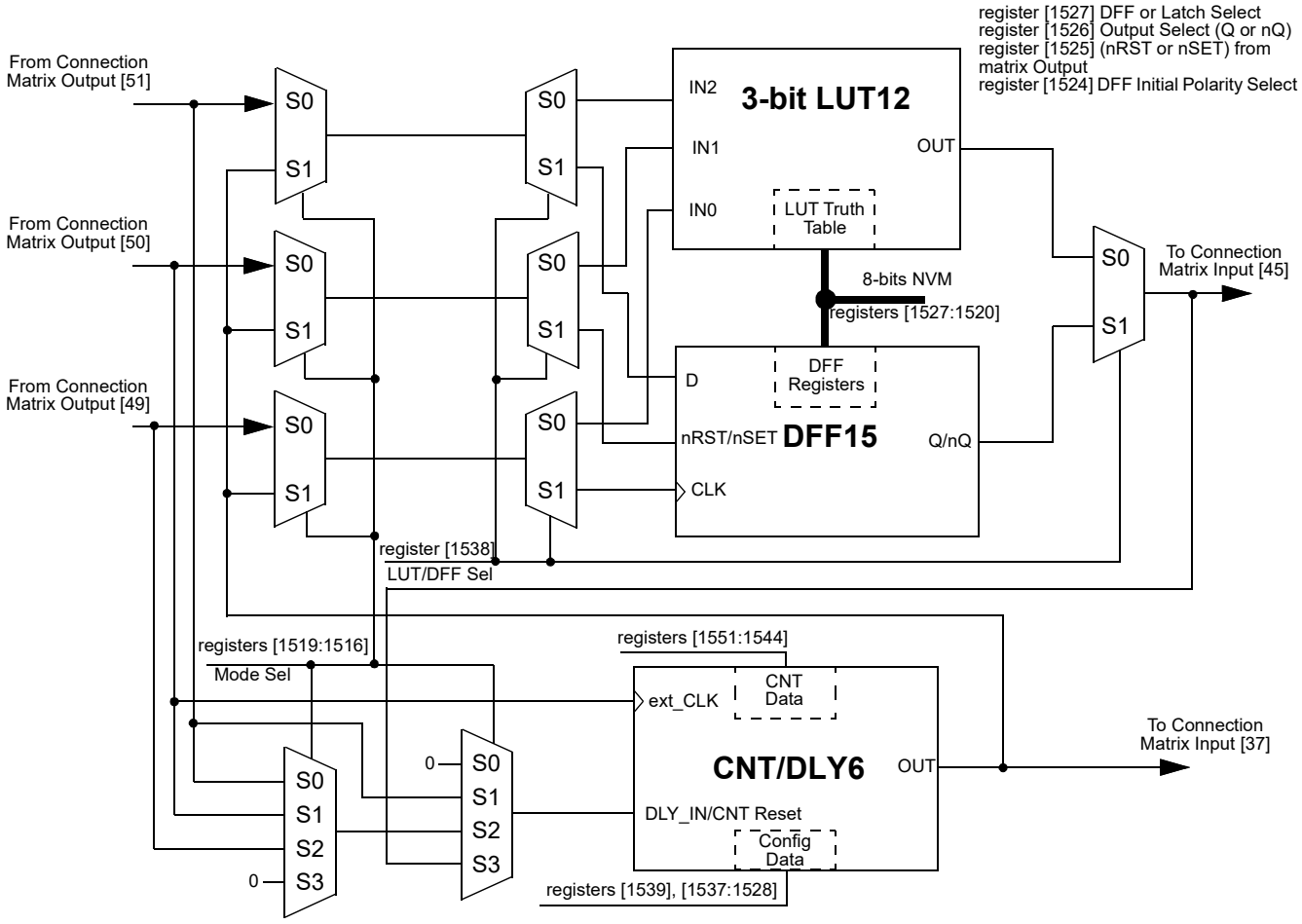

Figure 36: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT12/DFF15, CNT/DLY6)

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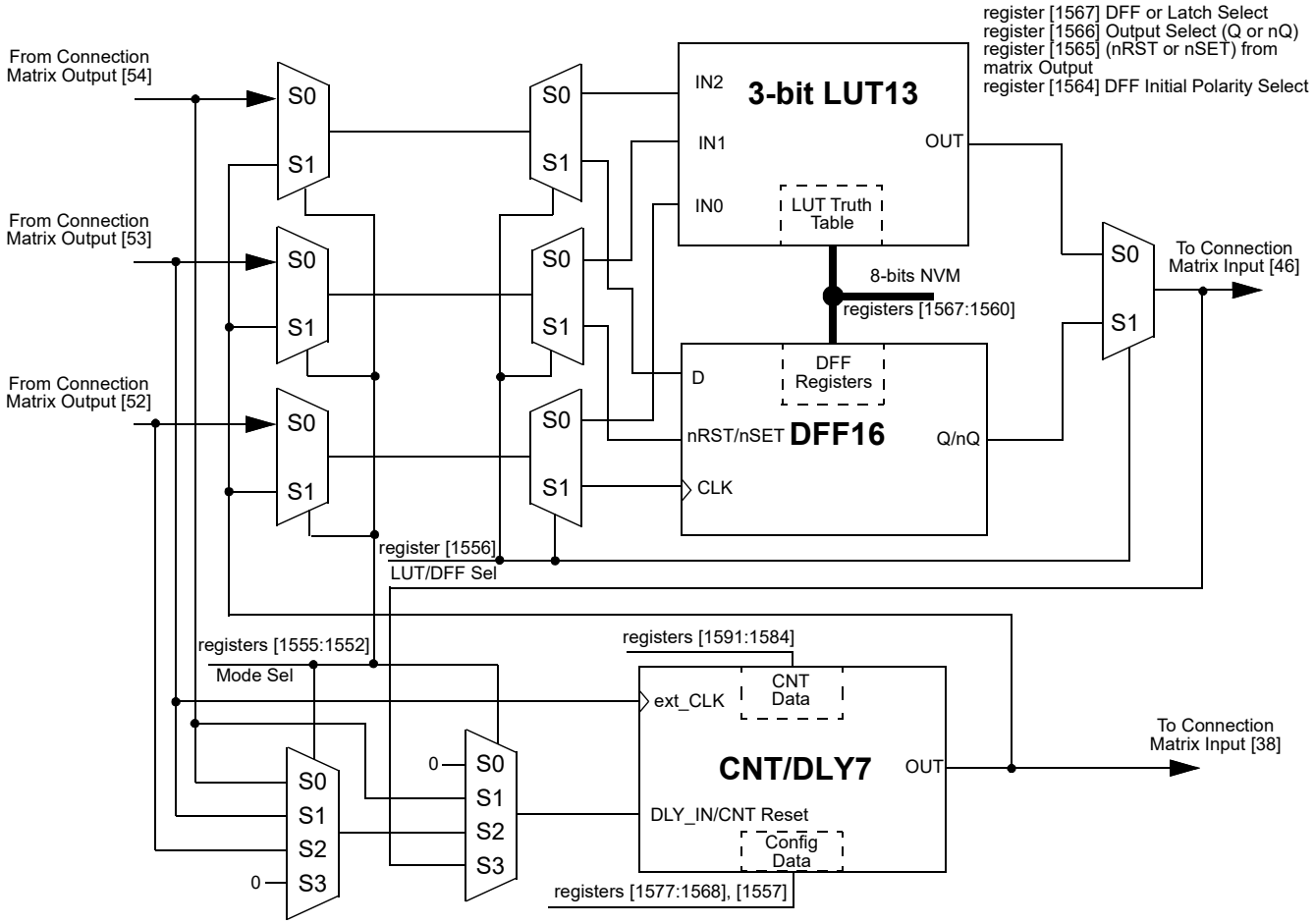

Figure 37: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT13/DFF16, CNT/DLY7)

As shown in Figures 24 to 30 there is a possibility to use LUT/DFF and CNT/DLY simultaneously.

Note: It is not possible to use LUT and DFF at once, one of these macrocells must be selected.

- Case 1. LUT/DFF in front of CNT/DLY. Three input signals from the connection matrix go to previously selected LUT or DFF's inputs and produce a single output which goes to a CND/DLY input. In its turn Counter/Delay's output goes back to the matrix.
- Case 2. CNT/DLY in front of LUT/DFF. Two input signals from the connection matrix go to CND/DLY's inputs (IN and CLK). Its output signal can be connected to any input of previously selected LUT or DFF, after which the signal goes back to the matrix.
- Case 3. Single LUT/DFF or CNT/DLY. Also, it is possible to use a standalone LUT/DFF or CNT/DLY. In this case, all inputs and output of the macrocell are connected to the matrix.

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8.1.2 3-Bit LUT or CNT/DLYs Used as 3-Bit LUTs

Table 38: 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1344]	LSB
0	0	1	register [1345]	
0	1	0	register [1346]	
0	1	1	register [1347]	
1	0	0	register [1348]	
1	0	1	register [1349]	
1	1	0	register [1350]	
1	1	1	register [1351]	MSB

Table 39: 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1376]	LSB
0	0	1	register [1377]	
0	1	0	register [1378]	
0	1	1	register [1379]	
1	0	0	register [1380]	
1	0	1	register [1381]	
1	1	0	register [1382]	
1	1	1	register [1383]	MSB

Table 40: 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1416]	LSB
0	0	1	register [1417]	
0	1	0	register [1418]	
0	1	1	register [1419]	
1	0	0	register [1420]	
1	0	1	register [1421]	
1	1	0	register [1422]	
1	1	1	register [1423]	MSB

Table 41: 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1448]	LSB
0	0	1	register [1449]	
0	1	0	register [1450]	
0	1	1	register [1451]	
1	0	0	register [1452]	
1	0	1	register [1453]	
1	1	0	register [1454]	
1	1	1	register [1455]	MSB

Table 42: 3-bit LUT11 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1488]	LSB
0	0	1	register [1489]	
0	1	0	register [1490]	
0	1	1	register [1491]	
1	0	0	register [1492]	
1	0	1	register [1493]	
1	1	0	register [1494]	
1	1	1	register [1495]	MSB

Table 43: 3-bit LUT12 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1520]	LSB
0	0	1	register [1521]	
0	1	0	register [1522]	
0	1	1	register [1523]	
1	0	0	register [1524]	
1	0	1	register [1525]	
1	1	0	register [1526]	
1	1	1	register [1527]	MSB

Table 44: 3-bit LUT13 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1560]	LSB
0	0	1	register [1561]	
0	1	0	register [1562]	
0	1	1	register [1563]	
1	0	0	register [1564]	
1	0	1	register [1565]	
1	1	0	register [1566]	
1	1	1	register [1567]	MSB

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Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT7 is defined by registers [1351:1344]

3-Bit LUT8 is defined by registers [1383:1376]

3-Bit LUT9 is defined by registers [1423:1416]

3-Bit LUT10 is defined by registers [1455:1448]

3-Bit LUT11 is defined by registers [1495:1488]

3-Bit LUT12 is defined by registers [1527:1520]

3-Bit LUT13 is defined by registers [1567:1560]

8.2 CNT/DLY/FSM TIMING DIAGRAMS

8.2.1 Delay Mode CNT/DLY0 to CNT/DLY7

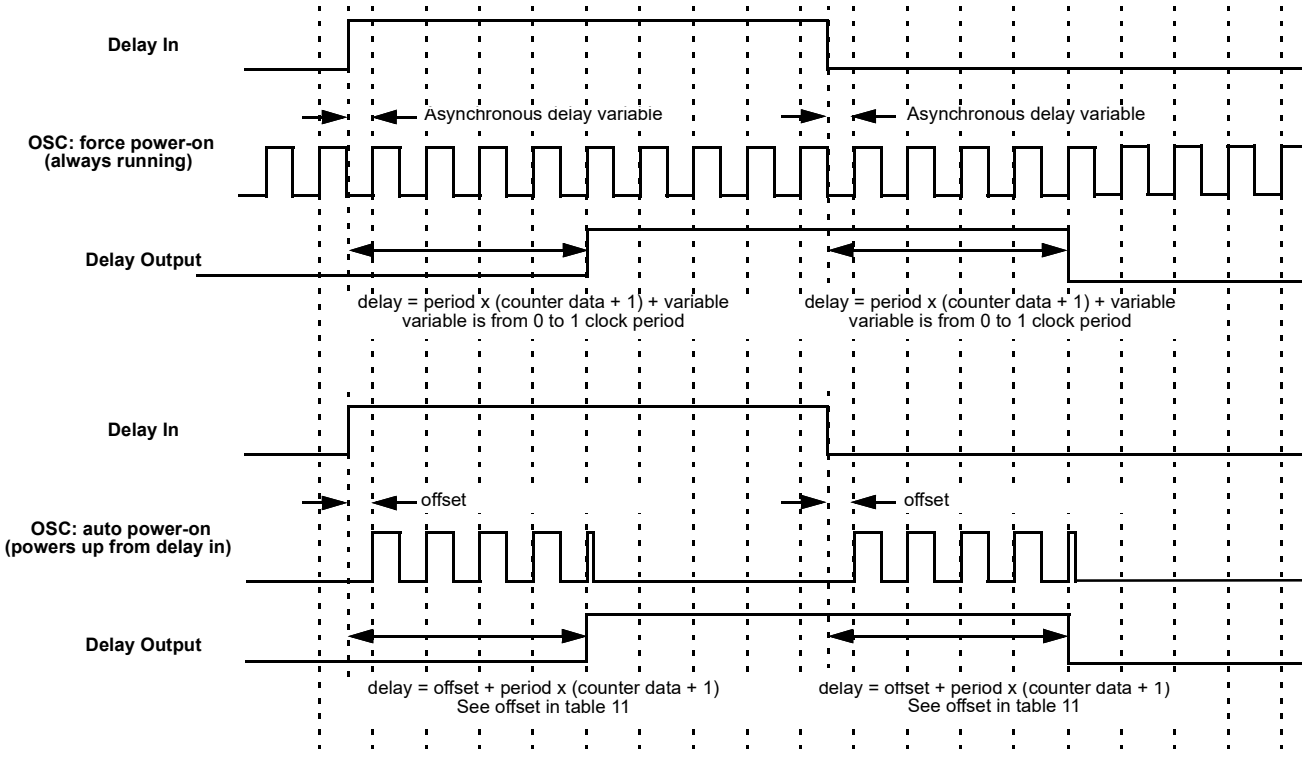

Figure 38: Delay Mode Timing Diagram, Edge Select: Both, Counter Data: 3

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The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter, if the input signal is shorter than the delay time.

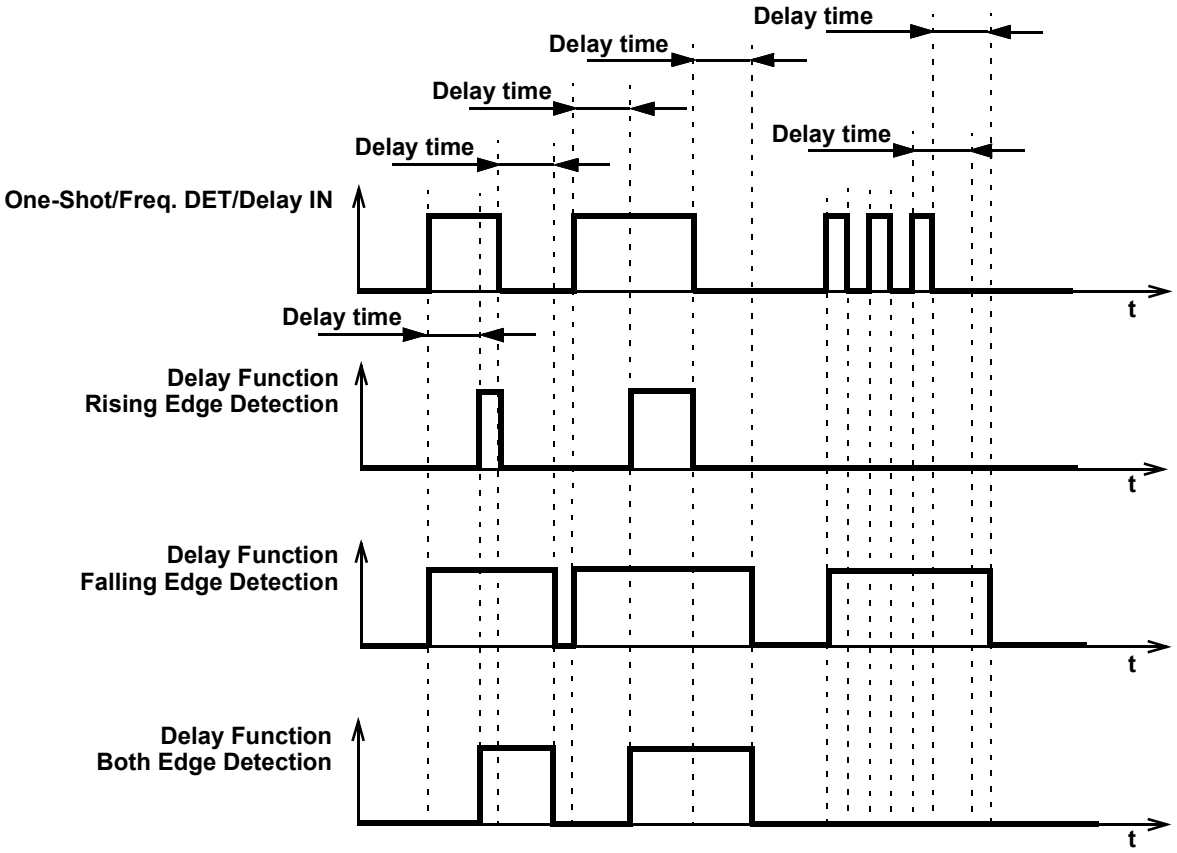

Figure 39: Delay Mode Timing Diagram for Different Edge Select Modes

8.2.2 Count Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY0 to CNT/DLY7

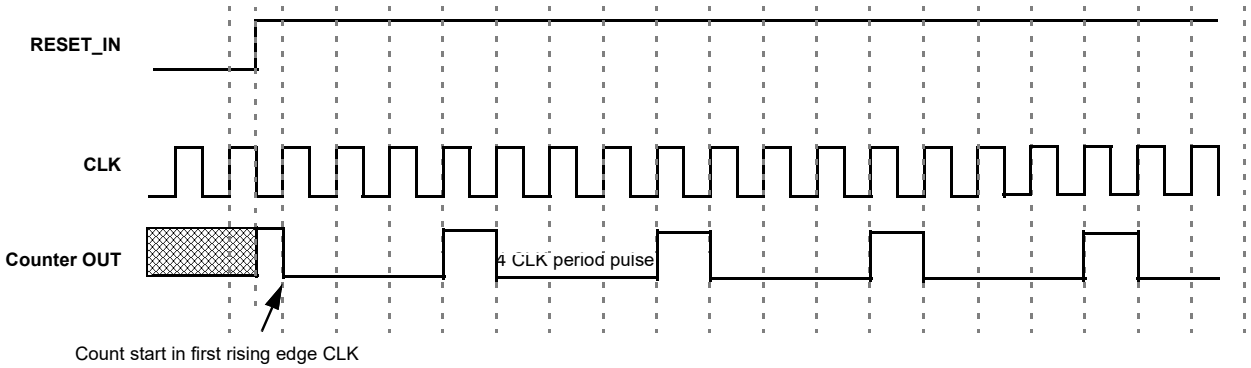

Figure 40: Counter Mode Timing Diagram without Two DFFs Synced Up

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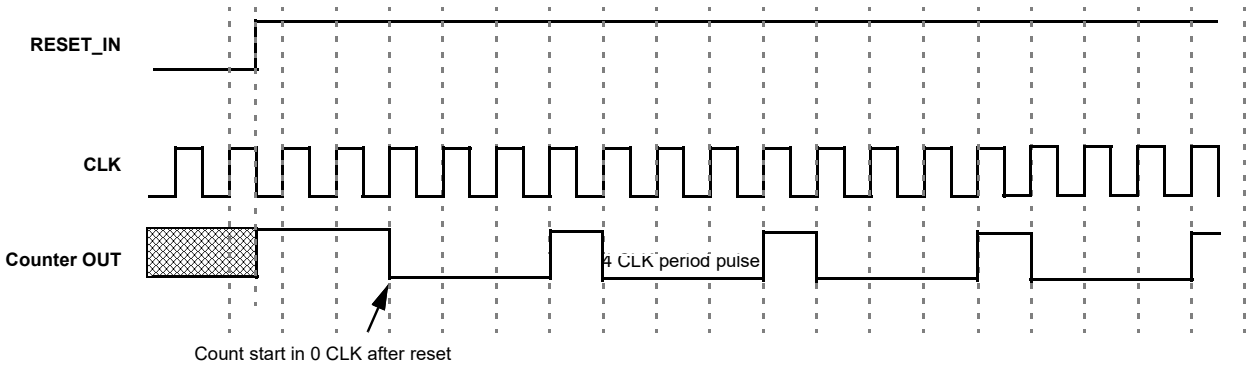

Figure 41: Counter Mode Timing Diagram with Two DFFs Synced Up

8.2.3 One-Shot Mode CNT/DLY0 to CNT/DLY7

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width determines by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

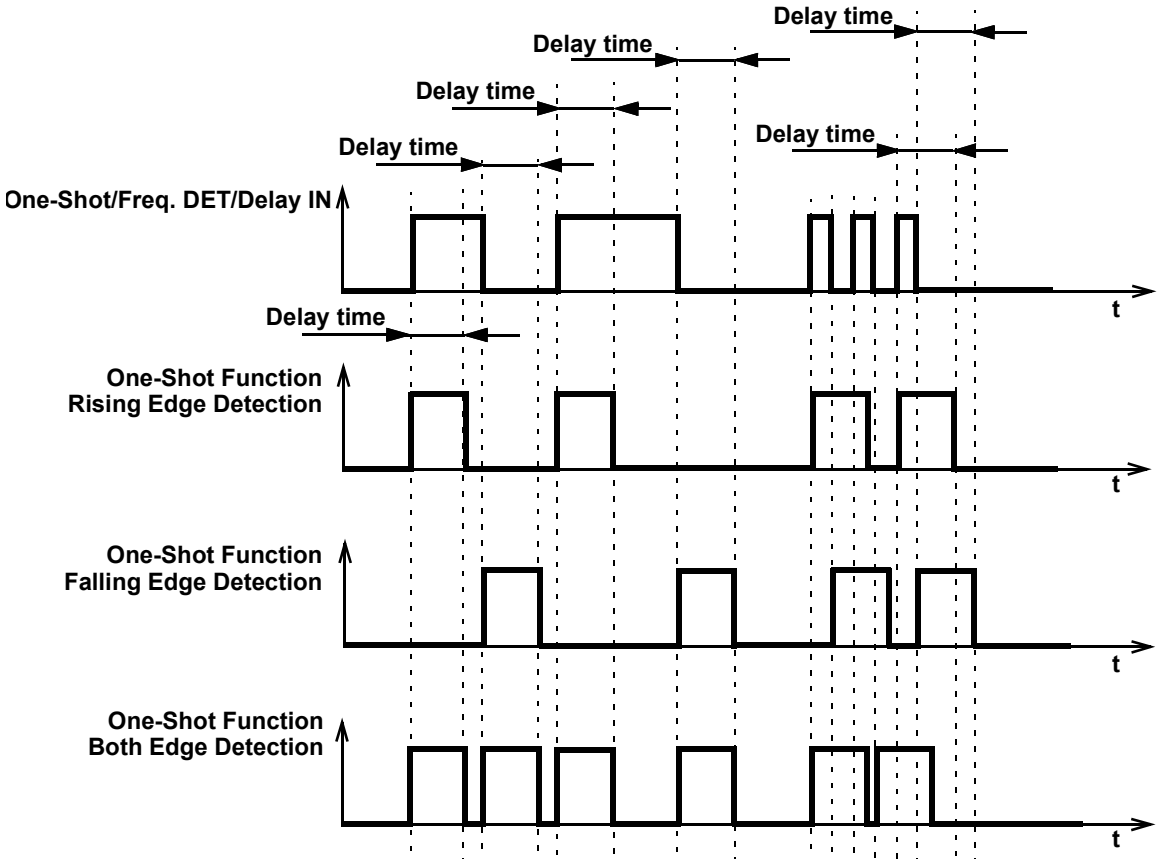

Figure 42: One-Shot Function Timing Diagram

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This macrocell generates a high level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is high.

8.2.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY7

Rising Edge: The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

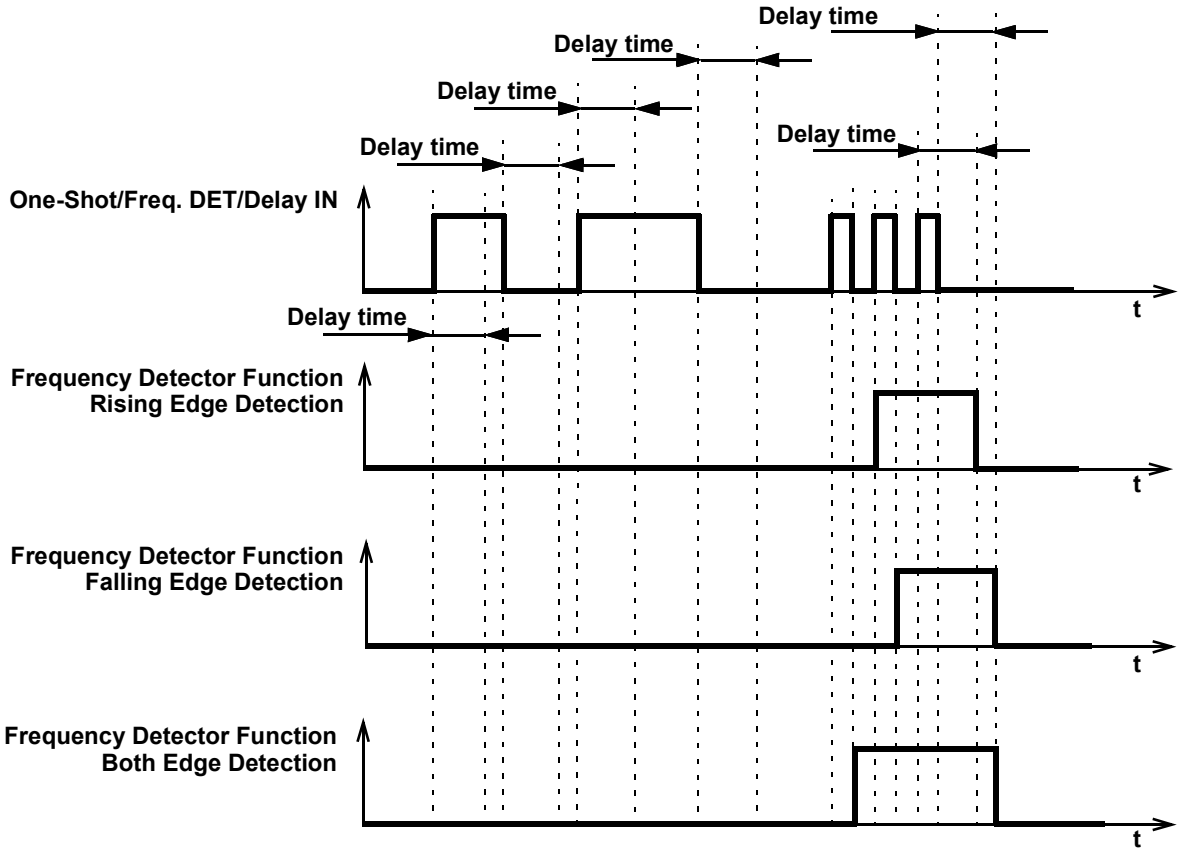

Figure 43: Frequency Detection Mode Timing Diagram

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8.2.5 Edge Detection Mode CNT/DLY1 to CNT/DLY7

The macrocell generates high level short pulse when detecting the respective edge. See Table 11.

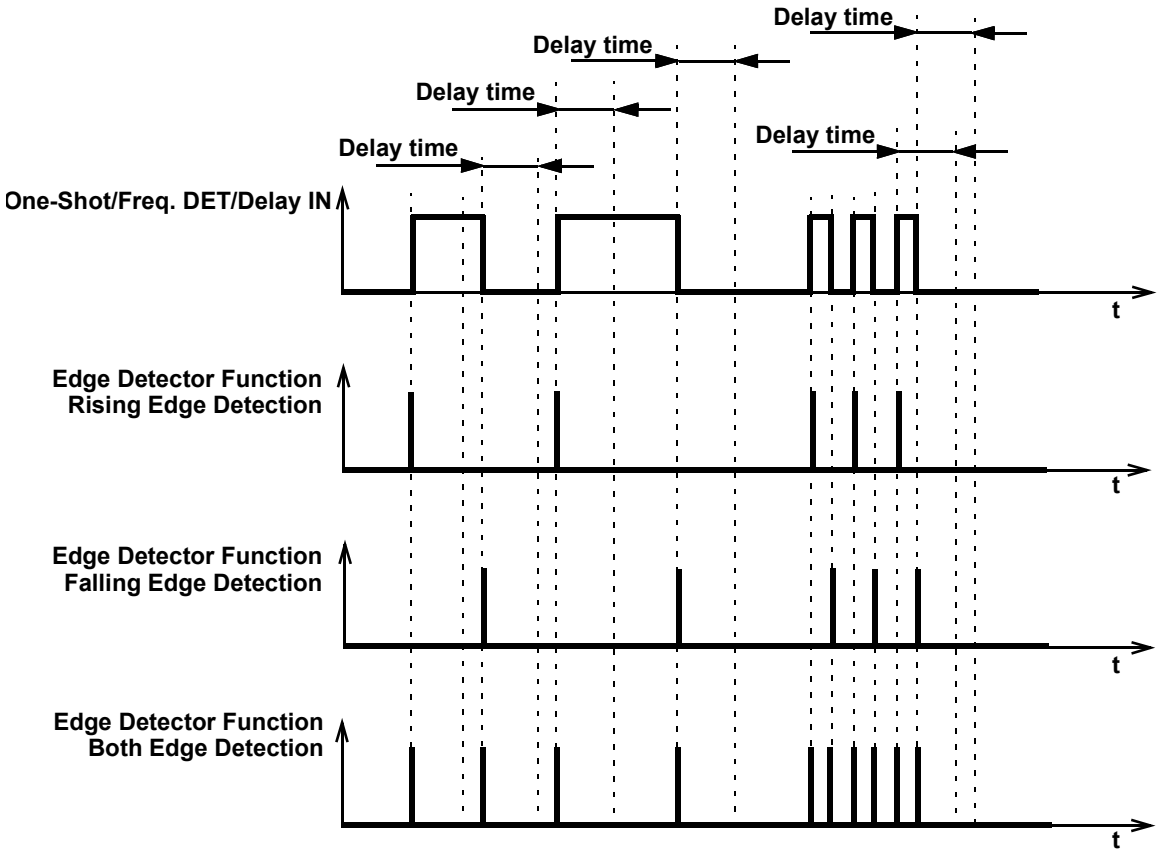

Figure 44: Edge Detection Mode Timing Diagram

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8.2.6 Delayed Edge Detection Mode CNT/DLY0 to CNT/DLY7

In Delayed Edge Detection Mode, High level short pulses are generated on the macrocell output after the configured delay time, if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated. See Figure 45.

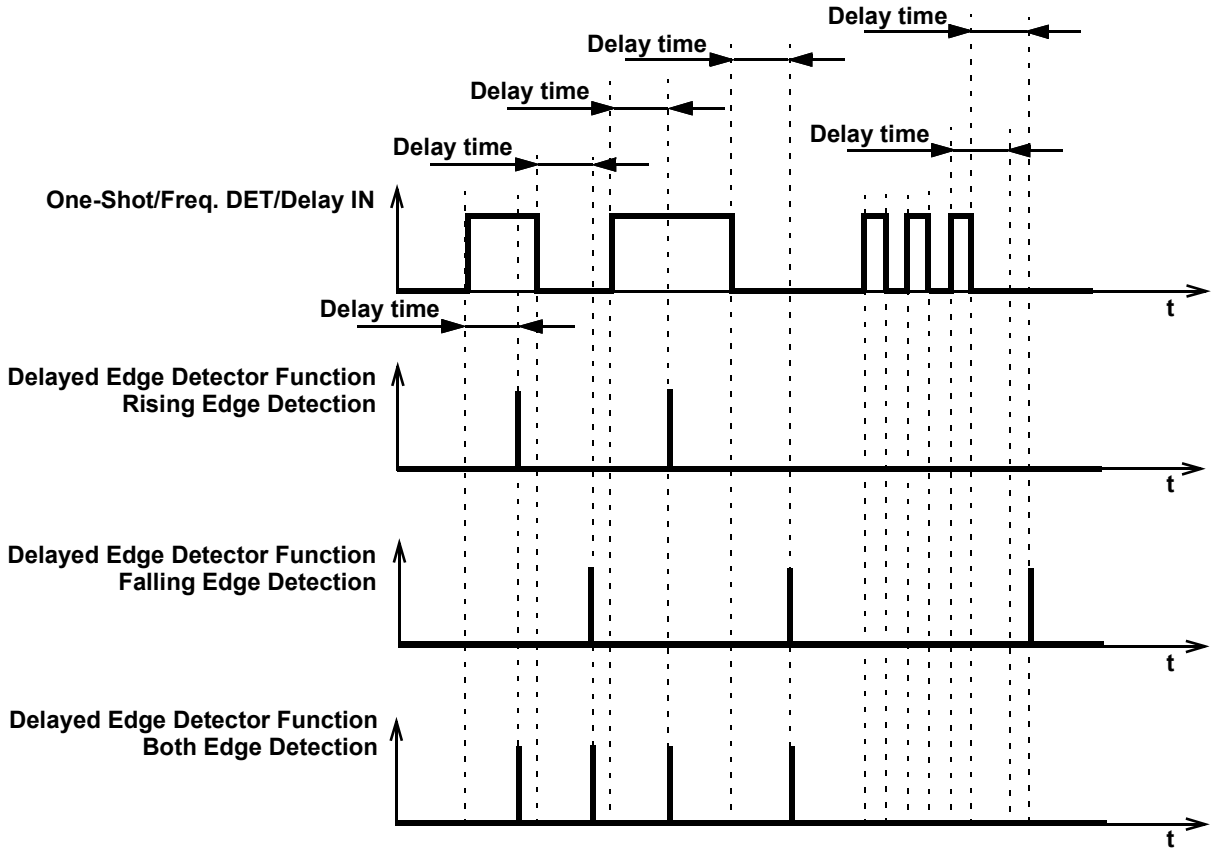

Figure 45: Delayed Edge Detection Mode Timing Diagram

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8.2.7 CNT/FSM Mode CNT/DLY0

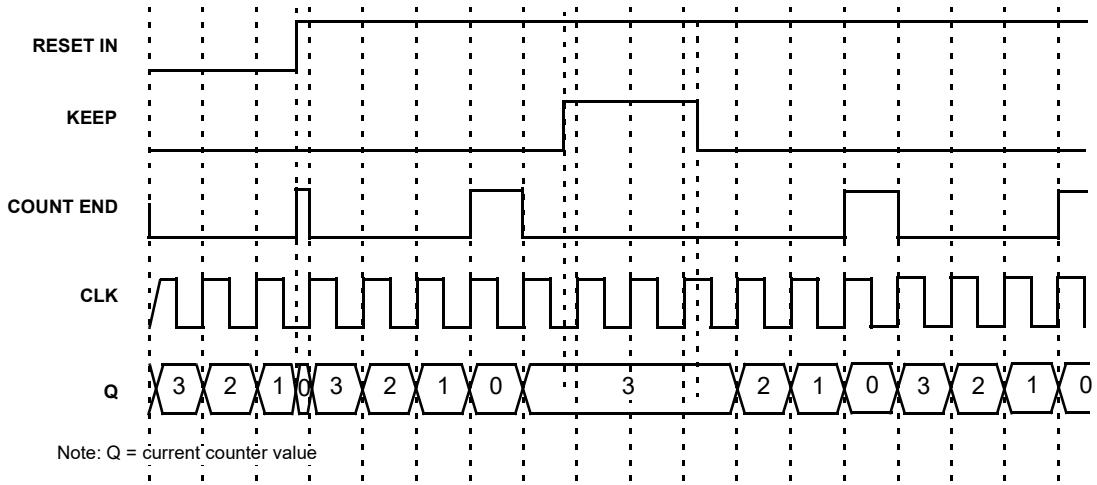

Figure 46: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

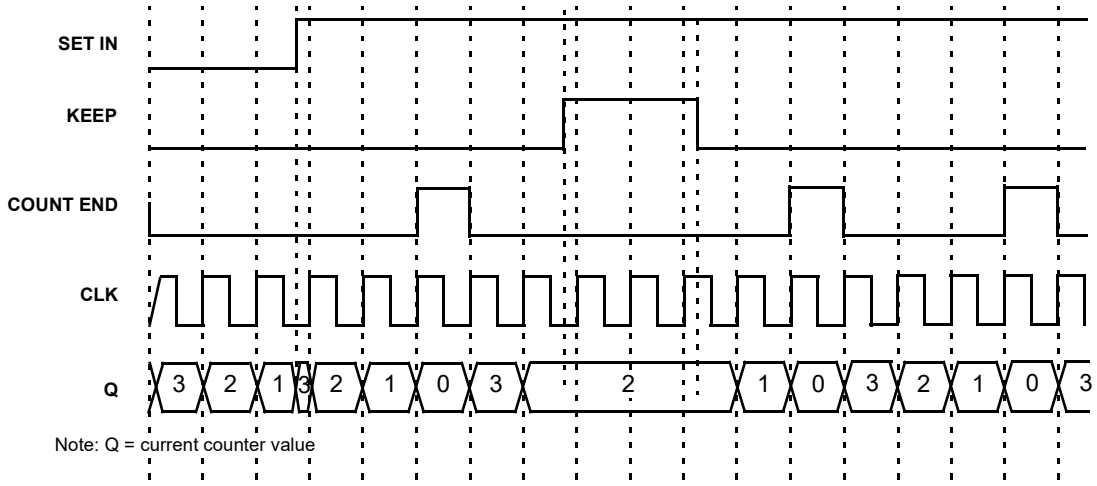

Figure 47: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

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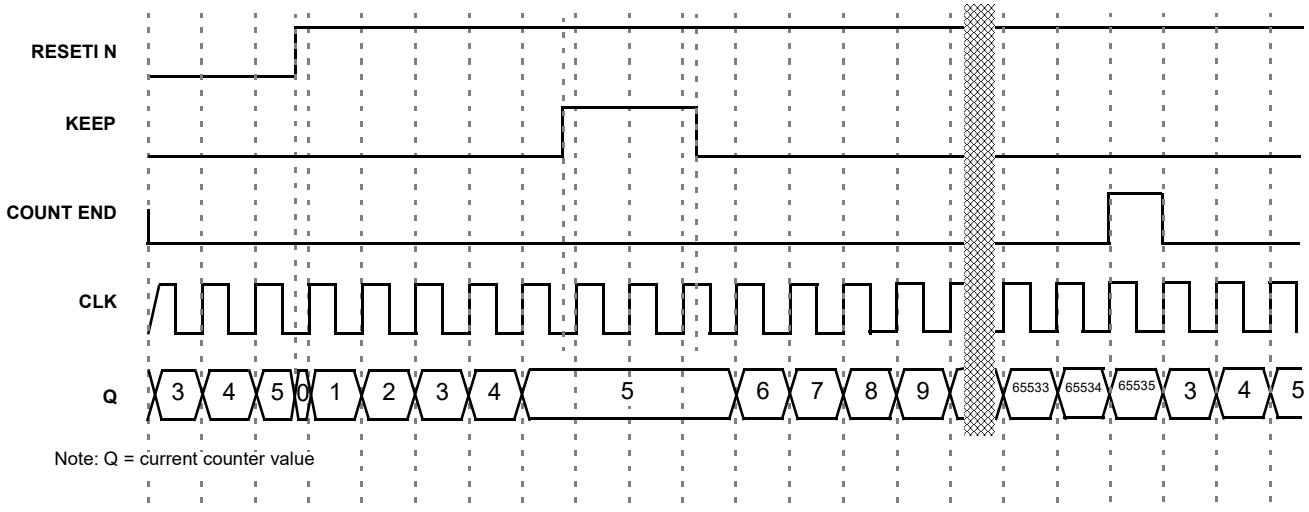

Figure 48: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3

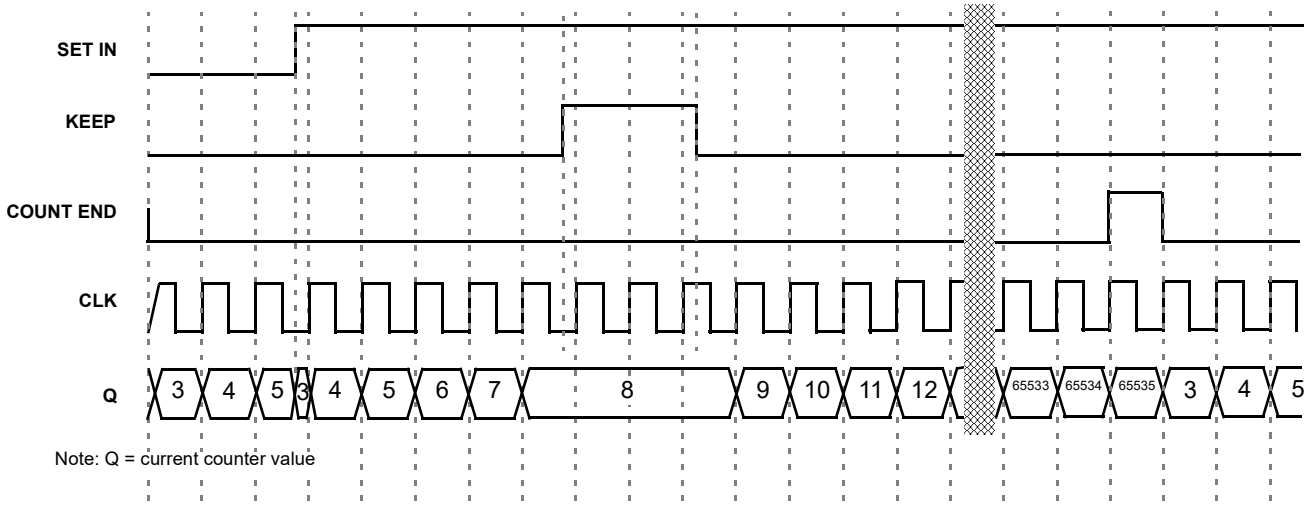

Figure 49: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3

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8.2.8 Difference in Counter Value for Counter, Delay, One-Shot, and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. The counter value is shifted for two rising edges of the clock signal in Delay/One-Shot/Frequency Detect modes compared to Counter mode. See Figure 50.

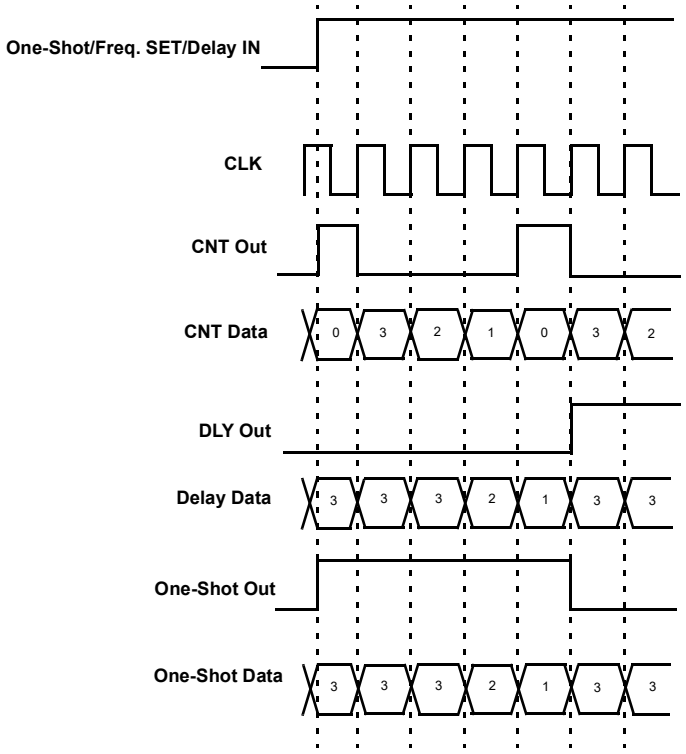

Figure 50: Counter Value, Counter Data = 3

8.3 4-BIT LUT OR DFF/LATCH WITH 16-BIT COUNTER/DELAY MACROCELL

There is one macrocell that can serve as either 4-bit LUT/D Flip-Flop or as 16-bit Counter/Delay.

When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix or can be connected to CNT/DLY's input or LUT/DFF's input.

When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

When used to implement 16-Bit Counter/Delay function, two of the four input signals from the connection matrix go to the external clock (EXT_CLK) and reset (DLY_IN/CNT Reset) for the counter/delay, with the output going back to the connection matrix.

This macrocell has an optional Finite State Machine (FSM) function. There are two additional matrix inputs for Up and Keep to support FSM functionality.

This macrocell can also operate in a one-shot mode, which will generate an output pulse of user-defined width.
This macrocell can also operate in a frequency detection.
This macrocell can have its active count value read via I^2C. See Section 15.7.1 for further details.

Note: After two DFF – counters initialize with counter data = 0 after POR.

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Initial state = 1 – counters initialize with counter data = 0 after POR.
Initial state = 0 And After two DFF is bypass – counters initialize with counter data after POR.

8.3.1 4-Bit LUT or 16-Bit CNT/DLY Block Diagram

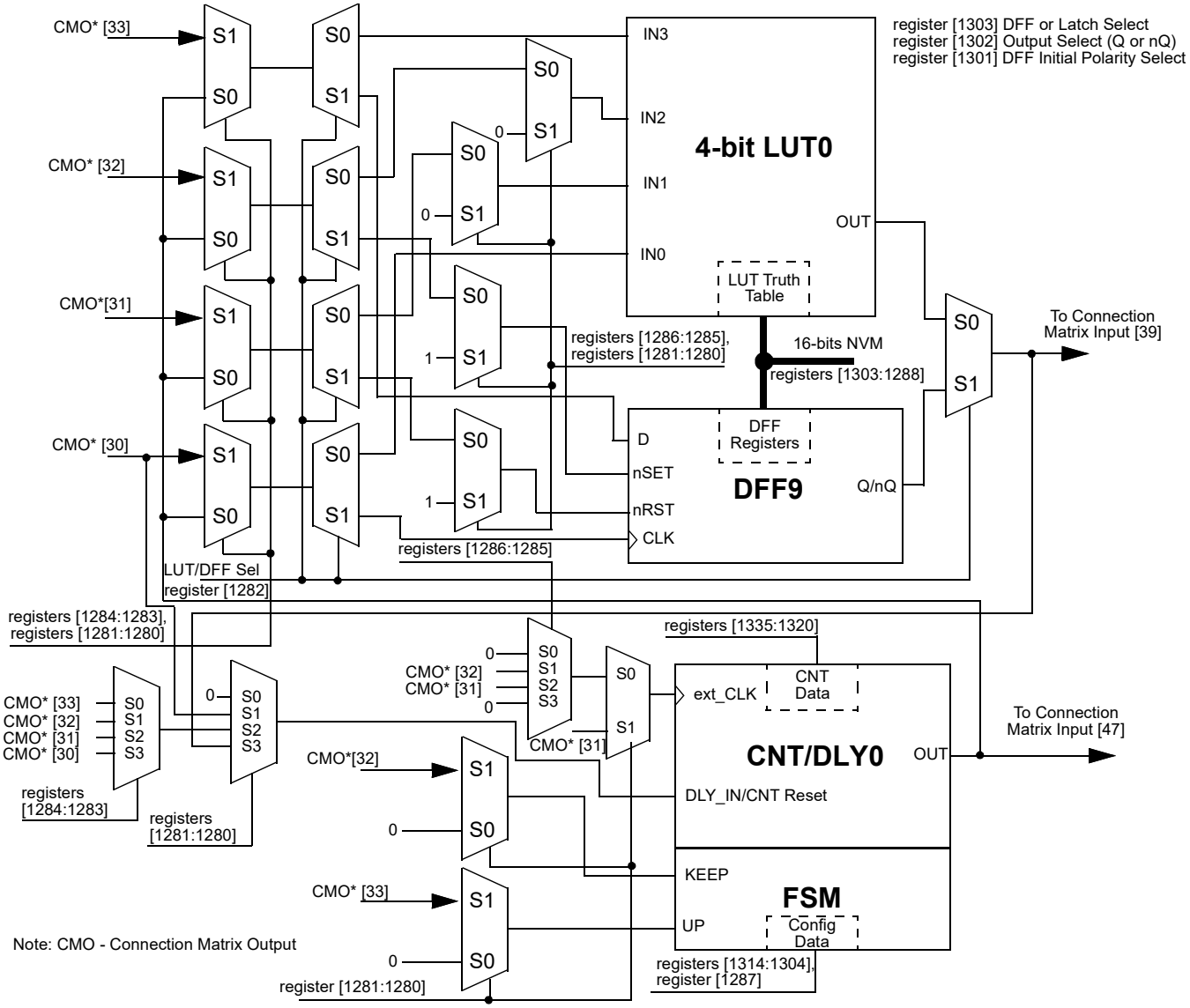

Figure 51: 4-bit LUT0 or CNT/DLY0

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8.3.2 4-Bit LUT or 16-Bit Counter/Delay Macrocells Used as 4-Bit LUTs

Table 45: 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1288]	LSB
0	0	0	1	register [1289]	
0	0	1	0	register [1290]	
0	0	1	1	register [1291]	
0	1	0	0	register [1292]	
0	1	0	1	register [1293]	
0	1	1	0	register [1294]	
0	1	1	1	register [1295]	
1	0	0	0	register [1296]	
1	0	0	1	register [1297]	
1	0	1	0	register [1298]	
1	0	1	1	register [1299]	
1	1	0	0	register [1300]	
1	1	0	1	register [1301]	
1	1	1	0	register [1302]	
1	1	1	1	register [1303]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT0 is defined by registers [1303:1288]

Table 46: 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

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8.4 WAKE AND SLEEP CONTROLLER

The SLG46826 has a Wake and Sleep (WS) function for ACMP0H and ACMP1H. The macrocell CNT/DLY0 can be reconfigured for this purpose registers [1305:1304] = 11 and register [1316] = 1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 16-bit counter.

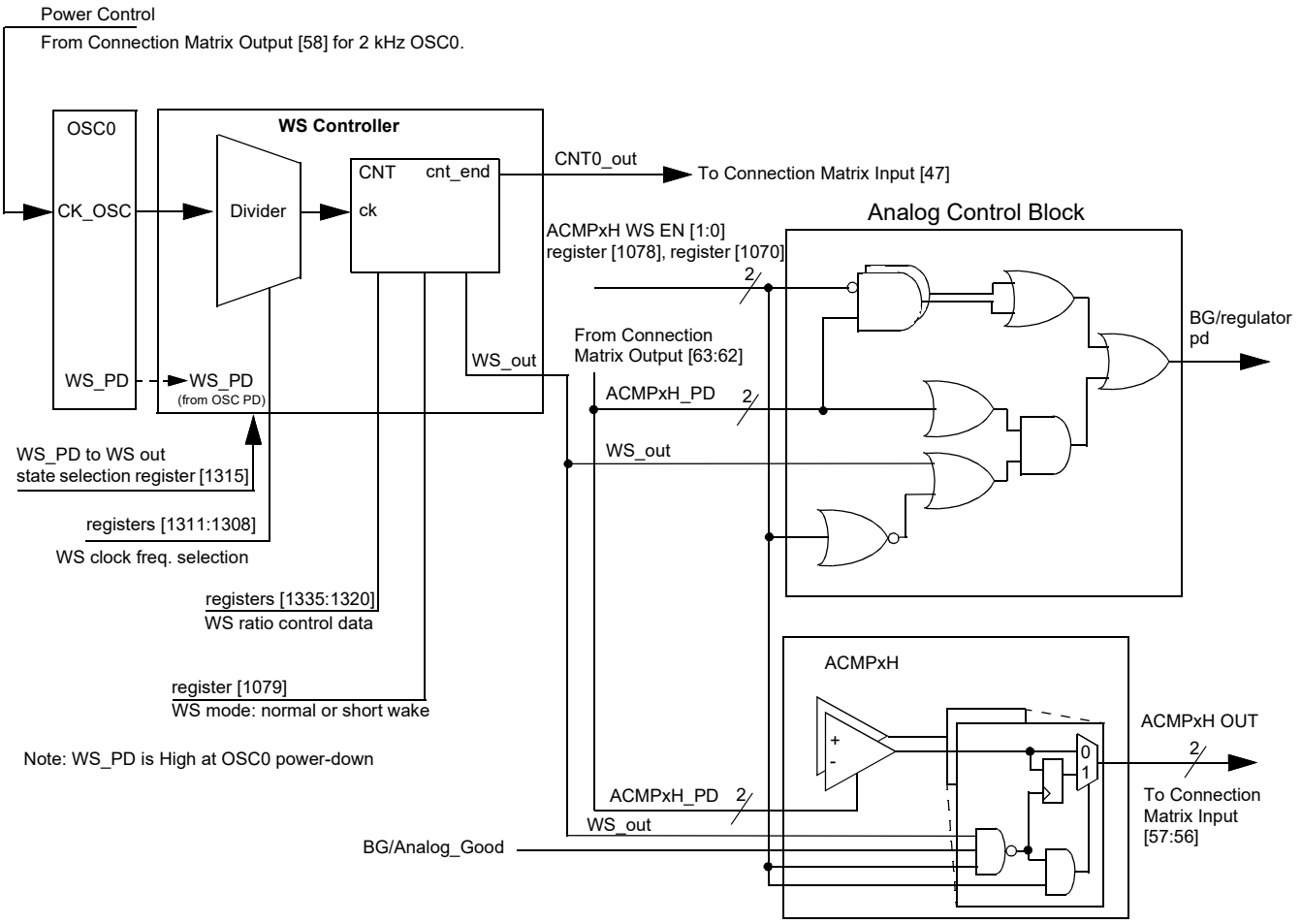

Figure 52: Wake and Sleep Controller

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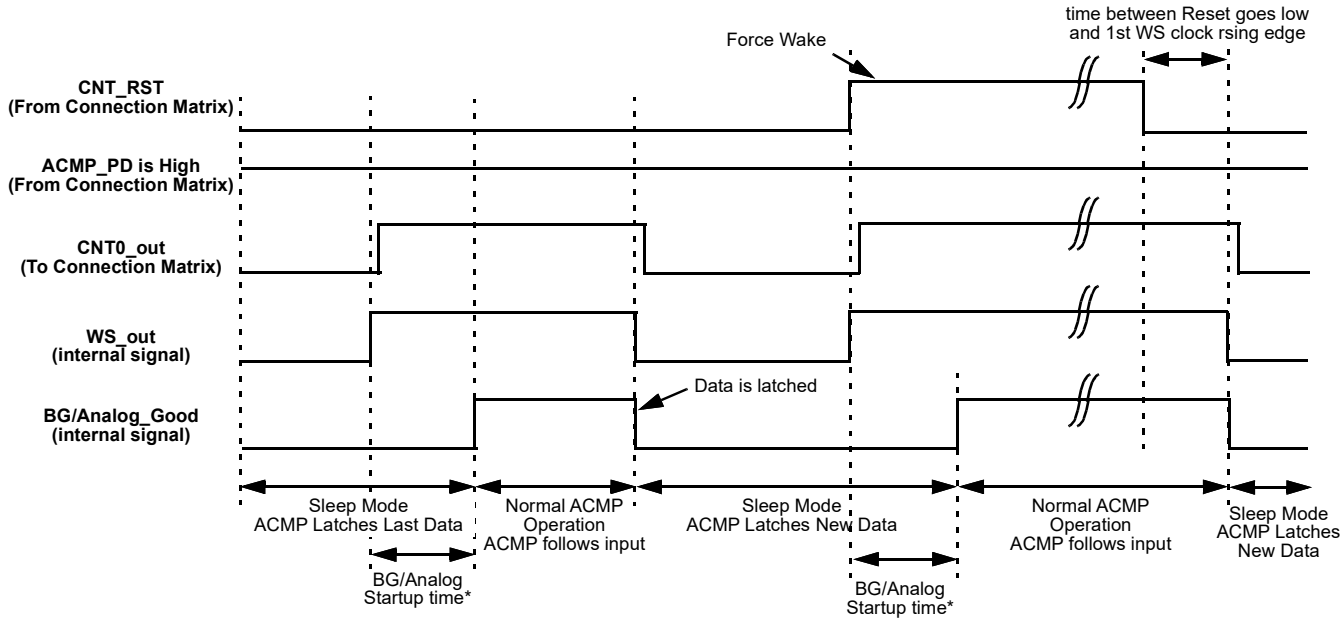
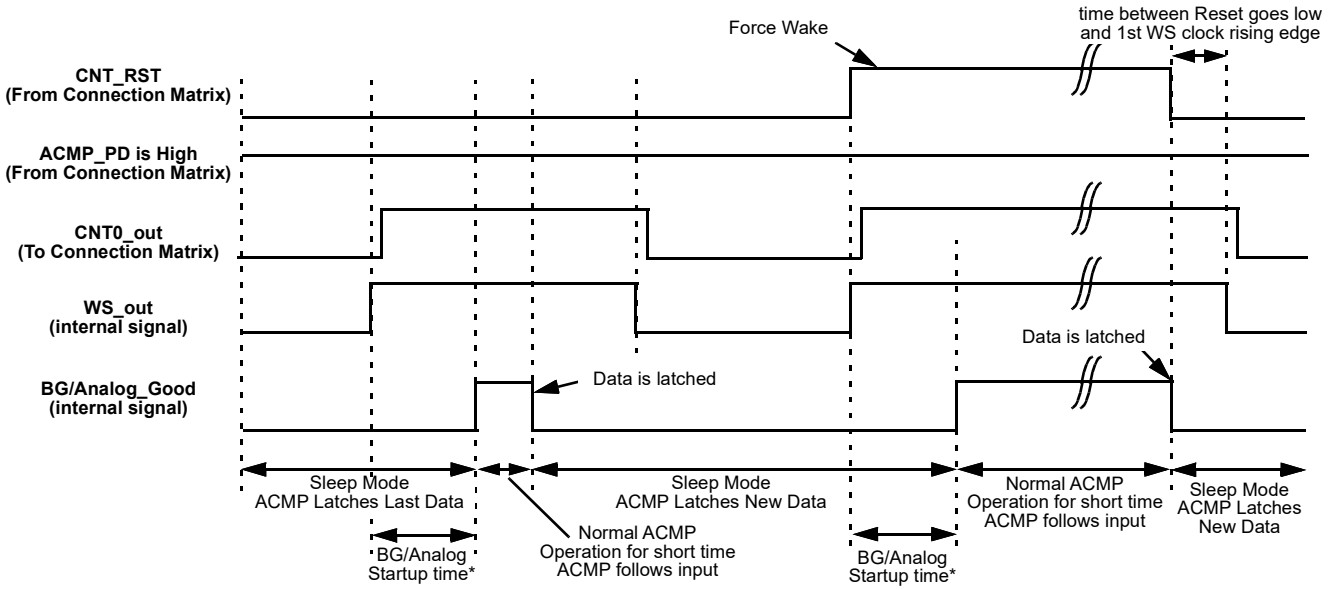


Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during LATCH.

Figure 53: Wake and Sleep Timing Diagram, Normal Wake Mode, Counter Reset is Used



Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during LATCH.

Figure 54: Wake and Sleep Timing Diagram, Short Wake Mode, Counter Reset is Used

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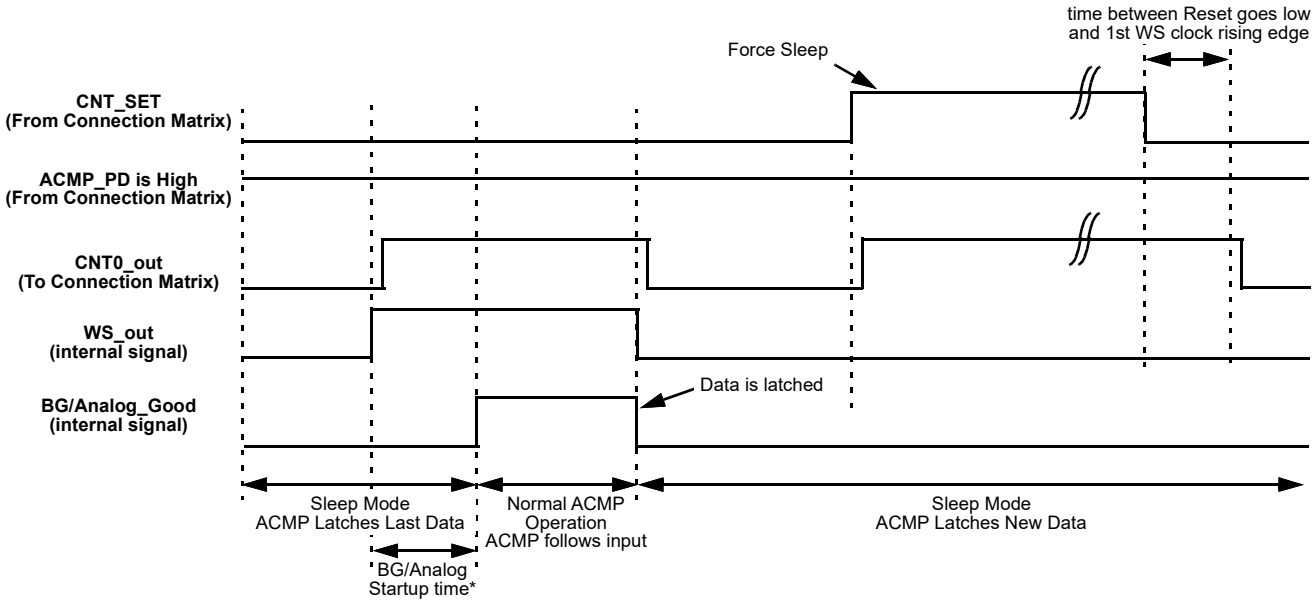
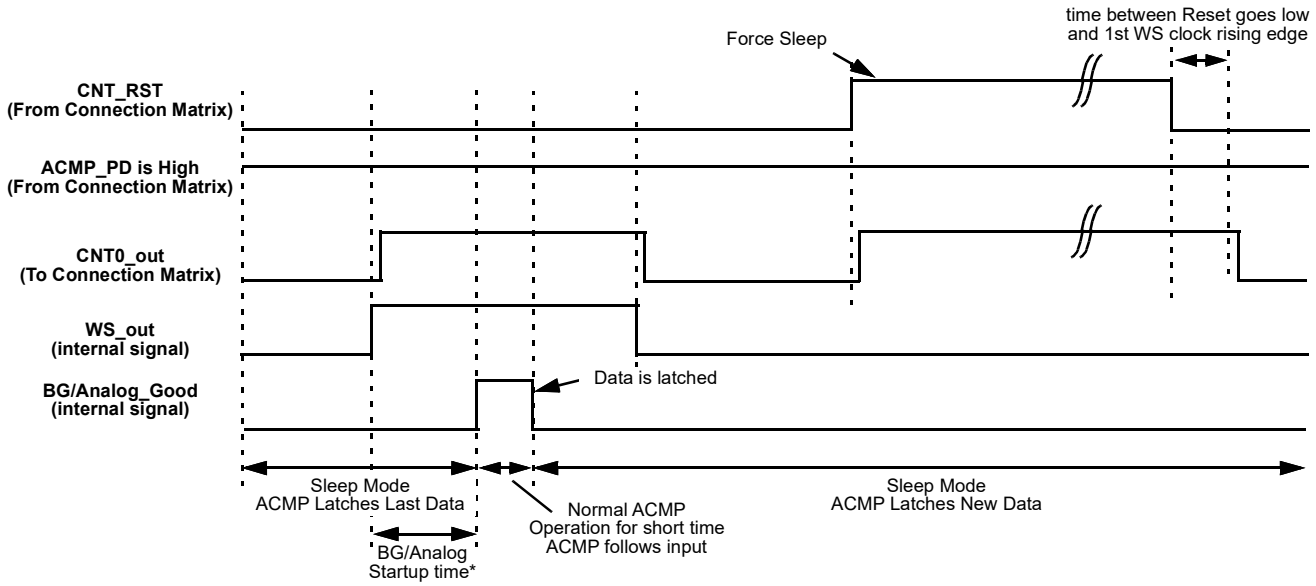


Note: CNT0_out is a delayed WS_out signal for 1 us to make sure the data is correct during LATCH.

Figure 55: Wake and Sleep Timing Diagram, Normal Wake Mode, Counter Set is Used



Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during LATCH.

Figure 56: Wake and Sleep Timing Diagram, Short Wake Mode, Counter Set is Used

Note: If low power BG is powered on/off by WS, the wake time should be longer than 2.62 ms. The BG/analog start up time will take maximal 2.62 ms. If low power BG is always on, OSC0 period is longer than required wake time. The short wake mode can be used to reduce the current consumption.

To use any ACMPxH under WS controller, the following settings must be done:

- ACMPxH Power Up Input from matrix = 1 (for each ACMPxH separately);

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- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMPxH);
- Register WS → enable (for each ACMPxH separately);
- CNT/DLY0 set/reset input = 0 (for all ACMPxH).

OSC0 is used to clock WS. The user can select a period of time while the ACMPxH is sleeping in a range of 1 - 65535 clock cycles. Before they are sent to sleep, their outputs are latched so the ACMPs remain their state (High or Low) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low)
  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = High, the ACMPxH is continuously on.
  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = Low, the ACMPxH is continuously off.
  Both cases WS function is turned off.

- Counter Data (Range: 1 to 65535)
  User can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.

- Q mode - defines the state of WS counter data when Set/Reset signal appears Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn on the ACMPs. When Reset signal goes out, the WS counter will go Low and turn off the ACMPxH until the counter counts up to the end. Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn off the ACMPxH. When Set signal goes out, the WS counter will go on counting and High level signal will turn on the ACMPxH while counter is counting up to the end.

Note: The OSC0 matrix power-down to control ACMP WS is not supported for short wait time option.

- Edge Select defines the edge for Q mode
  High level Set/Reset - switches mode Set/Reset when level is High

Note: Q mode operates only in case of "High Level Set/Reset".

- Wake time selection - time required for wake signal to turn the ACMPxH on

  Normal Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on until WS signal is Low again. Wake time is one clock period. It should be longer than BG turn on time and minimal required comparing time of the ACMP.

  Short Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on for 1 µs and turn off regardless of WS signal. The WS signal width does not matter.
- Keep - pauses counting while Keep = 1
- Up - reverses counting

  If Up = 1, CNT is counting up from user selected value to 65535.

  If Up = 0, CNT is counting down from user selected value to 0.

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9 Analog Comparators

There are four General Purpose Rail-to-Rail Analog Comparator (ACMP) macrocells in the SLG46826. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMP0H PWR UP, ACMP1H PWR UP, ACMP2L PWR UP, and ACMP3L PWR UP) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be on continuously, off continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, output is low.

Two of the four General Purpose Rail-to-Rail Analog Comparators are optimized for high speed operation (ACMP0H and ACMP1H), and two of the four are optimized for low power operation (ACMP2L and ACMP3L).

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage before connection to the analog comparator. Each of the ACMP cells has a negative input signal that is either created from an internal Vref or provided by way of the external sources.

PWR UP = 1 → ACMP is powered up.

PWR UP = 0 → ACMP is powered down.

During power-up, the ACMP output will remain LOW, and then become valid 51.4 µs (max) after power up signal goes high for ACMP0H and ACMP1H, and become valid 326.6 µs (max) after power up signal goes high for ACMP2L and ACMP3L. Input bias current < 1 nA (typ). The Gain divider is unbuffered and consists of 1 MΩ resistors.

Each High Speed ACMP (ACMP0H and ACMP1H) has an optional Rail-to-Rail Input Buffer, which can be used along with the Gain divider to increase ACMP input resistance. However, Input buffer will increase an input offset voltage.

Each cell also has a hysteresis selection, to offer hysteresis of (0, 32, 64, 192) mV. The hysteresis option is available when using an internal Vref only.

The ACMP0H has an additional option of connecting an internal 100 µA current source to its positive input, register [1071]. It is also possible to connect the 100 µA current source to each next ACMP via an internal analog MUX.

ACMP0H IN+ options are IO14, $V_{D,}$ internal 100 µA current source
ACMP1H IN+ options are IO13, ACMP0H IN+ MUX output
ACMP2L IN+ options are IO12, ACMP0H IN+ MUX output, ACMP1H IN+ MUX output
ACMP3L IN+ options are IO11, ACMP2L IN+ MUX output, Temp Sensor OUT

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9.1 ACMP0H BLOCK DIAGRAM

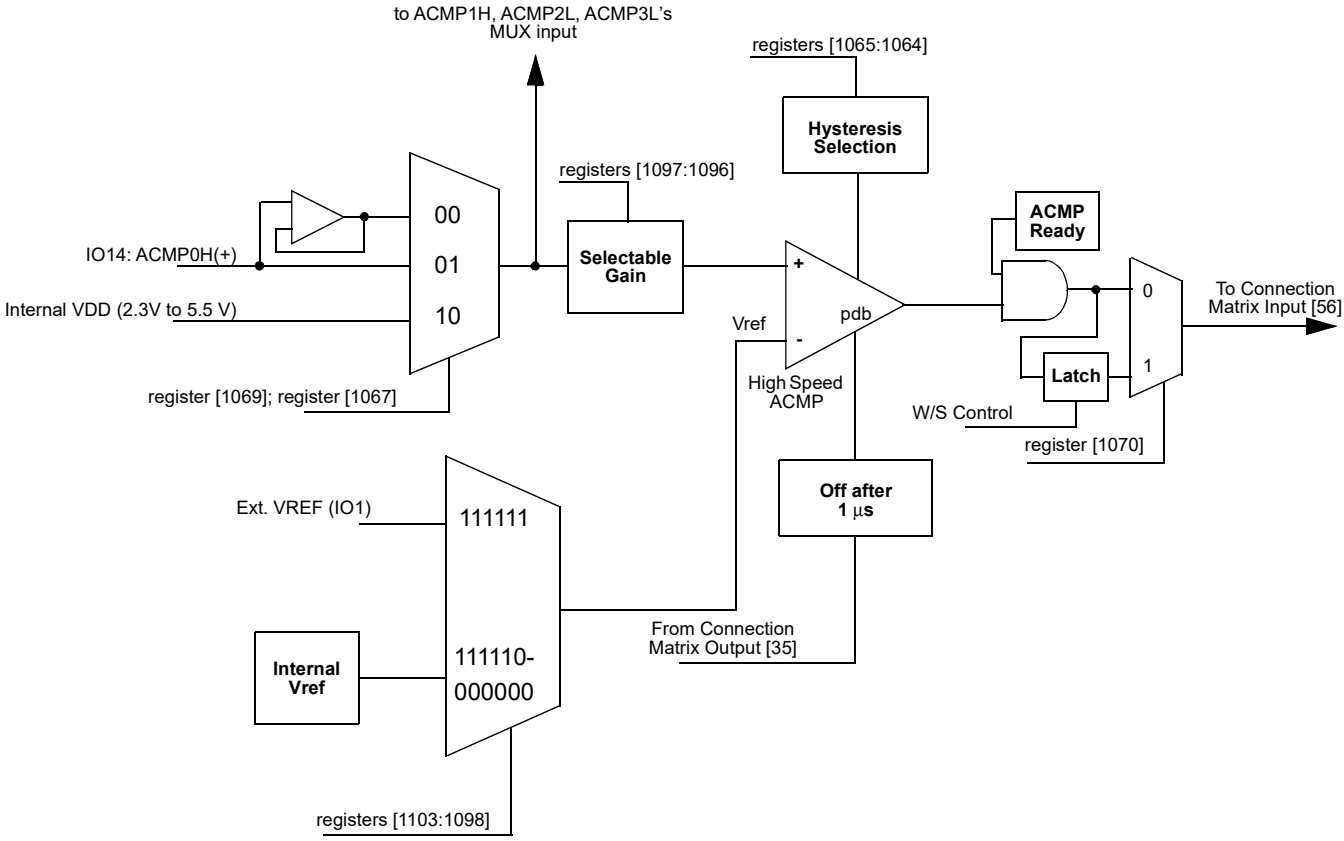

Figure 57: ACMP0H Block Diagram

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9.2 ACMP1H BLOCK DIAGRAM

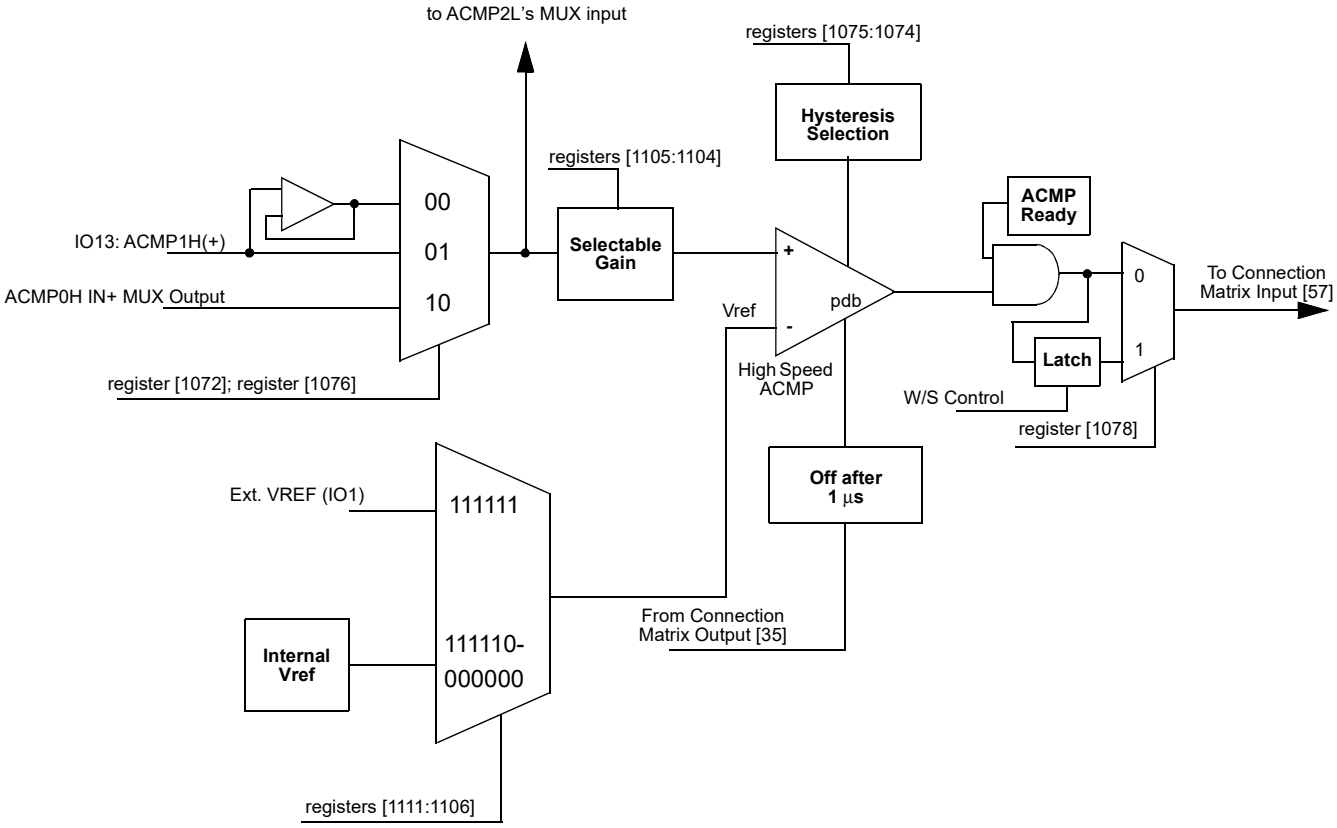

Figure 58: ACMP1H Block Diagram

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9.3 ACMP2L BLOCK DIAGRAM

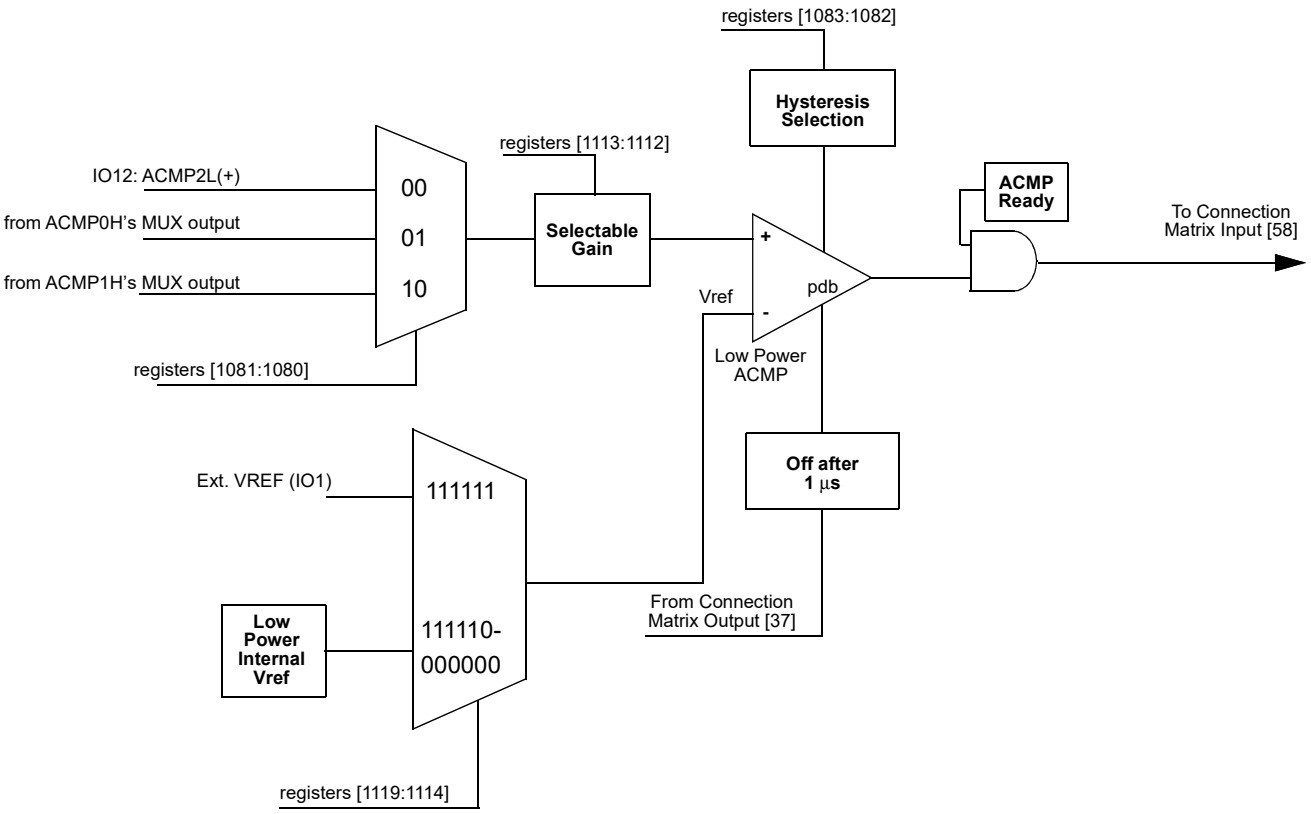

Figure 59: ACMP2L Block Diagram

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9.4 ACMP3L BLOCK DIAGRAM

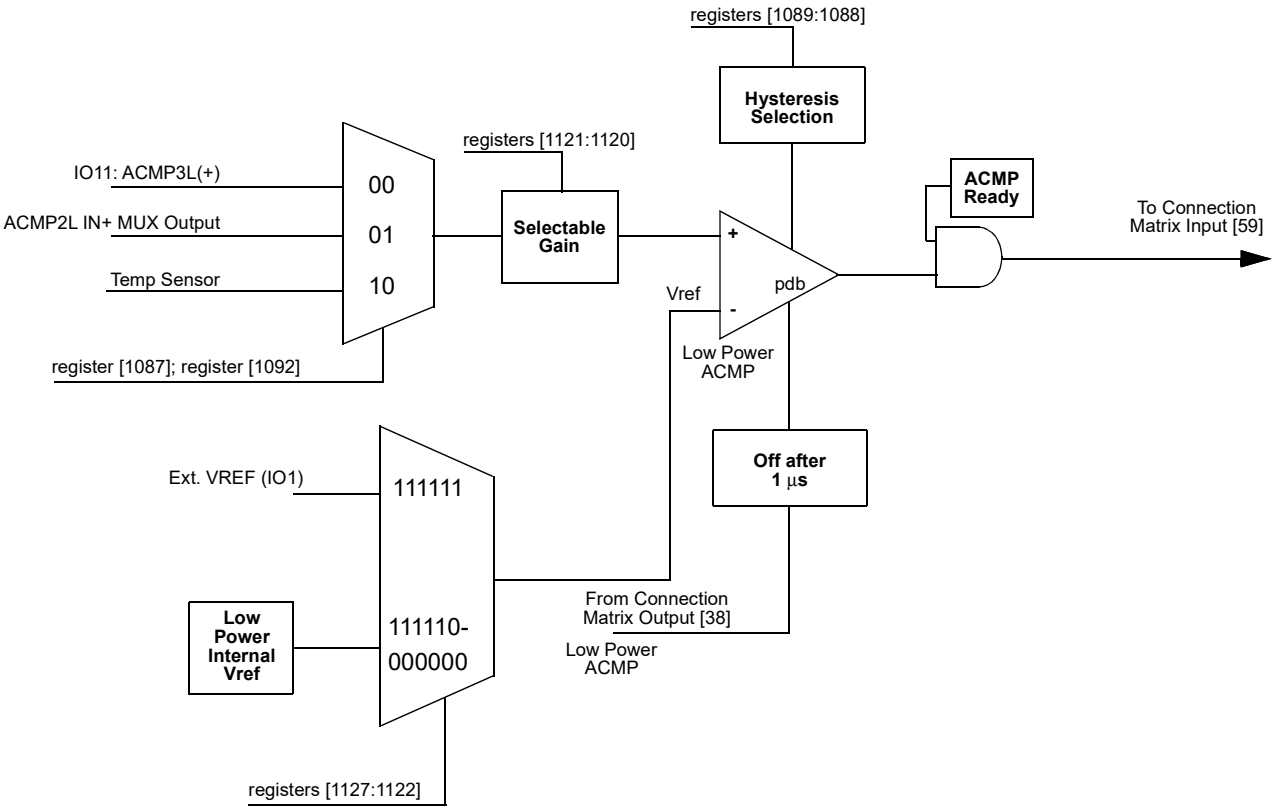

Figure 60: ACMP3L Block Diagram

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9.5 ACMP TYPICAL PERFORMANCE

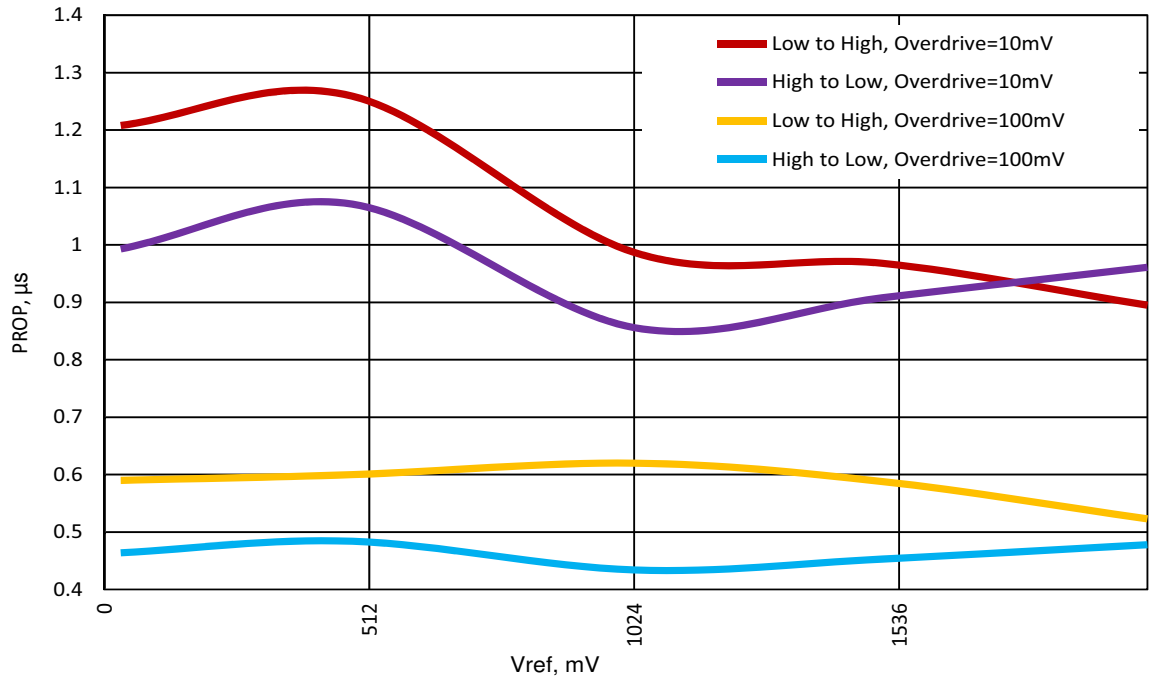

Figure 61: Typical Propagation Delay vs. Vref for ACMPxH at T = 25 °C, Gain = 1, Buffer - Disabled, Hysteresis = 0

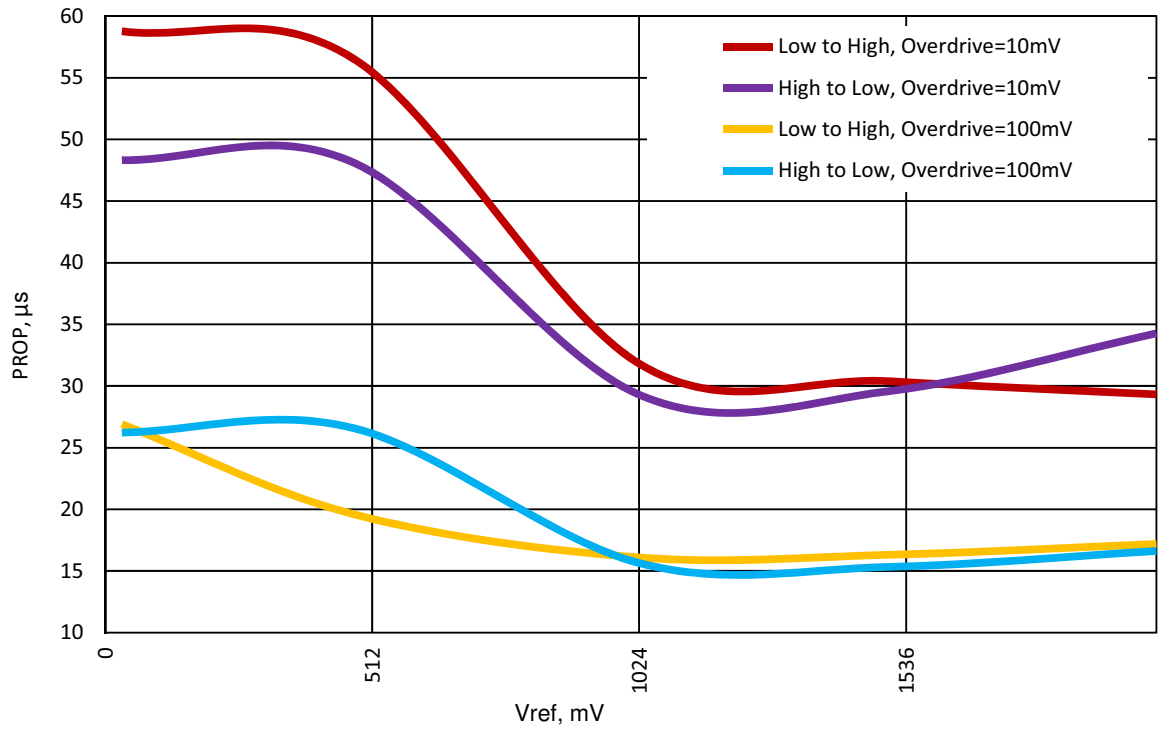

Figure 62: Typical Propagation Delay vs. Vref for ACMPxL at T = 25 °C, Gain = 1, Buffer - Disabled, Hysteresis = 0

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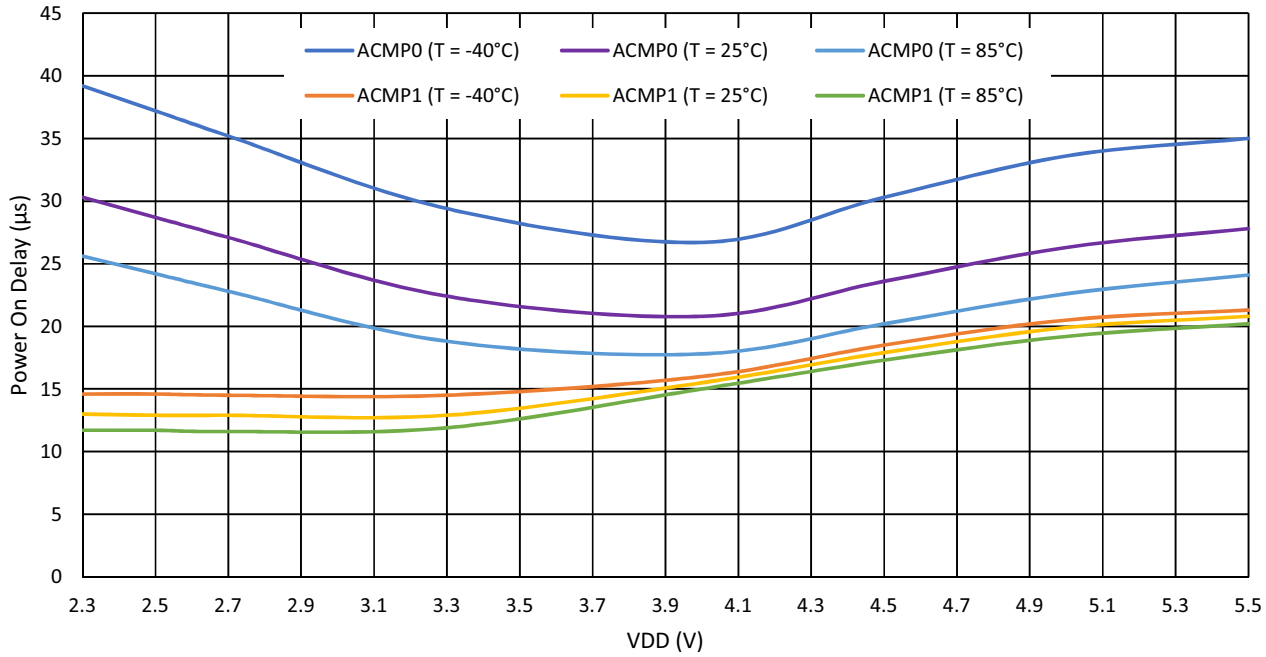

Figure 63: ACMPxH Power-On Delay vs. V_{DD}

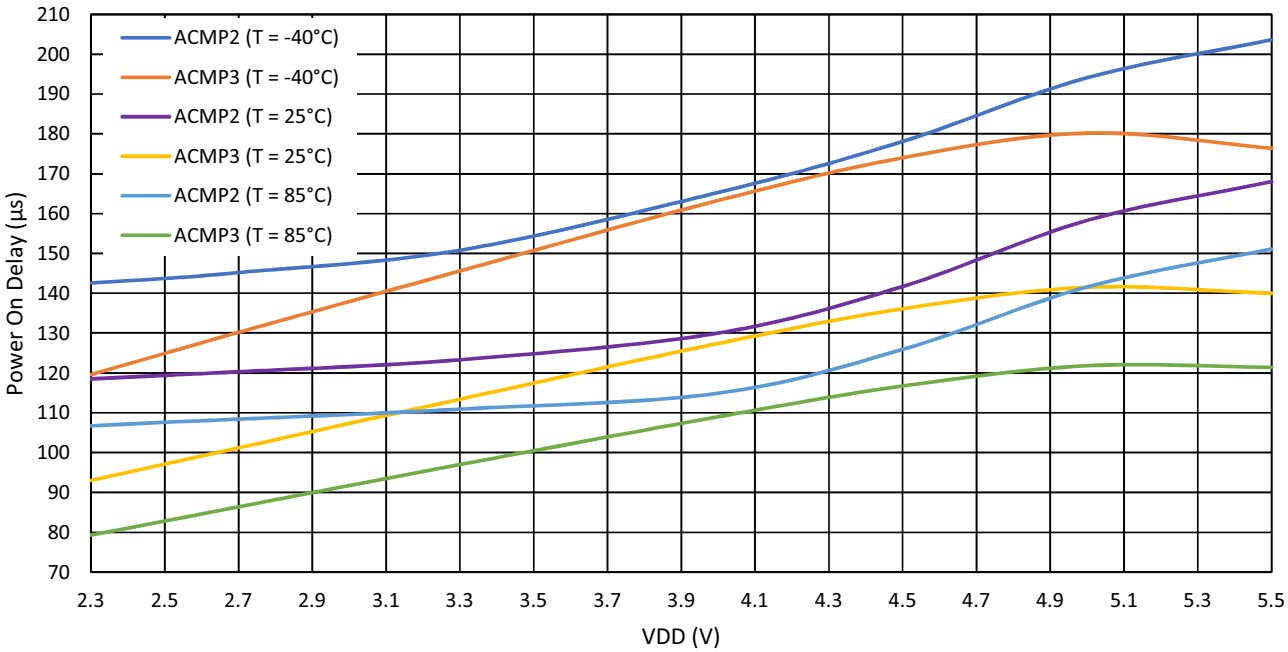

Figure 64: ACMPxL Power-On Delay vs. V_{DD}

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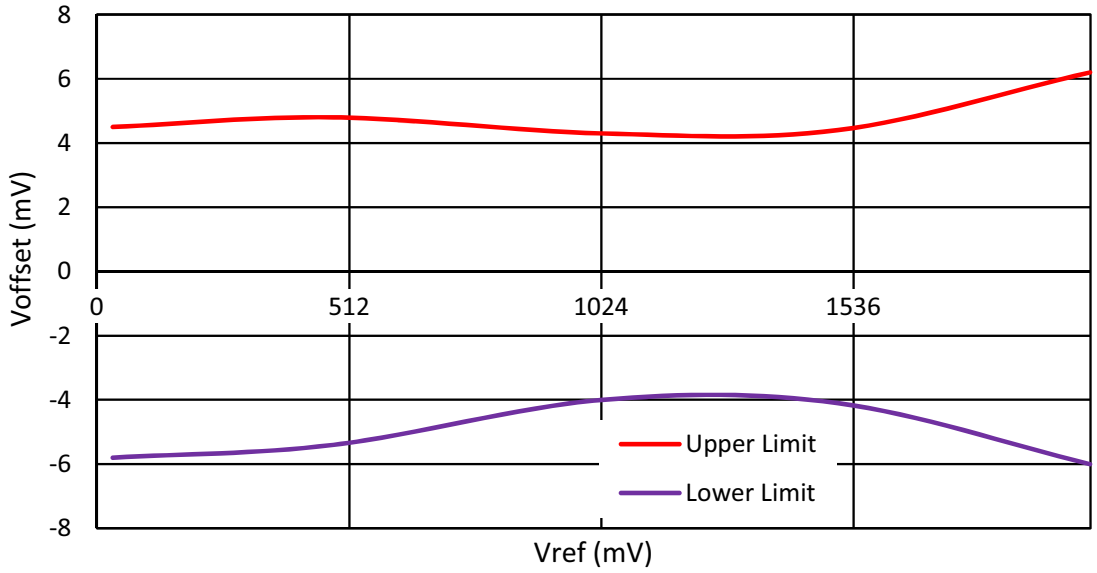

Figure 65: ACMPxH Input Offset Voltage vs. Vref at T = -40 °C to 85 °C, Input Buffer Disabled

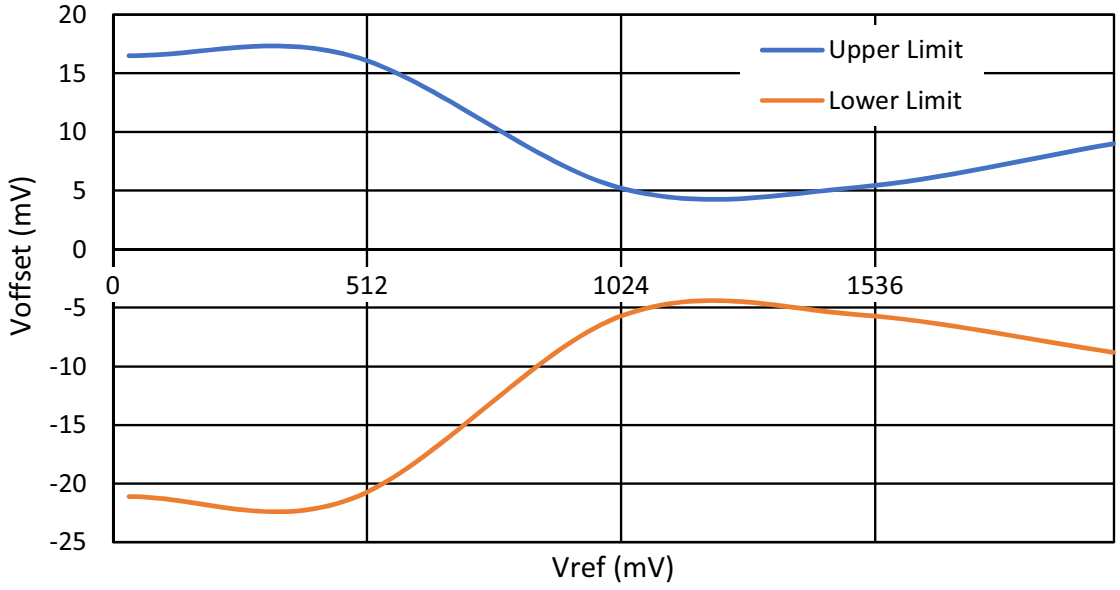

Figure 66: ACMPxH Input Offset Voltage vs. Vref at T = -40 °C to 85 °C, Input Buffer Enabled

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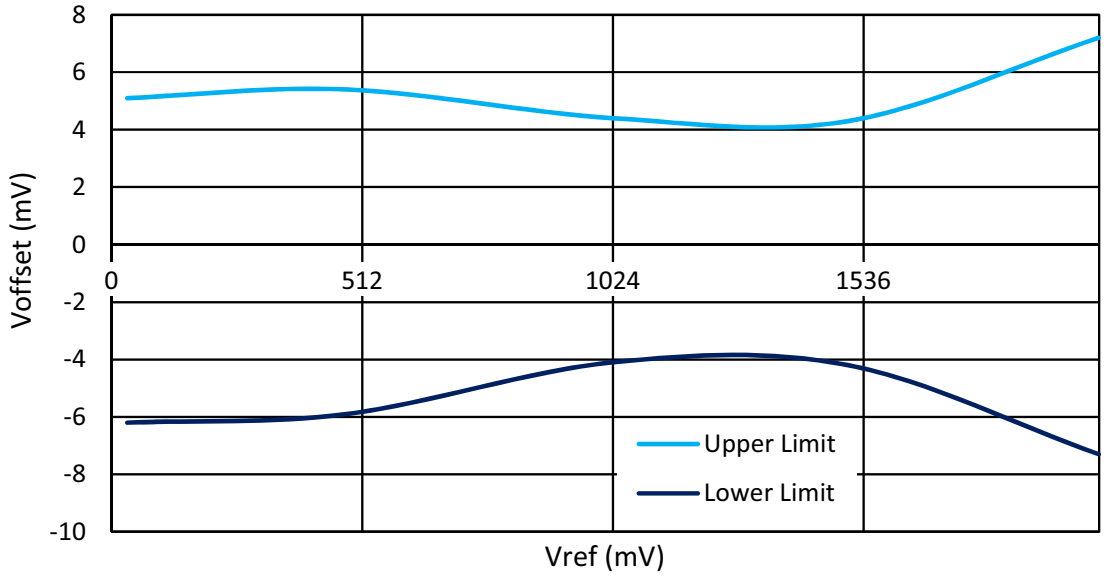

Figure 67: ACMPxL Input Offset Voltage vs. Vref at T = -40 °C to 85 °C

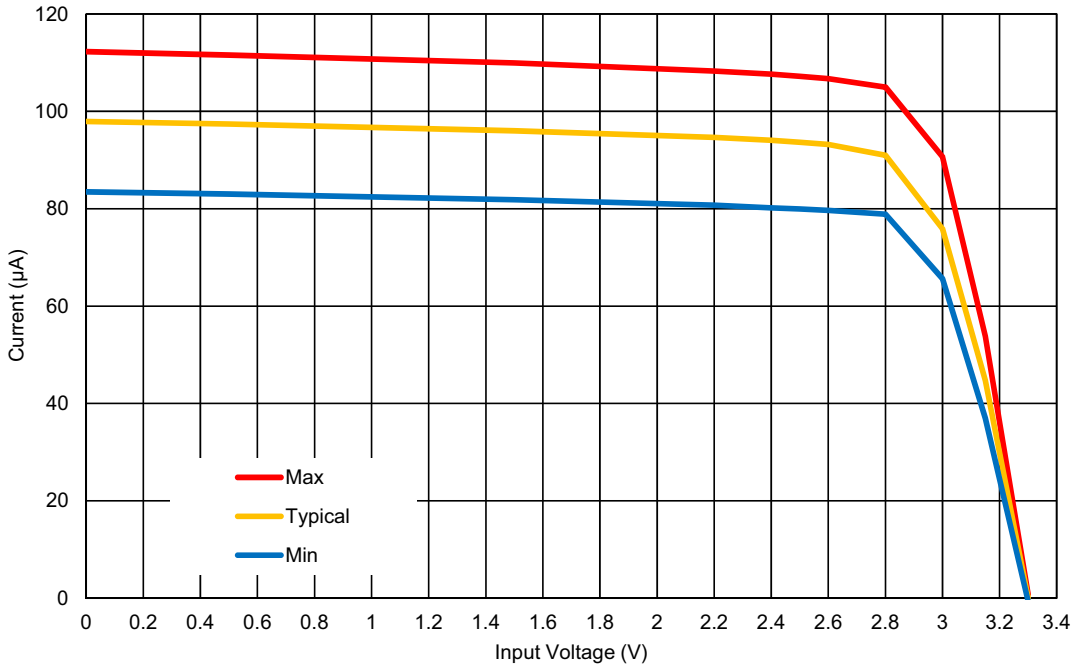

Figure 68: ACMP Input Current Source vs. Input Voltage at T = -40 °C to 85 °C, V_{DD} = 3.3 V

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10 Programmable Delay/Edge Detector

The SLG46826 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (time 2) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. See Figure 70 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

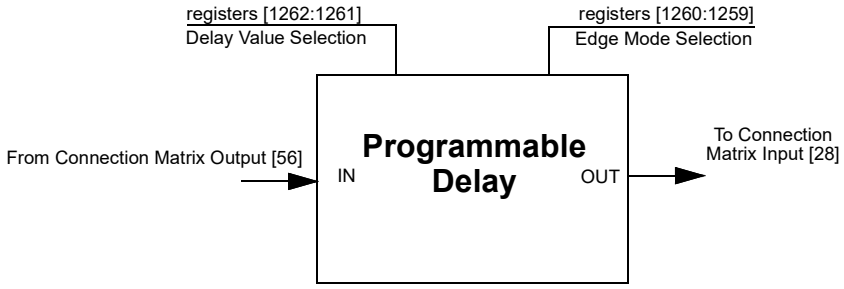

Figure 69: Programmable Delay

10.1 PROGRAMMABLE DELAY TIMING DIAGRAM - EDGE DETECTOR OUTPUT

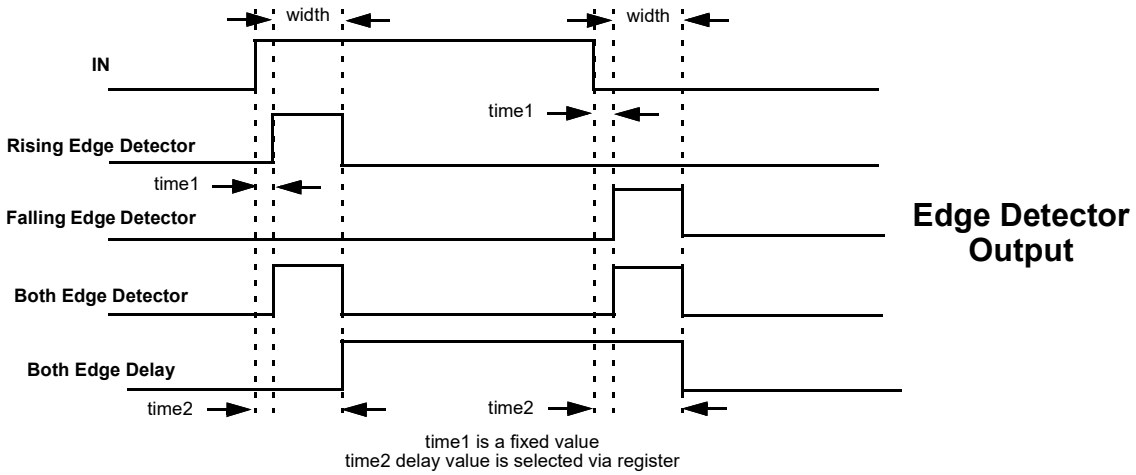

Figure 70: Edge Detector Output

Please refer to Table 11.

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11 Additional Logic Function. Deglitch Filter

The SLG46826 has one Deglitch Filter macrocell with inverter function that is connected directly to the Connection Matrix inputs and outputs. In addition, this macrocell can be configured as an Edge Detector, with the following settings:

- Rising Edge Detector
- Falling Edge Detector
- Both Edge Detector
- Both Edge Delay

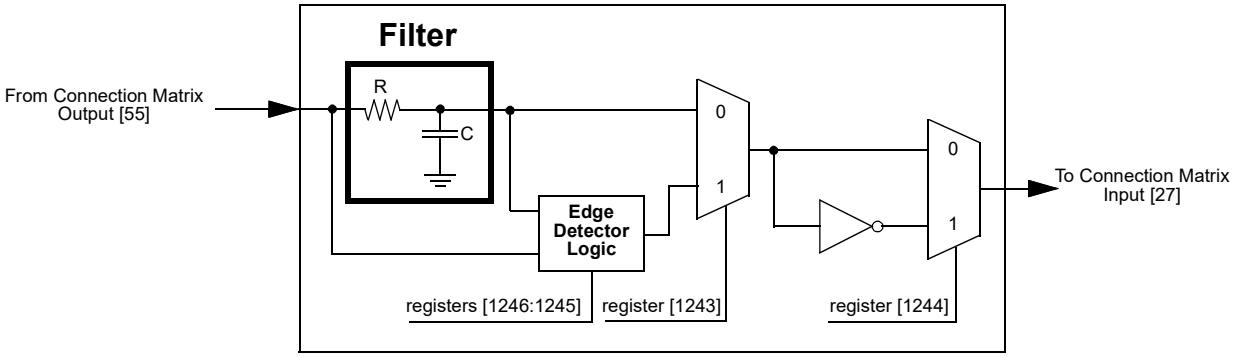

Figure 71: Deglitch Filter or Edge Detector

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12 Voltage Reference

12.1 VOLTAGE REFERENCE OVERVIEW

The SLG46826 has a Voltage Reference (Vref) Macrocell to provide references to the four analog comparators. This macrocell can supply a user selection of fixed voltage references, or temperature sensor output. The macrocell also has the option to output reference voltages on IO9 and IO10. See Table 47 for the available selections for each analog comparator. Also, see Figure 72, which shows the reference output structure.

12.2 VREF SELECTION TABLE

Table 47: Vref Selection Table

SEL[5:0]	Vref	SEL[5:0]	Vref
0	0.032	32	1.056
1	0.064	33	1.088
2	0.096	34	1.12
3	0.128	35	1.152
4	0.16	36	1.184
5	0.192	37	1.216
6	0.224	38	1.248
7	0.256	39	1.28
8	0.288	40	1.312
9	0.32	41	1.344
10	0.352	42	1.376
11	0.384	43	1.408
12	0.416	44	1.44
13	0.448	45	1.472
14	0.48	46	1.504
15	0.512	47	1.536
16	0.544	48	1.568
17	0.576	49	1.6
18	0.608	50	1.632
19	0.64	51	1.664
20	0.672	52	1.696
21	0.704	53	1.728
22	0.736	54	1.76
23	0.768	55	1.792
24	0.8	56	1.824
25	0.832	57	1.856
26	0.864	58	1.888
27	0.896	59	1.92
28	0.928	60	1.952
29	0.96	61	1.984
30	0.992	62	2.016
31	1.024	63	External

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12.3 VREF BLOCK DIAGRAM

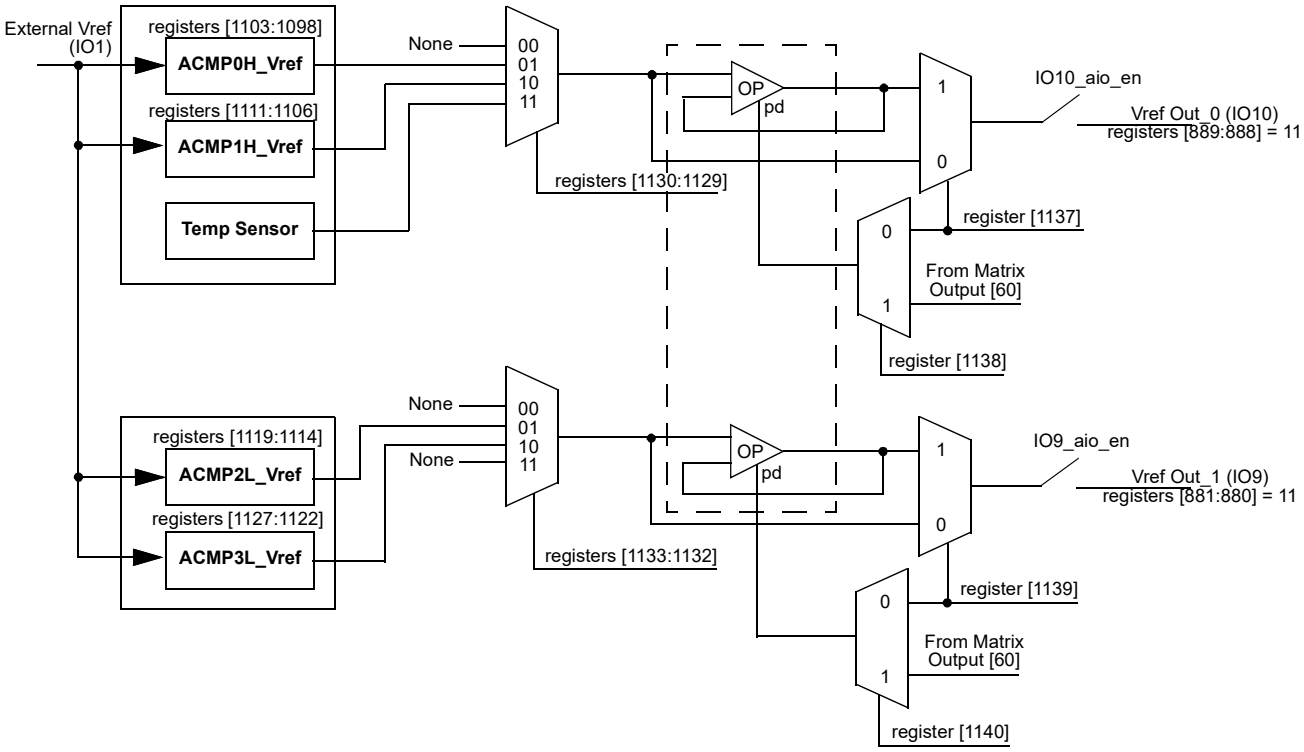

Figure 72: Voltage Reference Block Diagram

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12.4 VREF LOAD REGULATION

Note 1 It is not recommended to use Vref connected to external pin without buffer.

Note 2 Vref buffer performance is not guaranteed at V_{DD} < 2.7 V.

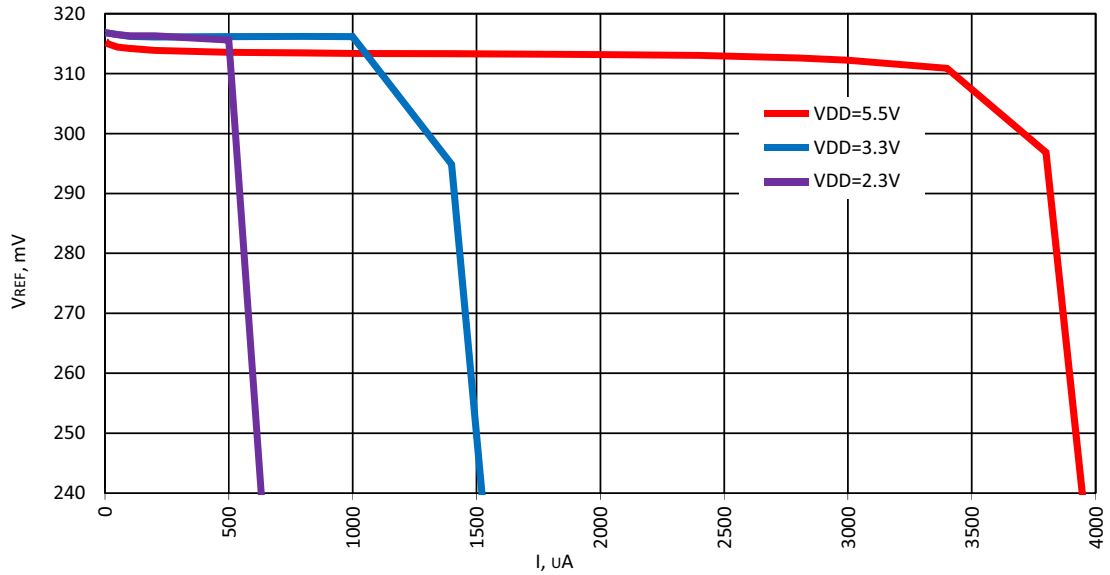

Figure 73: Typical Load Regulation, Vref = 320 mV, T = -40 °C to +85 °C, Buffer - Enable

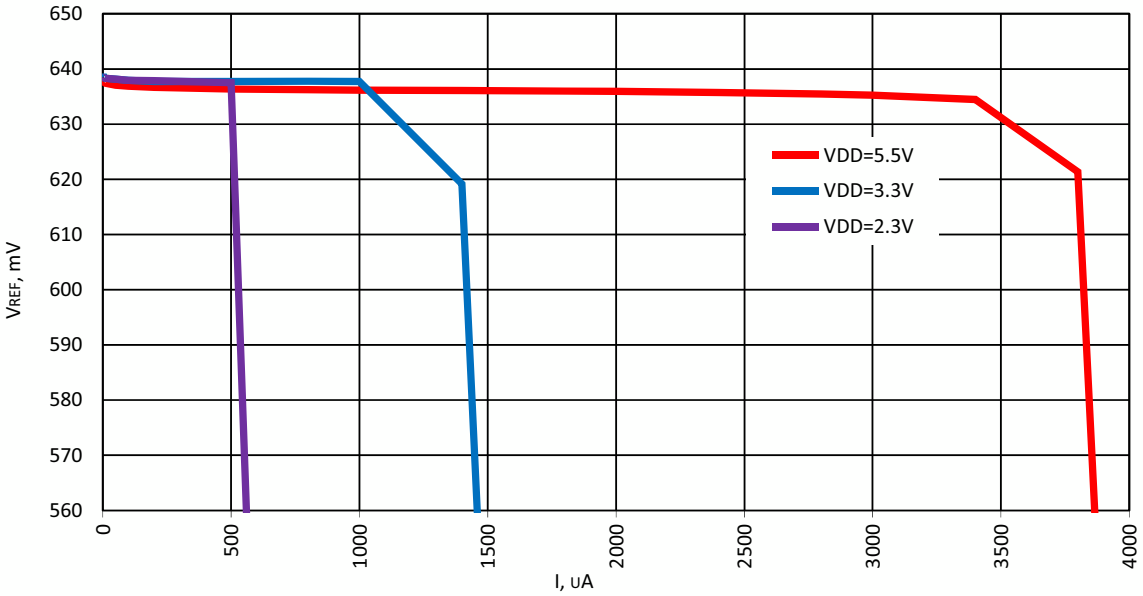

Figure 74: Typical Load Regulation, Vref = 640 mV, T = -40 °C to +85 °C, Buffer - Enable

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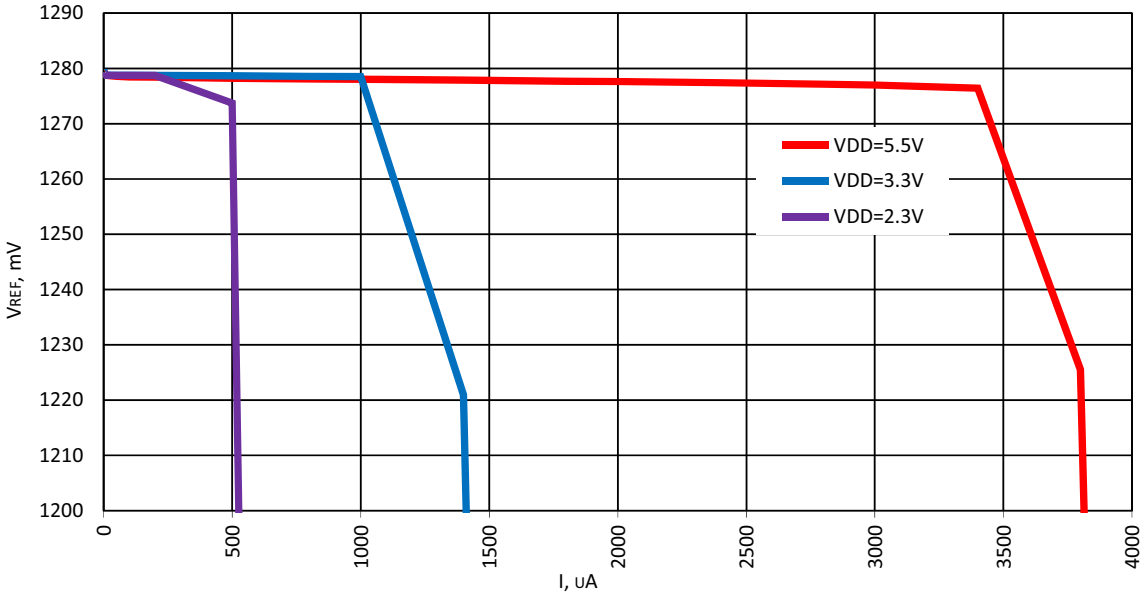

Figure 75: Typical Load Regulation, Vref = 1280 mV, T = -40 °C to +85 °C, Buffer - Enable

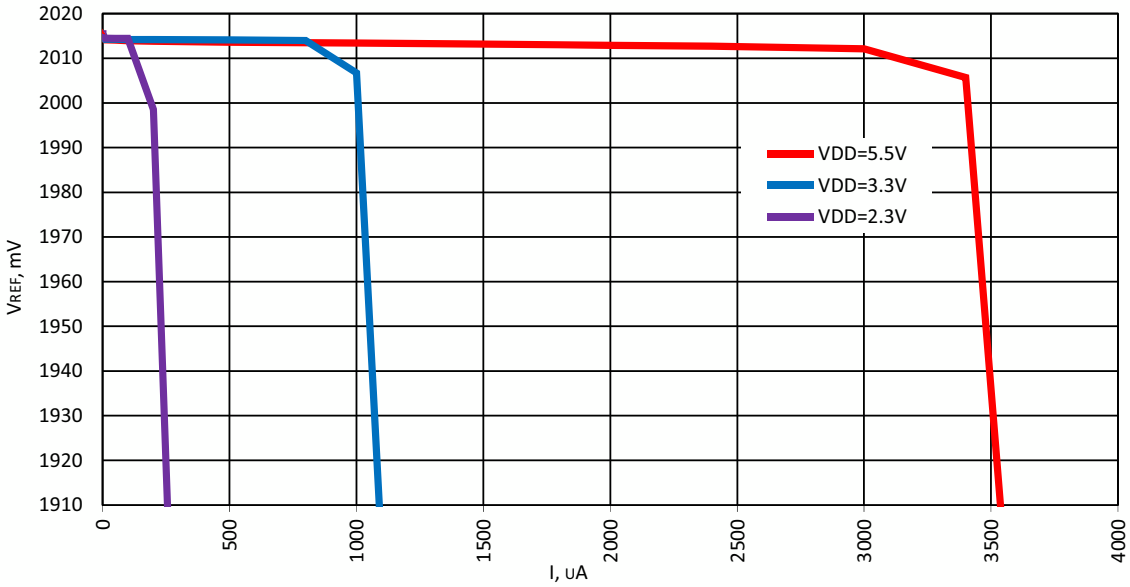

Figure 76: Typical Load Regulation, Vref = 2016 mV, T = -40 °C to +85 °C, Buffer - Enable

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13 Clocking

13.1 OSCILLATOR GENERAL DESCRIPTION

The SLG46826 has three internal oscillators to support a variety of applications:

- Oscillator0 (2.048 kHz)
- Oscillator1 (2.048 MHz)
- Oscillator2 (25 MHz)

There are two divider stages for each oscillator that gives the user flexibility for introducing clock signals to connection matrix, as well as various other Macrocells. The pre-divider (first stage) for Oscillator allows the selection of /1, /2, /4 or /8 to divide down frequency from the fundamental. The second stage divider has an input of frequency from the pre-divider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24 or /64 on Connection Matrix Input lines [27], [28], and [29]. Please see Figure 80 for more details on the SLG46826 clock scheme.

Oscillator2 (25 MHz) has an additional function of 100 ns delayed startup, which can be enabled/disabled by register [1052]. This function is recommended to use when analog blocks are used along with the Oscillator.

The Matrix Power-down/Force On function allows switching off or force on the oscillator using an external pin. The Matrix Power-down/Force On (Connection Matrix Output [72], [73], [74]) signal has the highest priority. The OSC operates according to the Table 48.

Table 48: Oscillator Operation Mode Configuration Settings

POR	External Clock Selection	Signal From Connection Matrix	Register: Power-Down or Force On by Matrix Input	Register: Auto Power-On or Force On	OSC Enable Signal from CNT/DLY Macrocells	OSC Operation Mode
0	X	X	X	X	X	OFF
1	1	X	X	X	X	Internal OSC is OFF, logic is ON
1	0	1	0	X	X	OFF
1	0	1	1	X	X	ON
1	0	0	X	1	X	ON
1	0	0	X	0	CNT/DLY requires OSC	ON
1	0	0	X	0	CNT/DLY does not require OSC	OFF

Note 1 The OSC will run only when any macrocell that uses OSC is powered on.

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13.2 OSCILLATOR0 (2.048 kHz)

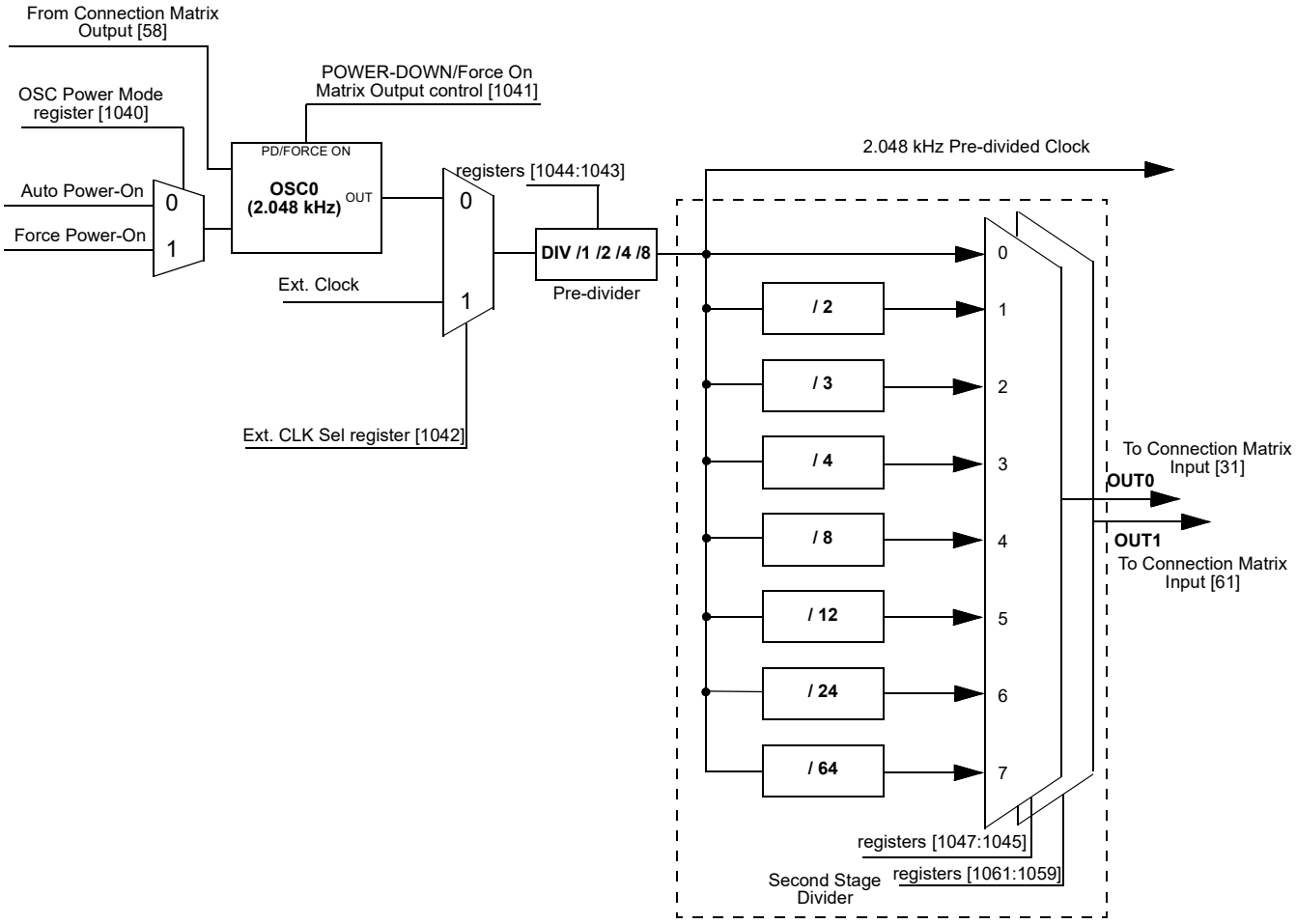

Figure 77: Oscillator0 Block Diagram

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13.3 OSCILLATOR1 (2.048 MHZ)

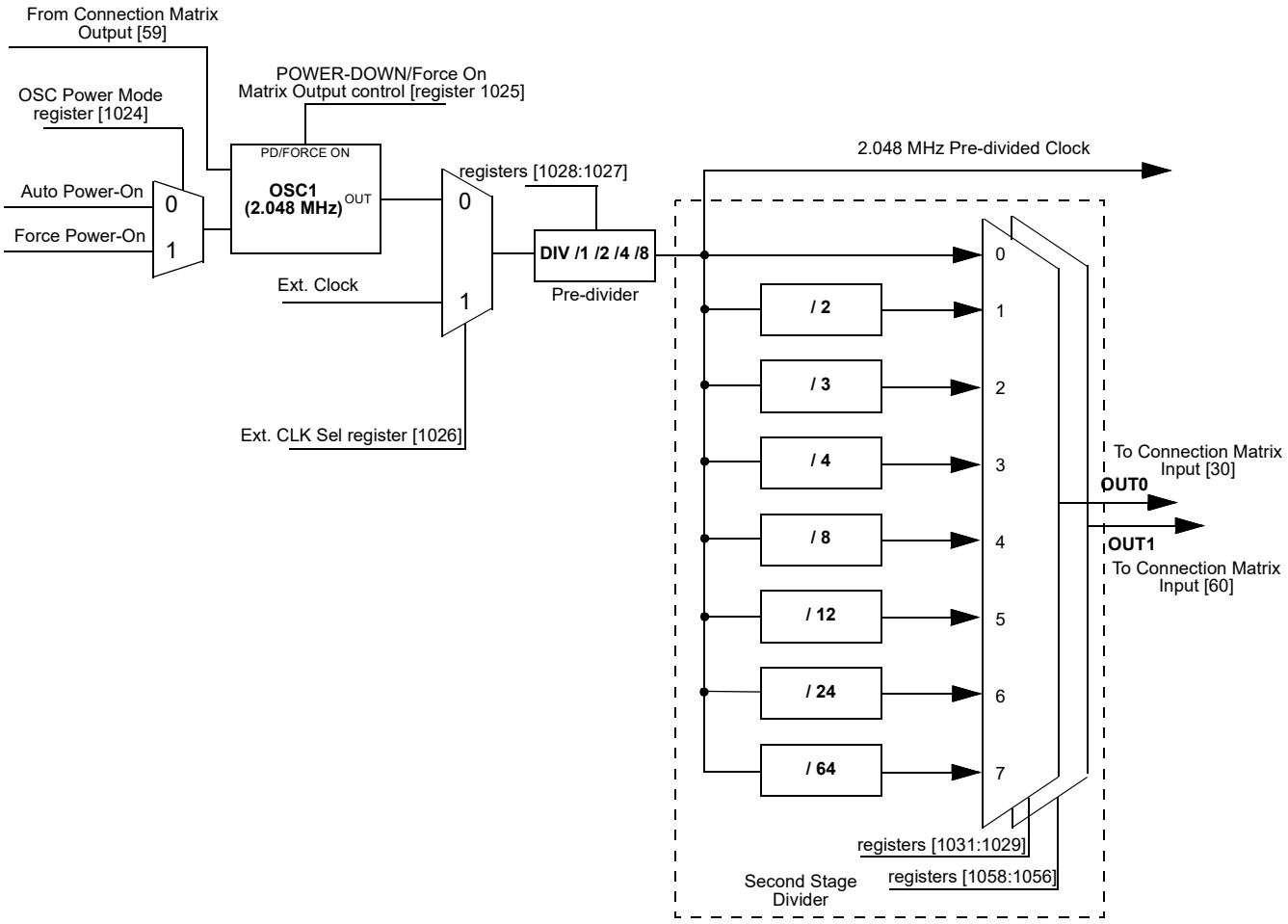

Figure 78: Oscillator1 Block Diagram

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13.4 OSCILLATOR2 (25 MHZ)

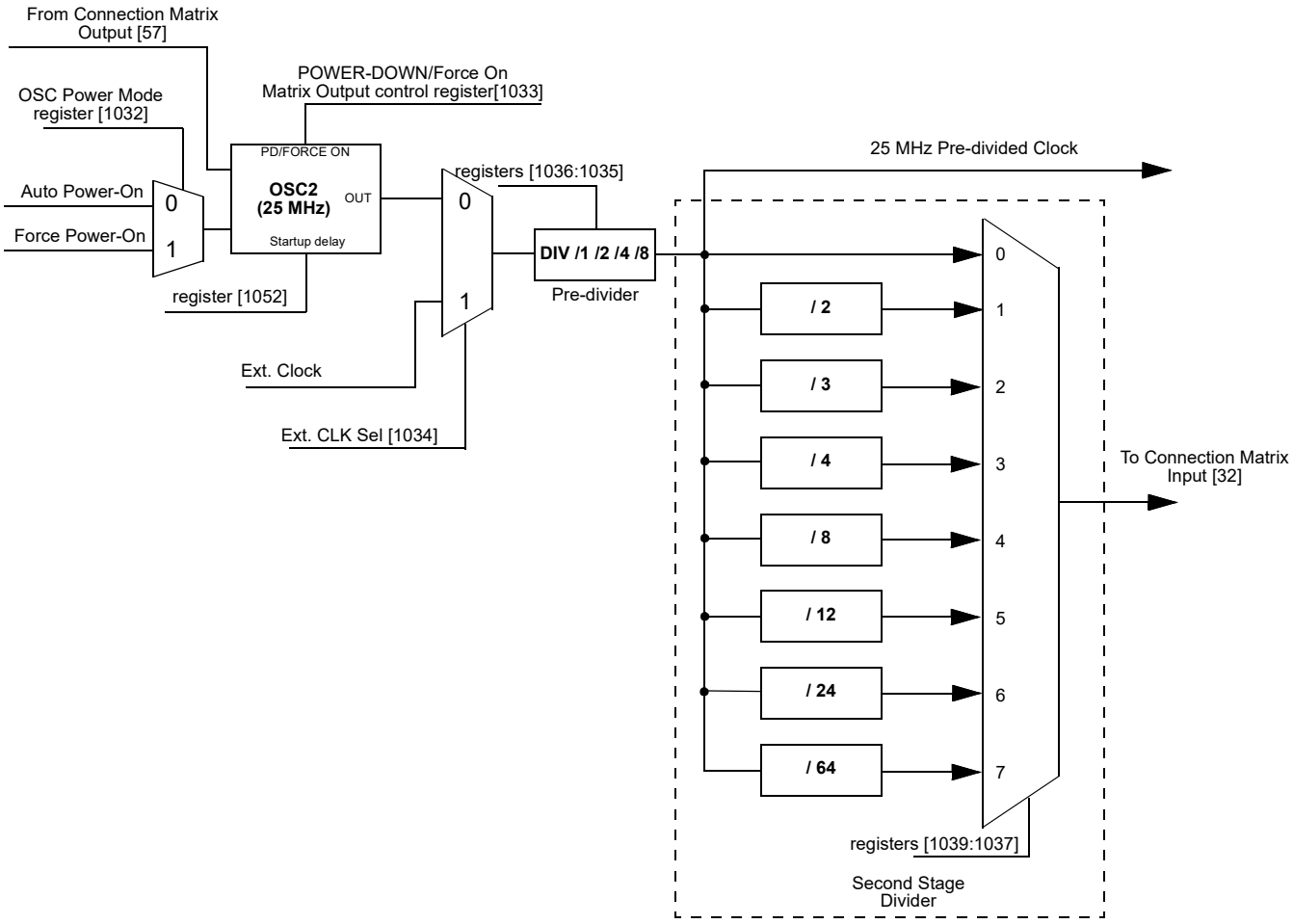

Figure 79: Oscillator2 Block Diagram

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13.5 CNT/DLY CLOCK SCHEME

Each CNT/DLY within Multi-Function macrocell has its own additional clock divider connected to oscillators pre-divider. Available dividers are:

- OSC0/1, OSC0/8, OSC0/64, OSC0/512, OSC0/4096, OSC0/32768, OSC0/262144
- OSC1/1, OSC1/8, OSC1/64, OSC1/512
- OSC2/1, OSC2/4

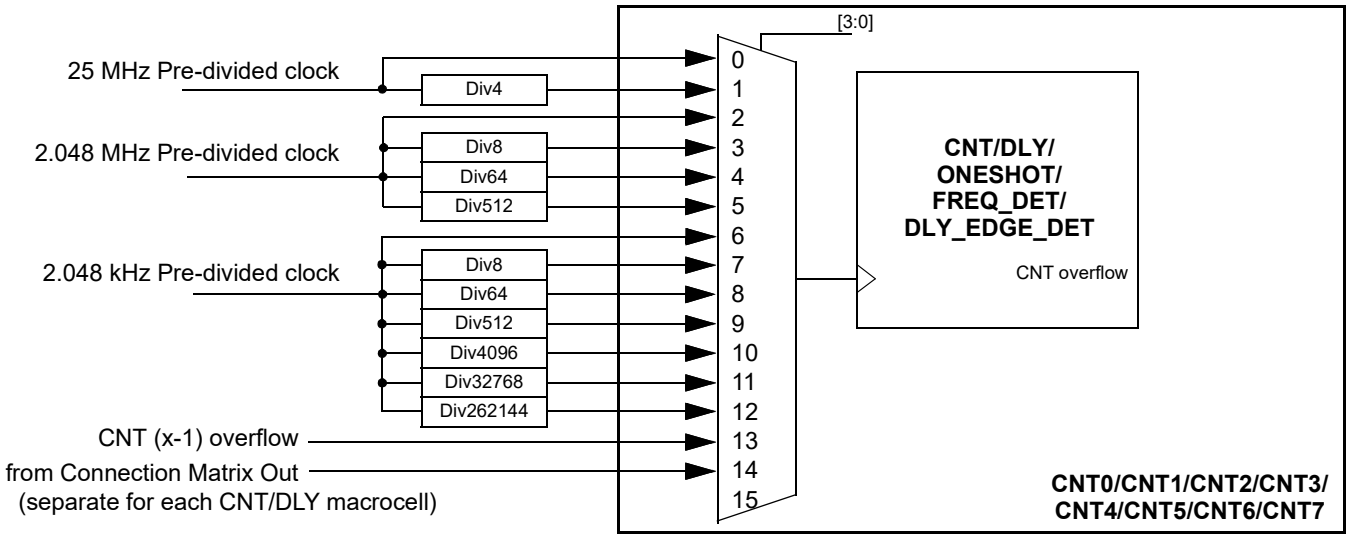

Figure 80: Clock Scheme

13.6 EXTERNAL CLOCKING

The SLG46826 supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

13.6.1 IO0 Source for Oscillator0 (2.048 kHz)

When register [1042] is set to 1, an external clocking signal on IO0 will be routed in place of the internal oscillator derived 2.048 kHz clock source. See Figure 77. The high and low limits for frequency that can be selected are 0 MHz and 10 MHz.

13.6.2 IO10 Source for Oscillator1 (2.048 MHz)

When register [1026] is set to 1, an external clocking signal on IO10 will be routed in place of the internal oscillator derived 2.048 MHz clock source. See Figure 78. The high and low limits for frequency that can be selected are 0 MHz and 10 MHz.

13.6.3 IO8 Source for Oscillator2 (25 MHz)

When register [1034] is set to 1, an external clocking signal on IO8 will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 79. The external frequency range is 0 MHz to 20 MHz at V_{DD} = 2.3 V, 0 MHz to 30 MHz at V_{DD} = 3.3 V, 0 MHz to 50 MHz at V_{DD} = 5.0 V. When an external clock is selected for OSC2, the oscillator's output signal will be inverted with respect to the IO8 input signal.

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13.7 OSCILLATORS POWER-ON DELAY

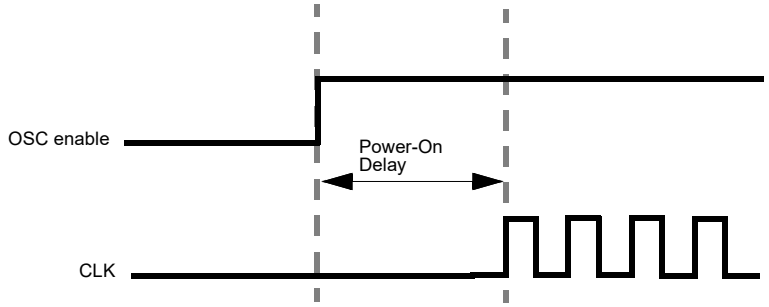

Figure 81: Oscillator Startup Diagram

Note 1 OSC power mode: “Auto Power-On”.

Note 2 “OSC enable” signal appears when any macrocell that uses OSC is powered on.

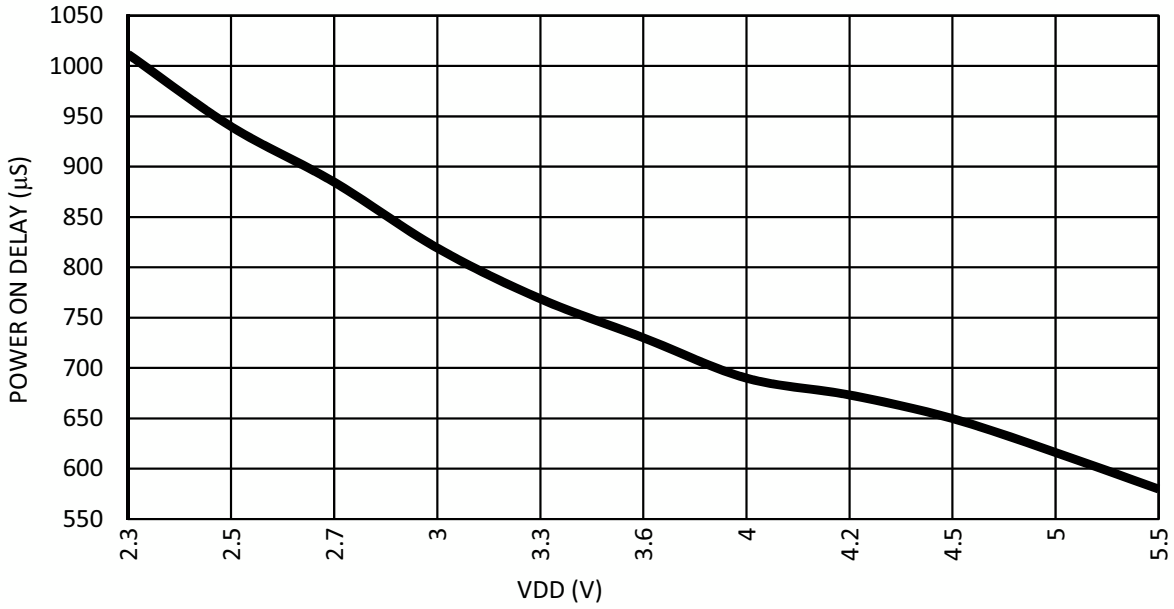

Figure 82: Oscillator0 Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC0 = 2.048 kHz

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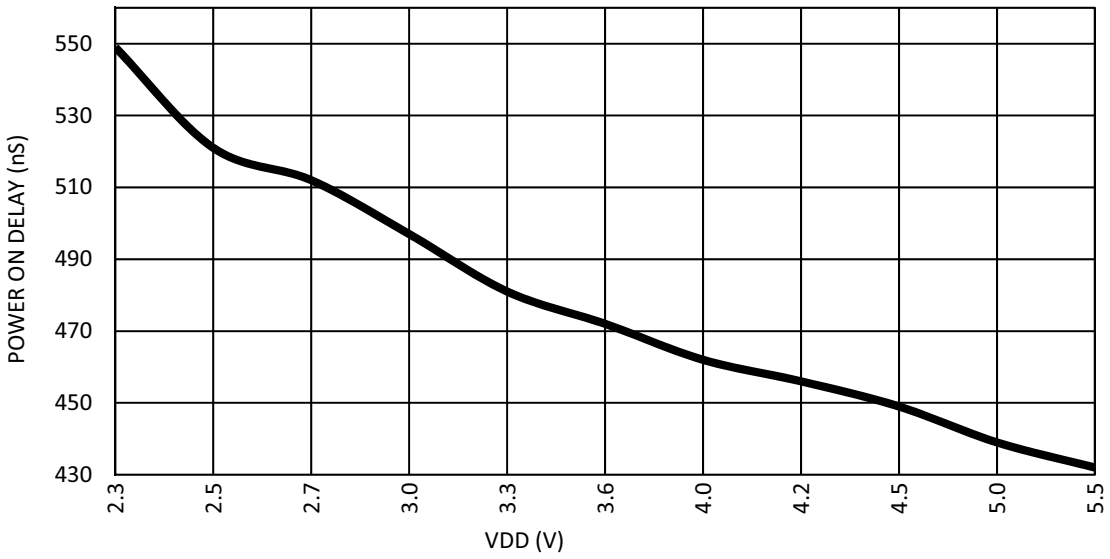

Figure 83: Oscillator1 Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC1 = 2.048 MHz

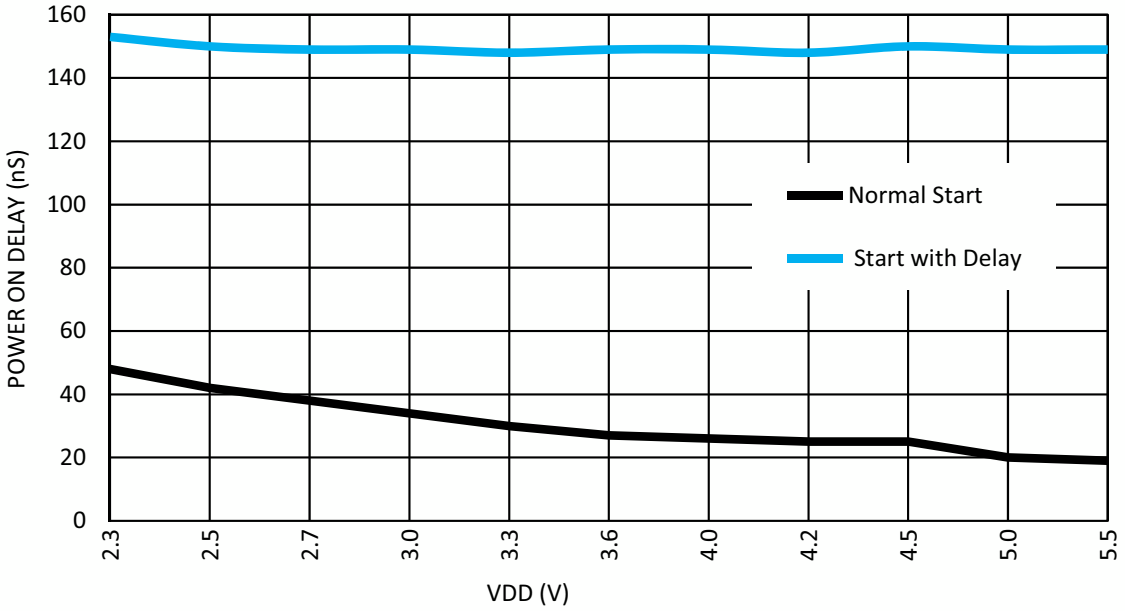

Figure 84: Oscillator2 Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC2 = 25 MHz

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13.8 OSCILLATORS ACCURACY

Note: OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

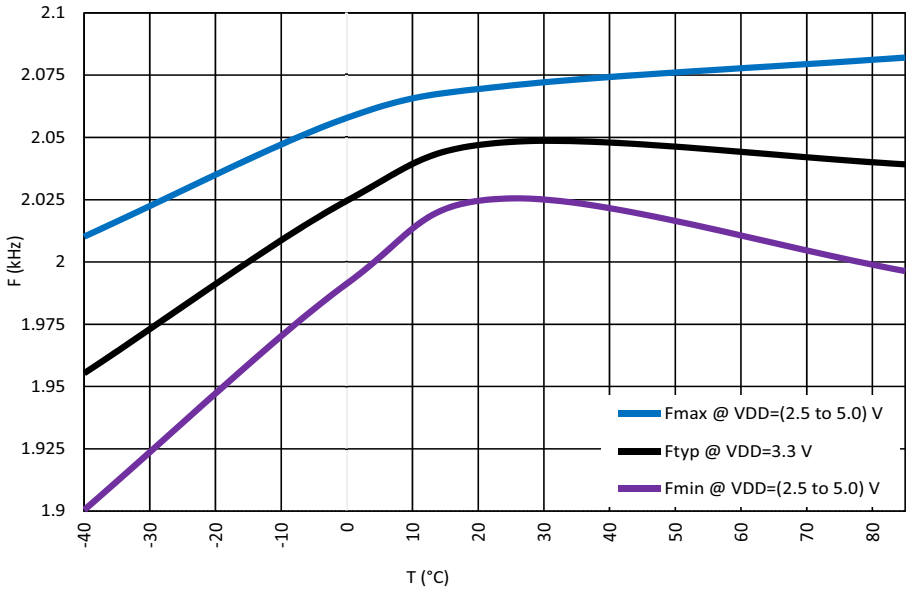

Figure 85: Oscillator0 Frequency vs. Temperature, OSC0 = 2.048 kHz

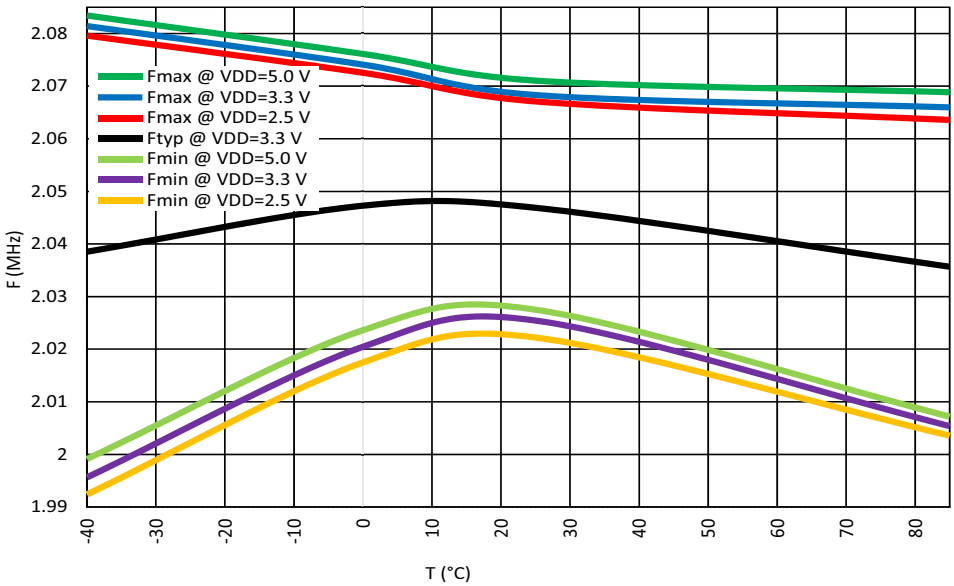

Figure 86: Oscillator1 Frequency vs. Temperature, OSC1 = 2.048 MHz

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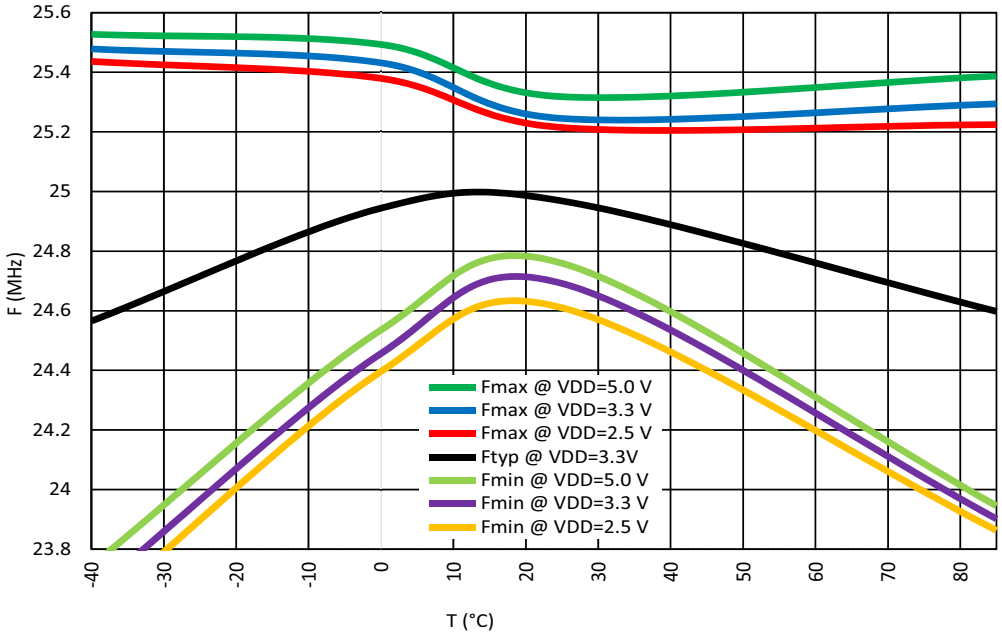

Figure 87: Oscillator2 Frequency vs. Temperature, OSC2 = 25 MHz

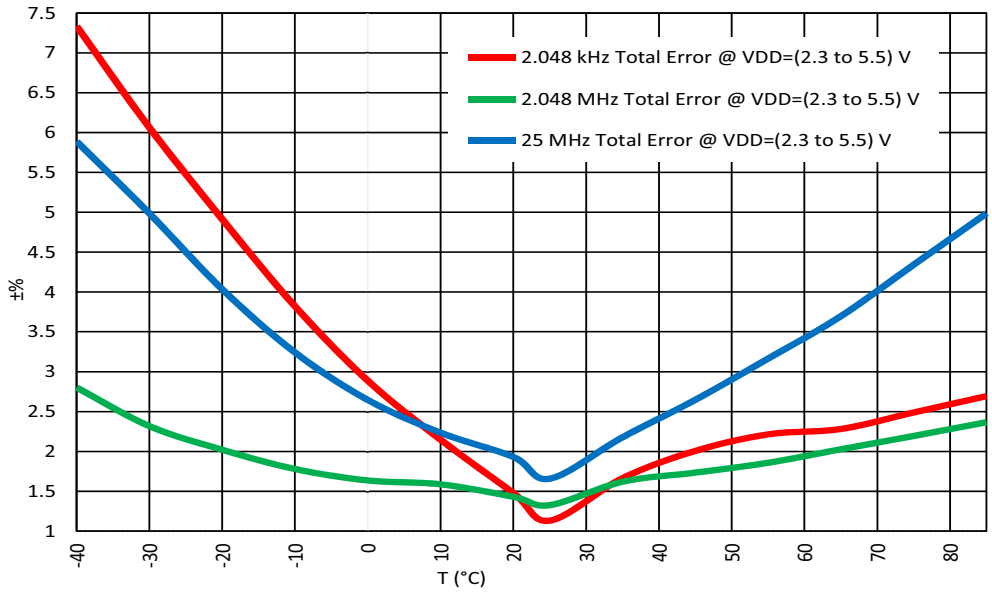

Figure 88: Oscillators Total Error vs. Temperature

Note: For more information see Section 3.6.

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Table 49: Oscillator Output Duty Cycle

	Second Stage Divider									
	OSC0 OSC1	OSC2	OSC0 OSC1 OSC2	OSC0 OSC1	OSC2	OSC0 OSC1 OSC2	OSC0 OSC1 OSC2	OSC0 OSC1 OSC2	OSC0 OSC1 OSC2	OSC0 OSC1 OSC2
Pre-divider	1		2	3		4	8	12	24	64
1	50	60	50	33.3	66	50	50	50	50	50
2	50	50	50	33.3	66	50	50	50	50	50
4	50	50	50	33.3	66	50	50	50	50	50
8	50	50	50	33.3	66	50	50	50	50	50

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14 Power-On Reset

The SLG46826 has a Power-On Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IOs.

14.1 GENERAL OPERATION

The SLG46826 is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on PIN1 for STQFN package; voltage on PIN20 for TSSOP package) is less than Power-Off Threshold (see in Table 3.4), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (Note) than the V_{DD} voltage is applied to any other PIN. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46826, the voltage applied on the V_{DD} should be higher than the Power-On threshold (Note). The full operational V_{DD} range for the SLG46826 is 2.3 V to 5.5 V. This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-On threshold. After the POR sequence has started, the SLG46826 will have a typical Startup Time (see in Table 3.4) to go through all the steps in the sequence, and will be ready and completely operational after the POR sequence is complete.

Note: The Power-On threshold is defined in Table 3.4.

To power-down the chip, the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down, it should be less than Power-Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before, the voltage on PINs can't be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

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14.2 POR SEQUENCE

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 89.

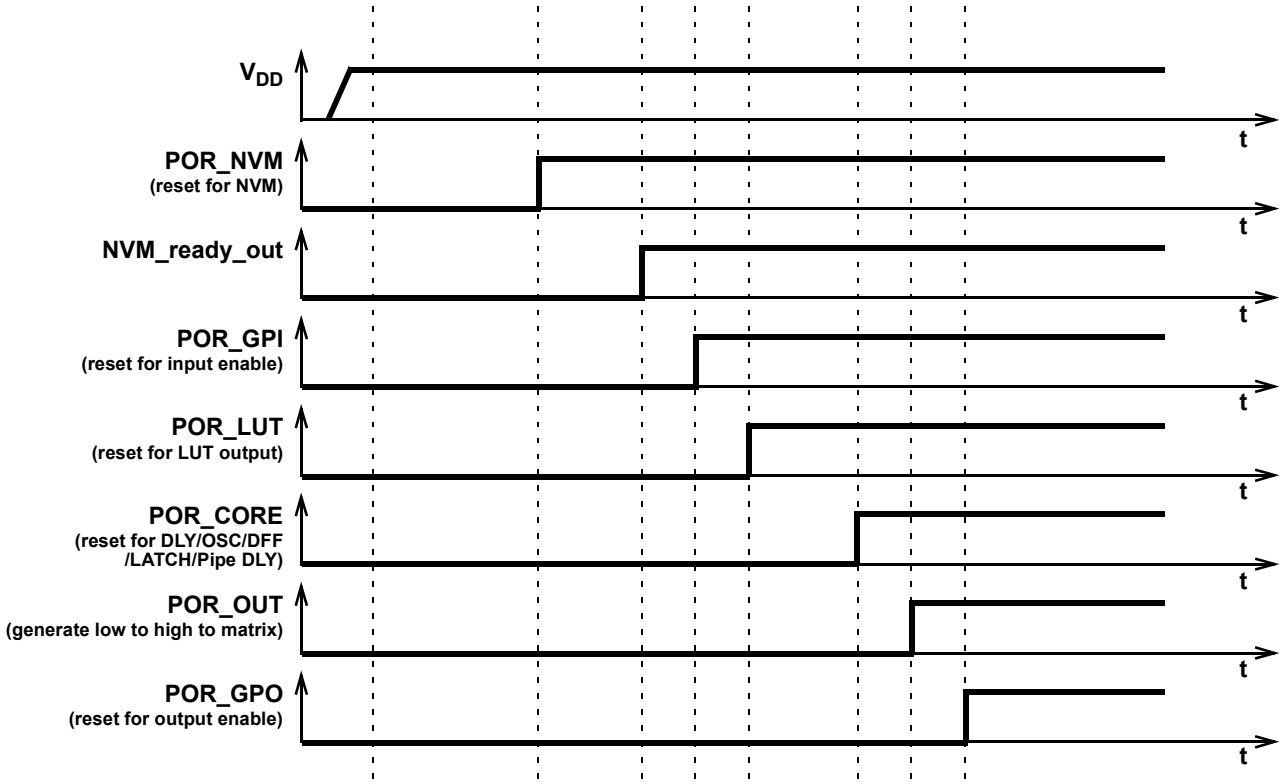

Figure 89: POR Sequence

As can be seen from Figure 89 after the V_{DD} has started ramping up and crossed the Power-On threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM, and transfers this information to a CMOS LATCH that serves to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs, the Delay cells, OSCs DFFs, LATCHES, and Pipe Delay are initialized. Only after all macrocells are initialized, internal POR signal (POR macrocell output) goes from LOW to HIGH (POR_OUT in Figure 89). The last portion of the device to be initialized is the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature, and even will vary from chip to chip (process influence).

14.3 MACROCELLS OUTPUT STATES DURING POR SEQUENCE

To have a full picture of SLG46826 operation during powering and POR sequence, refer to Figure 90, which describes the macrocell output states during the POR sequence.

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in high impedance state). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. After that input pins are enabled. Next, only LUTs are configured. Then, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output pins that become active and determined by the input signals.

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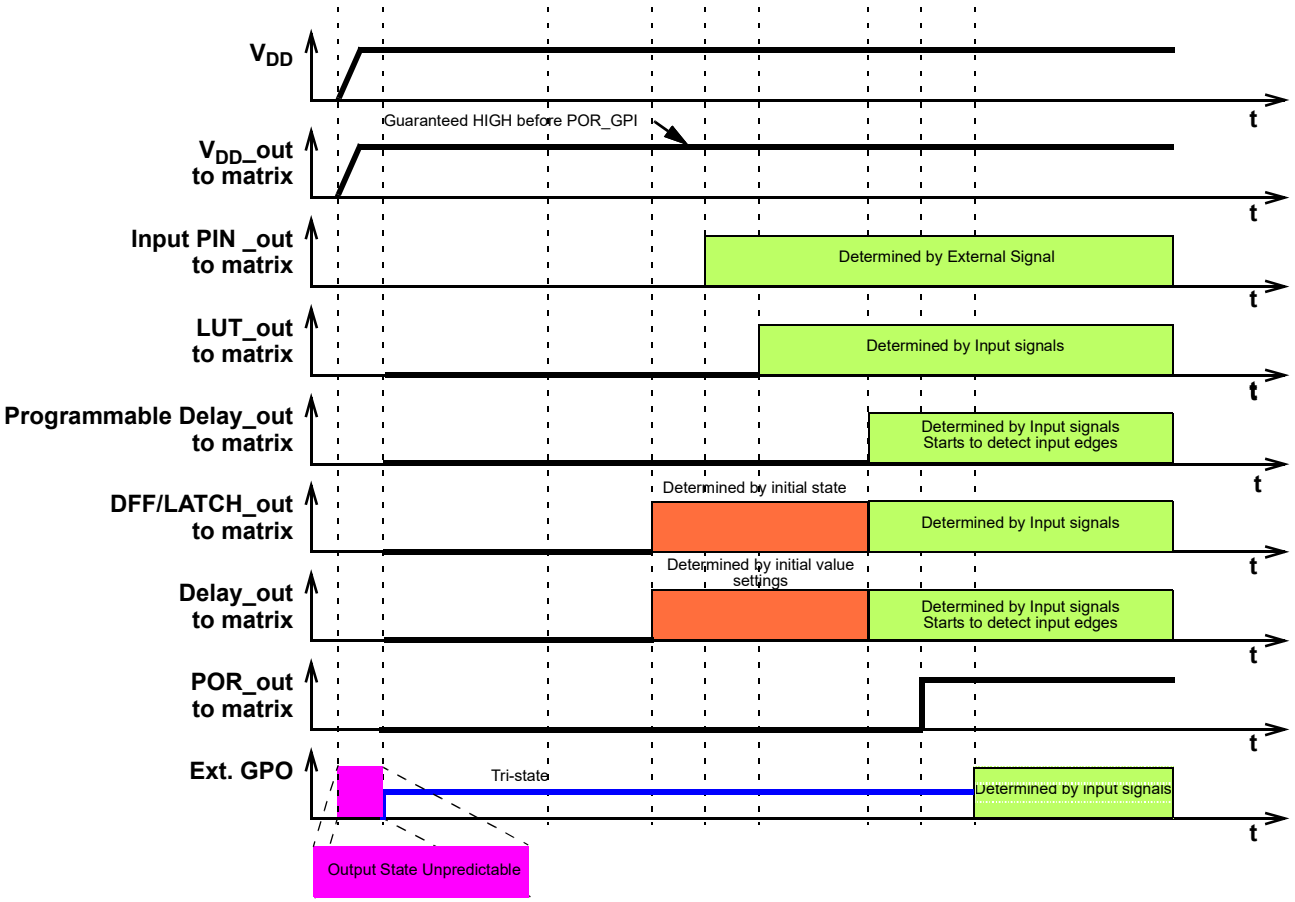

Figure 90: Internal Macrocell States during POR Sequence

14.3.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated power-up time of 1.60 V to 2.07 V, macrocells in SLG46826 are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input pins, Pull-up/down.
2. LUTs.
3. DFFs, Delays/Counters, Pipe Delay, OSCs, ACMPs.
4. POR output to matrix.
5. Output pin corresponds to the internal logic.

The Vref output pin driving signal can precede POR output signal going high by 3 µs to 5 µs. The POR signal going high indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any pin should not be higher than the V_{DD} level. There are ESD Diodes between pin → V_{DD} and pin → GND on each pin. Exceeding V_{DD} results in leakage current on the input pin, and V_{DD} will be pulled up, following the voltage on the input pin.

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14.3.2 Power-Down

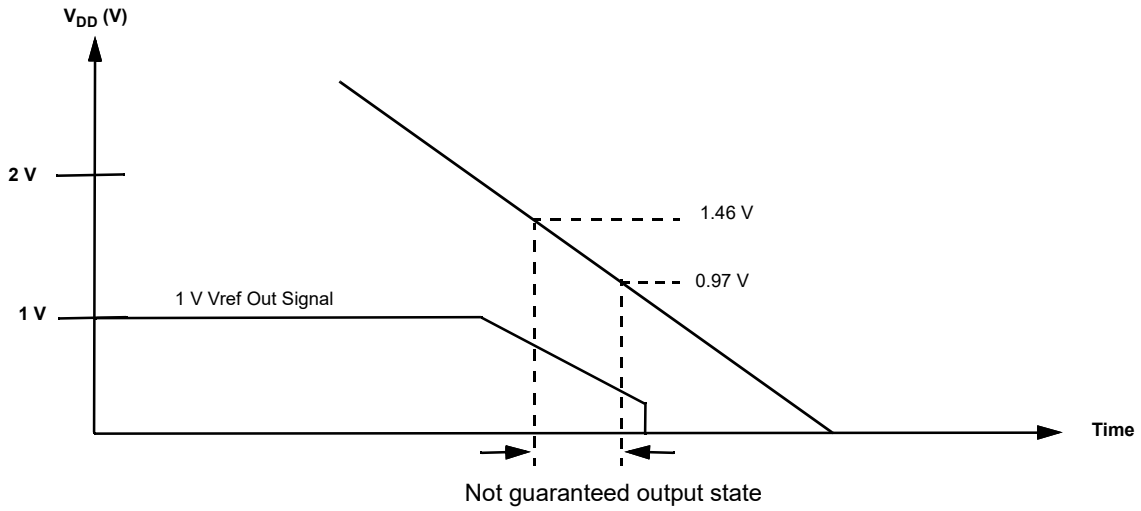

Figure 91: Power-Down

During power-down, macrocells in SLG46826 are powered off after V_{DD} falling down below Power-Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state.

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15 I²C Serial Communications Macrocell

15.1 I²C SERIAL COMMUNICATIONS MACROCELL OVERVIEW

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Controller (Master) to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

An I²C bus Controller is also able read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving an I²C bus Controller the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits registers [1795:1792]. See Section 16 for more details on I²C read/write memory protection.

15.2 I²C SERIAL COMMUNICATIONS DEVICE ADDRESSING

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 92. After the Start bit, the first four bits are a control code. Each bit in a control code can be sourced independently from the register or by value defined externally by IO5, IO4, IO3, and IO2. The LSB of the control code is defined by the value of IO2, while the MSB is defined by the value of IO5. The address source (either register bit or PIN) for each bit in the control code is defined by registers [1623:1620]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus.The default control code is 0001. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either "1111" or "0000" in a system with other target device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to insure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 16K bytes. The valid addresses are shown in the memory map in Figure 102.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address.

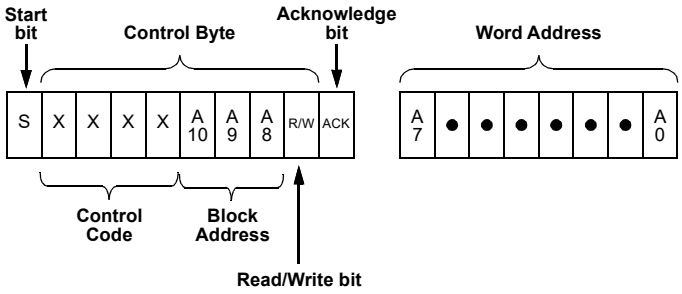

Figure 92: Basic Command Structure

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15.3 I²C SERIAL GENERAL TIMING

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 93. Timing specifications can be found in the Section 3.4.

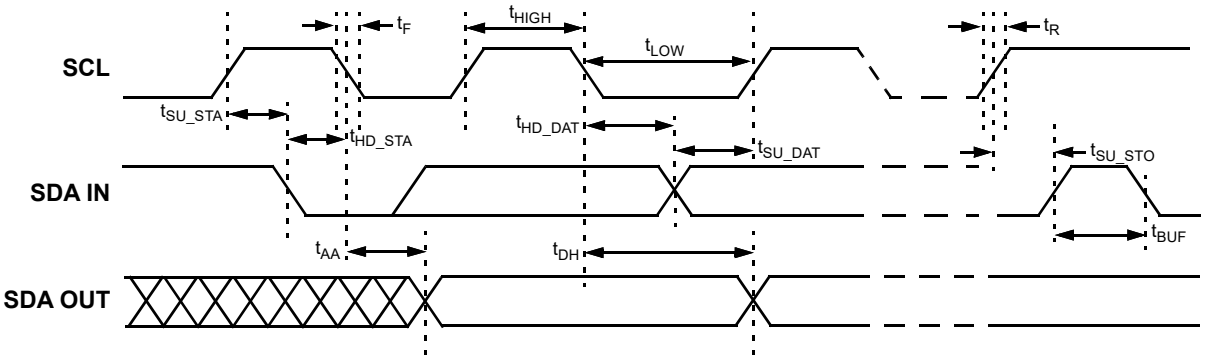

Figure 93: I²C General Timing Characteristics

15.4 I²C SERIAL COMMUNICATIONS COMMANDS

15.4.1 Byte Write Command

Following the Start condition from the Controller, the Control Code [4 bits], the Block Address [3 bits], and the R/W bit (set to “0”) are placed onto the I²C bus by the Controller. After the SLG46826 sends an Acknowledge bit (ACK), the next byte transmitted by the Controller is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG46826, where the data byte is to be written. After the SLG46826 sends another Acknowledge bit, the Controller will transmit the data byte to be written into the addressed memory location. The SLG46826 again provides an Acknowledge bit and then the Controller generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46826 generates the Acknowledge bit.

It is possible to latch all IOs during I²C write command to the register configuration data (block address A10A9A8 = 000), register [1602] = 0 - Enable. It means that IOs will remain their state until the write command is done.

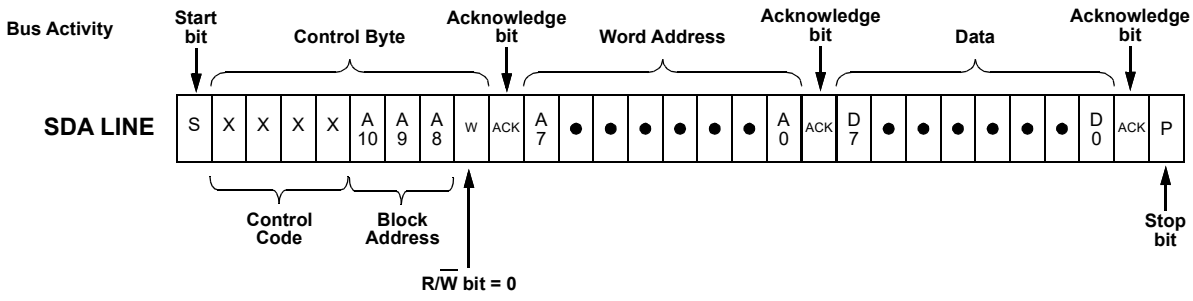

Figure 94: Byte Write Command, R/$\overline{W}$ = 0

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15.4.2 Sequential Write Command

The write Control Byte, Word Address, and the first data byte are transmitted to the SLG46826 in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Bus Controller continues to transmit data bytes to the SLG46826. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG46826 generates the Acknowledge bit.

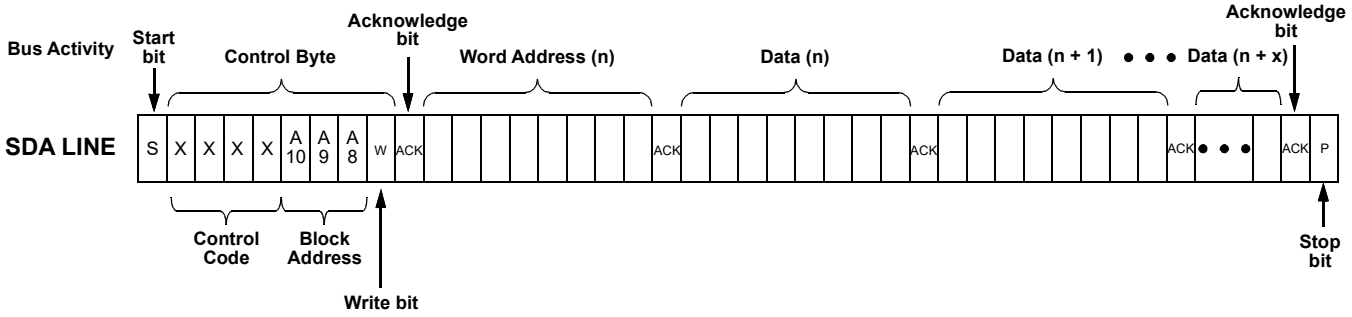

Figure 95: Sequential Write Command

15.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Sequential Read command (which contains a write control byte) reads data up to address n, the address pointer would get incremented to n + 1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n + 1. The Current Address Read Command contains the Control Byte sent by the Controller, with the R/$\overline{W}$ bit = “1”. The SLG46826 will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Controller will not issue an Acknowledge bit, and follow immediately with a Stop condition.

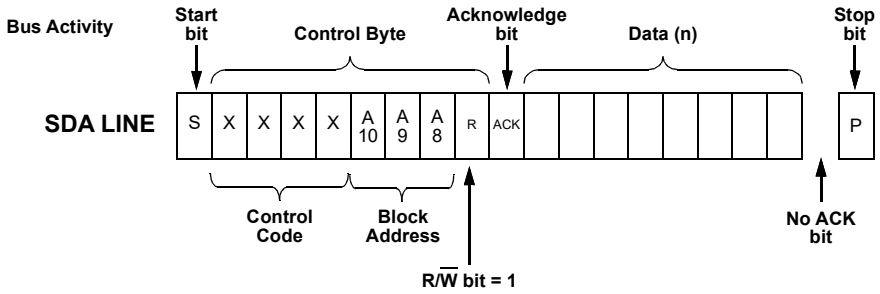

Figure 96: Current Address Read Command, R/$\overline{W}$ = 1

15.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Controller issues a second control byte with the R/W bit set to “1”, after which the SLG46826 issues an Acknowledge bit, followed by the requested eight data bits.

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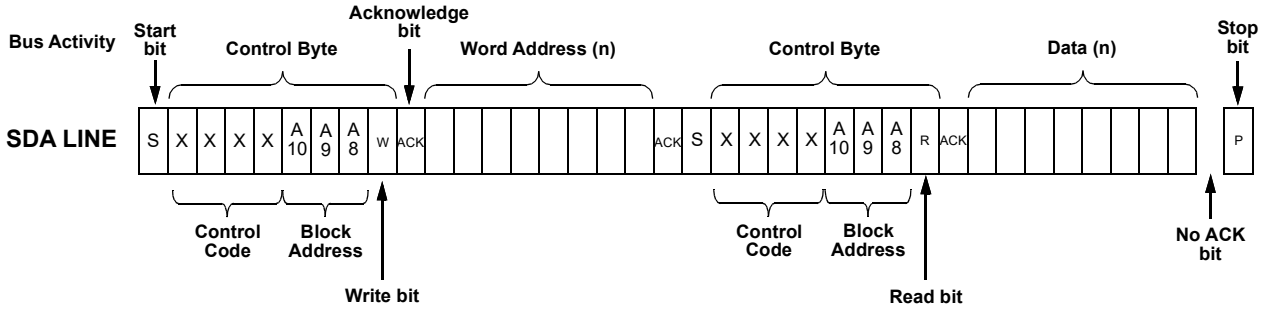

Figure 97: Random Read Command

15.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Random Read command, except that once the SLG46826 transmits the first data byte, the Bus Controller issues an Acknowledge bit as opposed to a Stop condition in a random read. The Bus Controller can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

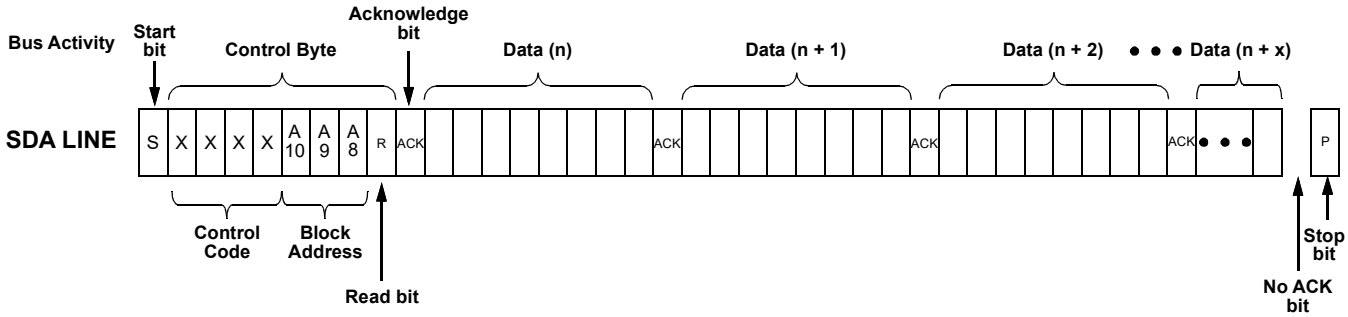

Figure 98: Sequential Read Command

15.4.6 I²C Serial Reset Command

If I²C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting register [1601] I²C reset bit to “1”, which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [1601] will be set to “0” automatically. Figure 99 illustrates the sequence of events for this reset function.

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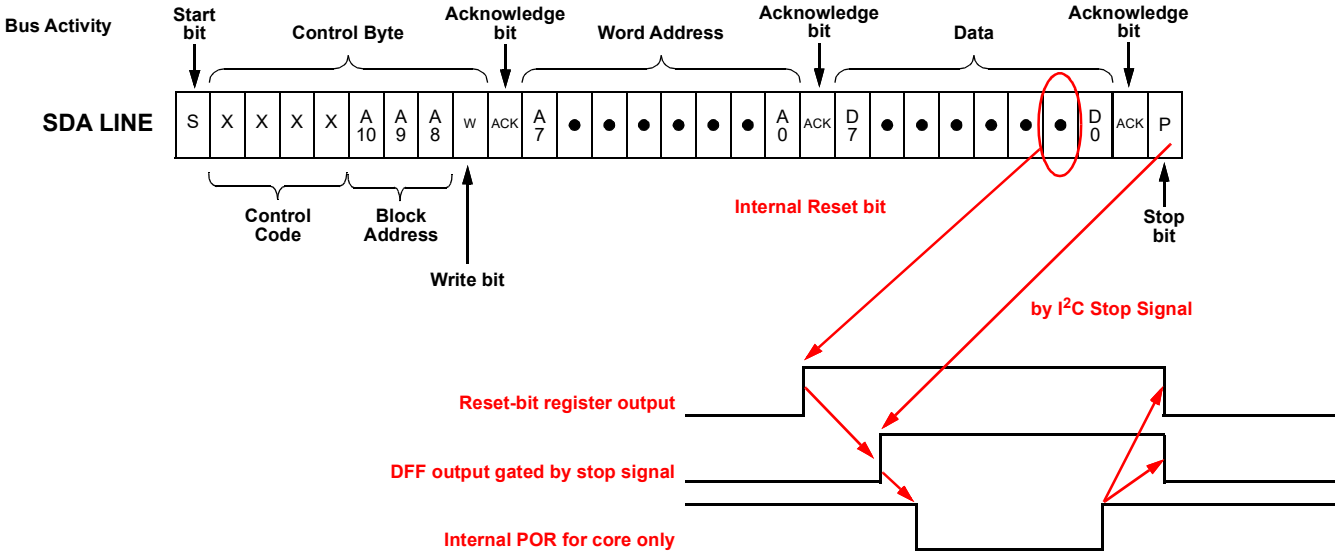

Figure 99: Reset Command Timing

15.5 CHIP CONFIGURATION DATA PROTECTION

The SLG46826 utilizes a scheme that allows a portion or the entire Register and NVM to be inhibited from being read or written/erased. There are two bytes that define the register and NVM access or change. The first byte RPR defines the 2k register read and write protection. The second byte NPR defines the 2k NVM data configuration read and write protection. If desired, the protection lock bit (PRL) can be set so that protection may no longer be modified, thereby making the current protection scheme permanent. The status of the RPR and NPR can be determined by following a Random Read sequence. Changing the state of the RPR and NPR is accomplished with a Byte Write sequence with the requirements outlined in this section.

The RPR register is located on H'E0 address, while NPR is located on H'E1 address.

The RPR format is shown in Table 50, and the RPR bit functions are included in Table 51.

Table 50: RPR Format

	b7	b6	b5	b4	b3	b2	b1	b0
RPR					RPRB3	RPRB2	RPRB1	RPRB0

Table 51: RPR Bit Function Description

Bit	Name		Type	Description
3:2	RPRB3	2k Register Write Selection Bits	R/W*	00: 2k register data is unprotected for write; 01: 2k register data is partly protected for write; Please refer to the Table 54. 10: 2k register data is fully protected for write.
	RPRB2		R/W*	
1:0	RPRB1	2k Register Read Selection Bits	R/W*	00: 2k register data is unprotected for read; 01: 2k register data is partly protected for read; Please refer to the Table 54. 10: 2k register data is fully protected for read.
	RPRB0		R/W*	

* Becomes read only after PRL is high. The content is permanently locked for write and erase after PRL is high.

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The NPR format is shown in Table 52, and the NPR bit functions are included in Table 53.

Table 52: NPR Format

	b7	b6	b5	b4	b3	b2	b1	b0
NPR							NPRB1	NPRB0

Table 53: NPR Bit Function Description

Bit	Name		Type	Description
1:0	NPRB1	2k NVM Configuration Selection Bits	R/W*	00: 2k NVM Configuration data is unprotected for read and write/erase; 01: 2k NVM Configuration data is fully protected for read; 10: 2k NVM Configuration data is fully protected for write/erase. 11: 2k NVM Configuration data is fully protected for read and write/erase.
	NPRB0		R/W*	

* Becomes read only after PRL is high. The content is permanently locked for write and erase after PRL is high.

The protection selection bits allow different levels of protection of the register and NVM Memory Array.

The Protect Lock Bit (PRL) is used to permanently lock (for write and erase) the current state of the RPR and NPR. A Logic 0 indicates that the protection byte can be modified, whereas a Logic 1 indicates the byte has been locked and can no longer be modified.

In this case it is impossible to erase the whole page E with protection bytes. The PRL is located at E4 address (register [1824]).

15.6 I²C SERIAL COMMAND REGISTER MAP

There are nine read/write protect modes for the design sequence from being corrupted or copied. See Table 54 for details.

Table 54: Read/Write Register Protection Options

Configurations	Protection Modes Configuration									Test Mode	Register Address
	Unlock	Partly Lock Read	Partly Lock Write	Partly Lock Read/ Write	Partly Lock Read & Lock Write	Lock Read & Partly Lock Write	Lock Read	Lock Write	Lock Read/ Write (Note 3)		
RPR[1:0]	**00**	**01**	**00**	**01**	**01**	**10**	**10**	**00**	**10**		
RPR[3:2]	**00**	**00**	**01**	**01**	**10**	**01**	**00**	**10**	**10**		
I²C Byte Write Bit Masking (section 15.7.3)	R/W	R/W	R/W	R/W	R	W	W	R	-	-	C9
I²C Serial Reset Command (section 15.4.6)	R/W	R/W	R/W	R/W	R	W	W	R	-	-	C8b'1
Outputs Latching During I²C Write	R/W	R/W	R/W	R/W	R	W	W	R	-	-	C8b'2
Connection Matrix Virtual Inputs (section 6.3)	R/W	R/W	R/W	R/W	R	W	W	R	-	-	7A
Configuration Bits for All Macrocells (IOs, ACMPs, Combination Function Macrocells, etc.)	R/W	W	R	-	-	-	W	R	-	-	

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Table 54: Read/Write Register Protection Options(Continued)

Configurations	Protection Modes Configuration									Test Mode	Register Address
	Unlock	Partly Lock Read	Partly Lock Write	Partly Lock Read/ Write	Partly Lock Read & Lock Write	Lock Read & Partly Lock Write	Lock Read	Lock Write	Lock Read/ Write (Note 3)		
RPR[1:0]	**00**	**01**	**00**	**01**	**01**	**10**	**10**	**00**	**10**		
RPR[3:2]	**00**	**00**	**01**	**01**	**10**	**01**	**00**	**10**	**10**		
Macrocells Inputs Configuration (Connection Matrix Outputs)	R/W	W	R	-	-	-	W	R	-	-	00~47
Protection Mode Selection	R/W	R/W	R	R	R	R	R/W	R	R	R	E4
Macrocells Output Values (Connection Matrix Inputs, section	R	R	R	R	R	-	-	R	-	R	74~79;7B
Counter Current Value	R	R	R	R	R	-	-	R	-	R	7C~7F
Silicon Identification Service Bits	R	R	R	R	R	R	R	R	R	R	F9b'3~F9 b'2
I²C Control Code	R/W	R/W	R	R	R	R	R/W	R	R	R	CAb'3~CA b'0
Page Erase byte	W**	W**	W**	W**	W**	W**	W**	W**	W**	W**	E3

R/W	Allow Read and Write Data
W	Allow Write Data Only
W**	Pages that can be erased are defined by NVM write protection
R	Allow Read Data Only
-	The Data is protected for Read and Write

Note 1 R/W becomes read only if protection mode selection (lock bit) is set to 1.

Note 2 R/W Readable/writable depend on the "Trim mode enable" bit. If “Trim mode enable” bit value = 1, then trim bits are enable.

Note 3 Valid for designs where IO1 is configured as input or not used.

It is possible to read some data from macrocells, such as counter current value, connection matrix, and connection matrix virtual inputs. The I²C write will not have any impact on data in case data comes from macrocell output, except Connection Matrix Virtual Inputs. The silicon identification service bits allows identifying silicon family, its revision, and others.

See Section 18 for detailed information on all registers.

15.7 I²C ADDITIONAL OPTIONS

When Output latching during I²C write to the register configuration data (block address A10A9A8 = 000), register [1602] = 0 allows all PINs output value to be latched while register content is changing. It will protect the output change due to configuration process during I²C write in case multiple register bytes are changed. Inputs and internal macrocells retain their status during I²C write.

See Section 18 for detailed information on all registers.

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15.7.1 Reading Counter Data via I²C

The current count value in three counters in the device can be read via I²C. The counters that have this additional functionality are 16-bit CNT0, and 8-bit counters CNT2 and CNT4.

15.7.2 I²C Expander

In addition to the eight Connection Matrix Virtual Inputs, the SLG46826 chip has four pins which can be used as an I²C Expander. These four pins are IO0, IO5, IO6, and IO9.

Each of these pins can be used as an I²C Expander output or used as a normal pin. Also each of these four expander outputs have initial state settings which are specified in registers [1599:1592].

15.7.3 I²C Byte Write Bit Masking

The I²C macrocell inside SLG46826 supports masking of individual bits within a byte that is written to the RAM memory space. This function is supported across the entire RAM memory space. To implement this function, the user performs a Byte Write Command (see Section 15.4.1 for details) on the I²C Byte Write Mask Register (address 0C9H) with the desired bit mask pattern. This sets a bit mask pattern for the target memory location that will take effect on the next Byte Write Command to this register byte. Any bit in the mask that is set to “1” in the I²C Byte Write Mask Register will mask the effect of changing that particular bit in the target register, during the next Byte Write Command. The contents of the I²C Byte Write Mask Register are reset (set to 00h) after valid Byte Write Command. If the next command received by the device is not a Byte Write Command, the effect of the bit masking function will be aborted, and the I²C Byte Write Mask Register will be reset with no effect. Figure 100 shows an example of this function.

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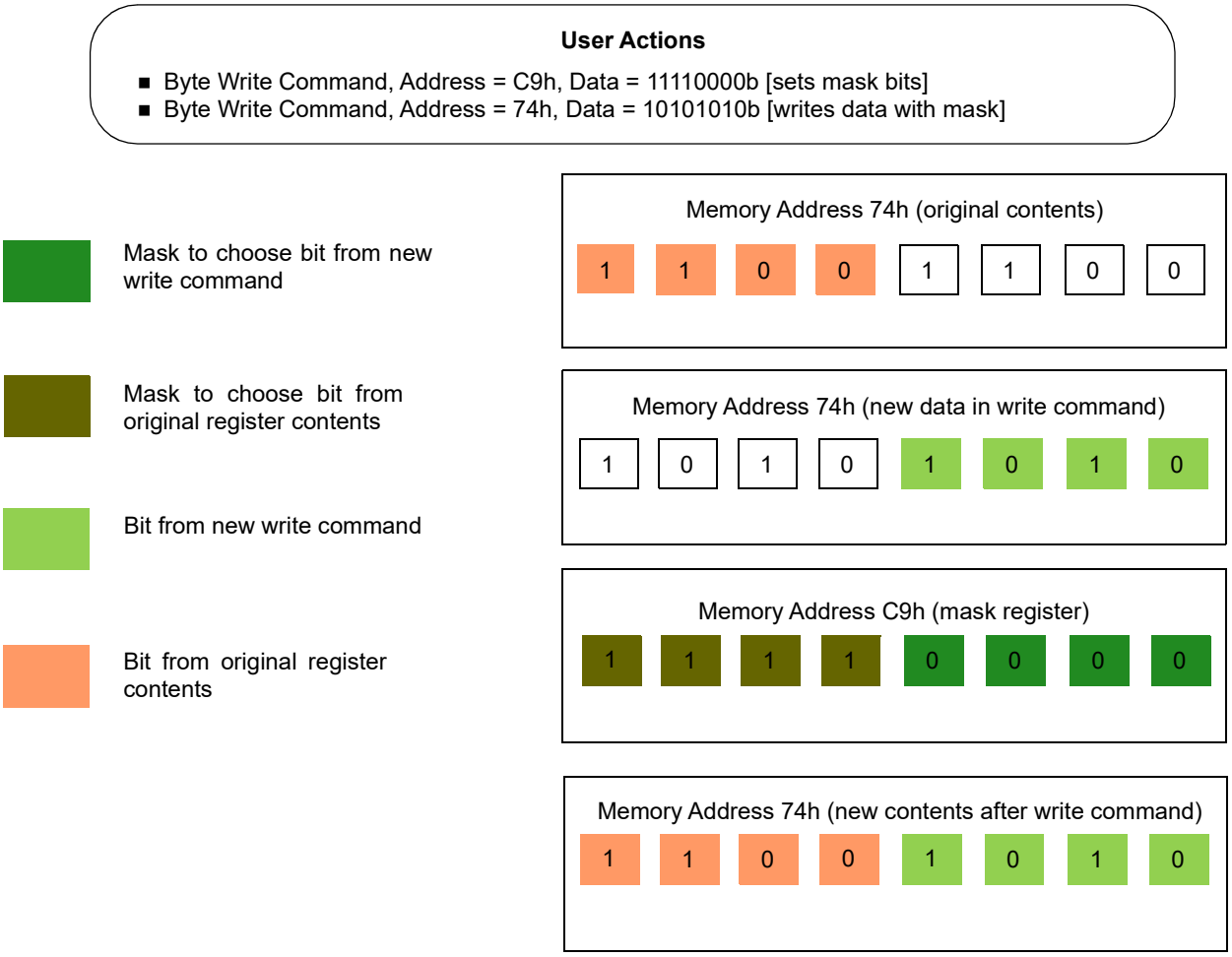

Figure 100: Example of I²C Byte Write Bit Masking

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16 Non-Volatile Memory

The SLG46826 provides 2,048 bits of Serial Electrically Erasable Configuration Register memory that is used for device configuration, and 2,048 bits Programmable Read-Only Memory (emulated EEPROM). Each of these memory spaces is internally organized as 16 pages of 16 bytes. The device features a Software Write Protection feature with five different programmable levels of protection for the emulated EEPROM array. The protection settings of the device can be made permanent if desired. The emulated EEPROM memory operates with a supply voltage ranging from 2.3 V to 5.5 V for Read and 2.5 V to 5.5 V for Write.

The emulated EEPROM inside the SLG46826 operates as a target device and utilizes a simple I^2C compatible 2-wire digital serial interface to communicate with a host controller commonly referred to as the bus Controller. The Controller initiates and controls all read and write operations to the target devices on the serial bus, and both the Controller and the target devices can transmit and receive data on the bus.

Key features:

- Low-voltage Operation
  - for Read: VCC = 2.3 V to 5.5 V
  - for Write: VCC = 2.5 V to 5.5 V
- I^2C-Compatible (2-Wire) Serial Interface
  - 100 kHz Standard Mode
  - 400 kHz Fast Mode (FM)
- Software Write Protection of the EEPROM Emulation Array
  - Five configuration options
  - Protection settings can be made permanent
- Low Current Consumption
  - Read Current 0.5 mA max
  - Page Write Current 3.0 mA max
  - Chip Erase Current 3.0 mA max
  - Standby Current (1.0 µA max)
- 16-byte Page Write Mode
- Self-timed Write/Erase Cycle (20 ms max)
- Reliability
  - Endurance: 1,000 write cycles
  - Data retention: 10 years at 125 °C

16.1 SERIAL NVM WRITE OPERATIONS

Write access to the NVM is possible by setting A3 A2 A1 A0 to “0000”, which allows serial write data for a single page only. Upon receipt of the proper Control Byte and Word Address bytes, the SLG46826 will send an ACK. The device will then be ready to receive page data, which is 16 sequential writes of 8-bit data words. The SLG46826 will respond with an ACK after each data word is received. The addressing device, such as a bus Controller, must then terminate the write operation with a Stop condition after all page data is written. At that time the device will enter an internally self-timed write cycle, which will be completed within t_{WR}. While the data is being written into the NVM Memory Array, all inputs, outputs, internal logic, and I^2C access to the Register data will be operational/valid. Please refer to Figure 102 for the SLG46826 Memory Map.

Note: The 16 programmed bytes should be in the same page. Any I^2C command that does not meet specific requirements will be ignored and NVM will remain unprogrammed.

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Data “1” cannot be re-programmed as data “0” without erasure. Each byte can only be programmed one time without erasure.

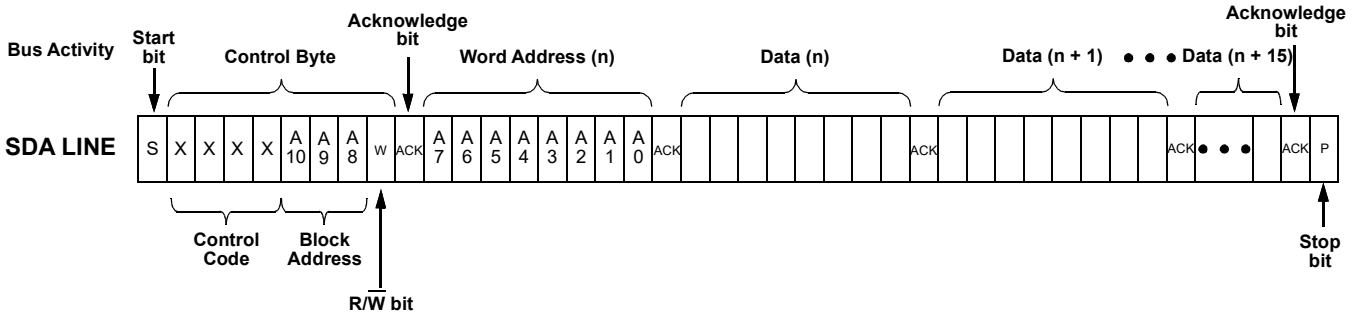

Figure 101: Page Write Command

A10 will be ignored during communication to SLG46826.

A9 = 1 will enable access to the NVM.

A9 = 1 and A8 = 0 corresponds to the 2K bits chip configuration NVM data.

A9 = 1 and A8 = 1 corresponds to the 2K bits of emulated EEPROM data.

A3, A2, A1, and A0 should be 0000 for the page write operation.

In a single page, if the data written to any byte is 00H, the contents of the matching byte in NVM memory will not be altered.

	I^2C Block Address			Memory Space
Lowest I^2C Address = 000h	A10 = 0	A9 = 0	A8 = X	**2 Kbits Register Data Configuration**
	A10 = 0	A9 = 1	A8 = 0	**2 Kbits NVM Data Configuration**
	A10 = 0	A9 = 1	A8 = 1	**2 Kbits EEPROM**
Highest I^2C Address = 7FFh	A10 = 1	A9 = X	A8 = X	**Not Used**

Figure 102: I^2C Block Addressing

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16.2 SERIAL NVM READ OPERATIONS

There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read

Please refer to the Section 15 for more details.

16.3 SERIAL NVM ERASE OPERATIONS

The erase scheme allows a 16 byte page in the emulated EEPROM space or in the NVM chip configuration space to be erased by modifying the contents of the Erase Register (ERSR). When the ERSE bit is set in the ERSR register, the device will start a self-timed erase cycle which will complete in a maximum of t_{ER} ms.

The V_{DD} pin requires a voltage ranging from 2.5 V to 5.5 V for Programming and Erase operations.

Changing the state of the ERSR is accomplished with a Byte Write sequence with the requirements outlined in this section.

The ERSR register is located on I^2C Block Address = 000b, I^2C Word Address = E3H.

The ERSR format is shown in Table 55, and the ERSR bit functions are included in Table 56.

Table 55: Erase Register Bit format

	b7	b6	b5	b4	b3	b2	b1	b0
Page Erase Register	ERSE	--	--	ERSEB4	ERSEB3	ERSEB2	ERSEB1	ERSEB0

Table 56: Erase Register Bit Function Description

Bit	Name		Type	Description
7	ERSE	Erase Enable	W	Setting b7 bit to "1" will start an internal erase cycle on the page defined by ERSEB4-0
6	--	--	--	--
5	--	--	--	--
4	ERSEB4	Page Selection for Erase	W	Define the page address, which will be erased. ERSB4 = 0 corresponds to the Upper 2K NVM used for chip configuration; ERSB4 = 1 corresponds to the 2-k emulated EEPROM.
3	ERSEB3		W	
2	ERSEB2		W	
1	ERSEB1		W	
0	ERSEB0		W	

Upon receipt of the proper Device Address and Erase Register Address, the SLG46826 will send an ACK. The device will then be ready to receive Erase Register data. The SLG46826 will respond with an ACK after Erase Register data word is received. The addressing device, such as a bus Controller, must then terminate the write operation with a Stop condition. At that time the device will enter an internally self-timed erase cycle, which will be completed within t_{ER} ms. While the data is being written into the Memory Array, all inputs, outputs, internal logic, and I^2C access to the Register data will be operational/valid.

After the erase has taken place, the contents of ERSE bits will be set to “0” automatically. The internal erase cycle will be triggered at the time the Stop Bit in the I^2C command is received.

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16.4 ACKNOWLEDGE POLLING

An Acknowledge Polling routine can be implemented to optimize time sensitive applications that would prefer not to wait the fixed maximum write cycle time (t_{WR}) or erase maximum cycle time (t_{ER}). This method allows the application to know immediately when the Serial EEPROM emulation write/erase cycle has completed, so a subsequent operation can be started. Once the internally self-timed write/erase cycle has started, an Acknowledge Polling routine can be initiated. This involves repeatedly sending a Start condition followed by a valid Device Address byte (NVM block address) with the R/W bit set at Logic 0. The device will not respond with an ACK while the write cycle is ongoing. Once the internal write/erase cycle has completed, emulated EEPROM will respond with an ACK, allowing a new read, erase, or write operation to be immediately initiated.

The length of the self-timed write cycle (t_{WR}) and self-timed erase cycle (t_{ER}) is defined as the amount of time from the Stop condition that begins the internal write operation to the Start condition of the first Device Address byte that includes NVM address (A9 = 1; A8 = X) sent to the SLG46826 that it subsequently responds to with an ACK.

16.5 LOW POWER STANDBY MODE

Emulated EEPROM inside the SLG46826 has a low power standby mode which is enabled when any one of the following occurs:

- A valid power-up sequence is performed
- A Stop condition is received by the devices unless it initiates an internal write/erase cycle
- At the completion of an internal write/erase cycle
- An unsuccessful match of the device type identifier or hardware address in the Device Address byte occurs

16.6 EMULATED EEPROM WRITE PROTECTION

The SLG46826 utilizes a software scheme that allows a portion or the entire emulated EEPROM to be inhibited from being written or erased by modifying the contents of the Write Protection Register (WPR). If desired, the WPR can be set so that it may no longer be modified/erased, thereby making the current protection scheme permanent. The status of the WPR can be determined by following a Random Read sequence. Changing the state of the WPR is accomplished with a Byte Write sequence with the requirements outlined in this section.

The WPR register is located on I^2C Block Address = 010b, I^2C Word Address = E2H.

The WPR format is shown in Table 57, and the WPR bit functions are included in Table 58.

Table 57: Write/Erase Protect Register Format

	b7	b6	b5	b4	b3	b2	b1	b0
WPR						WPRE	WPB1	WPB0

Table 58: Write/Erase Protect Register Bit Function Description

Bit	Name		Type	Description
2	WPRE	Write Protect Register Enable	R/W	0: No Software Write Protection enabled (default) 1: Write Protection is set by the state of WPB [1:0] bits
1:0	WPB1	Write Protect Block Bits	R/W	00: Upper quarter of emulated EEPROM is write protected (default) 01: Upper half of emulated EEPROM is write protected 10: Upper 3/4 of emulated EEPROM is write protected. 11: Entire emulated EEPROM is write protected.
	WPB0		R/W	

Write Protect Enable (WPRE): The Write Protect Enable Bit is used to enable or disable the device Software Write/Erase Protect. A Logic 0 in this position will disable Software Write/Erase Protection, and a Logic 1 will enable this function.

Write Protect Block Bits (WPB1:WPB0): The Write Protect Block bits allow four levels of protection of the Memory Array, provided that the WPRE bit is a Logic 1. If the WPRE bit is a Logic 0, the state of the WPB1:0 bits have no impact on device protection.

Protect Lock Bit (PRL): The Protect Lock Bit is used to permanently lock the current state of the WPR, as well as RPR and NPR (see Section 15.5). A Logic 0 indicates that the WPR, RPR, and NPR can be modified, whereas a Logic 1 indicates the WPR, RPR, and NPR has been locked and can no longer be modified. The PRL register bit is located at register [1824] address.

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17 Analog Temperature Sensor

The SLG46826 has an Analog Temperature sensor (TS) with an output voltage linearly-proportional to the Centigrade temperature. The TS cell shares buffer with Vref0, so it is impossible to use both cells simultaneously, its output can be connected directly to the IO10 or to the ACPM3_L positive input. Using buffer causes low-output impedance, linear output and makes interfacing to readout or control circuitry especially easy. The TS is rated to operate over a -40 °C to 85 °C temperature range. The error in the whole temperature range does not exceed ±0.85 %. TS output voltage variation over V_{DD} at constant temperature is less than ±0.08 %. For more detail refer to Section 3.

The equation below calculates the typical analog voltage passed from the TS to the ACMPs' IN+ source input. It is important to note that there will be a chip to chip variation of about ±2 °C.

$$V_{TS1} = -2.3 \times T + 905.3$$

$$V_{TS2} = -2.8 \times T + 1077.3$$

where:

V_{TS1} (mV) - TS Output Voltage, range 1

V_{TS2} (mV) - TS Output Voltage, range 2

T (°C) - Temperature

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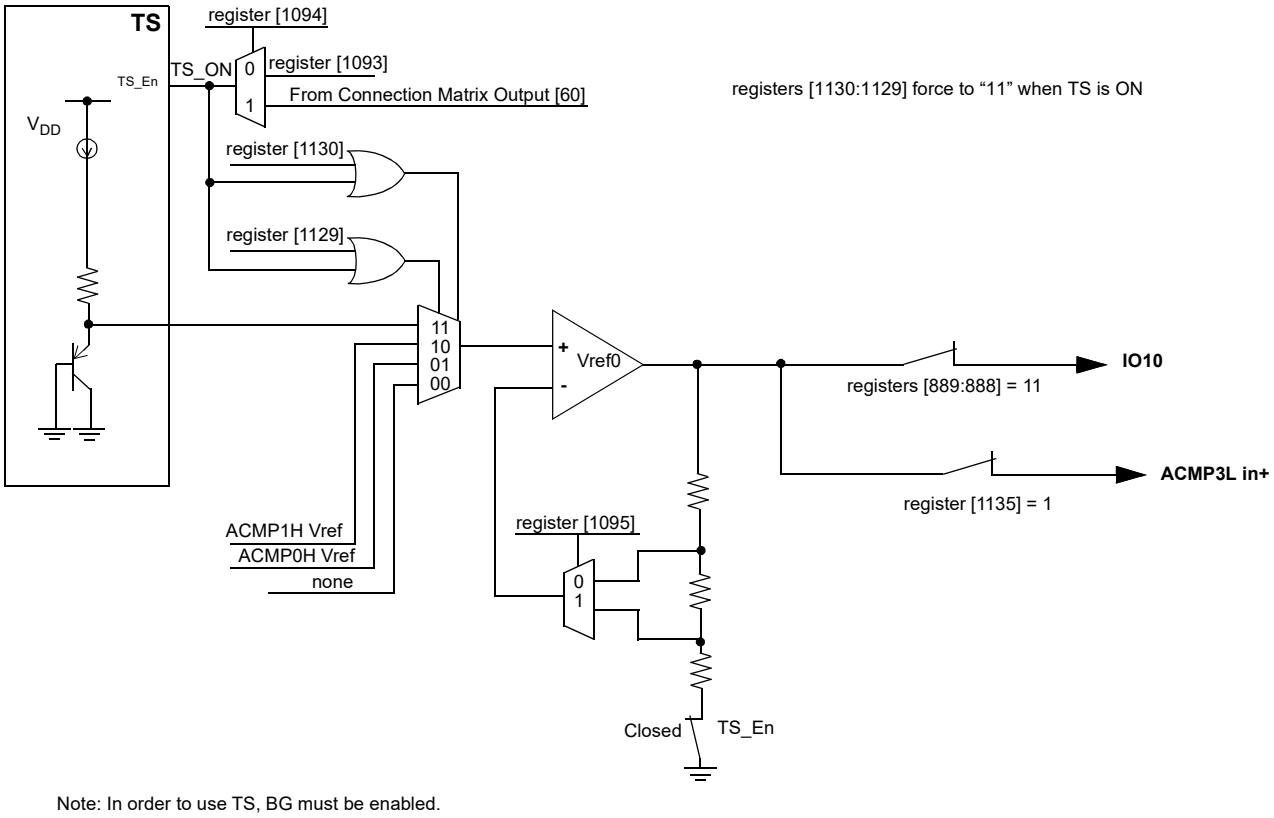

Note: In order to use TS, BG must be enabled.

Figure 103: Analog Temperature Sensor Structure Diagram

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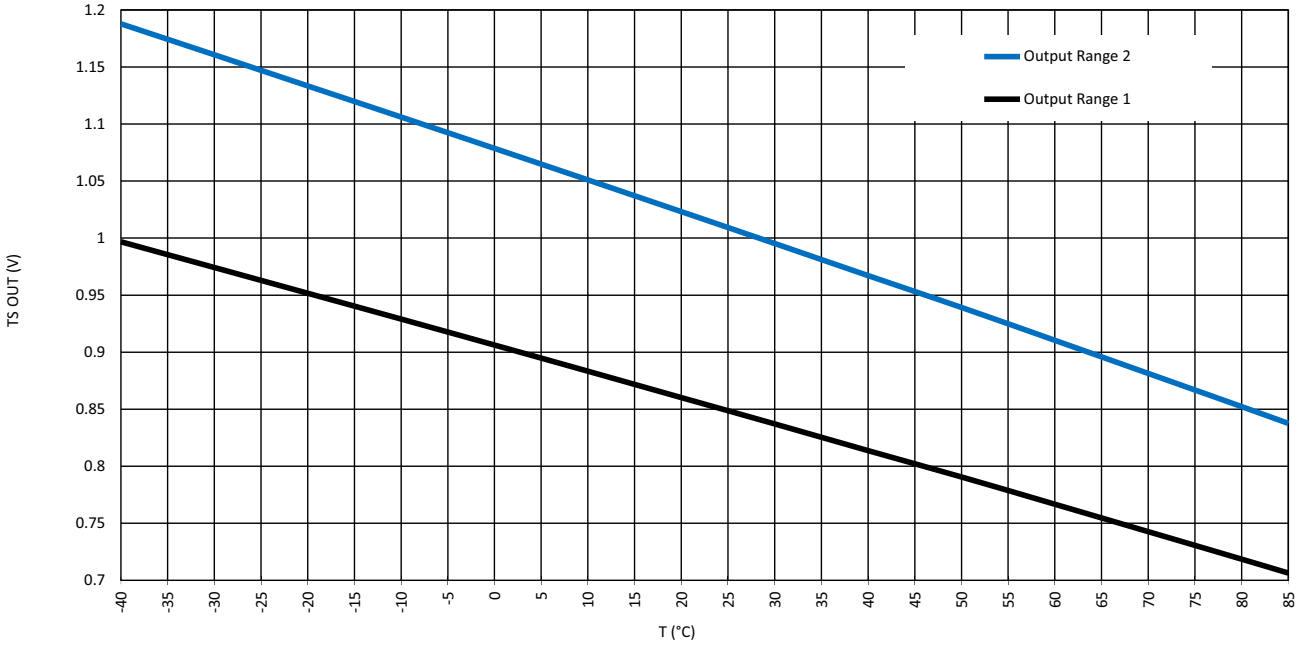

Figure 104: TS Output vs Temperature, V_{DD} = 2.3 V to 5.5 V

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18 Register Definitions

18.1 REGISTER MAP

Table 59: Register Map

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
Matrix Output			
00	5:0	Matrix OUT0	IN0 of 2-bit LUT0 or Clock Input of DFF0
00 01	11:6	Matrix OUT1	IN1 of 2-bit LUT0 or Data Input of DFF0
01 02	17:12	Matrix OUT2	IN0 of 2-bit LUT3 or Clock Input of PGen
02	23:18	Matrix OUT3	IN1 of 2-bit LUT3 or nRST of PGen
03	29:24	Matrix OUT4	IN0 of 2-bit LUT1 or Clock Input of DFF1
03 04	35:30	Matrix OUT5	IN1 of 2-bit LUT1 or Data Input of DFF1
04 05	41:36	Matrix OUT6	IN0 of 2-bit LUT2 or Clock Input of DFF2
05	47:42	Matrix OUT7	IN1 of 2-bit LUT2 or Data Input of DFF2
06	53:48	Matrix OUT8	IN0 of 3-bit LUT0 or Clock Input of DFF3
06 07	59:54	Matrix OUT9	IN1 of 3-bit LUT0 or Data Input of DFF3
07 08	65:60	Matrix OUT10	IN2 of 3-bit LUT0 or nRST(nSET) of DFF3
08	71:66	Matrix OUT11	IN0 of 3-bit LUT1 or Clock Input of DFF4
09	77:72	Matrix OUT12	IN1 of 3-bit LUT1 or Data Input of DFF4
09 0A	83:78	Matrix OUT13	IN2 of 3-bit LUT1 or nRST(nSET) of DFF4
0A 0B	89:84	Matrix OUT14	IN0 of 3-bit LUT2 or Clock Input of DFF5
0B	95:90	Matrix OUT15	IN1 of 3-bit LUT2 or Data Input of DFF5
0C	101:96	Matrix OUT16	IN2 of 3-bit LUT2 or nRST(nSET) of DFF5
0C 0D	107:102	Matrix OUT17	IN0 of 3-bit LUT3 or Clock Input of DFF6
0D 0E	113:108	Matrix OUT18	IN1 of 3-bit LUT3 or Data Input of DFF6
0E	119:114	Matrix OUT19	IN2 of 3-bit LUT3 or nRST(nSET) of DFF6
0F	125:120	Matrix OUT20	IN0 of 3-bit LUT4 or Clock Input of DFF7
0F 10	131:126	Matrix OUT21	IN1 of 3-bit LUT4 or Data Input of DFF7
10 11	137:132	Matrix OUT22	IN2 of 3-bit LUT4 or nRST(nSET) of DFF7
11	143:138	Matrix OUT23	IN0 of 3-bit LUT5 or Clock Input of DFF8
12	149:144	Matrix OUT24	IN1 of 3-bit LUT5 or Data Input of DFF8

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
12	155:150	Matrix OUT25	IN2 of 3-bit LUT5 or nRST(nSET) of DFF8
13			
13	161:156	Matrix OUT26	IN0 of 3-bit LUT6 or Input of Pipe Delay or UP Signal of RIPP CNT
14			
14	167:162	Matrix OUT27	IN1 of 3-bit LUT6 or nRST of Pipe Delay or STB of RIPP CNT
15	173:168	Matrix OUT28	IN2 of 3-bit LUT6 or Clock of Pipe Delay_RIPP_CNT
15	179:174	Matrix OUT29	Reserved
16			
16	185:180	Matrix OUT30	MULTFUNC_16BIT_0: IN0 of 4-bit LUT0 or Clock Input of DFF9; Delay0 Input (or Counter0 nRST/SET Input)
17			
17	191:186	Matrix OUT31	MULTFUNC_16BIT_0: IN1 of 4-bit LUT0 or nRST of DFF9; Delay0 Input (or Counter0 nRST Input) or Delay/Counter0 External Clock Source
18	197:192	Matrix OUT32	MULTFUNC_16BIT_0: IN2 of 4-bit LUT0 or nSET of DFF9; Delay0 Input (or Counter0 nRST Input) or Delay/Counter0 External Clock Source or KEEP Input of FSM0
18	203:198	Matrix OUT33	MULTFUNC_16BIT_0: IN3 of 4-bit LUT0 or Data Input of DFF9; Delay0 Input (or Counter0 nRST Input) or UP Input of FSM0
19			
19	209:204	Matrix OUT34	MULTFUNC_8BIT_1: IN0 of 3-bit LUT7 or Clock Input of DFF10; Delay1 Input (or Counter1 nRST Input)
1A			
1A	215:210	Matrix OUT35	MULTFUNC_8BIT_1: IN1 of 3-bit LUT7 or nRST (nSET) of DFF10; Delay1 Input (or Counter1 nRST Input) or Delay/Counter1 External Clock Source
1B	221:216	Matrix OUT36	MULTFUNC_8BIT_1: IN2 of 3-bit LUT7 or Data Input of DFF10; Delay1 Input (or Counter1 nRST Input)
1B	227:222	Matrix OUT37	MULTFUNC_8BIT_2: IN0 of 3-bit LUT8 or Clock Input of DFF11; Delay2 Input (or Counter2 nRST Input)
1C			
1C	233:228	Matrix OUT38	MULTFUNC_8BIT_2: IN1 of 3-bit LUT8 or nRST (nSET) of DFF11; Delay2 Input (or Counter2 nRST Input) or Delay/Counter2 External Clock Source
1D			
1D	239:234	Matrix OUT39	MULTFUNC_8BIT_2: IN2 of 3-bit LUT8 or Data Input of DFF11; Delay2 Input (or Counter2 nRST Input)
1E	245:240	Matrix OUT40	MULTFUNC_8BIT_3: IN0 of 3-bit LUT9 or Clock Input of DFF12; Delay3 Input (or Counter3 nRST Input)
1E	251:246	Matrix OUT41	MULTFUNC_8BIT_3: IN1 of 3-bit LUT9 or nRST (nSET) of DFF12; Delay3 Input (or Counter3 nRST Input) or Delay/Counter3 External Clock Source
1F			

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1F	257:252	Matrix OUT42	MULTFUNC_8BIT_3: IN2 of 3-bit LUT9 or Data Input of DFF12; Delay3 Input (or Counter3 nRST Input)
20			
20	263:258	Matrix OUT43	MULTFUNC_8BIT_4: IN0 of 3-bit LUT10 or Clock Input of DFF13; Delay4 Input (or Counter4 nRST Input)
21	269:264	Matrix OUT44	MULTFUNC_8BIT_4: IN1 of 3-bit LUT10 or nRST (nSET) of DFF13; Delay4 Input (or Counter4 nRST Input) or Delay/Counter4 External Clock Source
21	275:270	Matrix OUT45	MULTFUNC_8BIT_4: IN2 of 3-bit LUT10 or Data Input of DFF13; Delay4 Input (or Counter4 nRST Input)
22			
22	281:276	Matrix OUT46	MULTFUNC_8BIT_5: IN0 of 3-bit LUT11 or Clock Input of DFF14; Delay5 Input (or Counter5 nRST Input)
23			
23	287:282	Matrix OUT47	MULTFUNC_8BIT_5: IN1 of 3-bit LUT11 or nRST (nSET) of DFF14; Delay5 Input (or Counter5 nRST Input) or Delay/Counter5 External Clock Source
24	293:288	Matrix OUT48	MULTFUNC_8BIT_5: IN2 of 3-bit LUT11 or Data Input of DFF14; Delay5 Input (or Counter5 nRST Input)
24	299:294	Matrix OUT49	MULTFUNC_8BIT_6: IN0 of 3-bit LUT12 or Clock Input of DFF15; Delay6 Input (or Counter6 nRST Input)
25			
25	305:300	Matrix OUT50	MULTFUNC_8BIT_6: IN1 of 3-bit LUT12 or nRST (nSET) of DFF15; Delay6 Input (or Counter6 nRST Input) or Delay/Counter6 External Clock Source
26			
26	311:306	Matrix OUT51	MULTFUNC_8BIT_6: IN2 of 3-bit LUT12 or Data Input of DFF15; Delay6 Input (or Counter6 nRST Input)
27	317:312	Matrix OUT52	MULTFUNC_8BIT_7: IN0 of 3-bit LUT13 or Clock Input of DFF16; Delay7 Input (or Counter7 nRST Input)
27	323:318	Matrix OUT53	MULTFUNC_8BIT_7: IN1 of 3-bit LUT13 or nRST (nSET) of DFF16; Delay7 Input (or Counter7 nRST Input) or Delay/Counter7 External Clock Source
28			
28	329:324	Matrix OUT54	MULTFUNC_8BIT_7: IN2 of 3-bit LUT13 or Data Input of DFF16; Delay7 Input (or Counter7 nRST Input)
29			
29	335:330	Matrix OUT55	Filter/Edge detect input
2A	341:336	Matrix OUT56	Programmable delay/edge detect input
2A	347:342	Matrix OUT57	OSC2 ENABLE from matrix
2B			
2B	353:348	Matrix OUT58	OSC0 ENABLE from matrix
2C			
2C	359:354	Matrix OUT59	OSC1 ENABLE from matrix

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
2D	365:360	Matrix OUT60	Vref PD from matrix
2D 2E	371:366	Matrix OUT61	BG power-down from matrix
2E 2F	377:372	Matrix OUT62	PWR UP of ACMP0H from matrix
2F	383:378	Matrix OUT63	PWR UP of ACMP1H from matrix
30	389:384	Matrix OUT64	PWR UP of ACMP2L from matrix
30 31	395:390	Matrix OUT65	PWR UP of ACMP3L from matrix
31 32	401:396	Matrix OUT66	Reserved
32	407:402	Matrix OUT67	IO0 Digital Output
33	413:408	Matrix OUT68	IO1 Digital Output
33 34	419:414	Matrix OUT69	IO1 Digital Output OE
34 35	425:420	Matrix OUT70	IO2 Digital Output
35	431:426	Matrix OUT71	IO3 Digital Output
36	437:432	Matrix OUT72	IO4 Digital Output
36 37	443:438	Matrix OUT73	IO4 Digital Output OE
37 38	449:444	Matrix OUT74	IO5 Digital Output
38	455:450	Matrix OUT75	IO5 Digital Output OE
39	461:456	Matrix OUT76	IO6 Digital Output
39 3A	467:462	Matrix OUT77	IO7 Digital Output
3A 3B	473:468	Matrix OUT78	IO8 Digital Output
3B	479:474	Matrix OUT79	IO8 Digital Output OE
3C	485:480	Matrix OUT80	IO9 Digital Output
3C 3D	491:486	Matrix OUT81	IO9 Digital Output OE
3D 3E	497:492	Matrix OUT82	IO10 Digital Output
3E	503:498	Matrix OUT83	IO10 Digital Output OE
3F	509:504	Matrix OUT84	IO11 Digital Output
3F 40	515:510	Matrix OUT85	IO11 Digital Output OE
40 41	521:516	Matrix OUT86	IO12 Digital Output
41	527:522	Matrix OUT87	IO12 Digital Output OE

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
42	533:528	Matrix OUT88	IO13 Digital Output
42	539:534	Matrix OUT89	IO13 Digital Output OE
43			
43	545:540	Matrix OUT90	IO14 Digital Output
44			
44	551:546	Matrix OUT91	IO14 Digital Output OE
45	557:552	Matrix OUT92	Reserved
45	563:558	Matrix OUT93	Reserved
46			
46	569:564	Matrix OUT94	Reserved
47			
47	575:570	Matrix OUT95	Reserved
48	583:576	Reserved	
49	591:584		
4A	599:592	Reserved	
4B	607:600		
4C	615:608	Reserved	
4D	623:616		
4E	631:624	Reserved	
4F	639:632		
50	647:640	Reserved	
51	655:648		
52	663:656	Reserved	
53	671:664		
54	679:672	Reserved	
55	687:680		
56	695:688	Reserved	
57	703:696		
58	711:704		
59	719:712	Reserved	
5A	727:720		
5B	735:728	Reserved	
5C	743:736		
5D	751:744	Reserved	
5E	759:752		
5F	767:760	Reserved	
IO Common			
60	768	IO fast Pull-up/down enable	0: disable 1: enable
	769	I^2C mode selection	0: I^2C standard/fast mode 1: I^2C fast mode+
	775:770	Reserved	

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
IO0			
61	777:776	IO0 input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: reserved
	779:778	IO0 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	781:780	IO0 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	782	IO0 Pull-up/down selection	0: Pull-down 1: Pull-up
	783	IO0 output enable	0: disable 1: enable
IO1			
62	785:784	IO1 input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: analog input
	787:786	IO1 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	789:788	IO1 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	790	IO1 Pull-up/down selection	0: Pull-down 1: Pull-up
	791	Reserved	
Reserved			
63	793:792	Reserved	
	795:794	Reserved	
	797:796	Reserved	
	798	Reserved	
	799	Reserved	
IO2			

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
64	801:800	IO2 input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: reserved
	803:802	IO2 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	805:804	IO2 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	806	IO2 Pull-up/down selection	0: Pull-down 1: Pull-up
	807	IO2 output enable	0: disable 1: enable
IO3			
65	809:808	IO3 input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: reserved
	811:810	IO3 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	813:812	IO3 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	814	IO3 Pull-up/down selection	0: Pull-down 1: Pull-up
	815	IO3 output enable	0: disable 1: enable
IO4			
66	817:816	IO4 input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: reserved
	819:818	IO4 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	821:820	IO4 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	822	IO4 Pull-up/down selection	0: Pull-down 1: Pull-up
	823	Reserved	
IO5			

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
67	825:824	IO5 input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: reserved
	827:826	IO5 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	829:828	IO5 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	830	IO5 Pull-up/down selection	0: Pull-down 1: Pull-up
	831	Reserved	
SCL			
68	832	Reserved	
	834:833	SCL input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: Reserved
	836:835	SCL Pull-up/down resistance selection	00: floating 01: Reserved 10: Reserved 11: Reserved
	837	Reserved	
	839:838	Reserved	
SDA			
69	840	Reserved	
	842:841	SDA input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: Reserved
	844:843	SDA Pull-up/down resistance selection	00: floating 01: Reserved 10: Reserved 11: Reserved
	845	Reserved	
	847:846	Reserved	
IO6			

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
6A	849:848	Reserved	
	851:850	IO6 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	853:852	IO6 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	854	IO6 Pull-up/down selection	0: Pull-down 1: Pull-up
	855	IO6 output enable	0: disable 1: enable
IO7			
6B	857:856	Reserved	
	859:858	IO7 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	861:860	IO7 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	862	IO7 Pull-up/down selection	0: Pull-down 1: Pull-up
	863	IO7 output enable	0: disable 1: enable
IO8			
6C	865:864	IO8 input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: reserved
	867:866	IO8 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	869:868	IO8 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	870	IO8 Pull-up/down selection	0: Pull-down 1: Pull-up
	871	Reserved	
Reserved			
6D	873:872	Reserved	
	875:874	Reserved	
	877:876	Reserved	
	878	Reserved	
	879	Reserved	

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
IO9			
6E	881:880	IO9 input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: analog output
	883:882	IO9 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	885:884	IO9 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	886	IO9 Pull-up/down selection	0: Pull-down 1: Pull-up
	887	Reserved	
IO10			
6F	889:888	IO10 input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: analog output
	891:890	IO10 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	893:892	IO10 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	894	IO10 Pull-up/down selection	0: Pull-down 1: Pull-up
	895	Reserved	
IO11			
70	897:896	IO11 input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: analog input
	899:898	IO11 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	901:900	IO11 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	902	IO11 Pull-up/down selection	0: Pull-down 1: Pull-up
	903	Reserved	
IO12			

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
71	905:904	IO12 input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: analog input
	907:906	IO12 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	909:908	IO12 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	910	IO12 Pull-up/down selection	0: Pull-down 1: Pull-up
	911	Reserved	
IO13			
72	913:912	IO13 input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: analog IO
	915:914	IO13 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	917:916	IO13 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	918	IO13 Pull-up/down selection	0: Pull-down 1: Pull-up
	919	Reserved	
IO14			
73	921:920	IO14 input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger 10: low voltage digital in mode 11: analog input
	923:922	IO14 output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	925:924	IO14 Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	926	IO14 Pull-up/down selection	0: Pull-down 1: Pull-up
	927	Reserved	
Matrix Input			

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
74	928	Matrix Input 0	Tie low
	929	Matrix Input 1	IO0 Digital Input
	930	Matrix Input 2	IO1 Digital Input
	931	Matrix Input 3	IO2 Digital Input
	932	Matrix Input 4	IO3 Digital Input
	933	Matrix Input 5	IO4 Digital Input
	934	Matrix Input 6	IO5 Digital Input
	935	Matrix Input 7	IO8 Digital Input
75	936	Matrix Input 8	IO9 Digital Input
	937	Matrix Input 9	IO10 Digital Input
	938	Matrix Input 10	IO11 Digital Input
	939	Matrix Input 11	IO12 Digital Input
	940	Matrix Input 12	IO13 Digital Input
	941	Matrix Input 13	IO14 Digital Input
	942	Matrix Input 14	2-bit LUT0_DFF0_OUT
	943	Matrix Input 15	2-bit LUT1_DFF1_OUT
76	944	Matrix Input 16	2-bit LUT2_DFF2_OUT
	945	Matrix Input 17	2-bit LUT3_PGEN_OUT
	946	Matrix Input 18	3-bit LUT0_DFF3_OUT
	947	Matrix Input 19	3-bit LUT1_DFF4_OUT
	948	Matrix Input 20	3-bit LUT2_DFF5_OUT
	949	Matrix Input 21	3-bit LUT3_DFF6_OUT
	950	Matrix Input 22	3-bit LUT4_DFF7_OUT
	951	Matrix Input 23	3-bit LUT5_DFF8_OUT
77	952	Matrix Input 24	3-bit LUT6_PIPEDLY_RIPP_CNT_OUT0
	953	Matrix Input 25	PIPEDLY_RIPP_CNT_OUT1
	954	Matrix Input 26	RIPP_CNT_OUT2
	955	Matrix Input 27	EDET_FILTER_OUT
	956	Matrix Input 28	PROG_DLY_EDET_OUT
	957	Matrix Input 29	MULTFUNC_8BIT_1: DLY_CNT_OUT
	958	Matrix Input 30	CKOSC1_MATRIX: OSC1 matrix input
	959	Matrix Input 31	CKOSC0_MATRIX: OSC0 matrix input
78	960	Matrix Input 32	CKOSC2_MATRIX: OSC2 matrix input
	961	Matrix Input 33	MULTFUNC_8BIT_2: DLY_CNT_OUT
	962	Matrix Input 34	MULTFUNC_8BIT_3: DLY_CNT_OUT
	963	Matrix Input 35	MULTFUNC_8BIT_4: DLY_CNT_OUT
	964	Matrix Input 36	MULTFUNC_8BIT_5: DLY_CNT_OUT
	965	Matrix Input 37	MULTFUNC_8BIT_6: DLY_CNT_OUT
	966	Matrix Input 38	MULTFUNC_8BIT_7: DLY_CNT_OUT
	967	Matrix Input 39	MULTFUNC_16BIT_0: LUT_DFF_OUT

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
79	968	Matrix Input 40	MULTFUNC_8BIT_1: LUT_DFF_OUT
	969	Matrix Input 41	MULTFUNC_8BIT_2: LUT_DFF_OUT
	970	Matrix Input 42	MULTFUNC_8BIT_3: LUT_DFF_OUT
	971	Matrix Input 43	MULTFUNC_8BIT_4: LUT_DFF_OUT
	972	Matrix Input 44	MULTFUNC_8BIT_5: LUT_DFF_OUT
	973	Matrix Input 45	MULTFUNC_8BIT_6: LUT_DFF_OUT
	974	Matrix Input 46	MULTFUNC_8BIT_7: LUT_DFF_OUT
	975	Matrix Input 47	MULTFUNC_16BIT_0: DLY_CNT_OUT
7A	976	Matrix Input 48	Virtual Input [7]: register [976]
	977	Matrix Input 49	Virtual Input [6]: register [977]
	978	Matrix Input 50	Virtual Input [5]: register [978]
	979	Matrix Input 51	Virtual Input [4]: register [979]
	980	Matrix Input 52	Virtual Input [3]: register [980]
	981	Matrix Input 53	Virtual Input [2]: register [981]
	982	Matrix Input 54	Virtual Input [1]: register [982]
	983	Matrix Input 55	Virtual Input [0]: register [983]
7B	984	Matrix Input 56	ACMP0H OUT
	985	Matrix Input 57	ACMP1H OUT
	986	Matrix Input 58	ACMP2L OUT
	987	Matrix Input 59	ACMP3L OUT
	988	Matrix Input 60	2nd CKOSC1_MATRIX
	989	Matrix Input 61	2nd CKOSC0_MATRIX
	990	Matrix Input 62	POR CORE
	991	Matrix Input 63	Tie high
7C	999:992	CNT0(16-bit) Counted Value	Q[7:0]
7D	1007:1000	CNT0(16-bit) Counted Value	Q[15:8]
7E	1015:1008	CNT2(8-bit) Counted Value	Q[7:0]
7F	1023:1016	CNT4(8-bit) Counted Value	Q[7:0]
OSC/ACMP			

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
80	1024	OSC1 turn on by register	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
	1025	matrix power-down or on select	0: matrix down 1: matrix on
	1026	external clock source enable	0: internal OSC1 1: external clock from IO10
	1028:1027	post divider ration control	00: div1 01: div2 10: div4 11: div8
	1031:1029	matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
81	1032	OSC2 turn on by register	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
	1033	matrix power-down or on select	0: matrix down 1: matrix on
	1034	external clock source enable	0: internal OSC2 1: external clock from IO8
	1036:1035	post divider ration control	00: div1 01: div2 10: div4 11: div8
	1039:1037	matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
82	1040	OSC0 turn on by register	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
	1041	matrix power-down or on select	0: matrix down 1: matrix on
	1042	external clock source enable	0: internal OSC0 1: external clock from IO0
	1044:1043	post divider ration control	00: div1 01: div2 10: div4 11: div8
	1047:1045	matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
83	1048	Reserved	
	1049	OSC0 matrix out enable	0: disable 1: enable
	1050	OSC1 matrix out enable	0: disable 1: enable
	1051	OSC2 matrix out enable	0: disable 1: enable
	1052	OSC2 100 ns Startup Delay	0: enable 1: disable
	1053	OSC0 2nd matrix out enable	0: disable 1: enable
	1054	OSC1 2nd matrix out enable	0: disable 1: enable
	1055	Reserved	
84	1058:1056	OSC1 2nd matrix input: matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
	1061:1059	OSC0 2nd matrix input: matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
	1063:1062	Reserved	

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
85	1065:1064	ACMP0H hysteresis	00: 0 mV 01: 32 mV 10: 64 mV 11: 192 mV
	1066	Reserved	0: disable 1: enable
	1067	ACMP0H input buffer enable	0: disable 1: enable
	1068	Reserved	0: disable 1: enable
	1069	ACMP0H input tie to V_{DD} enable	0: disable 1: enable
	1070	ACMP0H wake/sleep enable	0: disable 1: enable
	1071	ACMP0H 100 uA current source enable	0: disable 1: enable
86	1072	ACMP1H positive input come from ACMP0H's input mux output enable	0: disable 1: enable
	1073	Reserved	0: disable 1: enable
	1075:1074	ACMP1H hysteresis	00: 0 mV 01: 32 mV 10: 64 mV 11: 192 mV
	1076	ACMP1H input buffer enable	0: disable 1: enable
	1077	Reserved	0: disable 1: enable
	1078	ACMP1H wake/sleep enable	0: disable 1: enable
	1079	ACMP wake/sleep time selection	0: short time wake/sleep 1: normal time wake/sleep
87	1080	ACMP2L positive input come from ACMP0H's input mux output enable	0: disable 1: enable
	1081	ACMP2L positive input come from ACMP1H's input mux output enable	0: disable 1: enable
	1083:1082	ACMP2L hysteresis	00: 0 mV 01: 32 mV 10: 64 mV 11: 192 mV
	1084	Reserved	0: disable 1: enable
	1085	Reserved	0: disable 1: enable
	1086	Reserved	
	1087	ACMP0H, ACMP1H input buffer WS enable	0: disable 1: enable

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
88	1089:1088	ACMP3L hysteresis	00: 0 mV 01: 32 mV 10: 64 mV 11: 192 mV
	1090	Reserved	0: disable 1: enable
	1091	Reserved	0: disable 1: enable
	1092	ACMP3L positive input come from ACMP2L's input mux output enable	0: disable 1: enable
	1093	Temp sensor register pd control	0: power-down 1: power-on
	1094	Temp sensor register pd select	0: come from register 1: come from matrix
	1095	Temp sensor range select	0: range 1 (0.62 V to 0.99 V typical) 1: range 2 (0.75 V to 1.2 V typical)
89	1097:1096	ACMP0H Gain divider	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
	1103:1098	ACMP0H Vref	ACMP Vref select: 000000: 32 mV ~ 111110: 2.016 V/step = 32 mV; 111111: External Vref
8A	1105:1104	ACMP1H Gain divider	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
	1111:1106	ACMP1H Vref	ACMP Vref select: 000000: 32 mV ~ 111110: 2.016 V/step = 32 mV; 111111: External Vref
8B	1113:1112	ACMP2L Gain divider	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
	1119:1114	ACMP2L Vref	ACMP Vref select: 000000: 32 mV ~ 111110: 2.016 V/step = 32 mV; 111111: External Vref
8C	1121:1120	ACMP3L Gain divider	00: 1x 01: 0.5x 10: 0.33x 11: 0.25x
	1127:1122	ACMP3L Vref	ACMP Vref select: 000000: 32 mV ~ 111110: 2.016 V/step = 32 mV; 111111: External Vref

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
8D	1128	Vref_OUT0 output OP	0: disable 1: enable
	1130:1129	Vref_OUT0 input selection	00: None 01: ACMP0H Vref 10: ACMP1H Vref 11: temp sensor
	1131	Vref_OUT1 output OP	0: disable 1: enable
	1133:1132	Vref_OUT1 input selection	00: None 01: ACMP2L Vref 10: ACMP3L Vref 11: Reserved
	1134	Reserved	
	1135	Tempsensed voltage to ACMP	0: disable connection from temp sensed voltage (VrefO0) to ACMP3L input 1: enable connection from temp sensed voltage (VrefO0) to ACMP3L input
8E	1136	Reserved	
	1137	Vref_OUT0 PD	0: Vref_OUT0 disable 1: Vref_OUT0 enable
	1138	Vref_OUT0 PD selection	0: enable/disable using Vref_OUT0 PD [1137] 1: enable/disable using matrix out[60] TS_OSC_PD
	1139	Vref_OUT1 PD	0: Vref_OUT1 disable 1: Vref_OUT1 enable
	1140	Vref_OUT1 PD selection	0: enable/disable using Vref_OUT1 PD [1139] 1: enable/disable using matrix out[60] TS_OSC_pd
	1143:1141	Reserved	
8F	1145:1144	Reserved	
	1151:1146	Reserved	
Digital Macrocell			
90	1155:1152	2-bit LUT0/DFF0 setting	[3]: 2-bit LUT0[3]/DFF0 or LATCH Select 0: DFF function 1: LATCH function [2]: 2-bit LUT0[2]/DFF0 Output Sel 0: Q output 1: QB output [1]: 2-bit LUT0[1]/DFF0 Initial Polarity Select 0: Low 1: High [0]: 2-bit LUT0[0]
	1159:1156	2-bit LUT1/DFF1 setting	[3]: 2-bit LUT1[3]/DFF1 or LATCH Select 0: DFF function 1: LATCH function [2]: 2-bit LUT1[2]/DFF1 Output Select 0: Q output 1: QB output [1]: 2-bit LUT1[1]/DFF1 Initial Polarity Select 0: Low 1: High [0]: 2-bit LUT1[0]

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
91	1163:1160	2-bit LUT2/DFF2 setting	[3]: 2-bit LUT2[3]/DFF2 or LATCH Select 0: DFF function 1: LATCH function [2]: 2-bit LUT2[2]/DFF2 Output Select 0: Q output 1: QB output [1]: 2-bit LUT2[1]/DFF2 Initial Polarity Select 0: Low 1: High [0]: 2-bit LUT2[0]
	1167:1164	2-bit LUT3_VAL or PGEN_data	2-bit LUT3[3:0] or PGen 4bit counter data[3:0]
92	1175:1168	PGen data [7:0]	PGen data [7:0]
93	1183:1176	PGen data [15:8]	PGen data [15:8]
94	1191:1184	3-bit LUT0_DFF3 setting	[7]: 3-bit LUT0[7]/DFF3 or LATCH Select 0: DFF function 1: LATCH function [6]: 3-bit LUT0[6]/DFF3 Output Select 0: Q output 1: QB output [5]: 3-bit LUT0[5]/DFF3 0: nRST from Matrix Output 1: nSET from Matrix Output [4]: 3-bit LUT0[4]/DFF3 Initial Polarity Select 0: Low 1: High [3:0]: 3-bit LUT0[3:0]
95	1199:1192	3-bit LUT1_DFF4 setting	[7]: 3-bit LUT1[7]/DFF4 or LATCH Select 0: DFF function 1: LATCH function [6]: 3-bit LUT1[6]/DFF4 Output Select 0: Q output 1: QB output [5]: 3-bit LUT1[5]/DFF4 0: nRST from Matrix Output 1: nSET from Matrix Output [4]: 3-bit LUT1[4]/DFF4 Initial Polarity Select 0: Low 1: High [3:0]: 3-bit LUT1[3:0]
96	1207:1200	3-bit LUT2_DFF5 setting	[7]: 3-bit LUT2[7]/DFF5 or LATCH Select 0: DFF function 1: LATCH function [6]: 3-bit LUT2[6]/DFF5 Output Select 0: Q output 1: QB output [5]: 3-bit LUT2[5]/DFF5 0: nRST from Matrix Output 1: nSET from Matrix Output [4]: 3-bit LUT2[4]/DFF5 Initial Polarity Select 0: Low 1: High [3:0]: 3-bit LUT2[3:0]

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
97	1215:1208	3-bit LUT3_DFF6 setting	[7]: 3-bit LUT3[7]/DFF6 or LATCH Select 0: DFF function 1: LATCH function [6]: 3-bit LUT3[6]/DFF6 Output Select 0: Q output 1: QB output [5]: 3-bit LUT3[5]/DFF6 0: nRST from Matrix Output 1: nSET from Matrix Output [4]: 3-bit LUT3[4]/DFF6 Initial Polarity Select 0: Low 1: High [3:0]: 3-bit LUT3[3:0]
98	1223:1216	3-bit LUT4_DFF7 setting	[7]: 3-bit LUT4[7]/DFF7 or LATCH Select 0: DFF function 1: LATCH function [6]: 3-bit LUT4[6]/DFF7 Output Select 0: Q output 1: QB output [5]: 3-bit LUT4[5]/DFF7 0: nRST from Matrix Output 1: nSET from Matrix Output [4]: 3-bit LUT4[4]/DFF7 Initial Polarity Select 0: Low 1: High [3:0]: 3-bit LUT4[3:0]
99	1231:1224	3-bit LUT5_DFF8 setting	[7]: 3-bit LUT5[7]/DFF8 or LATCH Select 0: DFF function 1: LATCH function [6]: 3-bit LUT5[6]/DFF8 Output Select 0: Q output 1: QB output [5]: 3-bit LUT5[5]/DFF8 0: RSTB from Matrix Output 1: SETB from Matrix Output [4]: 3-bit LUT5[4]/DFF8 Initial Polarity Select 0: Low 1: High [3:0]: 3-bit LUT5[3:0]

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
9A	1232	2-bit LUT0 or DFF0 Select	0: 2-bit LUT0 1: DFF0
	1233	2-bit LUT1 or DFF1 Select	0: 2-bit LUT1 1: DFF1
	1234	2-bit LUT2 or DFF2 Select	0: 2-bit LUT2 1: DFF2
	1235	2-bit LUT3 or PGen Select	0: 2-bit LUT3 1: PGen
	1236	3-bit LUT0 or DFF3 Select	0: 3-bit LUT0 1: DFF3
	1237	DFF3_SECONDQ_Sel	0: Q of first DFF 1: Q of second DFF
	1238	3-bit LUT1 or DFF4 Select	0: 3-bit LUT1 1: DFF4
	1239	3-bit LUT2 or DFF5 Select	0: 3-bit LUT2 1: DFF5
9B	1240	3-bit LUT3 or DFF6 Select	0: 3-bit LUT3 1: DFF6
	1241	3-bit LUT4 or DFF7 Select	0: 3-bit LUT4 1: DFF7
	1242	3-bit LUT5 or DFF8 Select	0: 3-bit LUT5 1: DFF8
	1243	Filter or Edge Detector selection	0: filter 1: edge det
	1244	output Polarity Select	0: Filter/edge detect output 1: Filter/edge detect output inverted
	1246:1245	Select the edge mode	00: Rising Edge Det 01: Falling Edge Det 10: Both Edge Det 11: Both Edge DLY
	1247	Reserved	
9C	1255:1248	LUT value or Pipe Delay out SEL or nSET/END value	[7:4]:3-bit LUT6[7:4]/REG_S1[3:0]Pipe Delay out1 SEL [3:0]:3-bit LUT6[3:0]/REG_S0[3:0]Pipe Delay out0 SEL at RIPP CNT mode: bit[1250:1248] is the nSET value bit[1253:1251] is the END value bit[1254] functional mode:0: full cycle; 1: ranged cycle bit[1255] not used

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
9D	1256	Pipe Delay OUT1 Polarity Select	0: Non-inverted 1: Inverted
	1257	3-bit LUT6 or Pipe Delay Select	0: 3-bit LUT6 1: Pipe Delay or RIPP CNT
	1258	PIPE_RIPP_CNT_S	0: Pipe delay mode selection 1: Ripple Counter mode selection
	1260:1259	Select the Edge Mode of Programmable Delay & Edge Detector	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
	1262:1261	Delay Value Select for Programmable Delay & Edge Detector	00: 125ns 01: 250ns 10: 375ns 11: 500ns
	1263	Reserved	
9E	1264	Reserved	
	1265	Reserved	
	1266	Reserved	
	1271:1267	Reserved	
9F	1276:1272	Reserved	
	1277	Reserved	
	1278	Reserved	
	1279	Reserved	
Multifunction			
A0	1286 1285 1282 1284 1283 1281 1280	Single 4-bit LUT	0000000: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	0010000: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK (DLY_IN - LOW)
		Single CNT/DLY	0000001: Matrix A - UP (CNT); Matrix B - KEEP (CNT); Matrix C - EXT_CLK (CNT); Matrix D - DLY_IN (CNT) (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	0000010: Matrix A - DLY_IN; Matrix B - In2; Matrix C - In1; Matrix D - In0 (DLY_OUT connected to In3)

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
A0	1286 1285 1282 1284 1283 1281 1280	CNT/DLY → DFF	0000110: Matrix A - DLY_IN; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	0100010: Matrix A - DLY_IN; Matrix B - EXT_CLK (CNT); Matrix C - In1; Matrix D - In0 (DLY_OUT connected to In3; In2 - LOW)
		CNT/DLY → DFF	0100110: Matrix A - DLY_IN; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - CLK (DLY_OUT connected to D; nSET - HIGH)
		CNT/DLY → LUT	1000010: Matrix A - DLY_IN; Matrix B - In2; Matrix C - EXT_CLK (CNT); Matrix D - In0 (DLY_OUT connected to In3; In1 - LOW)
		CNT/DLY → DFF	1000110: Matrix A - DLY_IN; Matrix B - nSET; Matrix C - EXT_CLK (CNT); Matrix D - CLK (DLY_OUT connected to D; nRST - HIGH)
		CNT/DLY → LUT	0001010: Matrix A - In3; Matrix B - DLY_IN; Matrix C - In1; Matrix D - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	0001110: Matrix A - D; Matrix B - DLY_IN; Matrix C - nRST; Matrix D - CLK (DLY_OUT connected to nSET)
		CNT/DLY → LUT	1001010: Matrix A - In3; Matrix B - DLY_IN; Matrix C - EXT_CLK (CNT); Matrix D - In0 (DLY_OUT connected to In2; In1 - LOW)
		CNT/DLY → DFF	1001110: Matrix A - D; Matrix B - DLY_IN; Matrix C - EXT_CLK (CNT); Matrix D - CLK (DLY_OUT connected to nSET; nRST - HIGH)
		CNT/DLY → LUT	0010010: Matrix A - In3; Matrix B - In2; Matrix C - DLY_IN; Matrix D - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	0010110: Matrix A - D; Matrix B - nSET; Matrix C - DLY_IN; Matrix D - CLK (DLY_OUT connected to nRST)
		CNT/DLY → LUT	0110010: Matrix A - In3; Matrix B - EXT_CLK (CNT); Matrix C - DLY_IN; Matrix D - In0 (DLY_OUT connected to In1; In2 - LOW)
		CNT/DLY → DFF	0110110: Matrix A - D; Matrix B - EXT_CLK (CNT); Matrix C - DLY_IN; Matrix D - CLK (DLY_OUT connected to nRST; nSET - HIGH)
		CNT/DLY → LUT	0011010: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - DLY_IN (DLY_OUT connected to In0)

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
A0	1286 1285 1282 1284 1283 1281 1280	CNT/DLY → DFF	0011110: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - DLY_IN (DLY_OUT connected to CLK)
		CNT/DLY → LUT	0111010: Matrix A - In3; Matrix B - EXT_CLK (CNT); Matrix C - In1; Matrix D - DLY_IN (DLY_OUT connected to In0; In2 - LOW)
		CNT/DLY → DFF	0111110: Matrix A - D; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - DLY_IN (DLY_OUT connected to CLK; nSET - HIGH)
		CNT/DLY → LUT	1011010: Matrix A - In3; Matrix B - In2; Matrix C - EXT_CLK (CNT); Matrix D - DLY_IN (DLY_OUT connected to In0; In1 - LOW)
		CNT/DLY → DFF	1011110: Matrix A - D; Matrix B - nSET; Matrix C - EXT_CLK (CNT); Matrix D - DLY_IN (DLY_OUT connected to CLK; nRST - HIGH)
		LUT → CNT/DLY	0000011: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	0000111: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK (DFF_OUT connected to DLY_IN)
		LUT → CNT/DLY	0100011: Matrix A - In3; Matrix B - EXT_CLK (CNT); Matrix C - In1; Matrix D - In0 (LUT_OUT connected to DLY_IN; In2 - LOW)
		DFF → CNT/DLY	0100111: Matrix A - D; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - CLK (DFF_OUT connected to DLY_IN; nSET - HIGH)
		LUT → CNT/DLY	1000011: Matrix A - In3; Matrix B - In2; Matrix C - EXT_CLK (CNT); Matrix D - In0 (LUT_OUT connected to DLY_IN; In1 - LOW)
		DFF → CNT/DLY	1000111: Matrix A - D; Matrix B - nSET; Matrix C - EXT_CLK (CNT); Matrix D - CLK (DFF_OUT connected to DLY_IN; nRST - HIGH)
	1287	FSM0 SET/RST Selection	0: Reset to 0 1: Set to data
A1	1295:1288	4-bit LUT0_DFF9 setting [7:0]	[7:0]: 4-bit LUT0[7:0]
A2	1303:1296	4-bit LUT0_DFF9 setting [15:8]	[15]: 4-bit LUT0[15]/DFF or LATCH Select 0: DFF function; 1: LATCH function [14]: 4-bit LUT0[14]/DFF Output Select 0: Q output; 1: QB output [13]: 4-bit LUT0[13]/DFF Initial Polarity Select 0: Low; 1: High [12:8]: 4-bit LUT0[12:8]

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
A3	1305:1304	DLY/CNT0 Mode Selection	00: DLY 01: one shot 10: frequency det 11: CNT
	1307:1306	DLY/CNT0 edge Mode Selection	00: both edge 01: falling edge 10: rising edge 11: High Level Reset (only in CNT mode)
	1311:1308	DLY/CNT0 Clock Source Select	Clock source SEL [3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: Not used
A4	1312	CNT0 output pol selection	0: Default Output 1: Inverted Output
	1314:1313	CNT0 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1315	Wake sleep power-down state selection	0: low 1: high
	1316	Wake sleep mode selection	0: disable wake/sleep mode 1: enable wake/sleep mode
	1317	Keep signal SYNC selection	0: bypass 1: after two DFF
	1318	UP signal SYNC selection	0: bypass 1: after two DFF
	1319	CNT0 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection
A5	1327:1320	REG_CNT0_Data[7:0]	Data[7:0]
A6	1335:1328	REG_CNT0_Data[15:8]	Data[15:8]
A7	1336	CNT0 CNT mode SYNC selection	0: bypass 1: after two DFF
	1339 1341 1340 1338 1337	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
A7	1339 1341 1340 1338 1337	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	00110: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	01110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	10010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	00111: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
	1343:1342	CNT1 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
A8	1351:1344	3-bit LUT7_DFF10 setting	[7]: 3-bit LUT7[7]/DFF or LATCH Select 0: DFF function; 1: LATCH function [6]: 3-bit LUT7[6]/DFF Output Select 0: Q output; 1: QB output [5]: 3-bit LUT7[5]/DFF 0: nRST from Matrix Output; 1: nSET from Matrix Output [4]: 3-bit LUT7[4]/DFF Initial Polarity Select 0:Low; 1: High [3:0]: 3-bit LUT7[3:0]
A9	1355:1352	DLY/CNT1 Clock Source Select	Clock source SEL [3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: Not used
	1359:1356	CNT1 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay; 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
AA	1367:1360	REG_CNT1_Data[7:0]	Data[7:0]

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
AB	1368	CNT1 output pol selection	0: Default Output 1: Inverted Output
	1369	Reserved	
	1370	CNT1 CNT mode SYNC selection	0: bypass 1: after two DFF
	1371	CNT1 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection
	1394, 1375:1372	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
AB	1394, 1375:1372	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
AC	1383:1376	3-bit LUT8_DFF_11 setting	[7]: 3-bit LUT8[7]/DFF or LATCH Select 0: DFF function; 1: LATCH function [6]: 3-bit LUT8[6]/DFF Output Select 0: Q output; 1: QB output [5]: 3-bit LUT8[5]/DFF 0: nRST from Matrix Output; 1: nSET from Matrix Output [4]: 3-bit LUT8[4]/DFF Initial Polarity Select 0:Low; 1: High [3:0]: 3-bit LUT8[3:0]

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
AD	1387:1384	DLY/CNT2 Clock Source Select	Clock source SEL [3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: Not used
	1391:1388	CNT2 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay; 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
AE	1393:1392	CNT2 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1395	CNT2 output pol selection	0: Default Output 1: Inverted Output
	1396	Reserved	
	1397	CNT2 CNT mode SYNC selection	0: bypass 1: after two DFF
	1398	CNT2 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection
	1399	Reserved	
AF	1407:1400	REG_CNT2_Data[7:0]	Data[7:0]
B0	1408	Reserved	
	1411 1413 1412 1410 1409	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	00100: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
B0	1411 1413 1412 1410 1409	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	00110: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	01110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	10010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	00111: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
	1415:1414	CNT3 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
B1	1423:1416	3-bit LUT9_DFF12 setting	[7]: 3-bit LUT9[7]/DFF or LATCH Select 0: DFF function; 1: LATCH function [6]: 3-bit LUT9[6]/DFF Output Select 0: Q output; 1: QB output [5]: 3-bit LUT9[5]/DFF 0: nRST from Matrix Output; 1: nSET from Matrix Output [4]: 3-bit LUT9[4]/DFF Initial Polarity Select 0:Low; 1: High [3:0]: 3-bit LUT9[3:0]
B2	1427:1424	DLY/CNT3 Clock Source Select	Clock source SEL [3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: Not used
	1431:1428	CNT3 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay; 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
B3	1439:1432	REG_CNT3_Data[7:0]	Data[7:0]

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
B4	1440	CNT3 output pol selection	0: Default Output 1: Inverted Output
	1441	Reserved	
	1442	CNT3 CNT mode SYNC selection	0: bypass 1: after two DFF
	1443	CNT3 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection
	1466, 1447:1444	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
B4	1466, 1447:1444	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
B5	1455:1448	3-bit LUT10_DFF setting	[7]: 3-bit LUT10[7]/DFF or LATCH Select 0: DFF function; 1: LATCH function [6]: 3-bit LUT10[6]/DFF Output Select 0: Q output; 1: QB output [5]: 3-bit LUT10[5]/DFF 0: nRST from Matrix Output; 1: nSET from Matrix Output [4]: 3-bit LUT10[4]/DFF Initial Polarity Select 0:Low; 1: High [3:0]: 3-bit LUT10[3:0]

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
B6	1459:1456	DLY/CNT4 Clock Source Select	Clock source SEL [3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: Not used
	1463:1460	CNT4 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay; 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
B7	1465:1464	CNT4 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1467	CNT4 output pol selection	0: Default Output 1: Inverted Output
	1468	Reserved	
	1469	CNT4 CNT mode SYNC selection	0: bypass 1: after two DFF
	1470	CNT4 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection
	1471	Reserved	
B8	1479:1472	REG_CNT4_Data[7:0]	Data[7:0]
B9	1480	Reserved	
	1483 1485 1484 1482 1481	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	00100: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
B9	1483 1485 1484 1482 1481	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	00110: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	01110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	10010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	00111: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
	1487:1486	CNT5 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
BA	1495:1488	3-bit LUT11_DFF14 setting	[7]: 3-bit LUT11[7]/DFF or LATCH Select 0: DFF function; 1: LATCH function [6]: 3-bit LUT11[6]/DFF Output Select 0: Q output; 1: QB output [5]: 3-bit LUT11[5]/DFF 0: nRST from Matrix Output; 1: nSET from Matrix Output [4]: 3-bit LUT11[4]/DFF Initial Polarity Select 0:Low; 1: High [3:0]: 3-bit LUT11[3:0]
BB	1499:1496	DLY/CNT5 Clock Source Select	Clock source SEL [3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: Not used
	1503:1500	CNT5 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay; 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
BC	1511:1504	REG_CNT5_Data[7:0]	Data[7:0]

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
BD	1512	CNT5 output pol selection	0: Default Output 1: Inverted Output
	1513	Reserved	
	1514	CNT5 CNT mode SYNC selection	0: bypass 1: after two DFF
	1515	CNT5 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection
	1538, 1519:1516	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
BD	1538, 1519:1516	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
BE	1527:1520	3-bit LUT12_DFF15 setting	[7]: 3-bit LUT12[7]/DFF or LATCH Select 0: DFF function; 1: LATCH function [6]: 3-bit LUT12[6]/DFF Output Select 0: Q output; 1: QB output [5]: 3-bit LUT12[5]/DFF 0: nRST from Matrix Output; 1: nSET from Matrix Output [4]: 3-bit LUT12[4]/DFF Initial Polarity Select 0:Low; 1: High [3:0]: 3-bit LUT12[3:0]

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
BF	1531:1528	DLY/CNT6 Clock Source Select	Clock source SEL [3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: Not used
	1535:1532	CNT6 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay; 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
C0	1537:1536	CNT6 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1539	CNT6 output pol selection	0: Default Output 1: Inverted Output
	1540	Reserved	
	1541	CNT6 CNT mode SYNC selection	0: bypass 1: after two DFF
	1542	CNT6 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection
	1543	Reserved	
C1	1551:1544	REG_CNT6_Data[7:0]	Data[7:0]
C2	1556:1552	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
C2	1556:1552	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
	1557	CNT7 output pol selection	0: Default Output 1: Inverted Output
	1558	Reserved	
	1559	CNT7 CNT mode SYNC selection	0: bypass 1: after two DFF
C3	1567:1560	3-bit LUT13_DFF16 setting	[7]: 3-bit LUT13[7]/DFF or LATCH Select 0: DFF function; 1: LATCH function [6]: 3-bit LUT13[6]/DFF Output Select 0: Q output; 1: QB output [5]: 3-bit LUT13[5]/DFF 0: nRST from Matrix Output; 1: nSET from Matrix Output [4]: 3-bit LUT13[4]/DFF Initial Polarity Select 0:Low; 1: High [3:0]: 3-bit LUT13[3:0]
C4	1571:1568	DLY/CNT7 Clock Source Select	Clock source SEL [3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: Not used
	1575:1572	CNT7 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay; 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
C5	1577:1576	CNT7 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1578	CNT7 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection
	1583:1579	Reserved	
C6	1591:1584	REG_CNT7_Data[7:0]	Data[7:0]
C7	1592	IO0 I^2C output expander data	
	1593	IO0 I^2C output expander select	0: IO0 output come from matrix 1: IO0 output is register
	1594	IO5 I^2C output expander data	
	1595	IO5 I^2C output expander select	0: IO5 output come from matrix 1: IO5 output is register
	1596	IO6 I^2C output expander data	
	1597	IO6 I^2C output expander select	0: IO6 output come from matrix 1: IO6 output is register
	1598	IO9 I^2C output expander data	
	1599	IO9 I^2C output expander select	0: IO9 output come from matrix 1: IO9 output is register
C8	1600	Reserved	
	1601	I^2C reset bit with reloading NVM into Data register (soft reset)	0: Keep existing condition 1: Reset execution
	1602	IO latching enable during I^2C write interface	1: disable 0: enable
	1607:1603	Reserved	
C9	1615:1608	I^2C write mask bits	0: overwrite 1: mask
CA	1619:1616	I^2C target address	
	1620	Target address selection SA4	0: from register 1: from IO2
	1621	Target address selection SA5	0: from register 1: from IO3
	1622	Target address selection SA6	0: from register 1: from IO4
	1623	Target address selection SA7	0: from register 1: from IO5
CB	1631:1624	8-bit Pattern ID Byte 0 (From NVM): ID[23:16]	
CC	1639:1632	Reserved	
Reserved			
CD	1643:1640	Reserved	
	1647:1644	Reserved	

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
CE	1648	Reserved	
	1652:1649	Reserved	
	1653	Reserved	
	1654	Reserved	
	1655	Reserved	
CF	1657:1656	Reserved	
	1658	Reserved	
	1659	Reserved	
	1660	Reserved	
	1661	Reserved	
	1662	Reserved	
	1663	Reserved	
D0	1671:1664	Reserved	
D1	1679:1672	Reserved	
D2	1687:1680	Reserved	
D3	1695:1688	Reserved	
D4	1703:1696	Reserved	
D5	1711:1704	Reserved	
D6	1719:1712	Reserved	
D7	1727:1720	Reserved	
D8	1735:1728	Reserved	
D9	1743:1736	Reserved	
DA	1751:1744	Reserved	
DB	1759:1752	Reserved	
DC	1767:1760	Reserved	
DD	1775:1768	Reserved	
DE	1783:1776	Reserved	
DF	1791:1784	Reserved	
E0 RPR	1793:1792	2k Register Read Selection Bits RPRB[1:0]	00: 2k register data is unprotected for read; 01: 2k register data is partly protected for read; 10: 2k register data is fully protected for read; 11: reserved
	1795:1794	2k Register Write Selection Bits RPRB[3:2]	00: 2k register data is unprotected for write; 01: 2k register data is partly protected for write; 10: 2k register data is fully protected for write; 11: reserved
	1796	Reserved	
	1797	Reserved	
	1798	Reserved	
	1799	Reserved	

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
E1 NPR	1801:1800	2k NVM Configuration Selection Bits NPRB[1:0]	00: 2k NVM Configuration data is unprotected for read and write/erase; 01: 2k NVM Configuration data is fully protected for read; 10: 2k NVM Configuration data is fully protected for write/erase; 11: 2k NVM Configuration data is fully protected for read and write/erase.
	1802	Reserved	
	1803	Reserved	
	1804	Reserved	
	1805	Reserved	
	1806	Reserved	
	1807	Reserved	
E2 WPR	1809:1808	Reserved	
	1810	Write Protect Register Enable	0: No Software Write Protection enabled (default). 1: Write Protection is set by the state of the WPB[1:0] bits.
	1815:1811	Reserved	
E3	1820:1816	Page Selection for Erase ERSEB[4:0]	Define the page address which will be erased. ERSEB[4] = 0 corresponds to the upper 2k NVM used for chip configuration;
	1821	Reserved	
	1822	Reserved	
	1823	Erase Enable ERSE	0: erase disable 1: cause the NVM erase: full NVM (4k bits) erase for ERSCHIP = 1 (reg[1973]) if DIS_ERSCHIP = 0 (reg[1972]) or page erase for ERSCHIP = 0 (reg[1973]).
E4	1824	Protection Lock Bit (PRL)	0: RPR/WPR/NPR setting can be changed 1: RPR/WPR/NPR setting cannot be changed
	1831:1825	Reserved	
E5	1839:1832	Reserved	
E6	1847:1840	Reserved	
E7	1855:1848	Reserved	
E8	1863:1856	Reserved	
E9	1871:1864	Reserved	
EA	1879:1872	Reserved	
EB	1887:1880	Reserved	
EC	1895:1888	Reserved	
ED	1903:1896	Reserved	
EE	1911:1904	Reserved	
EF	1919:1912	Reserved	
F0	1926:1920	Reserved	
	1927	Reserved	
F1	1932:1928	Reserved	
	1934:1933		
	1935	Reserved	

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Table 59: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
F2	1940:1936	Reserved	
	1943:1941		
F3	1949:1944	Reserved	
	1951:1950		
F4	1957:1952	Reserved	
	1959:1958		
F5	1965:1960	Reserved	
	1967:1966		
F6	1968	Reserved	
	1971:1969	Reserved	
	1972	Reserved	
	1973	Reserved	
	1974	Reserved	
	1975	Reserved	
F7	1983:1976	Reserved	
F8	1991:1984	Reserved	
F9	1992	Reserved	
	1993	Reserved	
	1995:1994	Reserved	
	1999:1996	Reserved	
FA	2000	Reserved	
	2001	Reserved	
	2002	Reserved	
	2006:2003		
	2007	Reserved	
FB	2015:2008	Reserved	
FC	2023:2016	Reserved	
FD	2031:2024	Reserved	
FE	2039:2032	Reserved	
FF	2047:2040	Reserved	

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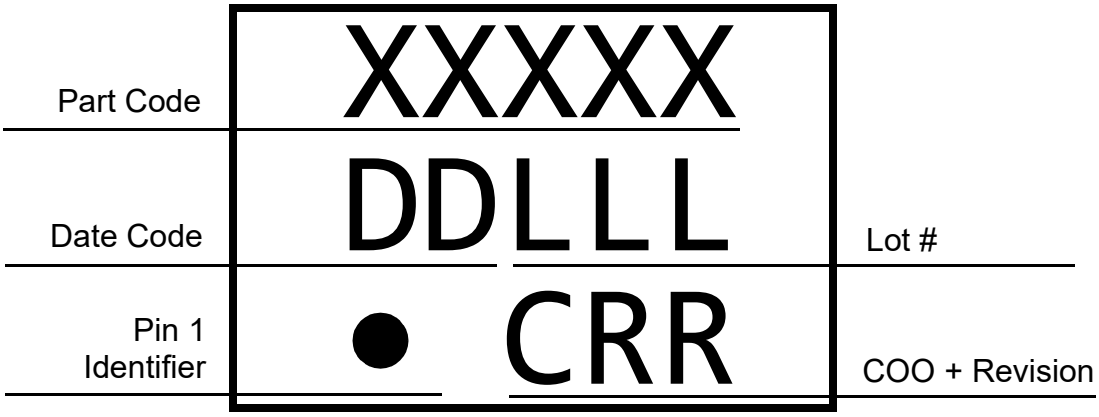
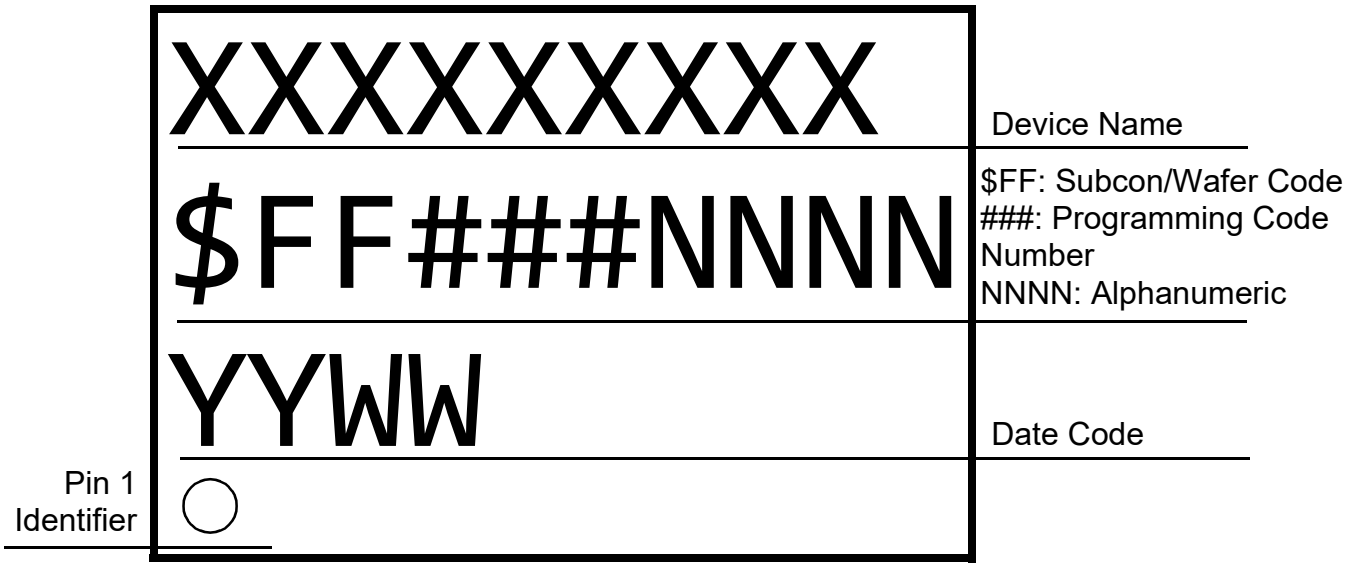
19 Package Top Marking System Definition

19.1 STQFN 20L 2 MM X 3 MM 0.4P FCD PACKAGE



XXXXX - Part ID Field identifies the specific device configuration
DD - Date Code Field: Coded date of manufacture
LLL - Lot Code: Designates Lot #
C - Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR - Revision Code: Device Revision

19.2 TSSOP-20



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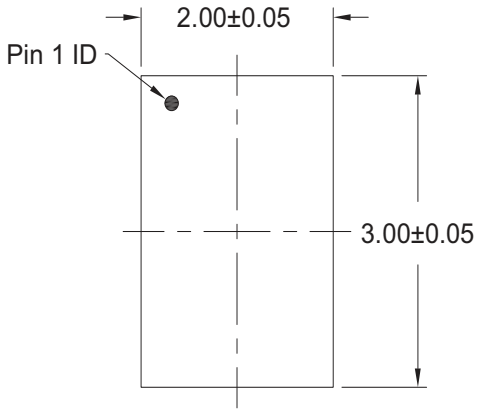
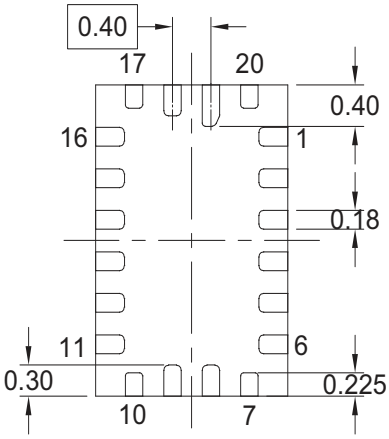
20 Package Information

20.1 PACKAGE OUTLINES FOR STQFN 20L 2 MM X 3 MM 0.4P FCD

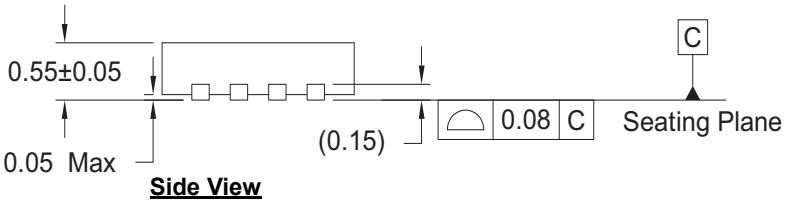
JEDEC MO-220, Variation WECE
IC Net Weight: 0.008 g



Top View



Bottom View



Side View

Notes:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for reference only

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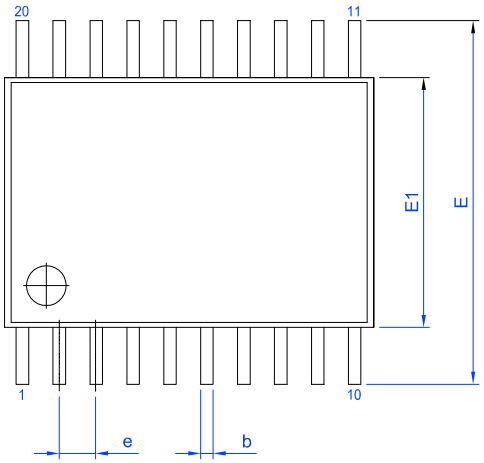
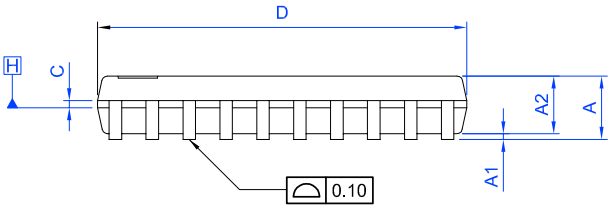
20.2 PACKAGE OUTLINES FOR TSSOP 20L 173 MIL GREEN

JEDEC MO-220, Variation WECE
IC Net Weight: 0.083 g

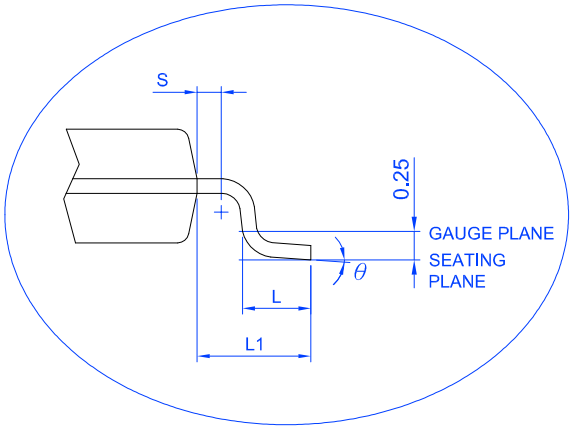


Marking View

Side View



Side view



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	-	-	1.20	D	6.40	6.50	6.60
A1	0.05	-	0.15	E1	4.30	4.40	4.50
A2	0.80	0.90	1.05	E	6.40 BSC		
b	0.19	-	0.30	L	0.50	0.60	0.75
C	0.09	-	0.20	L1	1.00 REF		
e	0.65 BSC			S	0.20	-	-
				Θ	0°	-	8°

NOTES:

1.JEDEC OUTLINE :
STANDARD : MO-153 AC REV.F
THERMALLY ENHANCED : MO-153 ACT REV.F

2.DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

3.DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

4.DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.

5.DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H

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20.3 STQFN AND TSSOP HANDLING

Be sure to handle STQFN and TSSOP packages only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle STQFN and TSSOP packages with fingers as this can contaminate the package pins and interface with solder reflow.

20.4 SOLDERING INFORMATION

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm^3 (nominal) for STQFN 20L Package and package volume of 25.74 mm^3 (nominal) for TSSOP-20 Package. More information can be found at www.jedec.org.

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21 Ordering Information

Part Number	Type
SLG46826V	20-pin STQFN
SLG46826VTR	20-pin STQFN - Tape and Reel (3k units)
SLG46826G	20-pin TSSOP
SLG46826GTR	20-pin TSSOP Tape and Reel (4k units)

Note 1 Use SLG46826V or SLG46826G to order. Shipments are automatically in Tape and Reel.
Note 2 "TR" suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

21.1 TAPE AND REEL SPECIFICATIONS

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
STQFN 20L 2 mm x3 mm 0.4P FCD	20	2 x 3 x 0.55	3,000	3,000	178/60	100	400	100	400	8	4
TSSOP 20L 173 MIL Green Package	20	6.5 x 6.4	4,000	4,000	330/100	42	336	42	336	16	8

21.2 CARRIER TAPE DRAWING AND DIMENSIONS

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2 mm x3 mm 0.4P FCD	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8
TSSOP 20L 173 MIL Green Package	6.8	6.9	1.6	4	8	1.5	1.75	7.5	16

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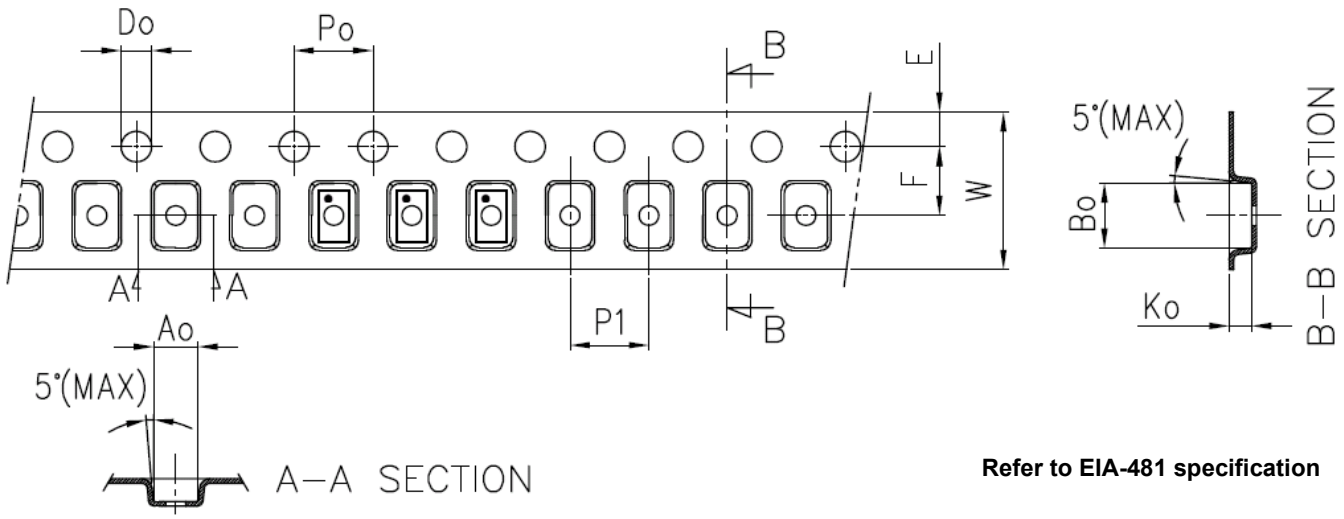
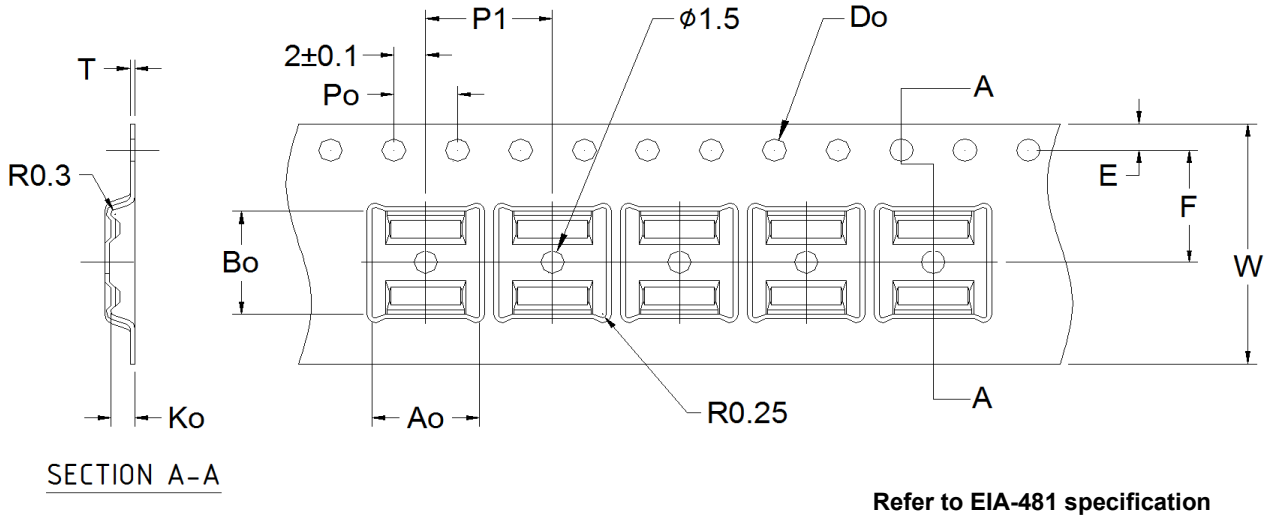
21.3 STQFN-20L



Refer to EIA-481 specification

21.4 TSSOP-20L



Refer to EIA-481 specification

Note: Orientation in carrier: Pin1 is at upper left corner (Quadrant1).

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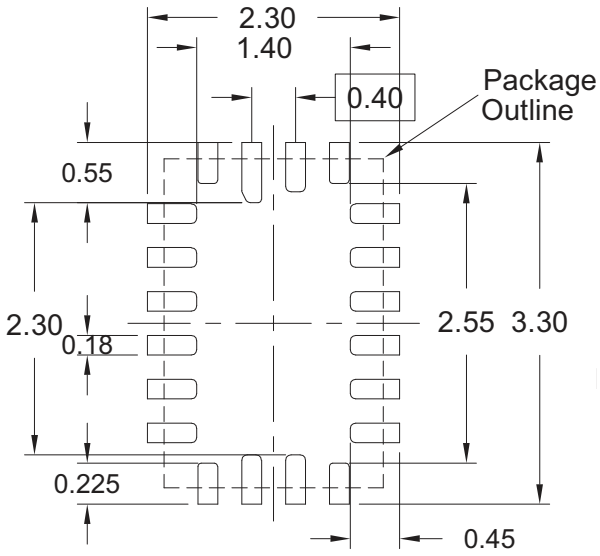
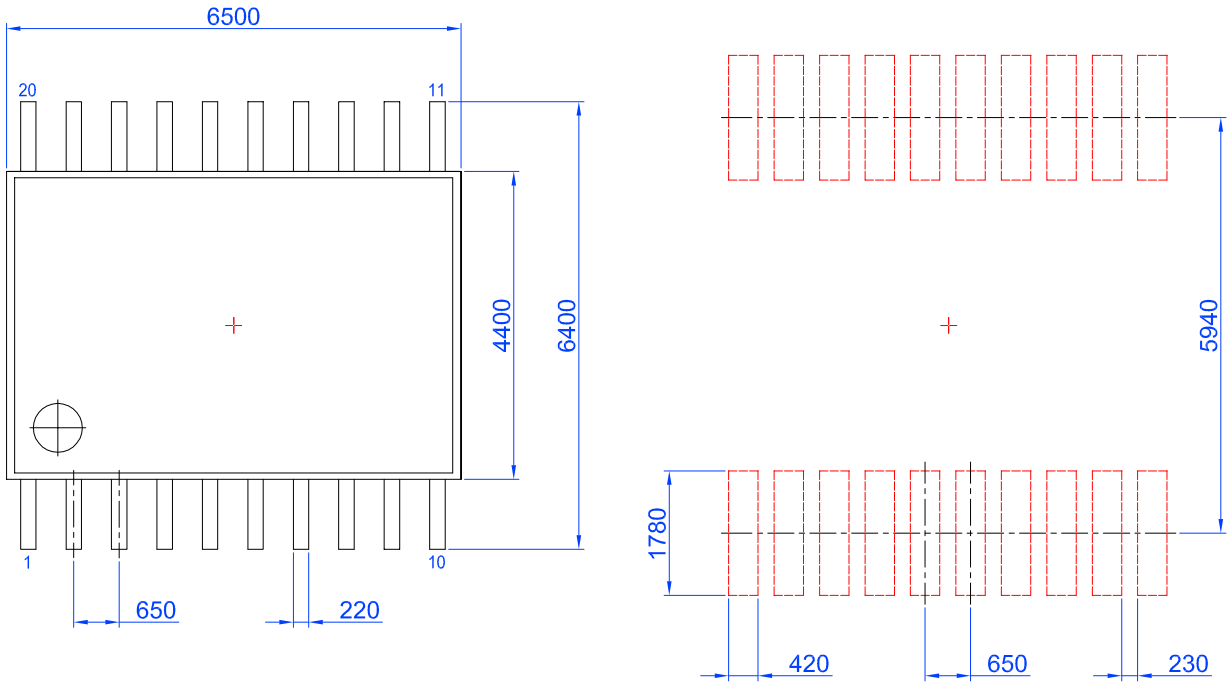
22 Layout Guidelines

22.1 STQFN 20L 2 MM X 3 MM 0.4P FCD PACKAGE



Unit: mm

22.2 TSSOP-20



Unit: µm

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Glossary

A

ACK	Acknowledge bit
ACMP	Analog Comparator
ACMPH	Analog Comparator High Speed
ACMPL	Analog Comparator Low Power

B

BG	Bandgap

C

CLK	Clock
CMO	Connection matrix output
CNT	Counter

D

DFF	D Flip-Flop
DLY	Delay

E

EC	Electrical Characteristics
ERSE	Erase Enable
ERSR	Erase Register
ESD	Electrostatic discharge
EV	End Value

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

I

IN	Input
IO	Input/Output

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L

LPF	Low Pass Filter
LSB	Least Significant Bit
LUT	Look Up Table
LV	Low Voltage

M

MSB	Most Significant Bit
MTP	Multiple-Time-Programmable
MUX	Multiplexer

N

NPR	Non-Volatile Memory Read/Write/Erase Protection
nRST	Reset
NVM	Non-Volatile Memory

O

OD	Open-Drain
OE	Output Enable
OSC	Oscillator
OUT	Output

P

PD	Power-down
PGen	Pattern Generator
POR	Power-On Reset
PP	Push-Pull
PRL	Protect Lock Bit
PWR	Power
P DLY	Programmable Delay

R

RPR	Register Read/Write Protection
RPRB	Register Read/Write Protection Bit
RPRL	Register Protection Read/Write/Erase Lock
R/W	Read/Write

S

SCL	I^2C Clock Input

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SDA	I^2C Data Input/Output
SLA	Target Address
SMT	With Schmitt Trigger
SV	nSET Value

T

TS	Temperature Sensor

V

Vref	Voltage Reference

W

WOSMT	Without Schmitt Trigger
WPB	Write Protect Bit
WPR	Write Protection Register
WPRE	Write Protect Enable
WS	Wake and Sleep Controller

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Revision History

Revision	Date	Description
3.22	16-Oct-2025	Updated Recommended Land Pattern Updated Package Drawing and Dimensions Updated LUT block names to match with Go Configure™ Software Hub Updated the terms Master/Slave to Controller/Target to comply with the latest I^2C
3.21	31-May-2024	Fixed typos Corrected register [1602] definition from 1 to 0 in section Byte Write Command and in section I^2C Additional Options
3.20	30-Nov-2023	Corrected registers [1623:1620]
3.19	10-Oct-2023	Updated Vref Block Diagram Corrected registers [1133:1132] Corrected registers [1316:1315] Corrected [395:372] Register Bit Definitions Corrected ACMP0H Block Diagram Fixed typos
3.18	27-Feb-2023	Added notes to section Ordering Information
3.17	3-Feb-2023	Updated Package Marking for TSSOP package
3.16	9-Sep-2022	Added Note to section I2C Serial Command Register Map
3.15	5-Aug-2022	Fixed typos Corrected register definitions [987:986]
3.14	7-Mar-2022	Updated Pull-up or Pull-down Resistance Parameter in EC table Renesas rebranding Added IC Net Weight in Package Information section Added information about SCL and SDA Pins' Schmitt Trigger Updated section IO8 Source for Oscillator2 (25 MHz) t_{start} updated in table ACMP Specifications Updated section Wake and Sleep Controller Corrected Wake and Sleep Controller Block Diagram
3.13	24-Feb-2021	Updated table ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted
3.12	10-Dec-2020	Updated register definitions: [984], [985] Corrected 3-Bit LUT or DFF/LATCH with 8-Bit Counter/Delay Macrocells section Corrected POR Initialization and Power Down sections Fixed typos Corrected table Oscillators Frequency Limits Added description for Internal 100 µA current source Corrected GPIO Register OE IO Structure Diagrams Added note in EC table Corrected I^2C Mode Structure (for SCL and SDA) Corrected Recommended Operating Conditions Corrected Figure TS Output vs Temperature Corrected Electrical Characteristics (I_{OH}) table
3.11	10-Mar-2020	Updated section CNT/DLY/FSM Timing Diagrams Corrected Functional Pin description Corrected registers[1623:1620] Corrected Register map's Bytes value Added note for CNTs Updated Typical Counter/Delay Offset Corrected EC of the I^2C Pins Table Updated PIN Block Diagrams Fixed typos Corrected Edge Detection Mode Timing Diagram Section Delayed Edge Detection Mode added Corrected ACMPs hysteresis selection options
3.10	15-Jul-2019	Corrected Vref electrical specification

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Revision	Date	Description
3.9	10-Jul-2019	Updated according to new template Corrected information in Analog Comparators section Fixed typos
3.8	10-Jun-2019	Updated Analog Temperature sensor section Updated according to Dialog's Writing Guideline Fixed typos Corrected Oscillators names Changed I^2C Serial Communications Macrocell section structure
3.7	9-Apr-2019	Corrected 2-bit LUT3 or PGen figure Corrected Electrical Spec
3.6	25-Mar-2019	Added new subsection Electrostatic Discharge Ratings Fixed typos Removed information about SCL and SDA Pins' Schmitt Trigger Corrected Absolute Maximum Ratings Corrected Pinout figure
3.5	20-Feb-2019	Updated Absolute Maximum Ratings Added Maximum Average or DC Current (Through pin) parameter Corrected ACMPs Block Diagrams Added ACMPs' hysteresis information Added additional information about V_{DD2} to IO Pins section Added graph for ACMP Input Current Source Updated Input Current Source Spec Corrected Absolute Maximum Ratings Updated table Typical Delay Fixed typos
3.4	2-Nov-2018	Updated ACMP section Extended ACMP spec Added graphs to ACMP section Updated Pinout Section Added Parameter ACMP0H Input Current Source Added graphs to IO pins section Fixed typos Updated Oscillator Startup Diagram Updated Analog Temperature Sensor Structure Diagram Updated Example of I^2C Byte Write Bit Masking Updated figures in Oscillators accuracy subsection Added table Oscillator Output Duty Cycle to Oscillators accuracy subsection
3.3	8-Aug-2018	Fixed typos
3.2	7-Aug-2018	Fixed typos Updated R_{PULL} in Electrical Spec Updated figure I^2C Block Addressing
3.1	24-May-2018	Updated Electrical Spec Fixed typos Updated register definitions: [1602], [2015:2008] Updated Electrical spec notes and conditions Updated STQFN and TSSOP Handling section
3.0	30-Apr-2018	Final version

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Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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