SLG46801V-PR

Multi-Time Programmable GreenPAK IC in STQFN Packaging

Description

The SLG46801V-PR integrates the most popular mixed-signal functions with multi-time programmable memory to provide a low power, highly flexible component for commonly used analog signal processing and mixed-signal functions. Individual analog comparators used in conjunction with configurable logic provide a way to solve a wide variety of tasks with minimal costs.

The non-volatile memory (NVM) used in the device is programmed via the configuration software and once deployed in the end application, can be reprogrammed for bug-fixing or device upgrades.

The SLG46801V-PR offers an I^2C serial communications bus for interfacing with the system and it is also used for MTP re-programming. With a very low voltage operating voltage range of 1.71 V to 5.5 V, the device offers extremely high flexibility for a wide variety of applications while occupying a minimum amount of board area. The device is available in the STQFN 12 lead package with a 1.6 mm x 1.6 mm x 0.55 mm size, offering small size and high GPIO count for industrial applications.

Features

- Multi-time programmable (MTP) memory for in-system programming
- Two high-speed analog comparators (ACMP)
- Two tolerant GPIO pins - can be safely driven above VDD
- I^2C Compatible Serial Interface
- Read Back Protection (Read Lock)
- Three Combination Function Macrocells
  - 3-bit LUTs or DFF/LATCHs with Reset/Set
- Three Multi-function Macrocells
  - Selectable DFF/LATCHs or 3-bit LUTs + 8-bit Delay/Counters
- Programmable Delay with Edge Detector Output
- Three 8-bit Delay/Counters
- Two Oscillators (OSC)
  - 10 kHz Oscillator
  - 25 MHz Oscillator
- Power-on Reset (POR) with Optional CRC
- 1.71 V to 5.5 V – operating and program/erase V_{DD} Range
- 12L 1.6 mm x 1.6 mm x 0.55 mm, 0.4 mm pitch STQFN package
- -40 °C to +105 °C Operating Temperature Range

Applications

- Consumer electronics
- Handheld and portable electronics
- Industrial automation and process control
- Personal computers and servers
- Battery voltage and current monitoring
- Smartphones and fitness bands
- Notebook and tablet PC

1. Overview

1.1 Block Diagram

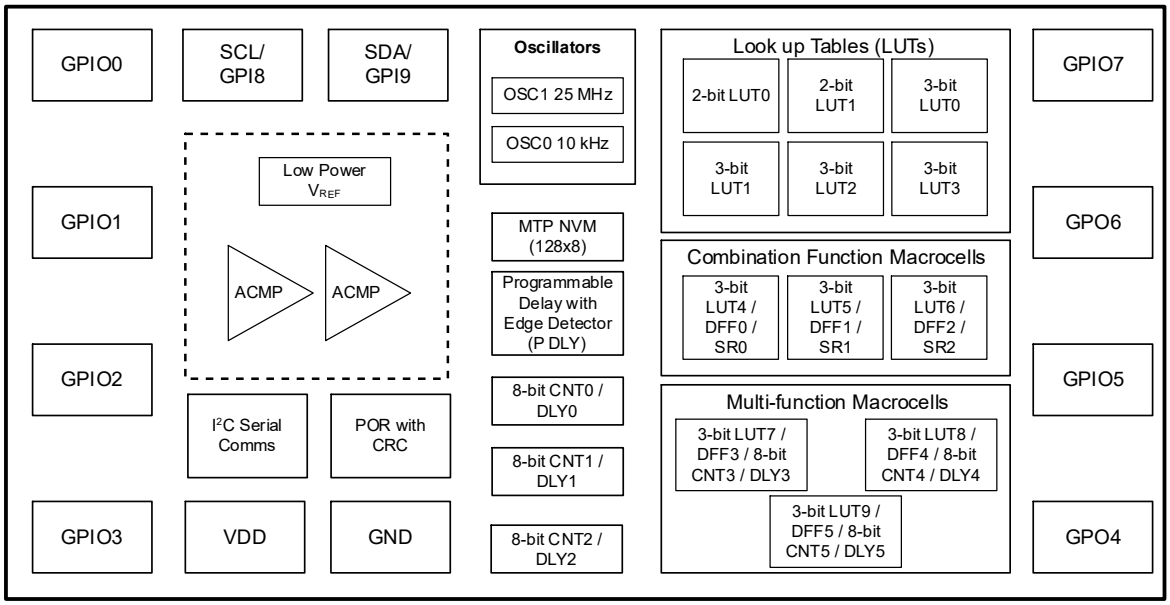


Figure 1. Block Diagram

2. Pin Information

2.1 Pin Assignments

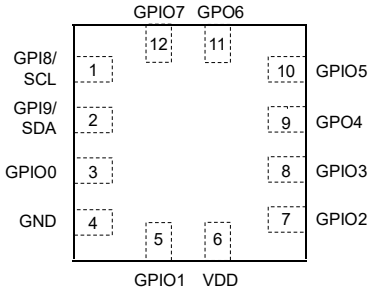


Figure 2. Pin Assignment – STQFN-12L (Top View)

2.2 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
7	GPIO2	GPIO, ACMP1+
6	VDD	Power supply
4	GND	Ground
8	GPIO3	GPIO, ACMP0+
3	GPIO0	GPIO, Ext Clk of RINGOSC
2	GPI9/SDA	I²C SDA/GPI
10	GPIO5	Tolerant GPIO with OE, Ext Clk of LFOSC

Pin Number	Pin Name	Description
12	GPIO7	GPIO with OE, Ext VREFIN
1	GPI8/SCL	I^2C SCL/GPI
5	GPIO1	Tolerant GPIO
9	GPO4	GPO
11	GPO6	GPO

Table 2. Functional Pin Description

Pin Name	Signal Name	Function	Input Option	Output Option
GPIO0	GPIO0	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
			Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
	Ext CLK	External Clock of RINGOSC	Digital Input without Schmitt Trigger	-
			Digital Input with Schmitt Trigger	
			Low-voltage Digital Input	
GPIO1	GPIO1	Tolerant General Purpose IO	Digital Input without Schmitt Trigger	-
			Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
GPIO2	GPIO2	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
			Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
	ACMP1+	Analog Comparator 1 Non-inverting Input	Analog	-
GPIO3	GPIO3	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
			Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
	ACMP0+	Analog Comparator 0 Non-inverting Input	Analog	-
GPO4	GPO4	General Purpose Output	-	Push-Pull (1x) (2x)
			-	Open-Drain NMOS (1x) (2x)
GPIO5	GPIO5	Tolerant General Purpose IO with OE	Digital Input without Schmitt Trigger	-
			Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
	Ext CLK	External Clock of LFOSC	Digital Input without Schmitt Trigger	-
			Digital Input with Schmitt Trigger	
			Low-voltage Digital Input	
GPO6	GPO6	General Purpose Output	-	Push-Pull (1x) (2x)
			-	Open-Drain NMOS (1x) (2x)
GPIO7	GPIO7	General Purpose IO with OE	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
			Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
			Low-voltage Digital Input	-
	EXT_VREF	Analog Comparator Inverting Input	Analog	-
SCL	SCL/GPI8	I^2C Serial Clock	-	-
			Digital Input without Schmitt Trigger	-

Pin Name	Signal Name	Function	Input Option	Output Option
		General Purpose Input	Digital Input with Schmitt Trigger	-
			Low-voltage Digital Input	-
SDA	SDA/GPI9	I^2C Serial Data	-	-
		General Purpose Input	Digital Input without Schmitt Trigger	-
			Digital Input with Schmitt Trigger	-
			Low-voltage Digital Input	-
VDD	VDD	Power Supply	-	-
GND	GND	Power Supply	-	-

3. Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to the absolute maximum conditions for extended periods may affect the device reliability.

Parameter	Min	Max	Unit
VDD Voltage to GND	-0.5	7.0	V
SDA and SCL Voltage to GND	-0.5	7.0	V
All GPIO, GPO Pin Voltage to GND	-0.5	V_{DD} + 0.5, up to 7.0	V
Tolerant GPIO Pin Voltage to GND	-0.5	7.0	V
VDD DC Current	-	TBD	mA
GND DC Current	-	TBD	mA
GPIO DC Current, Push-pull 1x Output Mode	-	12	mA
GPIO DC Current, Push-pull 2x Output Mode	-	24	mA
GPIO DC Current, Open-drain 1x Output Mode	-	12	mA
GPIO DC Current, Open-drain 2x Output Mode	-	24	mA
Continuous Power Dissipation (JESD51-7, T_A = +25ºC), STQFN-12L, Derate 13 mW / ºC above T_A = +25 ºC	-	1625	mW
Junction Temperature	-	+150	°C
Storage Temperature Range	-65	+150	°C

3.2 ESD Ratings

Parameter	Value	Unit
ESD Protection (Human Body Model), ANSI, ESDA, JEDEC JS-001 Standards	3000	V
ESD Protection (Charged Device Model), JEDEC JESD22-101 Standard	1500	V

3.3 Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
VDD Supply Voltage Range		1.71	5.5	V
	During NVM Write and Erase commands	1.71	5.5	V
SCL and SDA Voltage to GND		-0.3	5.5	V
GPIO and GPO Pin Voltage to GND		-0.3	VDD + 0.3, up to 5.5	V
Tolerant GPIO Pin Voltage to GND		-0.3	5.5	V
Logic Input Pin Current		-	1	µA
Operating Ambient Temperature Range		-40	+105	°C
Input Capacitor at VDD Pin		0.1	-	µF

3.4 Thermal Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Ambient	θ_{JA}[1]			76.9	--	°C/W
[1] θ_{JA} is measured on a JEDEC PCB with 70 µm thick (2 oz.) copper.						

4. Package Information

4.1 Package Outline Drawings

4.1.1 STQFN (1.6 mm x 1.6 mm x 0.55 mm, 0.4 mm Pitch)

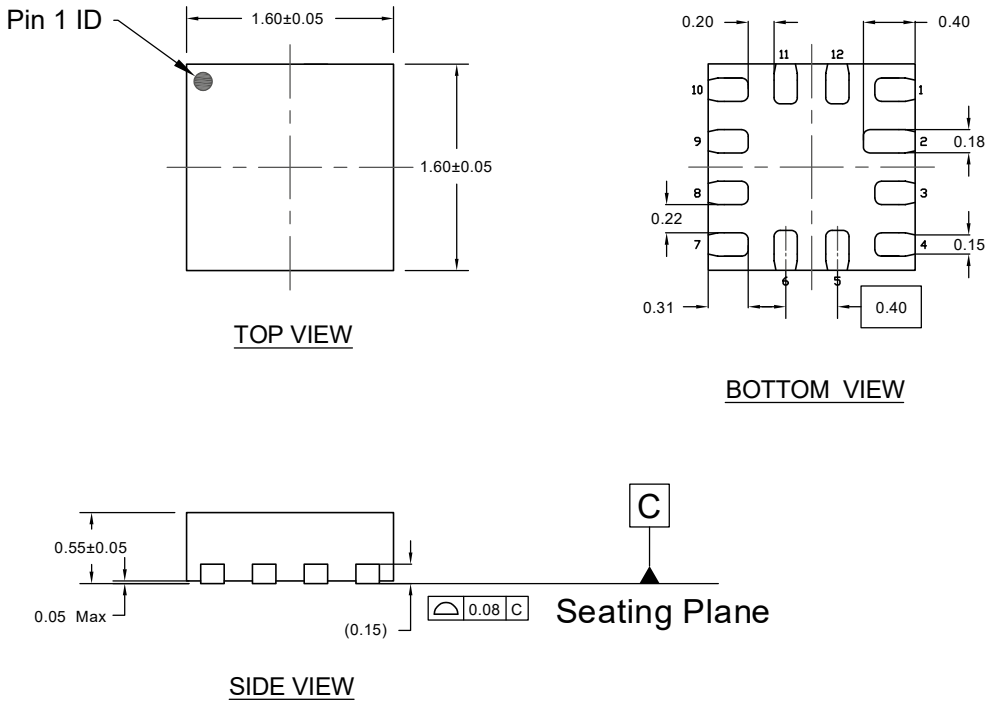


Figure 3. STQFN-12 Package Outline Drawing

4.2 Package Top Marking

4.2.1 STQFN (1.6 mm x 1.6 mm x 0.55 mm, 0.4 mm Pitch)

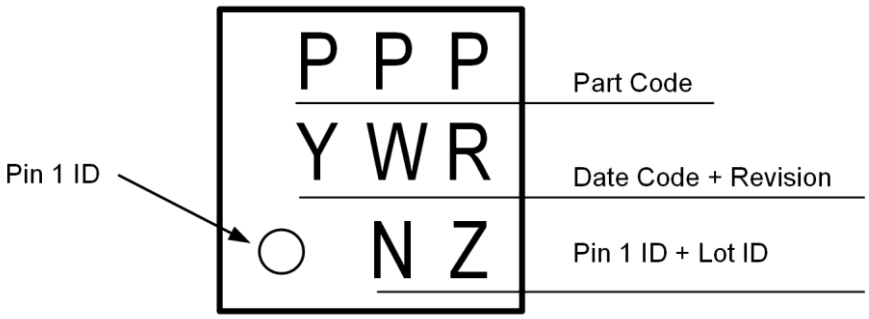
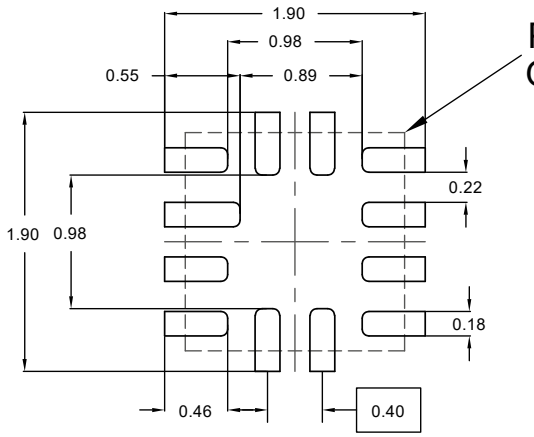


Figure 4. STQFN-12 Top Marking

5. Recommended Land Pattern

5.1 STQFN-12 Recommended Land Pattern



NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

Figure 5. STQFN-12 Recommended Land Pattern

6. Ordering Information

Part Number	Package Description	Carrier Type	Ambient Temperature Range
SLG46801V-PR[1]	STQFN-12, 1.6 mm x 1.6 mm x 0.55 mm	Tape and Reel	-40 °C to +105 °C

[1] This is a pre-release part number for samples only. The production part number is SLG46801V for the STQFN package option.

7. Revision History

Revision	Date	Description
0.01	May 26 2026	Initial Advance Datasheet