SH74593

RENESAS MCU

R01DS0186EJ0120
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1. Overview

The SH7459 Group is a single-chip RISC (reduced instruction set computer) microcontroller based on a Renesas original RISC CPU core.

Basically the SH7459 Group is the same as the SH7456 Group. Please refer to SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10 (Sep 22, 2011). Table 1.1 shows the differences between the SH7456 Group and the SH7459 Group.

* Henceforth, the bold letter portion (shaped portion) shows a difference from SH7456 Group.

Table 1.1 Products

Group	Product	Model	CPU Frequency	Memory Capacity	Package	FlexRay	Operating temperature (Ta)
SH7459	**SH74593**	**R5F74593LBG**	**240**MHz	ROM: **1.5**Mbytes IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: **512** Kbytes	PRBG0176GA-A	**Yes**	-40 to +**105**°C
SH7455	SH74552	R5F74552KBG	160MHz	ROM: 1Mbyte IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: 256 Kbytes		Yes	-40 to +125°C
SH7456	SH74562	R5F74562KBG				No	
SH7457	SH74572	R5F74572LBG	240MHz			Yes	-40 to +105°C

2. Details

This section shows the details of the difference from SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10 (Sep 22, 2011). Table 2.1 shows the difference between the SH74562 and the SH74593.

Table 2.1 Difference between SH74562 and SH74593

Page	Description
1-1	• 1.1 Features Product SuperHyway RAM (SHwyRAM) Capacity SH74562 256 Kbytes SH74593 **512** Kbytes
1-4	• Table 1.1 Specifications Overview: Descriptions of ROM Product ROM Capacity SH74562 1-Mbytes SH74593 **1.5**-Mbytes
	• Table 1.1 Specifications Overview: Descriptions of RAM Product RAM Capacity SH74562 256-Kbytes SH74593 **512**-Kbytes
1-4	• Table 1.1 Specifications Overview: Descriptions of CPG Product CPU clock (Ick) SH74562 160 MHz maximum SH74593 **240** MHz maximum

Page	Description
1-6	• Table 1.1 Specifications Overview: Descriptions of FlexRay Product Channels of FlexRay SH74562 None: SH7456 Group SH74593 **Two channels**: **SH7459** Group
1-7	• Table 1.1 Specifications Overview: Descriptions of Operating temperature Product Operating temperature SH74562 Ta = –40°C to +125°C SH74593 Ta = –40°C to +**105**°C
	• Table 1.2 Products Product Model ROM Capacity SHwyRAM Capacity FlexRay SH74562 R5F74562KBG 1 Mbyte 256 Kbytes No SH74593 **R5F74593LBG** **1.5 Mbytes** **512 Kbytes** **Yes** Please refer to Appendix A.
1-8	• Figure 1.1 Block Diagram Product SH-4A core clock ROM Capacity SHwyRAM Capacity SH74562 SH-4A core (160 MHz maximum) ROM (1 Mbyte) SHwyRAM (256 Kbytes) SH74593 SH-4A core (**240** MHz maximum) ROM (**1.5** Mbytes) SHwyRAM (**512** Kbytes)
1-9 1-15	• Figure 1.2 Pin Arrangement (Top Transparent View) • Table 1.3 Pin Functions of pin A6 Product A6 pin SH74562 Vcc SH74593 **Vss** Please refer to Appendix B.
11-2	• Figure 11.2 Address Space (P0/U0 Area): Descriptions of 29-bit physical address space (Single chip) Product ROM Capacity (Start address – Last address) SHwyRAM Capacity (Start address – Last address) SH74562 1 Mbyte (H'0000 0000 – H'000F FFFF) 256 Kbytes(H'1800 0000 – H'1803 FFFF) SH74593 **1.5** Mbytes (H'0000 0000 – **H'0017 FFFF**) **512** Kbytes(H'1800 0000 – **H'1807 FFFF**) Please refer to Appendix C.1.
11-3	• Figure 11.3 Address Space (P1 Area): Descriptions of 29-bit physical address space (Single chip) Product ROM Capacity (Start address – Last address) SHwyRAM Capacity (Start address – Last address) SH74562 1 Mbyte (H'8000 0000 – H'800F FFFF) 256 Kbytes(H'9800 0000 – H'9803 FFFF) SH74593 **1.5** Mbytes (H'8000 0000 – **H'8017 FFFF**) **512** Kbytes(H'9800 0000 – **H'9807 FFFF**) Please refer to Appendix C.2.
11-4	• Figure 11.4 Address Space (P2 Area): Descriptions of 29-bit physical address space (Single chip) Product ROM Capacity (Start address – Last address) SHwyRAM Capacity (Start address – Last address) SH74562 1 Mbyte (H'A000 0000 – H'A00F FFFF) 256 Kbytes(H'B800 0000 – H'B803 FFFF) SH74593 **1.5** Mbytes (H'A000 0000 – **H'A017 FFFF**) **512** Kbytes(H'B800 0000 – **H'B807 FFFF**) Please refer to Appendix C.3.
11-5	• Figure 11.5 Address Space (P3 Area): Descriptions of 29-bit physical address space (Single chip) Product ROM Capacity (Start address – Last address) SHwyRAM Capacity (Start address – Last address) SH74562 1 Mbyte (H'C000 0000 – H'C00F FFFF) 256 Kbytes(H'D800 0000 – H'D803 FFFF) SH74593 **1.5** Mbytes (H'C000 0000 – **H'C017 FFFF**) **512** Kbytes(H'D800 0000 – **H'D807 FFFF**) Please refer to Appendix C.4.

Page	Description
12-1	• 12. ROM Product ROM Capacity SH74562 1 Mbyte SH74593 **1.5 Mbytes**
	• 12.1 Overview Product Area SH74562 When the user boot MAT is selected, the area from H'0000 8000 to H'000F FFFF has an undefined value when read and both writing and erasing are disabled. SH74593 When the user boot MAT is selected, the area from H'0000 8000 to **H'0017 FFFF** has an undefined value when read and both writing and erasing are disabled.
	• Figure 12.1 Memory MAT Configuration in ROM: Descriptions of User MAT Product Read : Start address – Last address Program/erase : Start address – Last address SH74562 H'0000 0000 – H'000F FFFF H'FD80 0000 – H'FD8F FFFF SH74593 H'0000 0000 – **H'0017 FFFF** H'FD80 0000 – **H'FD97 FFFF** Please refer to Appendix D.1.

Page	Description
12-1 12-2	• 12.1 Overview • Figure 12.2 Block Diagram of ROM: Descriptions of ROM MAT Product Capacity of User MAT SH74562 1 Mbyte SH74593 **1.5 Mbytes**
12-3	• 12.1 Overview : Programming/erasing unit Product Number of 128-Kbytes block SH74562 three blocks SH74593 **seven** blocks
	• Figure 12.3 User MAT and Block Allocation Product Name of 128-Kbytes block SH74562 EB17 to EB19 SH74593 EB17 to **EB23** Added the following blocks Block name Read : Start address – Last address Program/erase : Start address – Last address **EB20 H'0010 0000 – H'0011 FFFF H'FD90 0000 – H'FD91 FFFF** **EB21 H'0012 0000 – H'0013 FFFF H'FD92 0000 – H'FD93 FFFF** **EB22 H'0014 0000 – H'0015 FFFF H'FD94 0000 – H'FD95 FFFF** **EB23 H'0016 0000 – H'0017 FFFF H'FD96 0000 – H'FD97 FFFF** Please refer to Appendix D.2.
12-4	• 12.1 Overview : Protection modes Product Description SH74562 This MCU supports two modes to protect memory against programming or erasure: hardware protection by the levels on the FWE and mode pins and software protection by the FENTRY0 bit or lock bit settings. The FENTRY0 bit enables or disables ROM programming or erasure by the FCU. SH74593 This MCU supports two modes to protect memory against programming or erasure: hardware protection by the levels on the FWE and mode pins and software protection by the **FENTRY1 and** FENTRY0 bits or lock bit settings. The **FENTRY1 and** FENTRY0 bits enable or disable ROM programming or erasure by the FCU.
12-7	• 12.3.2 Flash Access Status Register (FASTAT) : Description of ROMAE bit Product Conditions for setting to "1" SH74562 - A read access command is issued to ROM read addresses H'0000 0000 to H'000F FFFF while the FENTRYR register value is not H'0000. - An access command is issued to an address other than ROM program/erase addresses H'FD80 0000 to H'FD8F FFFF when the user boot MAT is selected. SH74593 **- A read access command is issued to ROM program/erase addresses H'FD90 0000 to H'FD97 FFFF while the FENTRY1 bit in the FENTRYR register is "1" in ROM P/E normal mode.** **- An access command is issued to ROM program/erase addresses H'FD90 0000 to H'FD97 FFFF while the FENTRY1 bit in the FENTRYR register is "0".** - A read access command is issued to ROM read addresses H'0000 0000 to **H'0017 FFFF** while the FENTRYR register value is not H'0000. - An access command is issued to an address other than ROM program/erase addresses H'FD8F 0000 to **H'FD80 7FFF** when the user boot MAT is selected. Please refer to Appendix D.3.

Page	Description
12-12	• 12.3.6 Flash P/E Mode Entry Register (FENTRYR) Product Description SH74562 To specify the P/E mode for the ROM so that the FCU can accept commands, set the FENTRY0 bit to "1". SH74592 To specify the P/E mode for the ROM so that the FCU can accept commands, set **either of bits FENTRY1 and FENTRY0** to "1".
	• 12.3.6 Flash P/E Mode Entry Register (FENTRYR) : Description of FEKEY bit Product Description SH74562 These bits enable or disable FENTRY0 bit modification. The data written to these bits are not retained. These bits are always read as "0". H'AA: Enable FENTRY0 bit modification. Other than H'AA: Disable FENTRY0 bit modification. SH74593 These bits enable or disable bit modification **of FENTRY1 and** FENTRY0. The data written to these bits are not retained. These bits are always read as "0". H'AA: Enable bit modification **of FENTRY1 and** FENTRY0. Other than H'AA: Disable bit modification **of FENTRY1 and** FENTRY0.
12-12	• 12.3.6 Flash P/E Mode Entry Register (FENTRYR) : Description of FENTRY1 bit Product R W Description SH74562 0 0 ROM P/E Mode Entry Bit 1 This bit is not supported by the MCU. Always write "0" to FENTRY1. SH74593 **R W** ROM P/E Mode Entry Bit 1 **These bits specify the P/E mode for the EB20 to EB23 blocks of ROM (read addresses: H'0010 0000 to H'0017 FFFF; program/erase addresses: H'FD90 0000 to H'FD97 FFFF).** **0: The block of ROM from EB20 to EB23 (0.5Mbytes) is in read mode** **1: The block of ROM from EB20 to EB23 (0.5Mbytes) is in P/E mode** **Programming is enabled when the following conditions are all satisfied:** **- The FWE bit in the FPMON register is "1".** **- The FRDY bit in the FSTATR0 register is "1".** **- H'AA is written to the FEKEY bit in word access.** **[Conditions for clearing to "0"]** **- The FRDY bit in the FSTATR0 register becomes "1" and the FWE bit in the FPMON register becomes "0".** **- This register is written to in byte access.** **- A value other than H'AA is written to the FEKEY bit in word access.** **- "0" is written to FENTRY1 while the write enabling conditions are satisfied.** **- The FENTRYR register is written to while the FENTRYR register is not H'0000 and the write enabling conditions are satisfied.** **[Condition for setting to "1"]** **- "1" is written to the FENTRY1 bit while the write enabling conditions are satisfied and the FENTRYR register is H'0000.** Please refer to Appendix D.4.
12-19	• Table 12.5 FCU Command Format: Description of Legend Product RA: ROM program/erase address SH74562 When the FENTRY0 bit is "1": An address in the range from H'FD80 0000 to H'FD8F FFFF SH74593 When the FENTRY0 bit is "1": An address in the range from H'FD80 0000 to H'FD8F FFFF **When the FENTRY1 bit is "1": An address in the range from H'FD90 0000 to H'FD97 FFFF**

Page	Description
12-20	• Figure 12.6 FCU Mode Transition Diagram (ROM-Related Modes) Product Transition from “ROM read mode” to “ROM P/E mode” SH74562 FENTRYR = H’0001 SH74593 FENTRYR = H’0001 **or FENTRYR = H’0002** Please refer to Appendix D.5.
12-20	• 12.6.2 Conditions for FCU Command Acceptance : (1) ROM read mode Product Description SH74562 This MCU switches to this mode when the FENTRY0 bit in the FENTRYR register is set to "0". SH74593 This MCU switches to this mode when **both the FENTRY1 and FENTRY0 bits** in the FENTRYR register are set to "0".
12-20	• 12.6.2 Conditions for FCU Command Acceptance : (2) ROM P/E mode Product Description SH74562 The FCU enters this mode when the FENTRY0 bit is set to "1". Table 12.6 lists the commands that the FCU accepts. The high-speed ROM readout operation cannot be used in this mode. Although read access to locations H'FD80 0000 to H'FD8F FFFF is illegal, undefined values will be returned. To read the ROM data, the FCU must switch to ROM read mode. If a peripheral-bus read access to a location from H'FD80 0000 to H'FD8F FFFF is issued in the state where the FENTRY0 bit is "1", a ROM access error will occur and the FCU will switch to the command-locked state. (See section 12.8.3, Error Protection.) SH74593 The FCU enters this mode when **either the FENTRY1 or FENTRY0 bit** is set to "1". Table 12.6 lists the commands that the FCU accepts. The high-speed ROM readout operation cannot be used in this mode. Although read access to locations H'FD80 0000 to **H'FD97 FFFF** is illegal, undefined values will be returned. To read the ROM data, the FCU must switch to ROM read mode. **If a peripheral-bus read access to a location from H'FD90 0000 to H'FD97 FFFF is issued in the state where the FENTRY1 bit is "1", or** If a peripheral-bus read access to a location from H'FD80 0000 to H'FD8F FFFF is issued in the state where the FENTRY0 bit is "1", a ROM access error will occur and the FCU will switch to the command-locked state. (See section 12.8.3, Error Protection.)
12-22	• Figure 12.7 Command State Transitions in ROM Read Mode and P/E mode Product Transition from “ROM read mode” to “ROM P/E mode” SH74562 FENTRYR = H’0001 SH74593 FENTRYR = H’0001 **or FENTRYR = H’0002** Please refer to Appendix D.6.
12-23	• 12.6.3 FCU Command Usage : (1) Methods for switching to ROM P/E mode Product Description SH74562 For an application to execute ROM related FCU commands, it is necessary to set the FCU to ROM P/E mode by setting the FENTRY0 bit in the FENTRYR register. (See section 12.6.2, Conditions for FCU Command Acceptance.) To use ROM related FCU commands, set the FENTRY0 bit to "1". See section 12.3.6, Flash P/E Mode Entry Register (FENTRYR) for the conditions for setting the FENTRY0 bit. SH74593 For an application to execute ROM related FCU commands, it is necessary to set the FCU to ROM P/E mode by setting **bits FENTRY1 and FENTRY0** in the FENTRYR register. (See section 12.6.2, Conditions for FCU Command Acceptance.) To use FCU commands for the first **1-Mbyte and second 0.5-Mbyte** sections of ROM, set **bits FENTRY1 and FENTRY0 to the corresponding state**. See section 12.3.6, Flash P/E Mode Entry Register (FENTRYR) for the conditions for setting **bits FENTRY1 and FENTRY0**.

Page	Description
12-23	• Figure 12.8 Procedure for Transition to ROM P/E Mode Product Specifies “ROM P/E mode” SH74562 To set FENTRY0 to 1 : Write H’AA01 SH74593 **To set FENTRY1 to 1 : Write H’AA02** To set FENTRY0 to 1 : Write H’AA01 Please refer to Appendix D.7.
12-24	• 12.6.3 FCU Command Usage : (2) Entering ROM Read Mode Product Description SH74562 To enable high-speed ROM read access over the SuperHyway bus, it is necessary to set the FCU to ROM read mode by clearing the FENTRY0 bit in the FENTRYR register. SH74593 To enable high-speed ROM read access over the SuperHyway bus, it is necessary to set the FCU to ROM read mode by clearing **bits FENTRY1 and FENTRY0** in the FENTRYR register.
12-25	• 12.6.3 FCU Command Usage : (3) Programming Product Description SH74562 The addresses that can be specified in the first to 131st cycles depend on the setting of the FENTRY0 bit in the FENTRYR register. An address in the range from H'FD80 0000 to H'FD8F FFFF is can be specified when the FENTRY0 bit is set to "1". If a command is issued while an illegal combination of the FENTRY0 bit value and addresses is specified, the FCU detects an error and enters command-locked state (see section 12.8.3, Error Protection). SH74593 The addresses that can be specified in the first to 131st cycles depend on the setting of **bits FENTRY1 and FENTRY0** in the FENTRYR register. **An address in the range from H'FD90 0000 to H'FD97 FFFF is can be specified when the FENTRY1 bit is set to "1", or** an address in the range from H'FD80 0000 to H'FD8F FFFF is can be specified when the FENTRY0 bit is set to "1". If a command is issued while an illegal combination of **FENTRY1 and** FENTRY0 bit values and addresses is specified, the FCU detects an error and enters command-locked state (see section 12.8.3, Error Protection).
12-33	• 12.8.1 Hardware Protection : (1) Protection through FWE Pin Product Description SH74562 In this state,"1" cannot be written to the FENTRY0 bit in the FENTRYR register; that is, ROM P/E mode cannot be entered, which prevents the ROM from being programmed or erased. When the FRDY bit is set to "1" and the FWE pin is "L" level, the FCU clears the FENTRY0 bit to disable ROM programming and erasure. SH74593 In this state,"1" cannot be written to **bits FENTRY1 and FENTRY0** in the FENTRYR register; that is, ROM P/E mode cannot be entered, which prevents the ROM from being programmed or erased. When the FRDY bit is set to "1" and the FWE pin is "L" level, the FCU clears **bits FENTRY1 and FENTRY0** to disable ROM programming and erasure.
12-33	• 12.8.2 Software Protection : (1) FENTRYR Protection Product Description SH74562 When the FENTRY0 bit is "0", the EB00 to EB19 blocks of ROM (read addresses: H'0000 0000 to H'000F FFFF, program/erase addresses: H'FD80 0000 to H'FD8F FFFF) goes to ROM read mode. SH74593 **When the FENTRY1 bit in the FENTRYR register is "0", the EB20 to EB23 blocks of ROM (read addresses: H'0010 0000 to H'0017 FFFF, program/erase addresses: H'FD90 0000 to H'FD97 FFFF) goes to ROM read mode.** When the FENTRY0 bit is "0", the EB00 to EB19 blocks of ROM (read addresses: H'0000 0000 to H'000F FFFF, program/erase addresses: H'FD80 0000 to H'FD8F FFFF) goes to ROM read mode.

Page	Description
12-34	• Table 12.7 Error Protection Types Product ROM access error SH74562 - A read access command has been issued to addresses H'0000 0000 to H'000F FFFF while the FENTRYR register value is not H'0000. SH74593 - **A read access command has been issued to addresses H'FD90 0000 to H'FD97 FFFF while FENTRY1 = "1" in ROM P/E normal mode.** - A read access command has been issued to addresses H'0000 0000 to **H'0017 FFFF** while the FENTRYR register value is not H'0000. Please refer to Appendix D.8.
13-1 13-2	• 13.1 Overview • Figure 13.2 Address Space : Descriptions of 29-bit physical address space (area 6) Product SHwyRAM Capacity (Start address – Last address) SH74562 256 Kbytes(H'1800 0000 – H'1803 FFFF) SH74593 **512** Kbytes(H'1800 0000 – **H'1807 FFFF**) Please refer to Appendix E.
13-1	• Figure 13.1 Block Diagram of SHwyRAM : Descriptions of Memory block Product Page number [Capacity] SH74562 Page 3 [64 KB] SH74593 **Page 7** [64 KB]
13-2	• Figure 13.2 Address Space Product Page SH74562 Page 0 to Page 3 SH74593 Page 0 to **Page 7** Added the following pages Page Address (29-bit physical address) **Page 4** **H'1804 0000 – H'1804 FFFF** **Page 5** **H'1805 0000 – H'1805 FFFF** **Page 6** **H'1806 0000 – H'1806 FFFF** **Page 7** **H'1807 0000 – H'1807 FFFF** Please refer to Appendix E.
14-1	• Table 14.1 Relation between Input Frequency and Input Clock • Figure 14.1 Block Diagram of CPG Product PLL frequency multiplier (input to CPU) SH74562 X8. SH74593 X**12**. Please refer to Appendix F.
14-1	• Table 14.1 Relation between Input Frequency and Input Clock Product CPU clock(MHz) SH74562 160. SH74593 **240** Please refer to Appendix F.
15-60	• Table 15.9 Minimum of Interrupt Response Time: Response time (Minimum) Product NMI IRQ Peripheral Module Remarks SH74562 40Icyc + S × Icyc 36Icyc + S × Icyc 32Icyc + S × Icyc When Icyc:Scyc: Pcyc = 4:2:1 SH74593 **55**Icyc + S × Icyc **49**Icyc + S × Icyc **43**Icyc + S × Icyc When Icyc:Scyc: Pcyc = **6**:2:1 Please refer to Appendix G.

Page	Description
28-1	• Table 28.1 DRIi Overview Product Access areas SH74562 All SHwyRAM areas (up to 256 Kbytes) SH74593 All SHwyRAM areas (up to **512** Kbytes) Please refer to Appendix H.1.
28-46	• 28.3.23 DRIi Address Reload Registers 0 and 1 (DRIiADR0RLD and DRIiADR1RLD) : Description of DRIADmRLD bit Product Description SH74562 Address Bits 18 to 2 Reload Value (256-Kbyte area) SH74593 Address Bits 18 to 2 Reload Value (**512**-Kbyte area) Please refer to Appendix H.2.
28-47	• 28.3.24 DRIi Address Counters 0 and 1 (DRIiADR0CT and DRIiADR1CT) : Description of DRIADn bit Product Description SH74562 Destination Address Bits 18 to 2 (256-Kbyte area) SH74593 Destination Address Bits 18 to 2 (**512**-Kbyte area) Please refer to Appendix H.3.
29-1	• Table 29.1 DRO Module Overview Product Access area SH74562 SHwyRAM area (256 Kbytes) SH74593 SHwyRAM area (**512** Kbytes) Please refer to Appendix I.
38-1	• Table 38.1 Absolute Maximum Ratings Product Power dissipation (Pd) SH74562 1000 mW ,Ta = –40°C to +125°C SH74593 **1200** mW ,Ta = –40°C to +**105**°C Please refer to Appendix J.1.
38-1	• Table 38.1 Absolute Maximum Ratings Product Operating temperature (Topr) SH74562 –40°C to +125°C SH74593 –40°C to +**105**°C Please refer to Appendix J.1.
38-10	• Table 38.14 DC Characteristics - Supply Current Product Core supply current (Vdd power supply) SH74562 IDD is 480 mA(maximum) Ick = 160 MHz SH74593 IDD is **560** mA(maximum) Ick = **240** MHz Please refer to Appendix J.2.
38-11	• 38.3 AC Characteristics: Descriptions of the timing conditions Product The timing conditions of AC Characteristics SH74562 Ta = –40°C to +125°C SH74593 Ta = –40°C to +**105**°C Please refer to Appendix J.3.

Appendix A

Section 1 Overview

1.2 Product Line Overview

Table 1.2 lists the products.

Table 1.2 Products

Product	Model	ROM Capacity	RAM Capacity	Package	FlexRay
SH74552	R5F74552KBG	1 Mbyte	IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: 256 Kbytes	PRBG0176GA-A	Yes
SH74562	R5F74562KBG				No
SH74572	R5F74572LBG				Yes
SH74593	**R5F74593LBG**	**1.5** Mbyte	IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwyRAM: **512** Kbytes		**Yes**

Appendix B

Section 1 Overview

1.4 Pin Arrangement

Figure 1.2 shows the pin arrangement.

Position of pin A1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	Vss (N.C.)	PG0/ MOSI0/ TO40	PF5/ SCL/ (CTX3)	PF1/ CTX0	DET3OR5	Vss	PL8/ TIA14/ IRQ7/ DREQ3	PL6/ TIA12/ (TIF1A)	PH15/ DROD7/ TO37/ DDC15	PH13/ DROD5/ (TO35)/ DDC13	PH9/ DROD1/ (TO31)/ DDC09/ CTS2#	PH5/ DROD13/ TO25/ DDC05/ TIA01	PH2/ DROD10/ TO22/ DDC02/ TIF1A	PH0/ DROD8/ TO20/ DDC00/ TIF0A	Vss (N.C.)	A
B	PG1/ MISO0/ TO41	PG2/ RSPCK0/ TO42	PG3/ TO43/ SSL00/ (IRQ7)	PF4/ SDA/ (CRX3)	PF0/ CRX0	ASEBRK#/ BRKACK	PL9/ TIA15/ AUDREVT#	PL5/ TIA11/ (TIF0B)	PL2/ DROWR	PH12/ DROD4/ TO34/ DDC12	PH8/ DROD0/ (TO30)/ DDC08/ RTS2#	PH4/ DROD12/ TO24/ DDC04/ TIA00	PH1/ DROD9/ TO21/ DDC01/ TIF0B	PH3/ DROD11/ TO23/ DDC03/ TIF1B	PK14/ AUDRSYN#	B
C	PG4/ IRQ2/ TO44/ SSL01	Vss	WDTOVF#	Vdd	Vdd	Vdd	PL4/ TIA10/ (TIF0A)	Vss	Vcc	PH14/ DROD6/ (TO36)/ DDC14/ IRQ1	PH10/ DROD2/ (TO32)/ DDC10	PH6/ DROD14/ TO26/ DDC06/ TIA02	PK12/ AUDRD3	PK13/ AUDRCLK	PK11/ AUDRD2	C
D	FWE	RESET#	Vss	Vss	Vdd	Vdd	PL3/ IRQ6	Vss	Vcc	PH11/ DROD3/ (TO33)/ DDC11	PH7/ DROD15/ (TO27)/ DDC07/ TIA03	PK8/ DREQ2	PK9/ AUDRD0/ RTS3#	PK10/ AUDRD1/ CTS3#	PK6/ TXD3	D
E	MD1	NMI	Vss	Vss								Vss	PK0/ IRQ5/ SSL10	PK5/ DINC4/ RXD3	PJ14/ TXD1/ MOSI1	E
F	XTAL	EXTAL	Vss	Vss								Vcc	PJ10/ RXD0/ PWMOFF4/ AD0TRG#	PJ15/ SCK1/ PSPCK1	PJ13/ RXD1/ MISO1	F
G	PLLVss	PLLVcc	MD0	MPMD								PJ1/ (CTX0)/ FTXA	PJ7/ CTX3/ TIF2B/ TXD2	PJ12/ SCK0/ TCLKB/ (IRQ0)	PJ11/ TXD0/ AD0END	G
H	TCK	TMS	MD2	TRST#								PJ0/ (CRX0)/ FRXA	PJ4/ CRX2/ FTXENA/ CTS0#	PJ6/ CRX3/ TIF2A/ RXD2/ TIA04	PJ5/ CTX2/ FTXENB/ SCK2	H
J	PD1/ PDIDATA1	TDO	TDI	Vss								PN1/ AD1IN1	PN0/ AD1IN0	PJ3/ CTX1/ FTXB/ RTS0#	PJ2/ CRX1/ FRXB	J
K	PD4/ PDIDATA4	PD3/ PDIDATA3	Vss	Vss								PN4/ AD1IN4	PN5/ AD1IN5	AVss	AVcc	K
L	PD8/ PDIDATA8	PD7/ PDIDATA7	Vcc	Vcc								PM0/ AD0IN0	AVss	AVREFL	AVREFH	L
M	PD9/ PDIDATA9	PD6/ PDIDATA6	PD0/ PDIDATA0	Vss	Vss	Vss	Vdd	Vdd	PC6/ CLKOUT/ TO36	Vcc	Vss	AVss	PM4/ AD0IN4	AVREFL	AVREFH	M
N	PD10/ PDIWR	PD5/ PDIDATA5	PA4/ TO04/ DDB04	PA7/ TO07/ DDB07	PA10/ TO12/ DDB10/ PSLDATA0	PA11/ TO13/ DDB11/ PSLDATA1	Vdd	Vdd	PC1/ TO31/ MISO2	Vcc	Vss	PM2/ AD0IN2	PM6/ AD0IN6	PM9/ AD0IN9	AVss	N
P	PD2/ PDIDATA2	PA3/ TO03/ DDB03	PA0/ TO00/ DDB00	PA2/ TO02/ DDB02	PA6/ TO06/ DDB06	PA9/ TO11/ DDB09/ PSLCLKA	PA13/ TO15/ DDB13/ PSLDATA3	PB1/ PWMOFF1/ DINB1	PC0/ TO30/ MOSI2/ (IRQ6)	PC3/ TO33/ SSL20/ IRQ0	PM15/ AD0IN15	PM13/ AD0IN13	PM11/ AD0IN11	PM8/ AD0IN8	AVcc	P
R	Vss (N.C.)	PE15/ TO27/ PSLCLR	PA1/ TO01/ DDB01	PA5/ TO05/ DDB05	PA8/ TO10/ DDB08/ PSLCLKB	PA12/ TO14/ DDB12/ PSLDATA2	PB0/ PWMOFF0/ DINB0	PB3/ PWMOFF3/ DINB3	PC2/ TO32/ RSPCK2/ DREQ0	PC5/ TO35	PC14	PM14/ AD0IN14	PM12/ AD0IN12	PM10/ AD0IN10	AVcc (N.C.)	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 1.2 Pin Arrangement (Top Transparent View)

Appendix C

Appendix C.1

Section 11 Address Space

For details on the P0/U0 area to the P4 area, see figures 11.2 to 11.6.

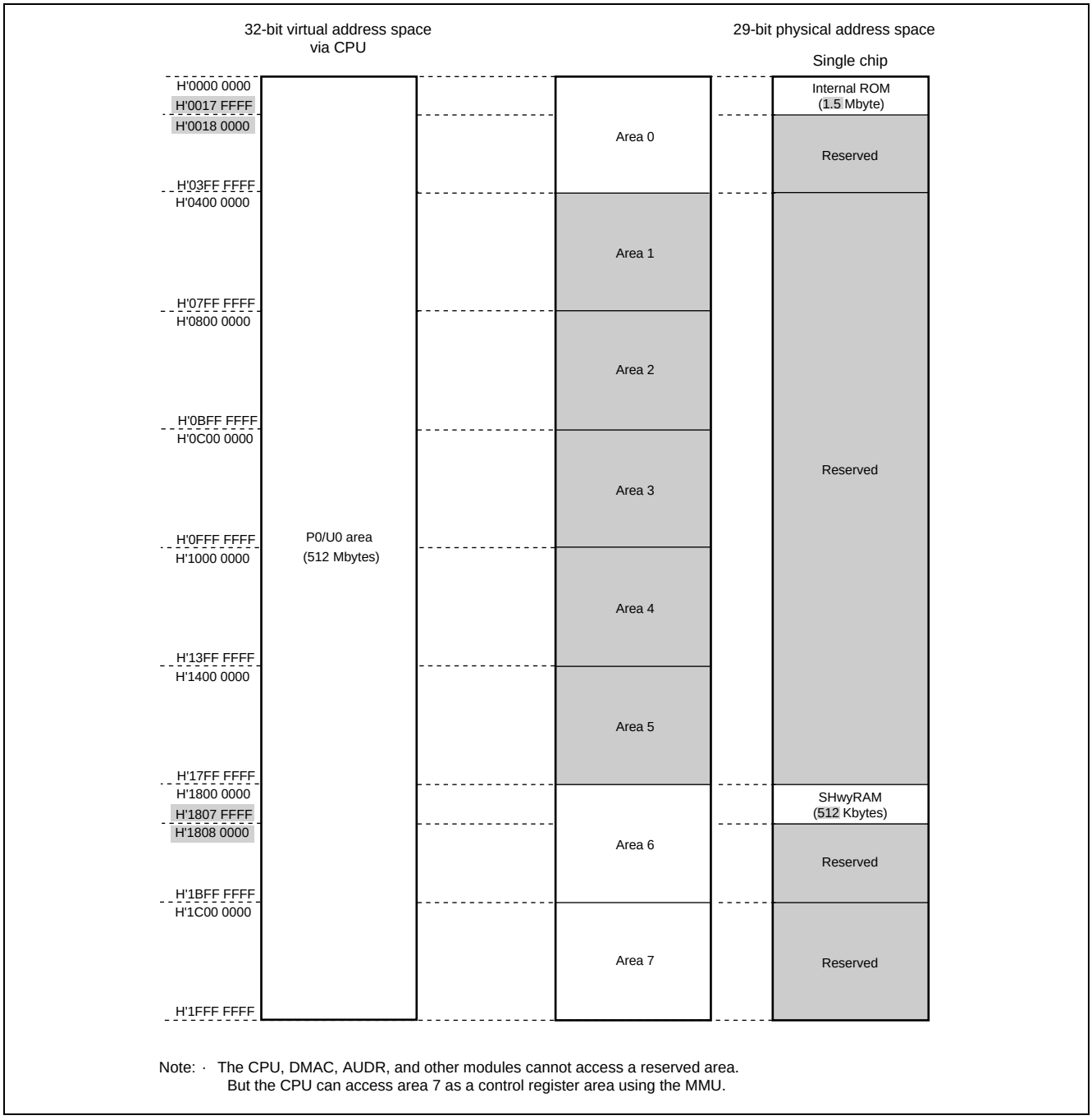


Figure 11.2 Address Space (P0/U0 Area)

Appendix C.2

Section 11 Address Space

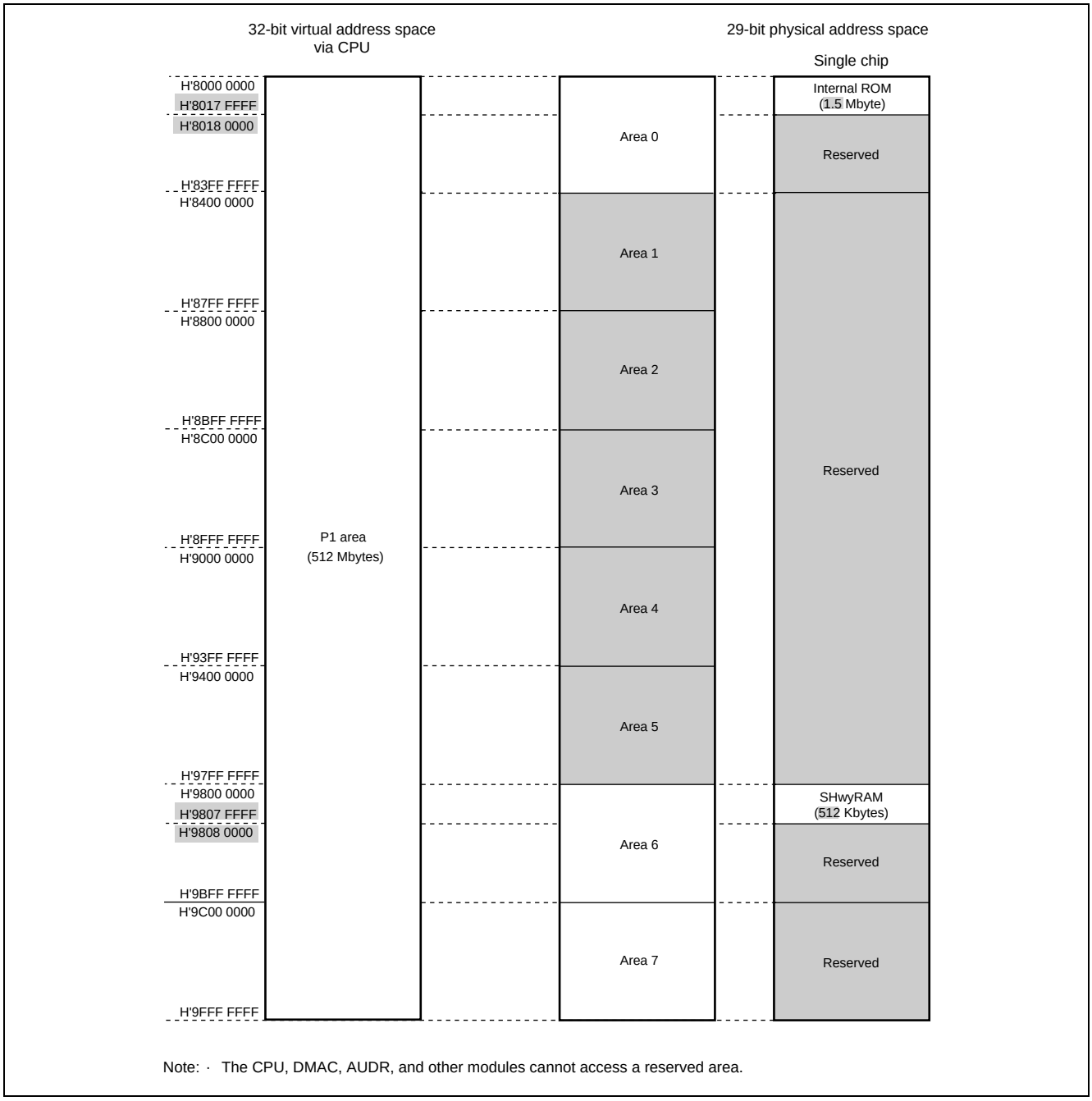


Figure 11.3 Address Space (P1 Area)

Appendix C.3

Section 11 Address Space

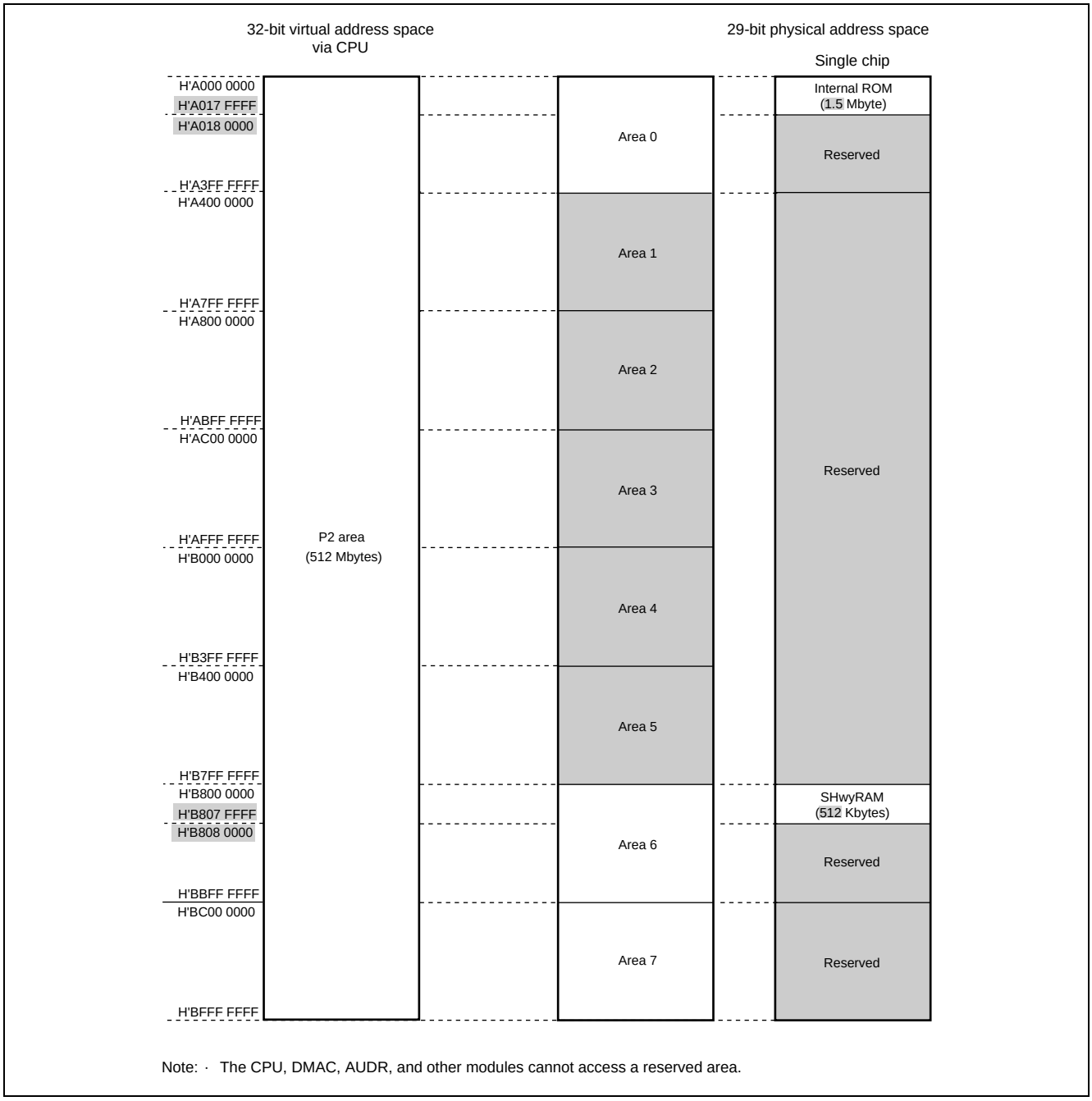


Figure 11.4 Address Space (P2 Area)

Appendix C.4

Section 11 Address Space

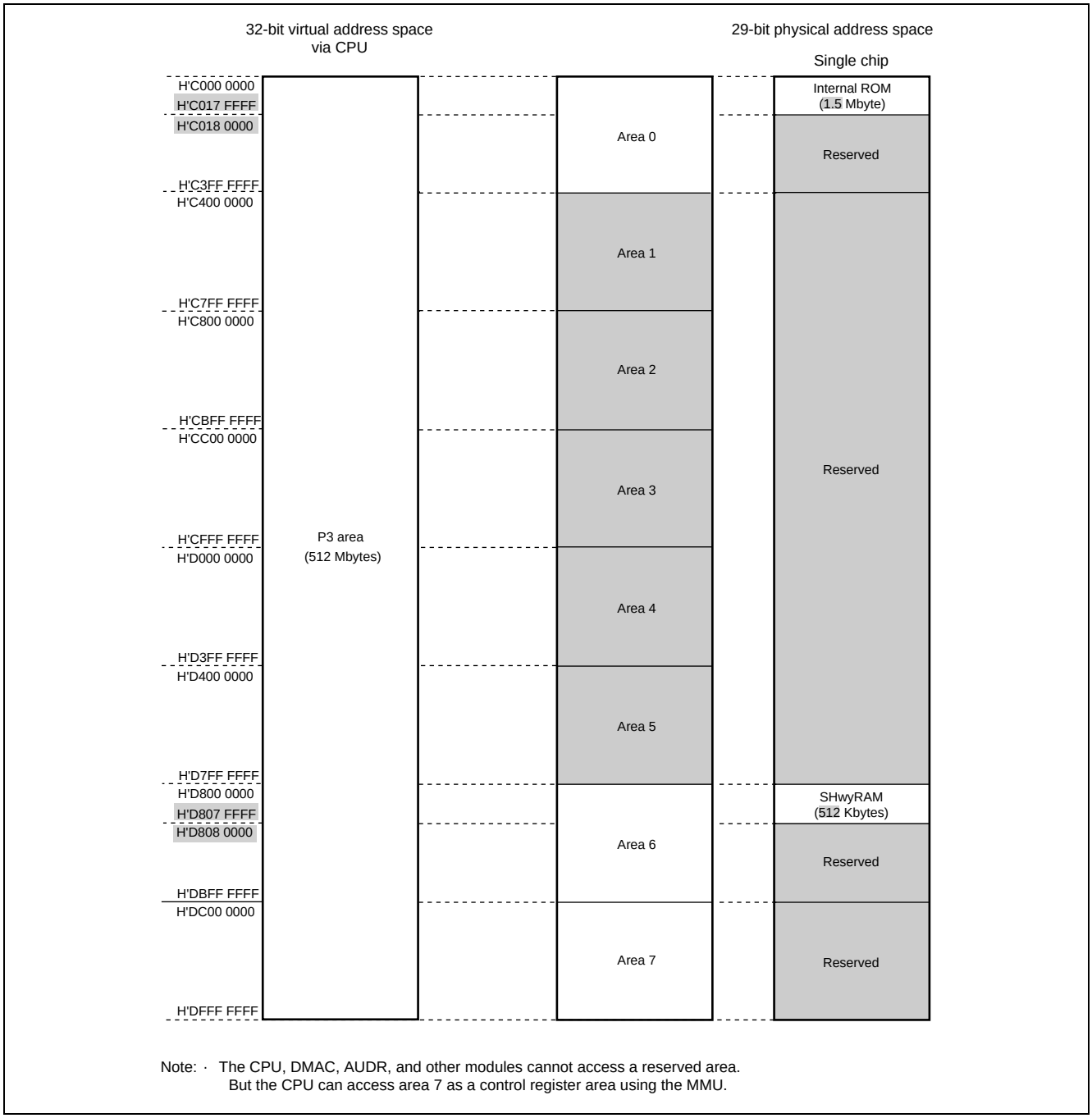


Figure 11.5 Address Space (P3 Area)

Appendix D

Section 12 ROM

Appendix D.1

12.1 Overview

- Two types of flash-memory MATs

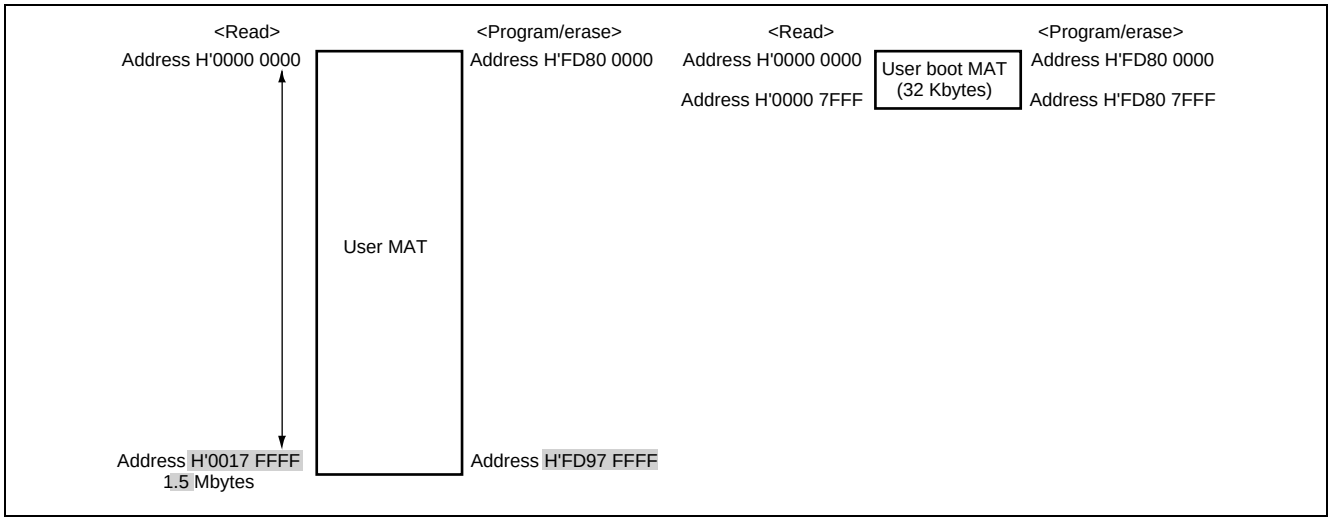


Figure 12.1 Memory MAT Configuration in ROM

Appendix D.2

12.1 Overview

- Programming/erasing unit
  Figure12.3 shows the block allocation of the user MAT.

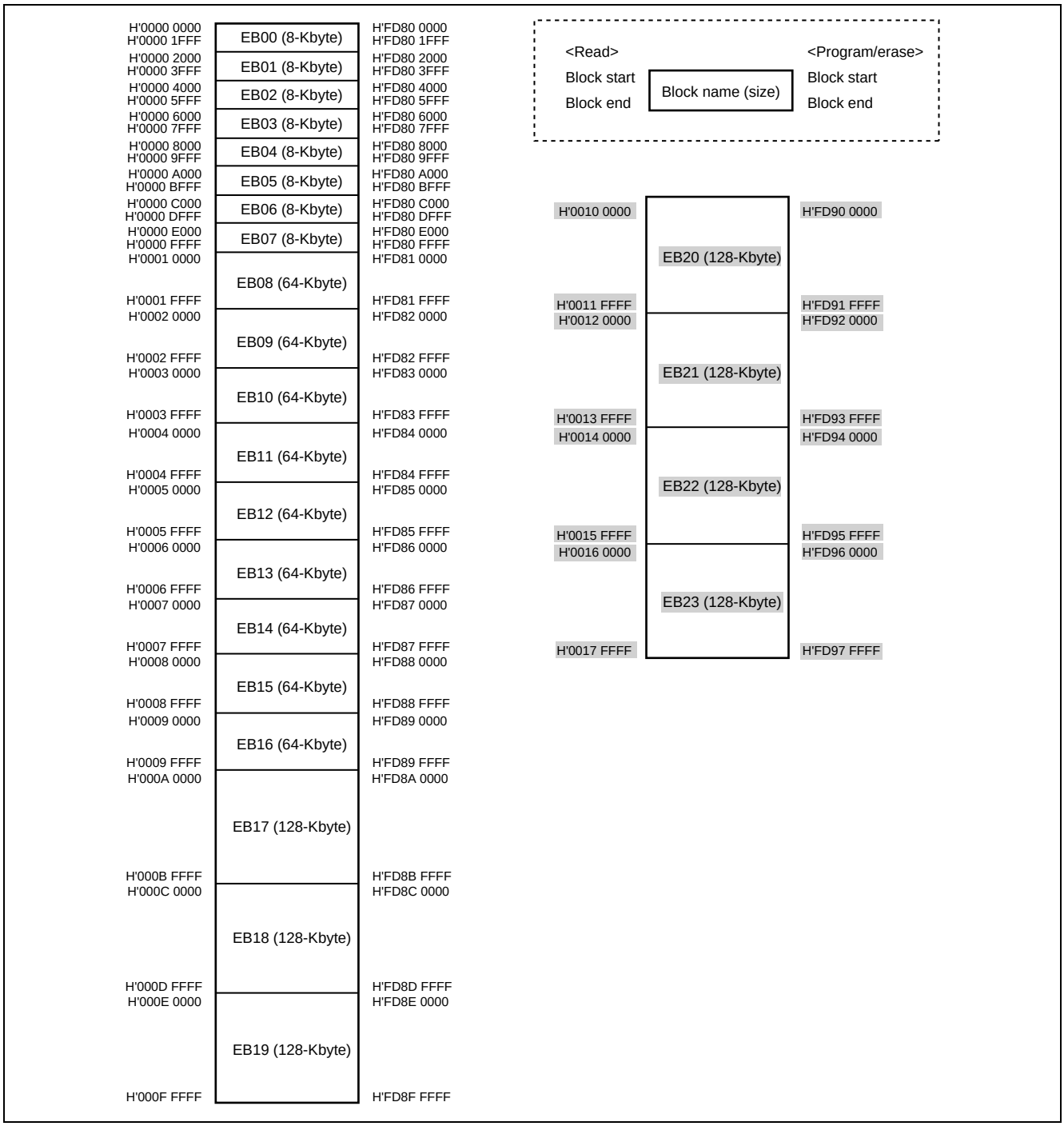


Figure 12.3 User MAT and Block Allocation

Appendix D.3

12.3.2 Flash Access Status Register (FASTAT)

The FASTAT register indicates the access error status for the ROM. If any bit in the FASTAT register is set to "1", the FCU enters command-locked state (see section 12.8.3, Error Protection). To cancel a command-locked state, set the FASTAT register to H'10, and then issue a status-clear command to the FCU.

Flash Access Status Register (FASTAT) <P4 address: location H'FDFF A810>

Bit:	7	6	5	4	3	2	1	0
	ROMAE	—	—	CMDLK	—	—	—	—
After Reset:	0	0	0	0	0	0	0	0

<After Reset: H'00>

Bit	Abbreviation	After Reset	R	W	Description
7	ROMAE	0	R	*1	Access Error Bit Indicates whether or not a ROM access error has been generated. If this bit becomes "1", the ILGLERR bit in the FSTATR0 register is set to "1" and the FCU enters a command-locked state. 0: No ROM access error has occurred. 1: A ROM access error has occurred. [Condition for clearing to "0"] • When "0" is written after reading out ROMAE with the value "1". [Conditions for setting to "1"] • **A read access command is issued to ROM program/erase addresses H'FD90 0000 to H'FD97 FFFF while the FENTRY1 bit in the FENTRYR register is "1" in ROM P/E normal mode.** • A read access command is issued to ROM program/erase addresses H'FD80 0000 to H'FD8F FFFF while the FENTRY0 bit in the FENTRYR register is "1" in ROM P/E normal mode. • **An access command is issued to ROM program/erase addresses H'FD90 0000 to H'FD97 FFFF while the FENTRY1 bit in the FENTRYR register is "0".** • An access command is issued to ROM program/erase addresses H'FD80 0000 to H'FD8F FFFF while the FENTRY0 bit in the FENTRYR register is "0". • A read access command is issued to ROM read addresses H'0000 0000 to **H'0017 FFFF** while the FENTRYR register value is not H'0000. • A block erase, program, or lock bit program command is issued to ROM when the user boot MAT is selected. • An access command is issued to an address other than ROM program/erase addresses H'FD80 0000 to **H'FD80 7FFF** when the user boot MAT is selected.
6, 5	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".

Bit	Abbreviation	After Reset	R	W	Description
4	CMDLK	0	R	—	FCU Command Lock Bit Indicates whether the FCU is in command-locked state (see section 12.8.3, Error Protection). 0: The FCU is not in a command-locked state 1: The FCU is in a command-locked state [Condition for clearing to "0"] • The FCU completes the status-clear command processing while the FASTAT register is H'10. [Condition for setting to "1"] • The FCU detects an error and enters command-locked state.
3 to 0	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".

Note: *1 Writing a "0" after reading a "1" is only allowed in order to clear the flag.

Appendix D.4

12.3.6 Flash P/E Mode Entry Register (FENTRYR)

The FENTRYR register specifies the P/E mode for the ROM. Writing to the FENTRYR register is enabled only when a specified value is written to the high-order byte. Writing any other value initializes this register. To specify the P/E mode for the ROM so that the FCU can accept commands, set **either of bits FENTRY1 and FENTRY0** to "1". Note that if this register is set to a value other than H'0001 or H'0002, the ILGLERR bit in the FSTATR0 register will be set to "1" and the FCU will switch to the command-locked state.

The FENTRYR register can be initialized by a hardware reset, or setting the FRESET bit in the FRESETR register to "1".

Flash P/E Mode Entry Register (FENTRYR) <P4 address: location H'FDFF A902>

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FEKEY								—	—	—	—	—	—	FENTRY1	FENTRY0
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<After Reset: H'0000>

Bit	Abbreviation	After Reset	R	W	Description
15 to 8	FEKEY	All 0	0	W	FENTRYR Register Write Key Code Bits These bits enable or disable bit modification of **FENTRY1 and** FENTRY0. The data written to these bits are not retained. These bits are always read as "0". H'AA: Enable bit modification of **FENTRY1 and** FENTRY0. Other than H'AA: Disable bit modification of **FENTRY1 and** FENTRY0.
7 to 2	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".
1	FENTRY1	0	**R**	**W**	ROM P/E Mode Entry Bit 1 **These bits specify the P/E mode for the EB20 to EB23 blocks of ROM (read addresses: H'0010 0000 to H'0017 FFFF; program/erase addresses: H'FD90 0000 to H'FD97 FFFF).** **0: The block of ROM from EB20 to EB23 (0.5Mbytes) is in read mode** **1: The block of ROM from EB20 to EB23 (0.5Mbytes) is in P/E mode** **Programming is enabled when the following conditions are all satisfied:** • **The FWE bit in the FPMON register is "1".** • **The FRDY bit in the FSTATR0 register is "1".** • **H'AA is written to the FEKEY bit in word access.** **[Conditions for clearing to "0"]** • **The FRDY bit in the FSTATR0 register becomes "1" and the FWE bit in the FPMON register becomes "0".** • **This register is written to in byte access.** • **A value other than H'AA is written to the FEKEY bit in word access.** • **"0" is written to FENTRY1 while the write enabling conditions are satisfied.** • **The FENTRYR register is written to while the FENTRYR register is not H'0000 and the write enabling conditions are satisfied.** **[Condition for setting to "1"]** • **"1" is written to the FENTRY1 bit while the write enabling conditions are satisfied and the FENTRYR register is H'0000.**

Bit	Abbreviation	After Reset	R	W	Description
0	FENTRY0	0	R	W	ROM P/E Mode Entry Bit 0 These bits specify the P/E mode for the EB00 to EB19 blocks of ROM (read addresses: H'0000 0000 to H'000F FFFF; program/erase addresses: H'FD80 0000 to H'FD8F FFFF). 0: The block of ROM from EB00 to EB19 (1Mbyte) is in read mode 1: The block of ROM from EB00 to EB19 (1Mbyte) is in P/E mode Programming is enabled when the following conditions are all satisfied: • The FWE bit in the FPMON register is "1". • The FRDY bit in the FSTATR0 register is "1". • H'AA is written to the FEKEY bit in word access. [Conditions for clearing to "0"] • The FRDY bit in the FSTATR0 register becomes "1" and the FWE bit in the FPMON register becomes "0". • This register is written to in byte access. • A value other than H'AA is written to the FEKEY bit in word access. • "0" is written to the FENTRY0 bit while the write enabling conditions are satisfied. • The FENTRYR register is written to while the FENTRYR register is not H'0000 and the write enabling conditions are satisfied. [Condition for setting to "1"] • "1" is written to FENTRY0 while the write enabling conditions are satisfied and the FENTRYR register is H'0000.

Appendix D.5

12.6.2 Conditions for FCU Command Acceptance

Figure 12.6 is an FCU mode transition diagram.

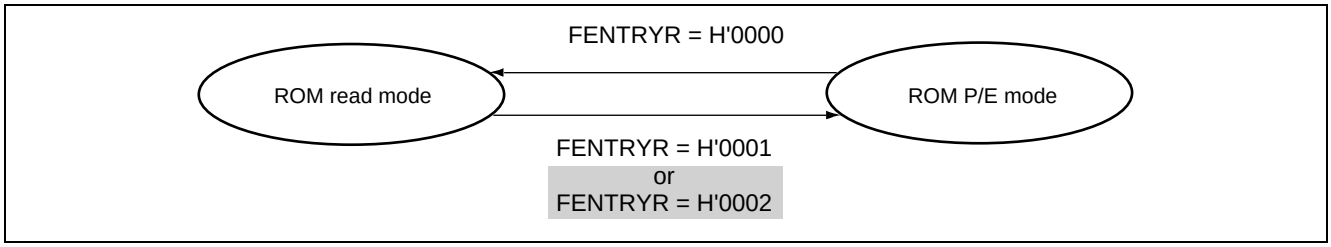


Figure 12.6 FCU Mode Transition Diagram (ROM-Related Modes)

Appendix D.6

12.6.2 Conditions for FCU Command Acceptance

(2) ROM P/E mode

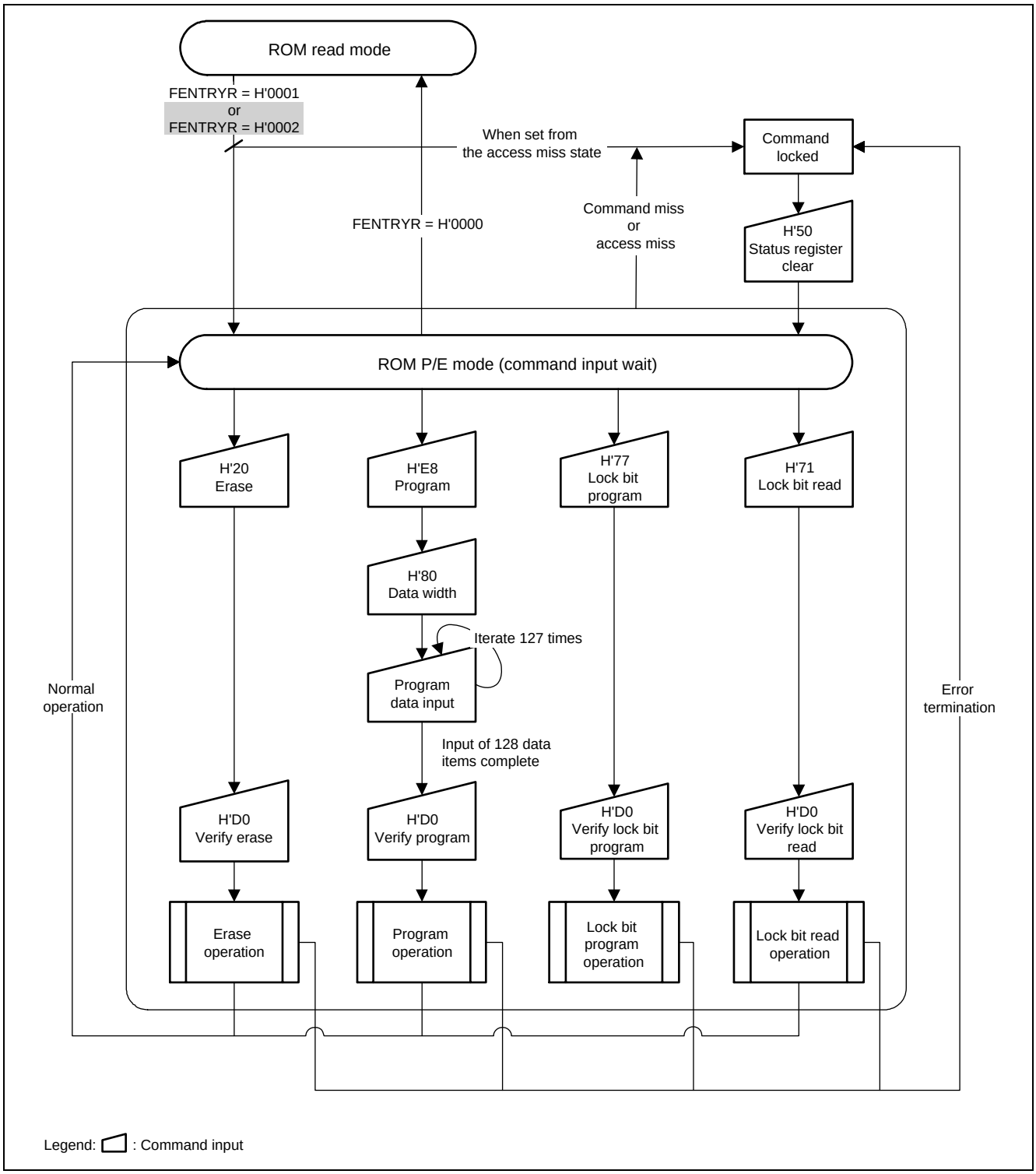


Figure 12.7 Command State Transitions in ROM Read Mode and P/E Mode

Appendix D.7

12.6.3 FCU Command Usage

(1) Methods for switching to ROM P/E mode

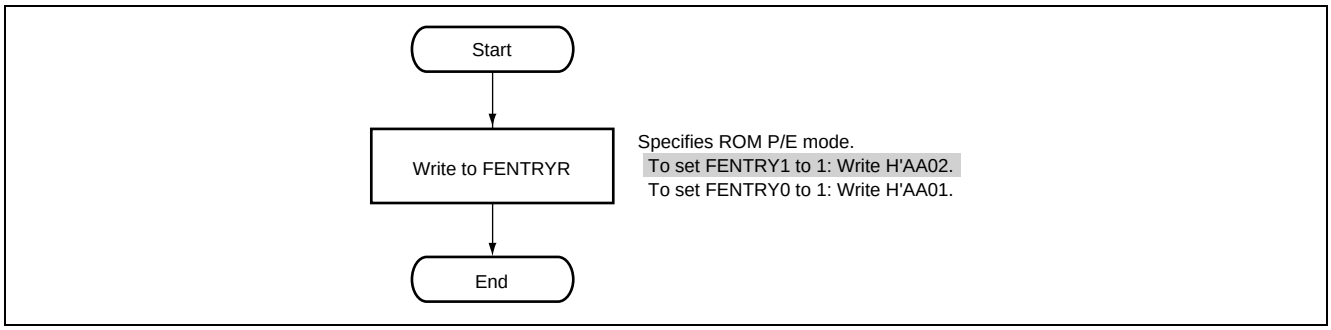


Figure 12.8 Procedure for Transition to ROM P/E Mode

Appendix D.8

12.8.3 Error Protection

Table 12.7 Error Protection Types

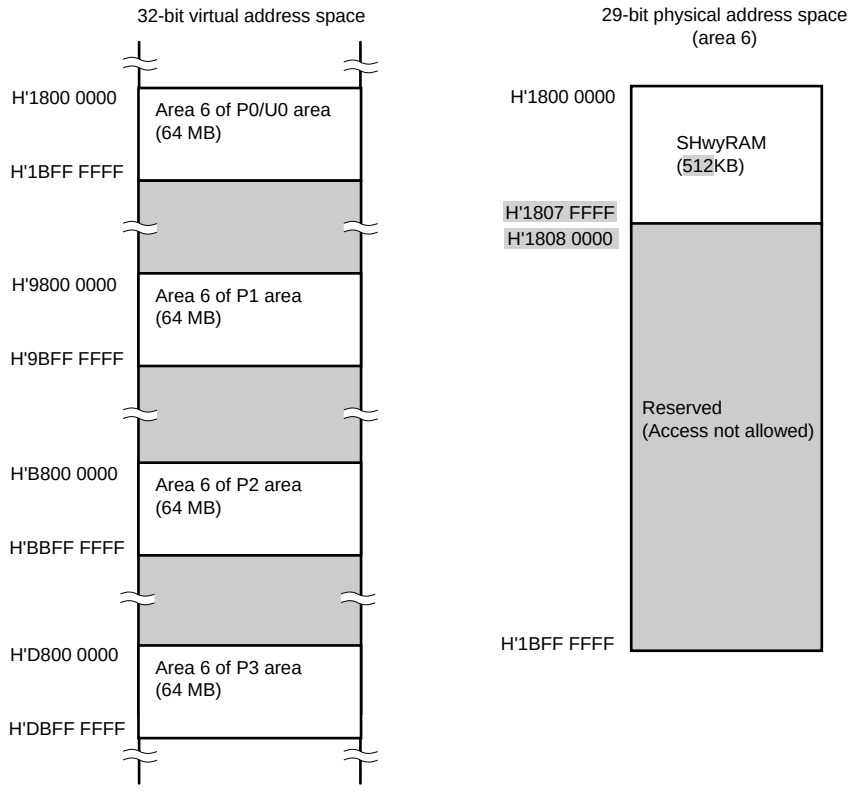
Error	Description	ILGLERR bit	ERSERR bit	PRGERR bit	FCUERR bit	FRDTCT bit	ROMAE bit
FENTRYR setting error	The key code (H'AA) has been supplied as the upper 8 bits of the FENTRYR register but the value of the lower 8 bits is other than H'01 or H'02.	1	0	0	0	0	0
Illegal command error	An undefined code has been specified in the first cycle of an FCU command.	1	0	0	0	0	0
	The value specified in the last of the multiple cycles of an FCU command is not H'D0.	1	0	0	0	0	0
	The value specified in the second cycle of a program command is not H'80.	1	0	0	0	0	0
	A command has been issued in command-locked state.	1	0/1	0/1	0/1	0/1	0/1
Erasure error	An error has occurred during erasure processing.	0	1	0	0	0	0
	A block erase command has been issued for the erasure block whose lock bit is set to "0" while the FPROTCN bit in the FPROTR register is "0".	0	1	0	0	0	0
Programming error	An error has occurred during programming processing.	0	0	1	0	0	0
	A program or lock bit program command has been issued for the erasure block whose lock bit is set to "0" while the FPROTCN bit in the FPROTR register is "0".	0	0	1	0	0	0
FCU error	An error has occurred during CPU processing in the FCU.	0	0	0	1	0	0
ROM access error	**A read access command has been issued to addresses H'FD90 0000 to H'FD97 FFFF while FENTRY1 = "1" in ROM P/E normal mode.**	**1**	**0**	**0**	**0**	**0**	**1**
	A read access command has been issued to addresses H'FD80 0000 to H'FD8F FFFF while FENTRY0 = "1" in ROM P/E normal mode.	1	0	0	0	0	1
	An access command has been issued to addresses H'FD90 0000 to H'FD9F FFFF while FENTRY1 = "0".	1	0	0	0	0	1
	An access command has been issued to addresses H'FD80 0000 to H'FD8F FFFF while FENTRY0 = "0".	1	0	0	0	0	1
	A read access command has been issued to addresses H'0000 0000 to **H'0017 FFFF** while the FENTRYR register value is not H'0000.	1	0	0	0	0	1
	A ROM programming or erasing command (program, lock bit program, or block erase command) has been issued while the user boot MAT is selected.	1	0	0	0	0	1
	An access command has been issued to an address other than the addresses for ROM programming/erasure H'FD80 0000 to H'FD80 7FFF while the user boot MAT is selected.	1	0	0	0	0	1

Appendix E

Section 13 SuperHyway RAM (SHwyRAM)

13.1 Overview

As shown in figure 13.2, the SHwyRAM is allocated to the upper 512 Kbytes of area 6 (H'1800 0000 to H'1807 FFFF in the 29-bit physical address space).



Page	Address (29-bit physical address)
Page 0	H'1800 0000 to H'1800 FFFF
Page 1	H'1801 0000 to H'1801 FFFF
Page 2	H'1802 0000 to H'1802 FFFF
Page 3	H'1803 0000 to H'1803 FFFF
Page 4	H'1804 0000 to H'1804 FFFF
Page 5	H'1805 0000 to H'1805 FFFF
Page 6	H'1806 0000 to H'1806 FFFF
Page 7	H'1807 0000 to H'1807 FFFF

Figure 13.2 Address Space

Appendix F

Section 14 Clock Generator (CPG)

14.1 Overview

Table 14.1 lists the relation between input frequency and input clock.

Table 14.1 Relation between Input Frequency and Input Clock

Input frequency (MHz)	PLL frequency multiplier (input to CPU)	CPU clock (MHz)	SHwy clock (MHz)	Peripheral clock (MHz)	Peripheral A clock (MHz)	FlexRay clock (MHz)
20	×12	240	80	40	80	80

Appendix G

Section15 Interrupt Controller (INTC)

15.5 Interrupt Response Time

Table 15.9 shows the interrupt response time, which is the interval from when an interrupt request occurs until the interrupt exception handling is started and the start instruction of the interrupt handling is fetched.

Table 15.9 Interrupt Response Time

Item		Number of State: NMI	IRQ	Peripheral Module	Remarks
Priority determination time		7 Pcyc	6 Pcyc	5Pcyc	
Wait time until the CPU finishes the current sequence			S-1 (≥ 0) × Icyc		
Interval from when interrupt exception handling begins (saving SR and PC) until a SHwy bus request is issued to fetch the start instruction of the interrupt handling			11Icyc + 1Scyc		
Response time	Total	(S + 10) Icyc + 1Scyc + 7 Pcyc	(S + 10) Icyc + 1Scyc + 6 Pcyc	(S + 10) Icyc + 1Scyc + 5Pcyc	
	Minimum	**55**Icyc + S × Icyc	**49**Icyc + S × Icyc	**43**Icyc + S × Icyc	When Icyc:Scyc: Pcyc = **6**:2:1

Legend:
Icyc: Period for one CPU clock cycle
Scyc: Period for one SHwy clock cycle
Pcyc: Period for one peripheral clock cycle
S: Number of instruction execution states

Appendix H

Section 28 Direct RAM Input Interface (DRI)

Appendix H.1

28.1 Overview

Table 28.1 lists the overview of the DRIi modules.

Table 28.1 DRIi Overview

Item	Description
Number of channels	3 channels
Operating frequency	80 MHz (when PAck = 80 MHz)
Transfer method	Clock synchronous parallel input
Access areas	All SHwyRAM areas (up to **512** Kbytes)
Maximum transfer rate	80 Mbytes/second (when the DRIi operating frequency is 80 MHz)
Minimum data acquisition period	The following are the minimum periods when the DRIi operating frequency is 80 MHz. 43.75 ns (special mode disabled and the input data bus width is 8 or 16 bits) 25 ns (special mode enabled)
Data acquisition bus width	8 or 16 bits
Event counter	16 bits × 6 counters (DEC5 to DEC0)
Bank switching function	Two banks can be specified as the data storage destination in SHwyRAM
Data acquisition edges	Either rising edges, falling edges, or both edges can be selected
Acquisition timing adjustment function	Sets the time between detection of the data acquisition edge and the acquisition operation
Decimation control function	Data can be acquired selectively using an event counter (DEC5 to DEC0)

Appendix H.2

28.3.23 DRIi Address Reload Registers 0 and 1 (DRIiADR0RLD and DRIiADR1RLD)

DRIiADR0CT and DRIiADR1CT are registers that hold counter reload values. When reload mode is selected with the DRIi transfer control register (DRIiTRMCNT) ADMD (address counter operating mode selection) bit, the corresponding DRIi address counters are reloaded with the values set in these registers when the DRIi data acquisition control register (DRIiDCAPCNT) DCPEN (acquisition enable) bit changes from "0" to "1".

Note: • These registers may only be rewritten when the DRIi data acquisition control register (DRIiDCAPCNT) DCPEN (acquisition enable) bit is in the "0" state.

DRI0 Address Reload Register 0 (DRI0ADR0RLD) <P4 address: location H'FFBF C024>
DRI1 Address Reload Register 0 (DRI1ADR0RLD) <P4 address: location H'FFBF D024>
DRI2 Address Reload Register 0 (DRI2ADR0RLD) <P4 address: location H'FFBF E024>

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	DRIAD0RLD		
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRIAD0RLD														—	—
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DRI0 Address Reload Register 1 (DRI0ADR1RLD) <P4 address: location H'FFBF C02C>
DRI1 Address Reload Register 1 (DRI1ADR1RLD) <P4 address: location H'FFBF D02C>
DRI2 Address Reload Register 1 (DRI2ADR1RLD) <P4 address: location H'FFBF E02C>

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	DRIAD1RLD		
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRIAD1RLD														—	—
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<After Reset: H'0000 0000>

Bit	Abbreviation	After Reset	R	W	Description
31 to 19	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".
18 to 2	DRIADmRLD	All 0	R	W	Address Bits 18 to 2 Reload Value (**512**-Kbyte area)
1, 0	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".

Legend: m = 0 or 1

Appendix H.3

28.3.24 DRIi Address Counters 0 and 1 (DRIiADR0CT and DRIiADR1CT)

The DRIiADR0CT and DRIiADR1CT counters are provided to specify bits A18 to A2 of the address in SHwyRAM that is the DRIi module transfer destination. Bits A31 to A19 are fixed at "0". These counters are incremented by "4" each time a DRIi transfer completes. There are two DRIi address counter operating modes, and applications can select the mode with the DRIi transfer control register (DRIiTRMCNT) ADMD bit. See the documentation of the DRIi transfer control register (DRIiTRMCNT) for details.

Notes:
- If a DRIi address counter value is a value other than an area in which SHwyRAM is located, the DRIi module will behave as though the DRIi transfers complete, but no writes of the acquired data will be performed whatsoever.
- A DRIi address counter is incremented by "4" when a DRIi transfer completed. This is performed for the one that is active at that time according to the setting of the DRIi transfer control register (DRIiTRMCNT) ADSL (address counter selection) bit.
- These registers must only be rewritten in the state where a DRIi transfer counter (DRIiTRMCT) underflow has occurred (the counter is stopped at the value H'0000 0000).

DRI0 Address Counters 0 (DRI0ADR0CT) <P4 address: location H'FFBF C028>
DRI1 Address Counters 0 (DRI1ADR0CT) <P4 address: location H'FFBF D028>
DRI2 Address Counters 0 (DRI2ADR0CT) <P4 address: location H'FFBF E028>

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	DRIAD0		
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRIAD0														—	—
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DRI0 Address Counters 1 (DRI0ADR1CT) <P4 address: location H'FFBF C030>
DRI1 Address Counters 1 (DRI1ADR1CT) <P4 address: location H'FFBF D030>
DRI2 Address Counters 1 (DRI2ADR1CT) <P4 address: location H'FFBF E030>

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	DRIAD1		
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRIAD1														—	—
After Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<After Reset: H'0000 0000>

Bit	Abbreviation	After Reset	R	W	Description
31 to 19	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".
18 to 2	DRIADn	All 0	R	W	Destination Address Bits 18 to 2 (**512**-Kbyte area)
1, 0	—	All 0	0	0	Reserved Bits These bits are always read as "0". The write value should always be "0".

Legend: n = 0 or 1

Appendix I

Section 29 Direct RAM Output Interface (DRO)

29.1 Overview

Table 29.1 lists the overview of the DRO module.

Table 29.1 DRO Module Overview

Item	Description
Transfer method	Parallel strobed output
Access area	SHwyRAM area (**512** Kbytes)
Output data width	Either 8-bits or 16-bits
Maximum transfer clock	10 MHz
Maximum transfer rate	20 Mbytes/s (when 16 bits is selected, Pck = 40MHz)
Strobe polarity	Either "H" active or "L" active may be selected.
Timing adjustment function	The setup and hold times can be programmed in 1Pck units relative to the strobe signal edge.
Interrupt request	An interrupt request is generated after a prespecified number of data items have been output.

Appendix J

Section 38 Electrical Characteristics

Appendix J.1

38.1 Absolute Maximum Ratings

Table 38.1 shows the absolute maximum ratings.

Table 38.1 Absolute Maximum Ratings

Item		Symbol	Rating	Unit	Remarks
Power supply voltage	V_{dd}	Vdd	–0.3 to +2.0	V	
	Vcc, PLLVcc	Vcc	–0.3 to +6.5	V	
Input voltage	Vcc power supply related pins	Vin	–0.3 to Vcc +0.3	V	
Analog supply voltage		AVcc	–0.3 to +6.5	V	
Analog reference voltage		AVREFH	–0.3 to AVcc +0.3	V	AVREFH > AVREFL
		AVREFL	–0.3 to AVss +0.3	V	
Analog input voltage		VAN	–0.3 to AVcc +0.3	V	
Vss differential voltage		Vss – PLLVss	–0.1 to +0.1	V	
		Vss – AVss	–0.1 to +0.1	V	
		PLLVss – AVss	–0.1 to +0.1	V	
Maximum input current per pin*2 (per pin)	Digital input pins	Imax	–20 to +20	mA	
	Analog input pins	Imax	–20 to +20	mA	
Power dissipation		Pd	**1200**	mW	Ta = –40°C to +**105**°C
Operating temperature*1		topr	–40 to +**105**	°C	
Storage temperature		tstg	–55 to +125	°C	Before assembly

[Usage Notes]

Operating the MCU in excess of the absolute maximum ratings may result in permanent damage. Be sure to use the MCU in compliance with the connection of power pins, combination conditions of applicable power supply voltages, voltage applicable to each pin, and conditions of output voltage, as specified in the manual. Connecting a non-specified power supply or using the MCU at an incorrect voltage may result in permanent damage of the MCU or the system that contains the MCU.

Notes: *1 This does not guarantee that the microcomputer can operate continuously at 85°C-plus. Consult Renesas if the microcomputer is going to be used for 85°C-plus applications.

*2 Ensure that the current input duration does not exceed 10 ms and that the total current input does not exceed 100 mA.

Appendix J.2

Section 38 Electrical Characteristics

Table 38.14 DC Characteristics - Supply Current

Recommended Operating Conditions: Vcc = PLLVcc = 5.0 V ±0.5 V/3.3 V ±0.3 V, AVcc = 5.0 V ±0.5 V/3.3 V ±0.3 V

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement Conditions
Core supply current (Vdd power supply)		I_{DD}	—	—	**560**	mA	Ick = **240** MHz
System consumption current (Vcc power supply)*1 (Including flash memory programming and erasure)		I_{CC}	—	—	90	mA	Pck = 40 MHz
PLL supply current (PLLVcc power supply)		I_{PLL}	—	—	10	mA	
Analog supply current (AVcc power supply)	During A/D conversion	I_{AVcc}	—	—	10	mA	2 modules, Pck = 40MHz
	Awaiting A/D conversion		—	—	1	mA	
ADC reference power supply current (AVREF)	During A/D conversion	I_{AVREF}	—	—	4	mA	2 modules, Pck = 40MHz
	Awaiting A/D conversion		—	—	3.5	mA	

Notes: *1 An inrush current of about 100 mA will be caused at power on.

- When the A/D converter is not used, do not leave the AVcc, AVref, and AVss pins open.
- The supply current is measured when V_{IH}min = Vcc – 0.5 V, V_{IL} = 0.5 V, with all output pins unloaded.

Appendix J.3

Section 38 Electrical Characteristics

38.3 AC Characteristics

- The timing conditions without specifications are the following :
  Vdd = 1.5 V + 0.15 V, -0.1 V, Vcc = PLLVcc = 5.0 V ±0.5 V/3.3 V ±0.3 V, AVcc = 5.0 V ±0.5 V/3.3 V ±0.3 V, AVREFH = 4.5 V to AVcc/3.0 V to AVcc,
  Vss = PLLVss = AVss = AVREFL = 0 V, Ta = -40°C to +**105**°C
  When not otherwise specified, the input threshold value is the value under conditions where all module input pins for the same channel are set to the same characteristics. When not otherwise specified, the output driving ability is the value under conditions where all module output pins for the same channel are set to the same characteristics.
- Standard values are guaranteed when the output load capacity of the measurement pin is 15 pF to 50 pF. Note that the output load capacity of the CLKOUT pin is 15pF to 30pF.

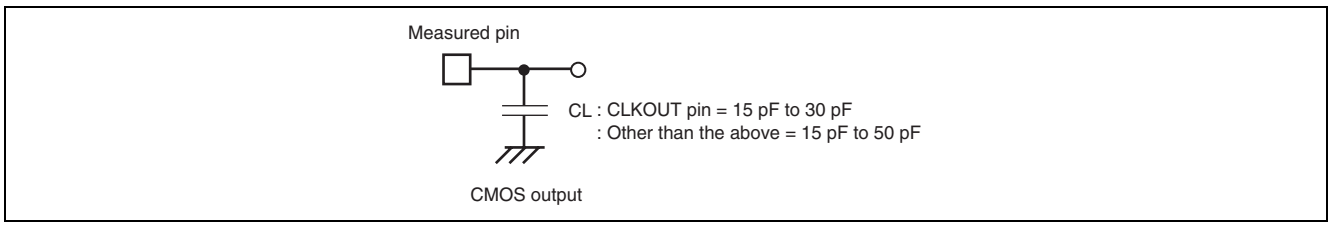


Figure 38.1 Measurement Circuit for Output Switching Characteristics

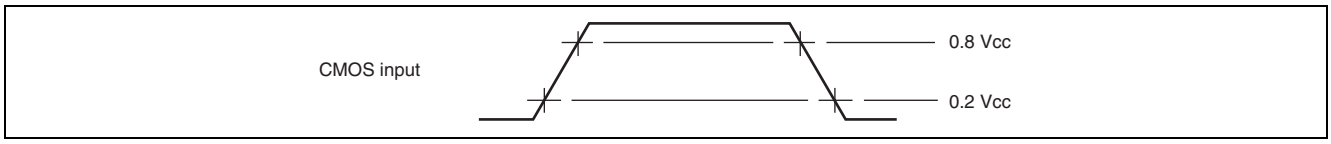


Figure 38.2 Input Waveform and Timing Check Points at Characteristics Measurement

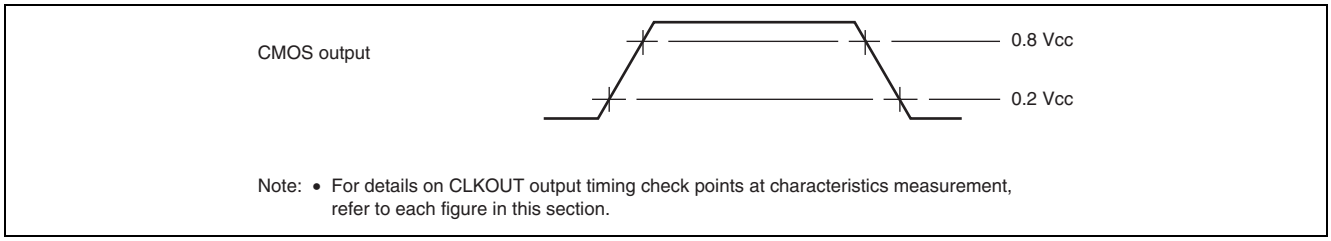


Figure 38.3 Output Timing Check Points at Characteristics Measurement

REVISION HISTORY	SH74593 Datasheet

Rev.	Date	Description	
		Page	Summary
1.20	Sep 10, 2012	-	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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