

# SH74572

R01DS0189EJ0120

## RENESAS MCU

Rev.01.20

Sep 10, 2012

### 1. Overview

The SH7457 Group is a single-chip RISC (reduced instruction set computer) microcontroller based on a Renesas original RISC CPU core.

Basically the SH7457 Group is the same as the SH7456 Group. Please refer to SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10 (Sep 22, 2011). Table 1.1 shows the differences between the SH7456 Group and the SH7457 Group.

\* Henceforth, the bold letter portion (shaped portion) shows a difference from SH7456 Group.

**Table 1.1 Products**

Group	Product	Model	CPU Frequency	Memory Capacity	Package	FlexRay	Operating temperature (Ta)
<b>SH7457</b>	<b>SH74572</b>	<b>R5F74572LBG</b>	<b>240MHz</b>	ROM: 1 Mbyte	PRBG0176GA-A	Yes	-40 to + <b>105</b> °C
SH7455	SH74552	R5F74552KBG	160MHz	IL memory: 8 Kbytes,		Yes	-40 to +125°C
SH7456	SH74562	R5F74562KBG		OL memory: 16 Kbytes, and SHwYRAM: 256 Kbytes		No	
SH7459	SH74593	R5F74593LBG	240MHz	ROM: 1.5 Mbytes IL memory: 8 Kbytes, OL memory: 16 Kbytes, and SHwYRAM: 512 Kbytes		Yes	-40 to +105°C

### 2. Details

This section shows the details of the difference from SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10 (Sep 22, 2011). Table 2.1 shows the difference between the SH74562 and the SH74572.

**Table 2.1 Difference between SH74562 and SH74572**

Page	Description
1-4	<ul style="list-style-type: none"> <li>Table 1.1 Specifications Overview: Descriptions of CPG Product CPU clock (Ick) SH74562 160 MHz maximum SH74572 <b>240</b> MHz maximum</li> </ul>
1-6	<ul style="list-style-type: none"> <li>Table 1.1 Specifications Overview: Descriptions of FlexRay Product Channels of FlexRay SH74562 None: SH7456 Group SH74572 <b>Two channels: SH7457</b> Group</li> </ul>

Page	Description															
1-7	<ul style="list-style-type: none"> <li>Table 1.1 Specifications Overview: Descriptions of Operating temperature</li> </ul> <table border="1"> <thead> <tr> <th>Product</th> <th>Model</th> </tr> </thead> <tbody> <tr> <td>SH74562</td> <td>Ta = -40°C to +125°C</td> </tr> <tr> <td>SH74572</td> <td>Ta = -40°C to +<b>105</b>°C</td> </tr> </tbody> </table> <hr/> <ul style="list-style-type: none"> <li>Table 1.2 Products</li> </ul> <table border="1"> <thead> <tr> <th>Product</th> <th>Model</th> <th>FlexRay</th> </tr> </thead> <tbody> <tr> <td>SH74562</td> <td>R5F74562KBG</td> <td>No</td> </tr> <tr> <td>SH74572</td> <td><b>R5F74572LBG</b></td> <td><b>Yes</b></td> </tr> </tbody> </table> <p>Please refer to Appendix A.</p>	Product	Model	SH74562	Ta = -40°C to +125°C	SH74572	Ta = -40°C to + <b>105</b> °C	Product	Model	FlexRay	SH74562	R5F74562KBG	No	SH74572	<b>R5F74572LBG</b>	<b>Yes</b>
Product	Model															
SH74562	Ta = -40°C to +125°C															
SH74572	Ta = -40°C to + <b>105</b> °C															
Product	Model	FlexRay														
SH74562	R5F74562KBG	No														
SH74572	<b>R5F74572LBG</b>	<b>Yes</b>														
1-8	<ul style="list-style-type: none"> <li>Figure 1.1 Block Diagram</li> </ul> <table border="1"> <thead> <tr> <th>Product</th> <th>SH-4A core clock</th> </tr> </thead> <tbody> <tr> <td>SH74562</td> <td>SH-4A core (160 MHz maximum)</td> </tr> <tr> <td>SH74572</td> <td>SH-4A core (<b>240</b> MHz maximum)</td> </tr> </tbody> </table>	Product	SH-4A core clock	SH74562	SH-4A core (160 MHz maximum)	SH74572	SH-4A core ( <b>240</b> MHz maximum)									
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SH74572	SH-4A core ( <b>240</b> MHz maximum)															
1-9	<ul style="list-style-type: none"> <li>Figure 1.2 Pin Arrangement (Top Transparent View)</li> </ul>															
1-15	<ul style="list-style-type: none"> <li>Table 1.3 Pin Functions of pin A6</li> </ul> <table border="1"> <thead> <tr> <th>Product</th> <th>A6 pin</th> </tr> </thead> <tbody> <tr> <td>SH74562</td> <td>Vcc</td> </tr> <tr> <td>SH74572</td> <td><b>Vss</b></td> </tr> </tbody> </table> <p>Please refer to Appendix B.</p>	Product	A6 pin	SH74562	Vcc	SH74572	<b>Vss</b>									
Product	A6 pin															
SH74562	Vcc															
SH74572	<b>Vss</b>															
14-1	<ul style="list-style-type: none"> <li>Table 14.1 Relation between Input Frequency and Input Clock</li> <li>Figure 14.1 Block Diagram of CPG</li> </ul> <table border="1"> <thead> <tr> <th>Product</th> <th>PLL frequency multiplier (input to CPU)</th> </tr> </thead> <tbody> <tr> <td>SH74562</td> <td>X8.</td> </tr> <tr> <td>SH74572</td> <td><b>X12.</b></td> </tr> </tbody> </table> <p>Please refer to Appendix C.</p>	Product	PLL frequency multiplier (input to CPU)	SH74562	X8.	SH74572	<b>X12.</b>									
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SH74572	<b>X12.</b>															
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SH74562	160.															
SH74572	<b>240</b>															
15-60	<ul style="list-style-type: none"> <li>Table 15.9 Minimum of Interrupt Response Time: Response time (Minimum)</li> </ul> <table border="1"> <thead> <tr> <th>Product</th> <th>NMI</th> <th>IRQ</th> <th>Peripheral Module</th> <th>Remarks</th> </tr> </thead> <tbody> <tr> <td>SH74562</td> <td>40Icyc + S × Icyc</td> <td>36Icyc + S × Icyc</td> <td>32Icyc + S × Icyc</td> <td>When Icyc:Scyc: Pcyc = 4:2:1</td> </tr> <tr> <td>SH74572</td> <td><b>55</b>Icyc + S × Icyc</td> <td><b>49</b>Icyc + S × Icyc</td> <td><b>43</b>Icyc + S × Icyc</td> <td>When Icyc:Scyc: Pcyc = <b>6</b>:2:1</td> </tr> </tbody> </table> <p>Please refer to Appendix D.</p>	Product	NMI	IRQ	Peripheral Module	Remarks	SH74562	40Icyc + S × Icyc	36Icyc + S × Icyc	32Icyc + S × Icyc	When Icyc:Scyc: Pcyc = 4:2:1	SH74572	<b>55</b> Icyc + S × Icyc	<b>49</b> Icyc + S × Icyc	<b>43</b> Icyc + S × Icyc	When Icyc:Scyc: Pcyc = <b>6</b> :2:1
Product	NMI	IRQ	Peripheral Module	Remarks												
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SH74572	<b>55</b> Icyc + S × Icyc	<b>49</b> Icyc + S × Icyc	<b>43</b> Icyc + S × Icyc	When Icyc:Scyc: Pcyc = <b>6</b> :2:1												
38-1	<ul style="list-style-type: none"> <li>Table 38.1 Absolute Maximum Ratings</li> </ul> <table border="1"> <thead> <tr> <th>Product</th> <th>Power dissipation (Pd)</th> </tr> </thead> <tbody> <tr> <td>SH74562</td> <td>1000 mW ,Ta = -40°C to +125°C</td> </tr> <tr> <td>SH74572</td> <td><b>1200</b> mW ,Ta = -40°C to +<b>105</b>°C</td> </tr> </tbody> </table> <p>Please refer to Appendix E.</p>	Product	Power dissipation (Pd)	SH74562	1000 mW ,Ta = -40°C to +125°C	SH74572	<b>1200</b> mW ,Ta = -40°C to + <b>105</b> °C									
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SH74562	-40°C to +125°C															
SH74572	-40°C to + <b>105</b> °C															

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**Page**    **Description**

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- 38-10    • Table 38.14 DC Characteristics - Supply Current  
Product    Core supply current (Vdd power supply)  
SH74562    IDD is 480 mA(maximum)    Ick = 160 MHz  
SH74572    IDD is **560** mA(maximum)    Ick = **240** MHz

Please refer to Appendix F.

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- 38-11    • 38.3 AC Characteristics: Descriptions of the timing conditions  
Product    The timing conditions of AC Characteristics  
SH74562    Ta = -40°C to +125°C  
SH74572    Ta = -40°C to **+105°C**

Please refer to Appendix G.

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## Appendix A

### Section 1 Overview

#### 1.2 Product Line Overview

Table 1.2 lists the products.

**Table 1.2 Products**

Product	Model	ROM Capacity	RAM Capacity	Package	FlexRay
SH74552	R5F74552KBG	1 Mbyte	IL memory: 8 Kbytes,	PRBG0176GA-A	Yes
SH74562	R5F74562KBG		OL memory: 16 Kbytes, and		No
<b>SH74572</b>	<b>R5F74572LBG</b>		SHwyRAM: 256 Kbytes		<b>Yes</b>
SH74593	R5F74593LBG	1.5 Mbyte	IL memory: 8 Kbytes,		Yes
			OL memory: 16 Kbytes, and		
			SHwyRAM: 512 Kbytes		

Appendix B

Section 1 Overview

1.4 Pin Arrangement

Figure 1.2 shows the pin arrangement.

Position of pin A1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	Vss (N.C.)	PG0/ MOSI0/ TO40	PF5/ SCL/ (CTX3)	PF1/ CTX0	DET3OR5	Vss	PL8/ TIA14/ IRQ7/ DREQ3	PL6/ TIA12/ (TIF1A)	PH15/ DROD7/ TO37/ DDC15	PH13/ DROD5/ (TO35)/ DDC13	PH9/ DROD1/ (TO31)/ DDC09/ CTS2#	PH5/ DROD13/ TO25/ DDC05/ TIA01	PH2/ DROD10/ TO22/ DDC02/ TIF1A	PH0/ DROD8/ TO20/ DDC00/ TIF0A	Vss (N.C.)	A
B	PG1/ MISO0/ TO41	PG2/ RSPCK0/ TO42	PG3/ TO43/ SSL00/ (IRQ7)	PF4/ SDA/ (CRX3)	PF0/ CRX0	ASEBRK#/ BRKACK	PL9/ TIA15/ AUDREVT#	PL5/ TIA11/ (TIF0B)	PL2/ DROWR	PH12/ DROD4/ TO34/ DDC12	PH8/ DROD0/ (TO30)/ DDC08/ RTS2#	PH4/ DROD12/ TO24/ DDC04/ TIA00	PH1/ DROD9/ TO21/ DDC01/ TIF0B	PH3/ DROD11/ TO23/ DDC03/ TIF1B	PK14/ AUDRSYN#	B
C	PG4/ IRQ2/ TO44/ SSL01	Vss	WDTOVF#	Vdd	Vdd	Vdd	PL4/ TIA10/ (TIF0A)	Vss	Vcc	PH14/ DROD6/ (TO36)/ DDC14/ IRQ1	PH10/ DROD2/ (TO32)/ DDC10	PH6/ DROD14/ TO26/ DDC06/ TIA02	PK12/ AUDRD3	PK13/ AUDRCLK	PK11/ AUDRD2	C
D	FWE	RESET#	Vss	Vss	Vdd	Vdd	PL3/ IRQ6	Vss	Vcc	PH11/ DROD3/ (TO33)/ DDC11	PH7/ DROD15/ (TO27)/ DDC07/ TIA03	PK8/ DREQ2	PK9/ AUDRD0/ RTS3#	PK10/ AUDRD1/ CTS3#	PK6/ TXD3	D
E	MD1	NMI	Vss	Vss								Vss	PK0/ IRQ5/ SSL10	PK5/ DINC4/ RXD3	PJ14/ TXD1/ MOSH1	E
F	XTAL	EXTAL	Vss	Vss								Vcc	PJ10/ RXD0/ PVMOFF4/ ADOTRG#	PJ15/ SCK1/ PSPCK1	PJ13/ RXD1/ MISO1	F
G	PLLvss	PLLvcc	MD0	MPMD								PJ1/ (CTX0)/ FTXA	PJ7/ CTX3/ TIF2B/ TXD2	PJ12/ SCK0/ TCLKB/ (IRQ0)	PJ11/ TXD0/ AD0END	G
H	TCK	TMS	MD2	TRST#								PJ0/ (CRX0)/ FRXA	PJ4/ CRX2/ TIF2A/ CTS0#	PJ6/ CRX3/ TIF2A/ RXD2/ TIA04	PJ5/ CTX2/ FTXENB/ SCK2	H
J	PD1/ PDIDATA1	TDO	TDI	Vss								PN1/ AD1IN1	PN0/ AD1IN0	PJ3/ CTX1/ FTXB/ RTS0#	PJ2/ CRX1/ FRXB	J
K	PD4/ PDIDATA4	PD3/ PDIDATA3	Vss	Vss	PN4/ AD1IN4	PN5/ AD1IN5	AVss	AVcc	K							
L	PD8/ PDIDATA8	PD7/ PDIDATA7	Vcc	Vcc	PM0/ AD0IN0	AVss	AVREFL	AVREFH	L							
M	PD9/ PDIDATA9	PD6/ PDIDATA6	PD0/ PDIDATA0	Vss	Vss	Vss	Vdd	Vdd	PC8/ CLKOUT/ TO36	Vcc	Vss	AVss	PM4/ AD0IN4	AVREFL	AVREFH	M
N	PD10/ PDIWR	PD5/ PDIDATA5	PA4/ TO04/ DDB04	PA7/ TO07/ DDB07	PA10/ TO12/ DDB10/ PSLDATA0	PA11/ TO13/ DDB11/ PSLDATA1	Vdd	Vdd	PC1/ TO31/ MISO2	Vcc	Vss	PM2/ AD0IN2	PM6/ AD0IN6	PM9/ AD0IN9	AVss	N
P	PD2/ PDIDATA2	PA3/ TO03/ DDB03	PA0/ TO00/ DDB00	PA2/ TO02/ DDB02	PA6/ TO06/ DDB06	PA9/ TO11/ DDB09/ PSLCLKA	PA13/ TO15/ DDB13/ PSLDATA3	PB1/ PVMOFF1/ DINB1	PC0/ TO30/ MOSI2/ (IRQ6)	PC3/ TO33/ SSL20/ IRQ0	PM15/ AD0IN15	PM13/ AD0IN13	PM11/ AD0IN11	PM8/ AD0IN8	AVcc	P
R	Vss (N.C.)	PE15/ TO27/ PSLCLR	PA1/ TO01/ DDB01	PA5/ TO05/ DDB05	PA8/ TO10/ DDB08/ PSLCLKB	PA12/ TO14/ DDB12/ PSLDATA2	PB0/ PVMOFF0/ DINB0	PB3/ PVMOFF3/ DINB3	PC2/ TO32/ RSPCK2/ DREQ0	PC5/ TO35	PC14	PM14/ AD0IN14	PM12/ AD0IN12	PM10/ AD0IN10	AVcc (N.C.)	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 1.2 Pin Arrangement (Top Transparent View)

## Appendix C

### Section 14 Clock Generator (CPG)

#### 14.1 Overview

Table 14.1 lists the relation between input frequency and input clock.

**Table 14.1 Relation between Input Frequency and Input Clock**

Input frequency (MHz)	PLL frequency multiplier (input to CPU)	CPU clock (MHz)	SHwy clock (MHz)	Peripheral clock (MHz)	Peripheral A clock (MHz)	FlexRay clock (MHz)
20	x12	240	80	40	80	80

## Appendix D

### Section15 Interrupt Controller (INTC)

#### 15.5 Interrupt Response Time

Table 15.9 shows the interrupt response time, which is the interval from when an interrupt request occurs until the interrupt exception handling is started and the start instruction of the interrupt handling is fetched.

**Table 15.9 Interrupt Response Time**

Item	Number of State			Remarks	
	NMI	IRQ	Peripheral Module		
Priority determination time	7 P <sub>cyc</sub>	6 P <sub>cyc</sub>	5P <sub>cyc</sub>		
Wait time until the CPU finishes the current sequence		$S-1 (\geq 0) \times I_{cyc}$			
Interval from when interrupt exception handling begins (saving SR and PC) until a SHwy bus request is issued to fetch the start instruction of the interrupt handling		$11I_{cyc} + 1S_{cyc}$			
Response time	Total	$(S + 10) I_{cyc} + 1S_{cyc} + 7 P_{cyc}$	$(S + 10) I_{cyc} + 1S_{cyc} + 6 P_{cyc}$	$(S + 10) I_{cyc} + 1S_{cyc} + 5P_{cyc}$	
	Minimum	<b>55</b> $I_{cyc} + S \times I_{cyc}$	<b>49</b> $I_{cyc} + S \times I_{cyc}$	<b>43</b> $I_{cyc} + S \times I_{cyc}$	When $I_{cyc}:S_{cyc}:P_{cyc} = 6:2:1$

Legend:

$I_{cyc}$ : Period for one CPU clock cycle

$S_{cyc}$ : Period for one SHwy clock cycle

$P_{cyc}$ : Period for one peripheral clock cycle

S: Number of instruction execution states

## Appendix E

### Section 38 Electrical Characteristics

#### 38.1 Absolute Maximum Ratings

Table 38.1 shows the absolute maximum ratings.

**Table 38.1 Absolute Maximum Ratings**

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	$V_{dd}$	-0.3 to +2.0	V	
	$V_{cc}$ , PLLVcc	-0.3 to +6.5	V	
Input voltage Vcc power supply related pins	$V_{in}$	-0.3 to $V_{cc} + 0.3$	V	
Analog supply voltage	AVcc	-0.3 to +6.5	V	
Analog reference voltage	AVREFH	-0.3 to AVcc +0.3	V	AVREFH > AVREFL
	AVREFL	-0.3 to AVss +0.3	V	
Analog input voltage	VAN	-0.3 to AVcc +0.3	V	
Vss differential voltage	$V_{ss} - PLLV_{ss}$	-0.1 to +0.1	V	
	$V_{ss} - AV_{ss}$	-0.1 to +0.1	V	
	$PLLV_{ss} - AV_{ss}$	-0.1 to +0.1	V	
Maximum input current per pin*2 (per pin)	Digital input pins	$I_{max}$	-20 to +20	mA
	Analog input pins	$I_{max}$	-20 to +20	mA
Power dissipation	$P_d$	<b>1200</b>	mW	$T_a = -40^{\circ}\text{C}$ to <b>+105<math>^{\circ}\text{C}</math></b>
Operating temperature*1	$t_{opr}$	-40 to <b>+105</b>	$^{\circ}\text{C}$	
Storage temperature	$t_{stg}$	-55 to +125	$^{\circ}\text{C}$	Before assembly

#### [Usage Notes]

Operating the MCU in excess of the absolute maximum ratings may result in permanent damage. Be sure to use the MCU in compliance with the connection of power pins, combination conditions of applicable power supply voltages, voltage applicable to each pin, and conditions of output voltage, as specified in the manual. Connecting a non-specified power supply or using the MCU at an incorrect voltage may result in permanent damage of the MCU or the system that contains the MCU.

Notes: \*1 This does not guarantee that the microcomputer can operate continuously at 85°C-plus. Consult Renesas if the microcomputer is going to be used for 85°C-plus applications.

\*2 Ensure that the current input duration does not exceed 10 ms and that the total current input does not exceed 100 mA.

## Appendix F

### Section 38 Electrical Characteristics

**Table 38.14DC Characteristics - Supply Current**

Recommended Operating Conditions:  $V_{CC} = PLLV_{CC} = 5.0\text{ V} \pm 0.5\text{ V}/3.3\text{ V} \pm 0.3\text{ V}$ ,  $AV_{CC} = 5.0\text{ V} \pm 0.5\text{ V}/3.3\text{ V} \pm 0.3\text{ V}$

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement Conditions	
Core supply current (V <sub>DD</sub> power supply)	$I_{DD}$	—	—	<b>560</b>	mA	$I_{CK} = 240\text{ MHz}$	
System consumption current (V <sub>CC</sub> power supply)* <sup>1</sup> (Including flash memory programming and erasure)	$I_{CC}$	—	—	90	mA	$P_{CK} = 40\text{ MHz}$	
PLL supply current (PLLV <sub>CC</sub> power supply)	$I_{PLL}$	—	—	10	mA		
Analog supply current (AV <sub>CC</sub> power supply)	During A/D conversion	$I_{AV_{CC}}$	—	—	10	mA	2 modules, $P_{CK} = 40\text{ MHz}$
	Awaiting A/D conversion		—	—	1	mA	
ADC reference power supply current (AVREF)	During A/D conversion	$I_{AV_{REF}}$	—	—	4	mA	2 modules, $P_{CK} = 40\text{ MHz}$
	Awaiting A/D conversion		—	—	3.5	mA	

Notes: \*1 An inrush current of about 100 mA will be caused at power on.

- When the A/D converter is not used, do not leave the AV<sub>CC</sub>, AV<sub>ref</sub>, and AV<sub>SS</sub> pins open.
- The supply current is measured when  $V_{IHmin} = V_{CC} - 0.5\text{ V}$ ,  $V_{IL} = 0.5\text{ V}$ , with all output pins unloaded.

## Appendix G

### Section 38 Electrical Characteristics

#### 38.3 AC Characteristics

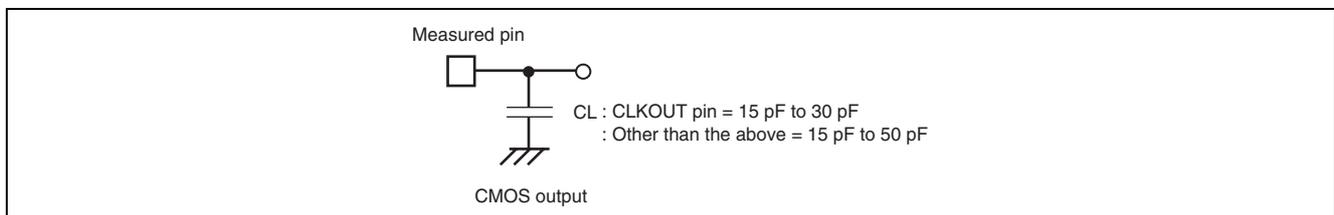
- The timing conditions without specifications are the following :

$V_{dd} = 1.5\text{ V} + 0.15\text{ V}$ ,  $-0.1\text{ V}$ ,  $V_{cc} = PLLV_{cc} = 5.0\text{ V} \pm 0.5\text{ V}/3.3\text{ V} \pm 0.3\text{ V}$ ,  $AV_{cc} = 5.0\text{ V} \pm 0.5\text{ V}/3.3\text{ V} \pm 0.3\text{ V}$ ,  
 $AV_{REFH} = 4.5\text{ V}$  to  $AV_{cc}/3.0\text{ V}$  to  $AV_{cc}$ ,

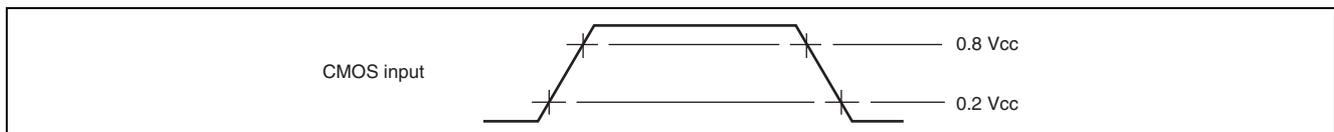
$V_{ss} = PLLV_{ss} = AV_{ss} = AV_{REFL} = 0\text{ V}$ ,  $T_a = -40^\circ\text{C}$  to  $+105^\circ\text{C}$

When not otherwise specified, the input threshold value is the value under conditions where all module input pins for the same channel are set to the same characteristics. When not otherwise specified, the output driving ability is the value under conditions where all module output pins for the same channel are set to the same characteristics.

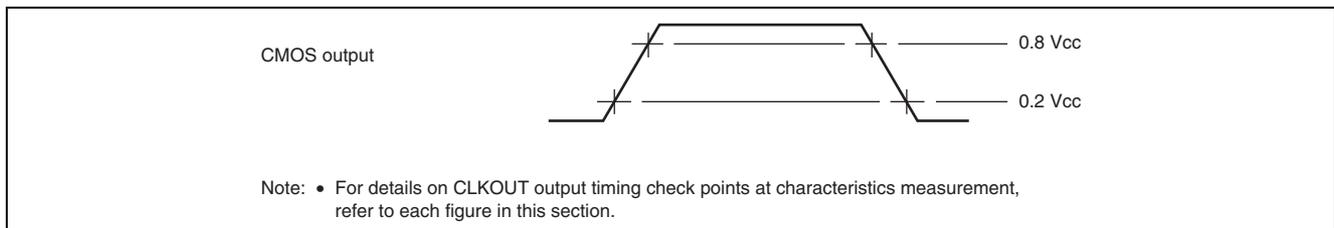
- Standard values are guaranteed when the output load capacity of the measurement pin is 15 pF to 50 pF. Note that the output load capacity of the CLKOUT pin is 15pF to 30pF.



**Figure 38.1 Measurement Circuit for Output Switching Characteristics**



**Figure 38.2 Input Waveform and Timing Check Points at Characteristics Measurement**



**Figure 38.3 Output Timing Check Points at Characteristics Measurement**

**REVISION HISTORY****SH74572 Datasheet**

Rev.	Date	Description	
		Page	Summary
1.10	Oct 26, 2011	-	First edition issued
1.20	Sep 10, 2012	Throughout Datasheet	Document number added
		1	1. Overview: Description changed. From: the SH7457 Group is the same as the SH7455 Group. To : the SH7457 Group is the same as the SH7456 Group.
			Table 1.1 Products: SH7459 Group added.
			Table 2.1 : Title and description changed. From: Difference between SH74552 and SH74572 To : Difference between SH74562 and SH74572
		4	Appendix A Table 1.2 Products: SH7459 Group added.
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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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