Section 1 Overview

1.1 Features

This LSI includes 1.8 GHz Quad Arm® Cortex®-A55 on-chip FPU, Neon™, L1-caches and L3-cache, 200MHz Arm® Cortex®-M33 on-chip FPU and DSP-extension, DRP-AI, Mali™-G31 (GE3D), Mali™-C55 (ISP), 1.5 MB of on-chip SRAM, 2ch GbEthernet MAC, 1ch USB2.0, USB3.2 Gen 2x1, 2-MIPI® CSI-2® camera input interface, 1-MIPI® DSI® video output interface, PCIe® Gen3 2Lane (EP/RC), various communication interfaces such as xSPI, eMMC™, I2S (TDM), I3C®, PDM, and security functions.

■ CPU

- On-chip Quad 64-bit Arm® Cortex®-A55 Core processors

  Application processing (up to 1.8 GHz)
- 32-bit Arm® Cortex®-M33 processor

  System management (up to 200 MHz)

■ Accelerator engines

- AI accelerator (dynamically reconfigurable processor for AI (DRP-AI (AI-MAC+DRP)))
- 3D graphics engine (GE3D) (option)
- Image signal processor (ISP) (option)
- Image scaling unit (ISU)
- Video codec unit (VCD)

■ On-chip SRAM and external memory interfaces

- On-chip shared SRAM (1.5-Mbyte on-chip SRAM with ECC)
- External DDR memory interface

  1-channel memory controller for LPDDR4-3200 or LPDDR4X-3200 with a 32-bit bus width
- xSPI interface
- SDHI (eMMC/SD (1-, 4-, 8-bit bus width) supported)

■ Boot

- Selectable boot CPU from Cortex®-M33 or Cortex®-A55

■ Extended-function timers

- 32-bit general-purpose timer (16 ch.)
- 32-bit CMTW (8 ch.)

■ Various communication/storage/network interfaces

- Ethernet (2 ch.: 10/100/1000 BASE)
- USB2.0 (1 ch.: Host/Function)
- USB3.2 Gen2 × 1 (1 ch.: Host-only)
- PCIe Gen3 (1, 2 lanes × 1 pair)
- MIPI CSI-2 (2 ch.: 1, 2, or 4 lanes)
- MIPI DSI (1 ch.: 1, 2, or 4 lanes)
- CAN/CANFD (compliant with ISO11898-1) (6 ch.)
- SCI (10 ch.: UART/SPI/I2C-host)
- SPI (3 ch.)
- I2C (9 ch.)
- I3C (1 ch.)

■ Audio

- Asynchronous sampling rate converter unit (SCU) (up to 192 kHz)
- DMAC for Audio (ADMAC) is available to transfer audio formats of I2S with SCU.
- Flexible audio clock generator (ADG) for audio functions.
- I2S (TDM) input/output interfaces (half-duplex 10 ch.; full-duplex 5 ch.)
- SPDIF input/output interfaces (3 ch.)
- Pulse density modulation (PDM) input interfaces (6 ch.)

■ Analog/Digital converter (ADC) and sensors

- 2.5 Msps 12-bit ADC (24 ch.)
- Internal temperature sensors (2 ch.)

■ Security

- Hardware cryptographic engine (option)

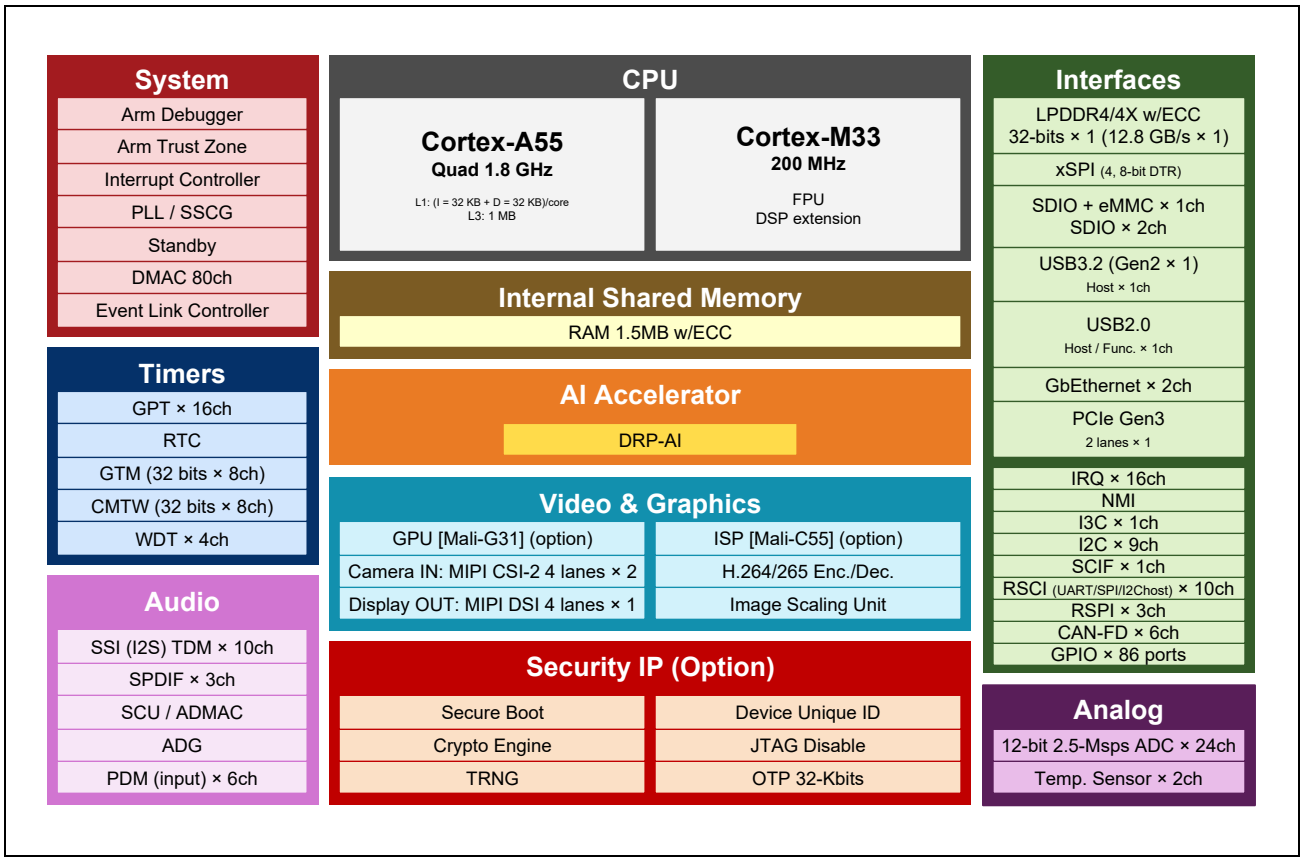


Figure 1.1-1 Diagram of Functional Overview

1.2 Product Lineup

Table 1.2-1 Product Lineup

Group	Name	Part Number	GE3D	Security	ISP
RZ/V2N	RZ/V2N	R9A09G056N41GBG	N/A	N/A	N/A
		R9A09G056N42GBG	Available (Mali-G31)		
		R9A09G056N45GBG	N/A	Available	
		R9A09G056N46GBG	Available (Mali-G31)		
	RZ/V2NP	R9A09G056N43GBG	N/A	N/A	Available (Mali-C55)
		R9A09G056N44GBG	Available (Mali-G31)		
		R9A09G056N47GBG	N/A	Available	
		R9A09G056N48GBG	Available (Mali-G31)		

Note: "#ACx" or "#BCx" is added to the end of part numbers. "#ACx" is packaged in the individual tray, and "#BCx" is packaged in the full carton.

1.3 Functions

The following tables list the functions of this LSI.

Table 1.3-1 CPU

Item	Description
Application Processor Cortex-A55 (CA55)	• Arm Cortex-A55 Quad Core 1.8 GHz with 0.9 V, 1.1 GHz with 0.8 V • L1 I-cache 32 Kbytes (with parity) and D-cache 32 Kbytes (with ECC) per core • L2 cache: 0 Kbyte • L3 cache: 1 Mbyte (with ECC)*1 • MMU supported • Neon™ and FPU supported • Cryptographic extension supported (for security-supported products only) • Armv8-A architecture
System Manager Cortex-M33 (CM33)	• Arm Cortex-M33 processor 200 MHz • FPU supported • DSP extension supported • Security extension supported • Armv8-M architecture
Debug Interface	• Arm® CoreSight® architecture • JTAG and SWD interfaces supported • ETF: Total of 52 Kbytes for program flow tracing • JTAG disabling supported (option)
Boundary Scan	• Boundary scan based on IEEE 1149.1 via the JTAG interface is supported. • Note that some module pins are not available on this boundary scan.

Note 1. The maximum operating frequency of the L3 cache is 1.26 GHz.

Table 1.3-2 Accelerator Engines

Item	Description
AI accelerator (DRP-AI)	• DRP-AI (AI-MAC + DRP) • Up to 4 dense TOPS • Up to 15 sparse TOPS
3D Graphics Engine (GE3D) (option)	• Arm Mali-G31 • One single-pixel shader core • 8-Kbyte L2 cache • OpenGL ES™ 1.1, 2.0, and 3.2 supported • OpenCL 2.0 full profile supported
Image Signal Processor Unit (ISP) (option*) *RZ/V2NP only	• Arm Mali-C55 • 1 unit, supporting 4K • Maximum pixel rate: 630 Mpixels/s • Supports the functions below: – Black level correction – WB gain – Defect pixel correction – Color correction – Gamma correction – Edge enhancement and sharpness filter – Down-scaling and cropping – Dynamic range correction – 2-exprosure HDR – Shading correction • Supports input formats: RAW8, 10, 12, 14, 16, 20 • Supports output formats: YUV422, YUV420, RGB
Image Scaling Unit (ISU)	• Scaling down function with bilinear interpolation • Input image size (max): 4096 × 4096 • Output image size (max): 4096 × 4096 • Supported color format: RGB/ARGB, YCbCr/YUV, RAW (Grayscale)
Video Codec Unit (VCD)	• H.264/H.265 codec module • Support for encoding and decoding – H.264/AVC (High Profile, level 4.2; Main Profile, level 4.2; Baseline Profile, level 4.2) – H.265/HEVC (Main Profile, level 5) • Maximum size – (H.264) 1920 × 1080 × 60 fps*1 – (H.265) 3840 × 2160p × 30 fps*1 • I-/P-slice supported for H.264/H.265 encoding and decoding

Note 1. Maximum frame rate for this size. The number of streams can be defined within this specification by software.

Table 1.3-3 On-chip SRAM and External Memory Interfaces

Item	Description
System RAM	• 1.5 Mbytes (with ECC)
External Bus Controller for LPDDR4/4X SDRAM (DDR)	• 1 channel • Support for LPDDR4-3200 and LPDDR4X-3200 • Bus width: 32-bits • In line ECC (16 ECC regions) supported (support for error detection interrupts) • Memory size: Up to 8 Gbytes • Auto-refresh, self-refresh, and IO retention supported • Memory access protection for secure regions using TZC-400 (Arm® TrustZone® supported)
xSPI Controller (xSPI)	• 1 channel (2 chip select signals) • Compliant with the xSPI protocol • Protocol mode 1, 4, or 8 pins with SDR or DDR (1S-1S-1S, 4S-4D-4D, 8D-8D-8D)*1 2 or 4 pins with SDR (1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S) • Support for XiP mode • Support for up to 256-Mbyte address space (support for up to 128M bytes per channel address space in boot sequence)
SD Card Host Interface/ Multimedia Card Interface (SD/MMC)	• 3 channels • Channel 0 supports SDHI and e-MMC. • Channels 1 and 2 support SDHI. • SD memory I/O card interface (1-bit or 4-bit SD bus) • SD, SDHC and SDXC SD memory card access supported • Compliant with SD specification version 3.01 • Default, high-speed, UHS-I/SDR50, SDR104 and DDR50 transfer modes supported • Error check function: CRC7 (command), CRC16 (data) • Support for card detection and write protection • MMC interface (1-bit, 4-bit, or 8-bit MMC bus) • e-MMC device access supported • Compliant with eMMC 4.51 • High-speed, HS200 and HS-DDR transfer modes supported

Note 1. DDR access without XSPI0_DS is not supported for 4S-4D-4D and 8D-8D-8D.

Table 1.3-4 Boot

Item	Description
Boot	• Boot CPU selectable as CA55 and CM33 • CM33 boot – Boot mode 2: Booting from a serial flash memory connected to the xSPI bus space – Boot mode 3: Booting from SCIF download • CA55 boot – Boot mode 0: Booting from eSD – Boot mode 1: Booting from eMMC – Boot mode 2: Booting from a serial flash memory connected to the xSPI bus space – Boot mode 3: Booting from SCIF download *Note:* 1.8 V or 3.3 V selectable for eMMC and xSPI interfaces.

Table 1.3-5 System, Data Transfer, Enhanced Interrupt Controller Unit, Clock Functions

Item	Description
Direct Memory Access Controller (DMAC)	• 80 channels • Transfer modes: Single transfer mode and block transfer mode • LINK mode (DMA transfer under descriptor control) supported • Transfer size: 1, 2, 4, 8, 16, 32, 64, or 128 bytes • Transfer request: Software trigger, external DMA requests (DREQ) and interrupt requests from peripheral functions • A specific DMA transfer interval can be specified to adjust the bus occupancy.
Clock Pulse Generator (CPG)	• Generates the clocks from an external clock or external resonator (24 MHz). – Maximum CA55 clock: 1.8 GHz (0.9 V), 1.1GHz (0.8 V) – Maximum CM33 clock: 200 MHz – Maximum DDR clock: 800 MHz (LPDDR4/4X-3200) – Maximum GE3D clock: 630 MHz – Maximum ISP clock: 630 MHz – Maximum H.264/H.265 clock: 400 MHz – Maximum system bus clock: 400 MHz • SSC (spread spectrum clock) supported
Interrupt Controller (GIC)	• Arm® CoreLink® generic interrupt controller (GIC-600) for CA55 • 32 priority levels available • Nested vectored interrupt controller (NVIC) for CM33 • External Interrupt pins (NMI, IRQ0 to IRQ15, and TINT0 to TINT31) • On-chip peripheral Interrupts: Priority level set for each module
Event Link Controller (ELC)	• Up to 461 event signals can be interlinked with the operation of modules. • In particular, the operation of timer modules can be started by input event signals. • Event-linked operation of signals of 16 port pins,P60 to 67 and P80 to 87, is to be possible.
Error Controller	• Error events from CPU and peripherals are captured and merged to interrupt with mask for CA55 and CM33 respectively. • System reset can be generated by error events.
Message Handling Unit (MHU)	• Message handling function between each core of CA55 and CM33 • Assert interrupts to inform messages and responses from/to every core

Table 1.3-6 Various Communication/Storage/Network Interfaces (1/3)

Item	Description
USB3.2 Host (USB3)	• 1 channel • Compliant with USB3.2 Gen2 × 1 • Maximum rate: 10 Gbps • Support for control, bulk, interrupt, and isochronous transfer • Internal dedicated DMA
USB2.0 Host/Function (USB2)	• 1 channel (Host/Function) • Compliant with USB2.0 • Support for On-The-Go (OTG) functionality (ch. 0 only) • Support for control, bulk, interrupt, and isochronous transfer • Internal dedicated DMA
PCIe Express® 3.0 (PCIE)	• PCIe Gen3 • Root complex or Endpoint selectable • Lane configuration selectable from below: – 1 or 2 lanes × 1 channel
MIPI CSI-2 Interface with camera image processing (CRU)	• 2 channels • Number of lanes: 1, 2, or 4 lanes per channel • Maximum bandwidth: 2.1 Gbps per lane • Support for the throughput up to 4K RAW12 30 fps • Support for 4 virtual channels selected from VC0 to VC15 • Support for input data formats: – YUV422 8 bits or 10 bits – RGB444, RGB555, RGB565, RGB666, RGB888 – RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20 – YUV420 8-bits or 10-bits (image processing not supported) – Legacy YUV420 8-bits (image processing not supported) – YUV420 8-bits or 10-bits (chroma shifted pixel sampling) (image processing not supported) – User defined byte-based data • The other formats from the MIPI CSI-2 interface can also be output without image processing. • Generic long packet data types 1 to 4 • User defined 8-bit data types 1 to 8
MIPI DSI Interface with LCD controller (LCDC)	• 1 channel • Number of lanes: 1, 2, or 4 lanes • Support for the throughput up to 1920 × 1200 RGB888 60 fps • Support for the throughput up to 1280 × 1024 RGB888 120 fps • Maximum bandwidth: 1.5 Gbps per lane • Support for 2-plane blending (with the ability to blend 2 differently sized images) • Support for image processing: – Dither processing (RGB666) – Clipping – RGB gamma correction LUT • Support for input data formats: – RGB565, RGB666, RGB888 – ARGB1555, ARGB4444, ARGB8888 – YUV (YcbCr) 444 8-bits, YUV (YcbCr) 422 8-bits, YUV (YcbCr) 420 8-bits • Support for output data formats: – RGB666, RGB888

Table 1.3-6 Various Communication/Storage/Network Interfaces (2/3)

Item	Description
Gigabit Ethernet Interface (GBETH)	• 2 channels • Compliant with IEEE802.3 • Compliant with IEEE802.1Qav, IEEE802.1Qat, and IEEE802.1AS • Compliant with IEEE1588-2008 with nano second timer in ch. 0 (main) and ch. 1 (sub) • Support for 10BASE, 100BASE, and 1000BASE • Support for full duplex and half duplex • Support for RGMII and MII Interfaces
CANFD Interface (CANFD)	• 6 channels • CAN-FD ISO 11898-1 (2015) compliant • Support for up to 8 MHz with payload transfer • Message buffer – 64 transmit message buffers per channel – 256 shared buffers for RXMB and FIFO buffers per channel
I3C Bus Interface (I3C)	• 1 channel • Support for 1.2 V and 1.8 V • Master or Slave mode selectable • Support for the multi-master • Compliant with MIPI I3C v1.0 and I3C Basic v1.0 The following functions are not supported: – Bridge device (I3C v1.0 and I3C Basic v1.0) – Asynchronous timing control async mode 2 & 3 (I3C v1.0) • Support for DMAC and event linking
I2C Bus Interface (RIIC)	• 9 channels • Master or Slave mode selectable • Support for the multi-master • Support for Standard mode (100 kHz), Fast mode (400 kHz), and Fast mode+ (1 MHz) • Support for DMAC and event linking
Renesas Serial Communication Interface (RSCI)	• 10 channels • 6 communication modes – Asynchronous interfaces – 8-bit clock synchronous interface – Simple IIC (host-only) – Simple SPI (with one chip select signal) – Smart card interface – Simple LIN (expanded SCIX mode) • 32-stage FIFO registers for transmission and reception • Clock source selectable from among four internal clock signals • Bit rate specifiable with the on-chip baud rate generator • Full-duplex and half-duplex communications • Data length: 7 to 9 bits • Bit-rate modulation • Double speed mode • Loopback function to enable self-diagnosis • Support for DMAC and event linking • Support for CRC calculation by the CRC unit

Table 1.3-6 Various Communication/Storage/Network Interfaces (3/3)

Item	Description
Renesas Serial Peripheral Interface (RSPI)	• 3 channels • SPI transfer facility The MOSI (master out slave in), MISO (master in slave out), SSL (slave select, 4 channels available), and RSPCK (SPI clock) signals enable serial transfer through SPI operation (four lines). The MOSI, MISO, and RSPCK signals enable clock-synchronous operation (three lines). Capable of handling serial transfer as a master or slave. • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or 20, 24, or 32 bits. 32-bit × 16-stage buffers for transmission and reception. Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits). • Buffered structure Independent 16 stages and channels for MOSI and MISO Double buffers for both transmission and reception • RSPCK can be stopped automatically with the reception buffer full for master reception. • Support for DMAC and event link • Support for CRC calculation by the CRC unit
CRC Calculator (CRC)	• 1 channel • CRC code generation for arbitrary amounts of data in 8-, 16-, or 32-bit units • Select any of four generating polynomials: – X32+X26+X23+X22+X16+X12+X11+X10+X8+X7+X5+X4+X2+X+1 (CRC-32) – X32+X28+X27+X26+X25+X23+X22 +X20+X19+X18+X14+X13+X11+X10+X9+X8+X6+1 (CRC-32C) – X16+X15+X2+1(CRC-16) – X16+X12+X5+1 (CRC-CCITT) – X8+X2+X+1 (CRC-8) • Support for RSCI and RSPI interfaces
Serial Communication Interface with FIFO (SCIF)	• 1 channel • Asynchronous mode • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud-rate generator • Separate 16-byte FIFO registers for transmission and reception

Table 1.3-7 Extended-Function Timers

Item	Description
General-Purpose Timer (GPT)	• 32 bits × 16 channels • Counting up or down (sawtooth-wave), counting up and down (triangle-wave) selectable for all channels • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Enabling synchronized operation of the several counters between 2 units • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Automatic generation of three-phase PWM waveforms incorporating dead times through the combination of three counters • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: Software and compare-match • Generation of triggers for A/D converter conversion • Digital noise filter functions for signals on the input capture and external trigger pins • Event linking by the ELC • Support for phase counting mode
Port Output Enable for GPT (POEG)	• Controlling the output disable for GPT waveform output • Initiation by input level detection of GTETRG pins • Initiation by an output disable request from GPT • Initiation by detection of oscillation stopping or by software
Compare Match Timer W (CMTW)	• 32 bits × 8 channels • Compare-match, input-capture input, and output-comparison output are available (ch. 0 to ch. 3) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events
Watchdog Timer (WDT)	• 4 channels • A counter underflow can reset the LSI.
General Timer (GTM)	• 32 bits × 8 channels • Two operating modes: – Interval timer mode – Free-running comparison mode
Real Time Clock (RTC)	• A 100-year calendar from 2000 to 2099 • BCD code display • Clock source is an oscillator dedicated to RTC (32.768-kHz) • Automatic adjustment function for leap years • Alarm function

Table 1.3-8 Audio

Item	Description
Sampling Rate Converter Unit (SCU)	• 10 channels • Sampling rate: Up to192 kHz • Asynchronous/synchronous sampling rate conversions are available. • Support for resolutions of up to 24 bits • High-sound-quality type (THD + N*1 is −132 dB) and general-sound-quality type (THD + N*1 is −96 dB) • Automatically generates antialiasing filter coefficients • Four modules support one, two, four, six, or eight channels, and six modules support one or two channels. *Note 1.* Total harmonic distortion plus noise
Audio Clock Generator Unit (ADG)	• Supplies clock signals to the SSIU, SCU and SPDIF module.
Direct Access Memory Controller for Audio (ADMAC)	• Allows transfer of L/R data via I2S • 29 channels • Controls data transfer between the audio modules (SSIU, SCU)
Serial Sound Interface Unit (SSIU)	• 10 channels for half-duplex communication with transmit or receive function • 5 channels for full-duplex communication (full-duplex pairing: ch. 0 & 9, ch.1 & 2, ch. 3 & 4, ch. 5 & 6, ch. 7 & 8) • Support for I2S, monaural, and TDM audio formats • Support for master and slave functions • Generation of programmable word clocks and bit clocks • Multi-channel formats • Support for 8, 16, 18, 20, 22, 24, and 32-bit data formats • Support for WS (word select) signal continuation with which the WS signal is not stopped • Support for DMAC
SPDIF Interface (SPDIF)	• 3 channels • Support for the IEC 60958 standard (stereo and consumer use modes only) • Sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz • Audio word sizes of 16 to 24 bits per sample • Bi-phase mark encoding • Double buffered data • Parity encoded serial data • Support for DMAC
Pulse Density Modulation (PDM)	• 6 channels • Direction: Input • Sampling rate: 8, 10, 12, 15, 16, 20, 24, 25, 30, 40, or 48 kHz • Capable of filtering 1-bit digital input data and converting them into 20-bit or 16-bit digital data • Support for the stereo microphone (L/R sampling by rising/falling clock edge) • Support for the sound activity detector to wake up CPU from WFI • Support for DMAC

Table 1.3-9 12-bit Analog to Digital Converter

Item	Description
A/D Converter (ADC0)	• 24 channels • Resolution: 12 bits • Input range: 0 V to 1.8 V • Conversion rate: 2.5 Msps, 2.0 Msps, 1.0 Msps, 0.5 Msps, 0.25 Msps • Operation mode: Single scan, continuous scan, group scan • Condition for starting A/D conversion – Software trigger – Asynchronous trigger: External ADTRG trigger supported – Synchronous trigger: ELC and GPT timers • Interrupt sources: A/D scan end, window compare match, compare match/mismatch, data register overwrite

Table 1.3-10 Internal Sensors

Item	Description
Temperature Sensor Unit (TSU)	• 2 channels for internal temperature • Includes a 12-bit A/D convertor per unit • Resolution: 0.0625°C/code • Rang: −40°C to 125°C • Precision: ±5°C • Conversion rate: 14.9 ksps • Operation mode: Single scan • Condition for starting measurement – Software trigger – Synchronous trigger: ELC • Interrupt sources: Conversion end, window compare match

Table 1.3-11 Security

Item	Description
Trusted Secure IP (option)	• Security algorism – Common key encryption: AES – Non-common key encryption: RSA, ECC • Other features – TRNG (true-random number generator) – Hash value generation: SHA-1, SHA-224, SHA-256, GHASH – Support for unique ID

Table 1.3-12 General-Purpose I/O Pins

Item	Description
General-purpose I/O ports (GPIO)	• Multiple I/O pins: 86 pins • Selectable: Pulling up or down by register settings • Selectable: N-ch. open-drain mode, Schmitt mode • 3.3-V tolerant pins available for use: 75 • 1.8-V tolerant pins available for use: 2 • Selectable IO-voltages for eight power blocks (7 blocks: 1.8 V or 3.3 V; 1 block: 1.2 V or 1.8 V)

Table 1.3-13 Power Supply Voltage

Item	Description
Power supply voltage	• VDD (core): 0.8 V • VDD (CA55): 0.8 V or 0.9 V • VDD (ADC, TSU, OTP): 1.8 V • VDD (DDR IO): 1.1 V, 0.6 V (only 0.6 V: for LPDDR4X) • VDD (MIPI DPHY): 1.2 V, 1.8 V (only 1.8 V: for MIPI CSI-2) • VDD (others): 1.8 V, 3.3 V

Table 1.3-14 Temperature Range

Item	Description
Junction temperature (Tj)	• −40°C to +125°C

Table 1.3-15 Quality Level

Item	Description
Quality level	• Industrial usage, etc.

Table 1.3-16 Package

Item	Description
Package	• 840-pin FCBGA, 15-mm square, 0.50-mm pitch

1.4 Block Diagram

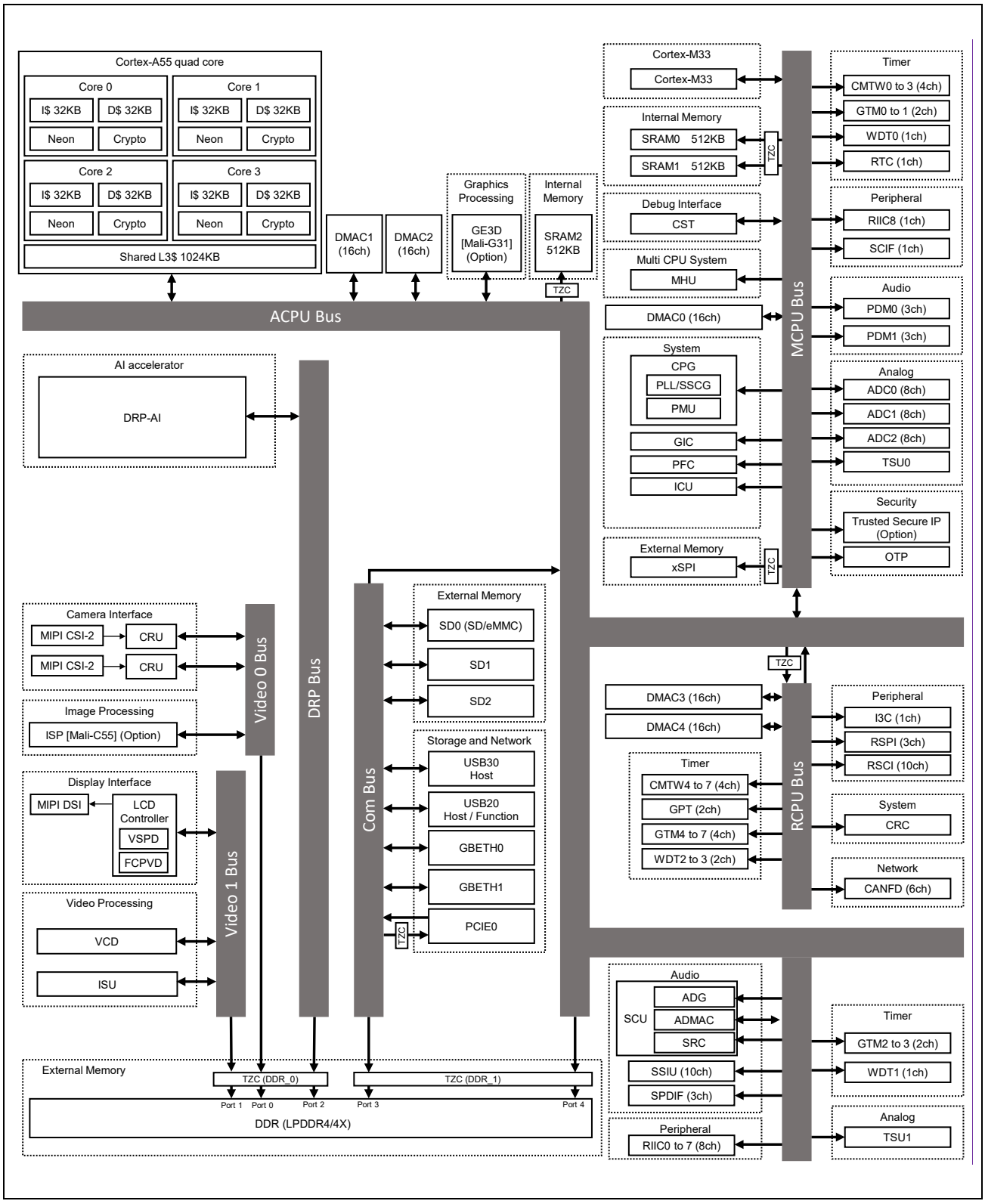


Figure 1.4-1 Block Diagram

Table 1.4-1 List of Units (1/2)

Unit Name	Unit Number	Function
ADC	ADC0 to ADC2	A/D converter
ADG	—	Audio clock generator
ADMAC	—	DMAC for audio
CA55	—	Arm Cortex-A55
CANFD	CANFD0	CAN-FD interface
CM33	—	Arm Cortex-M33
CMTW	CMTW0 to CMTW7	Compare match timer
CPG	—	Clock pulse generator
CRC	—	CRC operation unit
CRU	CRU0, CRU1	Camera data receive unit (MIPI CSI-2 interface)
CST	—	Debug interface (Arm CoreSight)
DDR	DDR0	LPDDR4/4X controller
DMAC	DMAC0 to DMAC4 (each 16 ch.)	Direct memory access (DMA) controller
DRP-AI	DRP0 and AI-MAC	AI accelerator
ELC	—	Event link controller
GBETH	GBETH0, GBETH1	Gigabit Ethernet interface
GE3D	—	3D graphics engine
GIC	—	Generic interrupt controller
GPT	GPT0, GPT1 (each 16 ch.)	General purpose timer
GTM	GTM0 to GTM7	General timer
GPV	—	Global programmers view
I3C	I3C0	I3C bus interface
ICU	—	Interrupt control unit
ISP	—	Image signal processor
ISU	—	Image scale unit
LCDC	—	LCD controller
MHU	—	Message handling unit
OTP	—	One time programmable memory
PCIE	PCIE0	PCIe Express 3.0 interface
PCU	—	Power control unit
PDM	PDM0, PDM1	Pulse density modulation (PDM) interface
PFC	—	Pin function controller
POEG	POEG0, POEG1	Port output enable for GPT
PMU	—	Power management unit
PWC	—	Power sequence controller
RIIC	RIIC0 to RIIC8	I2C bus interface
RSCI	RSCI0 to RSCI9	Serial communication interface
RSPI	RSPI0 to RSPI2	Serial peripheral interface
RTC	—	Real time clock
SCIF	SCIF0	Serial communication interface with FIFO
SD	SD0 to SD2	SD/MMC host interface
Secure IP	—	Trusted secure IP

Table 1.4-2 List of Units (2/2)

Unit Name	Unit Number	Functional Overview
SRAM	SRAM0 to SRAM2	SRAM
SRC	—	Sampling rate controller
SSIU	—	Serial sound interface unit
SYC	—	System counter
SYS	—	System controller
SYSTEM BUS	—	Internal bus
ACPU Bus	—	A bus connected to Cortex-A55, DDR memory controllers, SRAM, and its peripheral units
RCPU Bus	—	A bus connected to its peripheral units
MCPU Bus	—	A bus connected to Cortex-M33, SRAM, its peripheral units, and the system control units
DRP Bus	—	A bus connected to DRP-AI and DDR memory controllers
Video 0 Bus Video 1 Bus	—	A bus connected to image processing units and DDR memory controllers
COM Bus	—	A bus connected to communication interface units and DDR memory controllers
TSU	TSU0, TSU1	Temperature sensor unit
TZC	—	CoreLink™ TrustZone Address Space Controller
USB2	USB20	USB2.0 host / function interface
USB3	USB30	USB3.2 host interface
VCD	—	H.265/H.264 multi codec
WDT	WDT0 to WDT3	Watchdog timer
xSPI	xSPI0	xSPI controller

Section 2 Pin

This section describes the pins of this LSI.

2.1 Pin Assignment

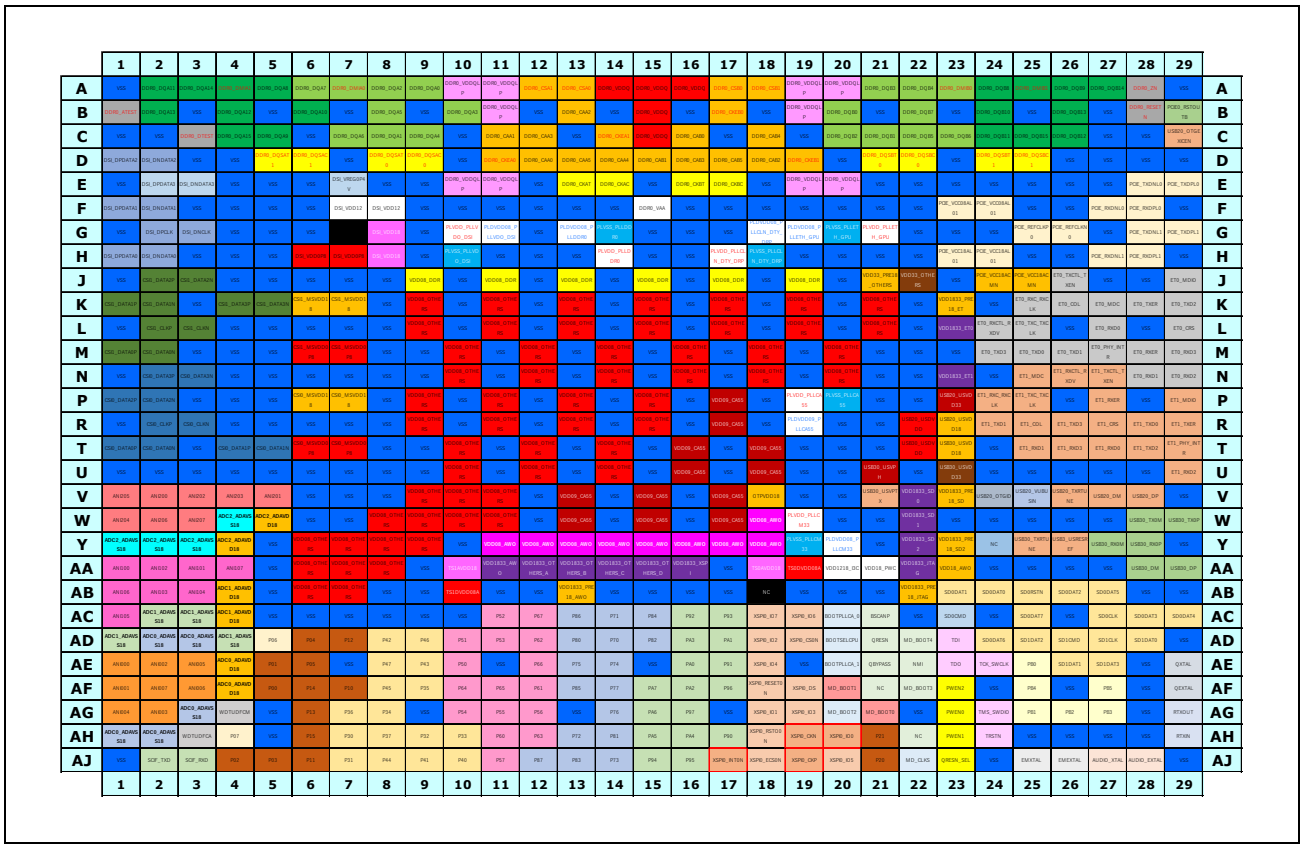


Figure 2.1-1 Pin Assignment (Top view)

Table 2.1-1 Ball Numbers and External Pin Names (1/8)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
A1	V_{SS}	B1	DDR0_ATEST	C1	V_{SS}	D1	DSI_DPDATA2
A2	DDR0_DQA11	B2	DDR0_DQA13	C2	V_{SS}	D2	DSI_DNDATA2
A3	DDR0_DQA14	B3	V_{SS}	C3	DDR0_DTEST	D3	V_{SS}
A4	DDR0_DMIA1	B4	DDR0_DQA12	C4	DDR0_DQA15	D4	V_{SS}
A5	DDR0_DQA8	B5	V_{SS}	C5	DDR0_DQA9	D5	DDR0_DQSAT1
A6	DDR0_DQA7	B6	DDR0_DQA10	C6	V_{SS}	D6	DDR0_DQSAC1
A7	DDR0_DMIA0	B7	V_{SS}	C7	DDR0_DQA6	D7	V_{SS}
A8	DDR0_DQA2	B8	DDR0_DQA5	C8	DDR0_DQA1	D8	DDR0_DQSAT0
A9	DDR0_DQA0	B9	V_{SS}	C9	DDR0_DQA4	D9	DDR0_DQSAC0
A10	DDR0_VDDQLP	B10	DDR0_DQA3	C10	V_{SS}	D10	V_{SS}
A11	DDR0_VDDQLP	B11	DDR0_VDDQLP	C11	DDR0_CAA1	D11	DDR0_CKEA0
A12	DDR0_CSA1	B12	V_{SS}	C12	DDR0_CAA3	D12	DDR0_CAA0
A13	DDR0_CSA0	B13	DDR0_CAA2	C13	V_{SS}	D13	DDR0_CAA5
A14	DDR0_VDDQ	B14	V_{SS}	C14	DDR0_CKEA1	D14	DDR0_CAA4
A15	DDR0_VDDQ	B15	DDR0_VDDQ	C15	DDR0_VDDQ	D15	DDR0_CAB1
A16	DDR0_VDDQ	B16	V_{SS}	C16	DDR0_CAB0	D16	DDR0_CAB3
A17	DDR0_CSB0	B17	DDR0_CKEB0	C17	V_{SS}	D17	DDR0_CAB5
A18	DDR0_CSB1	B18	V_{SS}	C18	DDR0_CAB4	D18	DDR0_CAB2
A19	DDR0_VDDQLP	B19	DDR0_VDDQLP	C19	V_{SS}	D19	DDR0_CKEB1
A20	DDR0_VDDQLP	B20	DDR0_DQB0	C20	DDR0_DQB2	D20	V_{SS}
A21	DDR0_DQB3	B21	V_{SS}	C21	DDR0_DQB1	D21	DDR0_DQSBT0
A22	DDR0_DQB4	B22	DDR0_DQB7	C22	DDR0_DQB5	D22	DDR0_DQSBC0
A23	DDR0_DMIB0	B23	V_{SS}	C23	DDR0_DQB6	D23	V_{SS}
A24	DDR0_DQB8	B24	DDR0_DQB10	C24	DDR0_DQB11	D24	DDR0_DQSBT1
A25	DDR0_DMIB1	B25	V_{SS}	C25	DDR0_DQB15	D25	DDR0_DQSBC1
A26	DDR0_DQB9	B26	DDR0_DQB13	C26	DDR0_DQB12	D26	V_{SS}
A27	DDR0_DQB14	B27	V_{SS}	C27	V_{SS}	D27	V_{SS}
A28	DDR0_ZN	B28	DDR0_RESETN	C28	V_{SS}	D28	V_{SS}
A29	V_{SS}	B29	PCIE0_RSTOUTB	C29	USB20_OTGEXICEN	D29	V_{SS}

Table 2.1-1 Ball Numbers and External Pin Names (2/8)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
E1	V_{SS}	F1	DSI_DPDATA1	G1	V_{SS}	H1	DSI_DPDATA0
E2	DSI_DPDATA3	F2	DSI_DNDATA1	G2	DSI_DPCLK	H2	DSI_DNDATA0
E3	DSI_DNDATA3	F3	V_{SS}	G3	DSI_DNCLK	H3	V_{SS}
E4	V_{SS}	F4	V_{SS}	G4	V_{SS}	H4	V_{SS}
E5	V_{SS}	F5	V_{SS}	G5	V_{SS}	H5	V_{SS}
E6	V_{SS}	F6	V_{SS}	G6	V_{SS}	H6	DSI_VDD0P8
E7	DSI_VREG0P4V	F7	DSI_VDD12	G7	—	H7	DSI_VDD0P8
E8	V_{SS}	F8	DSI_VDD12	G8	DSI_VDD18	H8	DSI_VDD18
E9	V_{SS}	F9	V_{SS}	G9	V_{SS}	H9	V_{SS}
E10	DDR0_VDDQLP	F10	V_{SS}	G10	PLVDD_PLLVDO_DSI	H10	PLVSS_PLLVDO_DSI
E11	DDR0_VDDQLP	F11	V_{SS}	G11	PLDVDD08_PLLVDO_DSI	H11	V_{SS}
E12	V_{SS}	F12	V_{SS}	G12	V_{SS}	H12	V_{SS}
E13	DDR0_CKAT	F13	V_{SS}	G13	PLDVDD08_PLLDDR0	H13	V_{SS}
E14	DDR0_CKAC	F14	V_{SS}	G14	PLVSS_PLLDDR0	H14	PLVDD_PLLDDR0
E15	V_{SS}	F15	DDR0_VAA	G15	V_{SS}	H15	V_{SS}
E16	DDR0_CKBT	F16	V_{SS}	G16	V_{SS}	H16	V_{SS}
E17	DDR0_CKBC	F17	V_{SS}	G17	V_{SS}	H17	PLVDD_PLLCLN_DTY_DRP
E18	V_{SS}	F18	V_{SS}	G18	PLDVDD08_PLLCLN_DTY_DRP	H18	PLVSS_PLLCLN_DTY_DRP
E19	DDR0_VDDQLP	F19	V_{SS}	G19	PLDVDD08_PLLETH_GPU	H19	V_{SS}
E20	DDR0_VDDQLP	F20	V_{SS}	G20	PLVSS_PLLETH_GPU	H20	V_{SS}
E21	V_{SS}	F21	V_{SS}	G21	PLVDD_PLLETH_GPU	H21	V_{SS}
E22	V_{SS}	F22	V_{SS}	G22	V_{SS}	H22	V_{SS}
E23	V_{SS}	F23	PCIE_VCC08AL01	G23	V_{SS}	H23	PCIE_VCC18AL01
E24	V_{SS}	F24	PCIE_VCC08AL01	G24	V_{SS}	H24	PCIE_VCC18AL01
E25	V_{SS}	F25	V_{SS}	G25	PCIE_REFCLKP0	H25	V_{SS}
E26	V_{SS}	F26	V_{SS}	G26	PCIE_REFCLKN0	H26	V_{SS}
E27	V_{SS}	F27	PCIE_RXDNL0	G27	V_{SS}	H27	PCIE_RXDNL1
E28	PCIE_TXDNL0	F28	PCIE_RXDPL0	G28	PCIE_TXDNL1	H28	PCIE_RXDPL1
E29	PCIE_TXDPL0	F29	V_{SS}	G29	PCIE_TXDPL1	H29	V_{SS}

Table 2.1-1 Ball Numbers and External Pin Names (3/8)

Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name	Ball Num.	External Pin Name
J1	V_{SS}	K1	CSI1_DATA1P	L1	V_{SS}	M1	CSI1_DATA0P
J2	CSI1_DATA2P	K2	CSI1_DATA1N	L2	CSI1_CLKP	M2	CSI1_DATA0N
J3	CSI1_DATA2N	K3	V_{SS}	L3	CSI1_CLKN	M3	V_{SS}
J4	V_{SS}	K4	CSI1_DATA3P	L4	V_{SS}	M4	V_{SS}
J5	V_{SS}	K5	CSI1_DATA3N	L5	V_{SS}	M5	V_{SS}
J6	V_{SS}	K6	CSI1_MSVDD18	L6	V_{SS}	M6	CSI1_MSVDD0P8
J7	V_{SS}	K7	CSI1_MSVDD18	L7	V_{SS}	M7	CSI1_MSVDD0P8
J8	V_{SS}	K8	V_{SS}	L8	V_{SS}	M8	V_{SS}
J9	VDD08_DDR	K9	VDD08_OTHERS	L9	VDD08_OTHERS	M9	V_{SS}
J10	V_{SS}	K10	VSS	L10	V_{SS}	M10	VDD08_OTHERS
J11	VDD08_DDR	K11	VDD08_OTHERS	L11	VDD08_OTHERS	M11	V_{SS}
J12	V_{SS}	K12	V_{SS}	L12	V_{SS}	M12	VDD08_OTHERS
J13	VDD08_DDR	K13	VDD08_OTHERS	L13	VDD08_OTHERS	M13	V_{SS}
J14	V_{SS}	K14	V_{SS}	L14	V_{SS}	M14	VDD08_OTHERS
J15	VDD08_DDR	K15	VDD08_OTHERS	L15	VDD08_OTHERS	M15	V_{SS}
J16	V_{SS}	K16	V_{SS}	L16	V_{SS}	M16	VDD08_OTHERS
J17	VDD08_DDR	K17	VDD08_OTHERS	L17	VDD08_OTHERS	M17	V_{SS}
J18	V_{SS}	K18	V_{SS}	L18	V_{SS}	M18	VDD08_OTHERS
J19	VDD08_DDR	K19	VDD08_OTHERS	L19	VDD08_OTHERS	M19	V_{SS}
J20	V_{SS}	K20	V_{SS}	L20	V_{SS}	M20	VDD08_OTHERS
J21	VDD33_PRE18_OTHERS	K21	VDD08_OTHERS	L21	VDD08_OTHERS	M21	V_{SS}
J22	VDD33_OTHERS	K22	V_{SS}	L22	V_{SS}	M22	V_{SS}
J23	V_{SS}	K23	VDD1833_PRE18_ET	L23	VDD1833_ET0	M23	V_{SS}
J24	PCIE_VCC18ACMN	K24	V_{SS}	L24	ET0_RXCTL_RXDV	M24	ET0_TXD3
J25	PCIE_VCC18ACMN	K25	ET0_RXC_RXCLK	L25	ET0_TXC_TXCLK	M25	ET0_TXD0
J26	ET0_TXCTL_TXEN	K26	ET0_COL	L26	V_{SS}	M26	ET0_TXD1
J27	V_{SS}	K27	ET0_MDC	L27	ET0_RXD0	M27	ET0_PHY_INTR
J28	V_{SS}	K28	ET0_TXER	L28	V_{SS}	M28	ET0_RXER
J29	ET0_MDIO	K29	ET0_TXD2	L29	ET0_CRS	M29	ET0_RXD3

Table 2.1-1 Ball Numbers and External Pin Names (4/8)

Ball Num.	External Pin Name
N1	V_{SS}
N2	CSI0_DATA3P
N3	CSI0_DATA3N
N4	V_{SS}
N5	V_{SS}
N6	V_{SS}
N7	V_{SS}
N8	V_{SS}
N9	V_{SS}
N10	VDD08_OTHERS
N11	V_{SS}
N12	VDD08_OTHERS
N13	V_{SS}
N14	VDD08_OTHERS
N15	V_{SS}
N16	VDD08_OTHERS
N17	V_{SS}
N18	VDD08_OTHERS
N19	V_{SS}
N20	VDD08_OTHERS
N21	V_{SS}
N22	V_{SS}
N23	VDD1833_ET1
N24	V_{SS}
N25	ET1_MDC
N26	ET1_RXCTL_RXDV
N27	ET1_TXCTL_TXEN
N28	ET0_RXD1
N29	ET0_RXD2

Ball Num.	External Pin Name
P1	CSI0_DATA2P
P2	CSI0_DATA2N
P3	V_{SS}
P4	V_{SS}
P5	V_{SS}
P6	CSI0_MSVDD18
P7	CSI0_MSVDD18
P8	V_{SS}
P9	VDD08_OTHERS
P10	V_{SS}
P11	VDD08_OTHERS
P12	V_{SS}
P13	VDD08_OTHERS
P14	V_{SS}
P15	VDD08_OTHERS
P16	V_{SS}
P17	VDD09_CA55
P18	V_{SS}
P19	PLVDD_PLLCA55
P20	PLVSS_PLLCA55
P21	V_{SS}
P22	V_{SS}
P23	USB20_USVDD33
P24	ET1_RXC_RXCLK
P25	ET1_TXC_TXCLK
P26	V_{SS}
P27	ET1_RXER
P28	V_{SS}
P29	ET1_MDIO

Ball Num.	External Pin Name
R1	V_{SS}
R2	CSI0_CLKP
R3	CSI0_CLKN
R4	V_{SS}
R5	V_{SS}
R6	V_{SS}
R7	V_{SS}
R8	V_{SS}
R9	VDD08_OTHERS
R10	V_{SS}
R11	VDD08_OTHERS
R12	V_{SS}
R13	VDD08_OTHERS
R14	V_{SS}
R15	VDD08_OTHERS
R16	V_{SS}
R17	VDD09_CA55
R18	V_{SS}
R19	PLDVDD09_PLLCA55
R20	V_{SS}
R21	V_{SS}
R22	USB20_USDVDD
R23	USB20_USVDD18
R24	ET1_TXD1
R25	ET1_COL
R26	ET1_TXD3
R27	ET1_CRS
R28	ET1_TXD0
R29	ET1_TXER

Ball Num.	External Pin Name
T1	CSI0_DATA0P
T2	CSI0_DATA0N
T3	V_{SS}
T4	CSI0_DATA1P
T5	CSI0_DATA1N
T6	CSI0_MSVDD0P8
T7	CSI0_MSVDD0P8
T8	V_{SS}
T9	V_{SS}
T10	VDD08_OTHERS
T11	V_{SS}
T12	VDD08_OTHERS
T13	V_{SS}
T14	VDD08_OTHERS
T15	V_{SS}
T16	VDD09_CA55
T17	V_{SS}
T18	VDD09_CA55
T19	V_{SS}
T20	V_{SS}
T21	V_{SS}
T22	USB30_USDVDD
T23	USB30_USVDD18
T24	V_{SS}
T25	ET1_RXD1
T26	ET1_RXD3
T27	ET1_RXD0
T28	ET1_TXD2
T29	ET1_PHY_INTR

Table 2.1-1 Ball Numbers and External Pin Names (5/8)

Ball Num.	External Pin Name
U1	V_{SS}
U2	V_{SS}
U3	V_{SS}
U4	V_{SS}
U5	V_{SS}
U6	V_{SS}
U7	V_{SS}
U8	V_{SS}
U9	V_{SS}
U10	VDD08_OTHERS
U11	V_{SS}
U12	VDD08_OTHERS
U13	V_{SS}
U14	VDD08_OTHERS
U15	V_{SS}
U16	VDD09_CA55
U17	V_{SS}
U18	VDD09_CA55
U19	V_{SS}
U20	V_{SS}
U21	USB30_USVPH
U22	V_{SS}
U23	USB30_USVDD33
U24	V_{SS}
U25	V_{SS}
U26	V_{SS}
U27	V_{SS}
U28	V_{SS}
U29	ET1_RXD2

Ball Num.	External Pin Name
V1	ANI205
V2	ANI200
V3	ANI202
V4	ANI203
V5	ANI201
V6	V_{SS}
V7	V_{SS}
V8	V_{SS}
V9	VDD08_OTHERS
V10	VDD08_OTHERS
V11	VDD08_OTHERS
V12	V_{SS}
V13	VDD09_CA55
V14	V_{SS}
V15	VDD09_CA55
V16	V_{SS}
V17	VDD09_CA55
V18	OTPVDD18
V19	V_{SS}
V20	V_{SS}
V21	USB30_USVPTX
V22	VDD1833_SD0
V23	VDD1833_PRE18_SD
V24	USB20_OTGID
V25	USB20_VUBUSIN
V26	USB20_TXRTUNE
V27	USB20_DM
V28	USB20_DP
V29	V_{SS}

Ball Num.	External Pin Name
W1	ANI204
W2	ANI206
W3	ANI207
W4	ADC2_ADAVSS18
W5	ADC2_ADAVDD18
W6	V_{SS}
W7	V_{SS}
W8	VDD08_OTHERS
W9	VDD08_OTHERS
W10	VDD08_OTHERS
W11	VDD08_OTHERS
W12	V_{SS}
W13	VDD09_CA55
W14	V_{SS}
W15	VDD09_CA55
W16	V_{SS}
W17	VDD09_CA55
W18	VDD08_AWO
W19	PLVDD_PLLCM33
W20	V_{SS}
W21	V_{SS}
W22	VDD1833_SD1
W23	V_{SS}
W24	V_{SS}
W25	V_{SS}
W26	V_{SS}
W27	V_{SS}
W28	USB30_TX0M
W29	USB30_TX0P

Ball Num.	External Pin Name
Y1	ADC2_ADAVSS18
Y2	ADC2_ADAVSS18
Y3	ADC2_ADAVSS18
Y4	ADC2_ADAVDD18
Y5	V_{SS}
Y6	VDD08_OTHERS
Y7	VDD08_OTHERS
Y8	VDD08_OTHERS
Y9	VDD08_OTHERS
Y10	V_{SS}
Y11	VDD08_AWO
Y12	VDD08_AWO
Y13	VDD08_AWO
Y14	VDD08_AWO
Y15	VDD08_AWO
Y16	VDD08_AWO
Y17	VDD08_AWO
Y18	VDD08_AWO
Y19	PLVSS_PLLCM33
Y20	PLDVDD08_PLLCM33
Y21	V_{SS}
Y22	VDD1833_SD2
Y23	VDD1833_PRE18_SD2
Y24	NC
Y25	USB30_TXRTUNE
Y26	USB3_USRESREF
Y27	USB30_RX0M
Y28	USB30_RX0P
Y29	V_{SS}

Table 2.1-1 Ball Numbers and External Pin Names (6/8)

Ball Num.	External Pin Name
AA1	ANI100
AA2	ANI102
AA3	ANI101
AA4	ANI107
AA5	V_{SS}
AA6	VDD08_OTHERS
AA7	VDD08_OTHERS
AA8	VDD08_OTHERS
AA9	V_{SS}
AA10	TS1AVDD18
AA11	VDD1833_AWO
AA12	VDD1833_OTHERS_A
AA13	VDD1833_OTHERS_B
AA14	VDD1833_OTHERS_C
AA15	VDD1833_OTHERS_D
AA16	VDD1833_XSPI
AA17	V_{SS}
AA18	TS0AVDD18
AA19	TS0DVDD08A
AA20	VDD1218_I3C
AA21	VDD18_PWC
AA22	VDD1833_JTAG
AA23	VDD18_AWO
AA24	V_{SS}
AA25	V_{SS}
AA26	V_{SS}
AA27	V_{SS}
AA28	USB30_DM
AA29	USB30_DP

Ball Num.	External Pin Name
AB1	ANI106
AB2	ANI103
AB3	ANI104
AB4	ADC1_ADAVDD18
AB5	V_{SS}
AB6	VDD08_OTHERS
AB7	VDD08_OTHERS
AB8	V_{SS}
AB9	V_{SS}
AB10	TS1DVDD08A
AB11	V_{SS}
AB12	V_{SS}
AB13	VDD1833_PRE18_AWO
AB14	V_{SS}
AB15	V_{SS}
AB16	V_{SS}
AB17	V_{SS}
AB18	NC
AB19	V_{SS}
AB20	V_{SS}
AB21	V_{SS}
AB22	VDD1833_PRE18_JTAG
AB23	SD0DAT1
AB24	SD0DAT0
AB25	SD0RSTN
AB26	SD0DAT2
AB27	SD0DAT5
AB28	V_{SS}
AB29	V_{SS}

Ball Num.	External Pin Name
AC1	ANI105
AC2	ADC1_ADAVSS18
AC3	ADC1_ADAVSS18
AC4	ADC1_ADAVDD18
AC5	V_{SS}
AC6	V_{SS}
AC7	V_{SS}
AC8	V_{SS}
AC9	V_{SS}
AC10	V_{SS}
AC11	P52
AC12	P67
AC13	P86
AC14	P71
AC15	P84
AC16	P92
AC17	P93
AC18	XSPI0_IO7
AC19	XSPI0_IO6
AC20	BOOTPLLCA_0
AC21	BSCANP
AC22	V_{SS}
AC23	SD0CMD
AC24	V_{SS}
AC25	SD0DAT7
AC26	V_{SS}
AC27	SD0CLK
AC28	SD0DAT3
AC29	SD0DAT4

Ball Num.	External Pin Name
AD1	ADC1_ADAVSS18
AD2	ADC0_ADAVSS18
AD3	ADC0_ADAVSS18
AD4	ADC1_ADAVSS18
AD5	P06
AD6	P04
AD7	P12
AD8	P42
AD9	P46
AD10	P51
AD11	P53
AD12	P62
AD13	P80
AD14	P70
AD15	P82
AD16	PA3
AD17	PA1
AD18	XSPI0_IO2
AD19	XSPI0_CS0N
AD20	BOOTSELCPU
AD21	QRESN
AD22	MD_BOOT4
AD23	TDI
AD24	SD0DAT6
AD25	SD1DAT2
AD26	SD1CMD
AD27	SD1CLK
AD28	SD1DAT0
AD29	V_{SS}

Table 2.1-1 Ball Numbers and External Pin Names (7/8)

Ball Num.	External Pin Name
AE1	ANI000
AE2	ANI002
AE3	ANI005
AE4	ADC0_ADAVDD18
AE5	P01
AE6	P05
AE7	V_{SS}
AE8	P47
AE9	P43
AE10	P50
AE11	V_{SS}
AE12	P66
AE13	P75
AE14	P74
AE15	V_{SS}
AE16	PA0
AE17	P91
AE18	XSPI0_IO4
AE19	V_{SS}
AE20	BOOTPLLCA_1
AE21	QBYPASS
AE22	NMI
AE23	TDO
AE24	TCK_SWCLK
AE25	PB0
AE26	SD1DAT1
AE27	SD1DAT3
AE28	V_{SS}
AE29	QXTAL

Ball Num.	External Pin Name
AF1	ANI001
AF2	ANI007
AF3	ANI006
AF4	ADC0_ADAVDD18
AF5	P00
AF6	P14
AF7	P10
AF8	P45
AF9	P35
AF10	P64
AF11	P65
AF12	P61
AF13	P85
AF14	P77
AF15	PA7
AF16	PA2
AF17	P96
AF18	XSPI0_RESET0N
AF19	XSPI0_DS
AF20	MD_BOOT1
AF21	NC
AF22	MD_BOOT3
AF23	PWEN2
AF24	V_{SS}
AF25	PB4
AF26	V_{SS}
AF27	PB5
AF28	V_{SS}
AF29	QEXTAL

Ball Num.	External Pin Name
AG1	ANI004
AG2	ANI003
AG3	ADC0_ADAVSS18
AG4	WDTUDFCM
AG5	V_{SS}
AG6	P13
AG7	P36
AG8	P34
AG9	V_{SS}
AG10	P54
AG11	P55
AG12	P56
AG13	V_{SS}
AG14	P76
AG15	PA6
AG16	P97
AG17	V_{SS}
AG18	XSPI0_IO1
AG19	XSPI0_IO3
AG20	MD_BOOT2
AG21	MD_BOOT0
AG22	V_{SS}
AG23	PWEN0
AG24	TMS_SWDIO
AG25	PB1
AG26	PB2
AG27	PB3
AG28	V_{SS}
AG29	RTXOUT

Ball Num.	External Pin Name
AH1	ADC0_ADAVSS18
AH2	ADC0_ADAVSS18
AH3	WDTUDFCA
AH4	P07
AH5	V_{SS}
AH6	P15
AH7	P30
AH8	P37
AH9	P32
AH10	P33
AH11	P60
AH12	P63
AH13	P72
AH14	P81
AH15	PA5
AH16	PA4
AH17	P90
AH18	XSPI0_RSTO0N
AH19	XSPI0_CKN
AH20	XSPI0_IO0
AH21	P21
AH22	NC
AH23	PWEN1
AH24	TRSTN
AH25	V_{SS}
AH26	V_{SS}
AH27	V_{SS}
AH28	V_{SS}
AH29	RTXIN

Table 2.1-1 Ball Numbers and External Pin Names (8/8)

Ball Num.	External Pin Name
AJ1	V_{SS}
AJ2	SCIF_TXD
AJ3	SCIF_RXD
AJ4	P02
AJ5	P03
AJ6	P11
AJ7	P31
AJ8	P44
AJ9	P41
AJ10	P40
AJ11	P57
AJ12	P87
AJ13	P83
AJ14	P73
AJ15	P94
AJ16	P95
AJ17	XSPI0_INT0N
AJ18	XSPI0_ECS0N
AJ19	XSPI0_CKP
AJ20	XSPI0_IO5
AJ21	P20
AJ22	MD_CLKS
AJ23	QRESN_SEL
AJ24	V_{SS}
AJ25	EMXTAL
AJ26	EMEXTAL
AJ27	AUDIO_XTAL
AJ28	AUDIO_EXTAL
AJ29	V_{SS}

Note: NC pins should be open.

2.2 External Pins

2.2.1 List of External Pins

Table 2.2-1 List of External Pins (1/12)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
QXTAL	Output	1.8	VDD18_AWO	Hi-Z	1.8-V OSC	Open for CLKIN into QEXTAL or always in use for the crystal resonator
QEXTAL	Input	1.8	VDD18_AWO	—	1.8-V OSC	Always in use
EMXTAL	Output	1.8	VDD18_AWO	Hi-Z	1.8-V OSC	Open
EMEXTAL	Input	1.8	VDD18_AWO	—	1.8-V OSC	V_{SS}
RTXOUT	Output	1.8	VDD18_AWO	Hi-Z	1.8-V OSC	Open
RTXIN	Input	1.8	VDD18_AWO	—	1.8-V OSC	V_{SS}
AUDIO_XTAL	Output	1.8	VDD18_AWO	Hi-Z	1.8-V OSC	Open
AUDIO_EXTAL	Input	1.8	VDD18_AWO	—	1.8-V OSC	V_{SS}
BOOTSELCPU	Input	1.8	VDD18_PWC	Pull down*2	1.8-V I/O	Always in use
BOOTPLLCA_1	Input	1.8	VDD18_PWC	Pull up*2	1.8-V I/O	Always in use
BOOTPLLCA_0	Input	1.8	VDD18_PWC	Pull down*2	1.8-V I/O	Always in use
MD_BOOT4	Input	1.8	VDD18_PWC	Pull down*2	1.8-V I/O	Always in use
MD_BOOT3	Input	1.8	VDD18_PWC	Pull down*2	1.8-V I/O	Always in use
MD_BOOT2	Input	1.8	VDD18_PWC	Pull up*2	1.8-V I/O	Always in use
MD_BOOT1	Input	1.8	VDD18_PWC	Pull up*2	1.8-V I/O	Always in use
MD_BOOT0	Input	1.8	VDD18_PWC	Pull down*2	1.8-V I/O	Always in use
MD_CLKS	Input	1.8	VDD18_PWC	Pull up*2	1.8-V I/O	Open
QRESN	Input	1.8	VDD18_PWC	—	1.8-V I/O	Always in use
NMI	Input	1.8	VDD18_PWC	—	1.8-V I/O	Pull down
QBYPASS	Input	1.8	VDD18_PWC	Pull down*2	1.8-V I/O	Open
BSCANP	Input	1.8	VDD18_PWC	Pull down*2	1.8-V I/O	Open
QRESNSEL	Input	1.8	VDD18_PWC	—	1.8-V I/O	Pull down
PWEN0	Output	1.8	VDD18_PWC	Low	1.8-V I/O	Open
PWEN1	Output	1.8	VDD18_PWC	Low	1.8-V I/O	Open
PWEN2	Output	1.8	VDD18_PWC	Low	1.8-V I/O	Open
TMS_SWDIO	Input / Output	1.8/3.3	VDD1833_JTAG	Hi-Z	3.3/1.8-V switching I/O (type 1)	Pull up
TCK_SWCLK	Input	1.8/3.3	VDD1833_JTAG	—	3.3/1.8-V switching I/O (type 1)	Pull up or pull down
TDO	Output	1.8/3.3	VDD1833_JTAG	Hi-Z*3	3.3/1.8-V switching I/O (type 1)	Open
TDI	Input	1.8/3.3	VDD1833_JTAG	—	3.3/1.8-V switching I/O (type 1)	Pull up or pull down
TRSTN	Input	1.8/3.3	VDD1833_JTAG	—	3.3/1.8-V switching I/O (type 1)	Pull down
VDD1833_JTAG	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_JTAG	—	1.8	—	—	—	Open*6
WDTUDFCM	Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 1)	Open
WDTUDFCA	Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 1)	Open
SCIF_RXD	Input	1.8/3.3	VDD1833_AWO	—	3.3/1.8-V switching I/O (type 1)	Pull up

Table 2.2-1 List of External Pins (2/12)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
SCIF_TXD	Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 1)	Open
ANIn00 to ANIn07 (n = 0 to 2)	Input	1.8	ADCn_ADAVDD18 (n = 0 to 2)	—	ADC I/O	Open
ADCn_ADAVDD18 (n = 0 to 2)	—	1.8	—	—	—	Always in use
ADCn_ADAVSS18 (n = 0 to 2)	—	—	—	—	—	Always in use
XSPI0_CKP	Output	1.8/3.3	VDD1833_XSPI	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
XSPI0_CKN	Output	1.8/3.3	VDD1833_XSPI	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
XSPI0_CS0N	Output	1.8/3.3	VDD1833_XSPI	Hi-Z	3.3/1.8-V switching I/O (type 1)	Open
XSPI0_DS	Input / Output	1.8/3.3	VDD1833_XSPI	Hi-Z	3.3/1.8-V switching I/O (type 3)	Pull up or pull down
XSPI0_IO0 to 7	Input / Output	1.8/3.3	VDD1833_XSPI	Hi-Z	3.3/1.8-V switching I/O (type 3)	Pull up or pull down
XSPI0_RESET0N	Output	1.8/3.3	VDD1833_XSPI	Hi-Z	3.3/1.8-V switching I/O (type 1)	Open
XSPI0_RSTO0N	Input	1.8/3.3	VDD1833_XSPI	—	3.3/1.8-V switching I/O (type 1)	Pull down
XSPI0_INT0N	Input	1.8/3.3	VDD1833_XSPI	—	3.3/1.8-V switching I/O (type 1)	Pull down
XSPI0_ECS0N	Input	1.8/3.3	VDD1833_XSPI	—	3.3/1.8-V switching I/O (type 1)	Pull down
VDD1833_XSPI	—	1.8/3.3	—	—	—	Open*6
SD0CLK	Output	1.8/3.3	VDD1833_SD0	Low	3.3/1.8-V switching I/O (type 3)	Open
SD0CMD	Input / Output	1.8/3.3	VDD1833_SD0	Hi-Z	3.3/1.8-V switching I/O (type 3)	Pull up or pull down
SD0DAT0 to 7	Input / Output	1.8/3.3	VDD1833_SD0	Hi-Z	3.3/1.8-V switching I/O (type 3)	Pull up or pull down
SD0RSTN	Output	1.8/3.3	VDD1833_SD0	Low	3.3/1.8-V switching I/O (type 3)	Open
VDD1833_SD0	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_SD	—	1.8	—	—	—	Open*6
SD1CLK	Output	1.8/3.3	VDD1833_SD1	Low	3.3/1.8-V switching I/O (type 3)	Open
SD1CMD	Input / Output	1.8/3.3	VDD1833_SD1	Hi-Z	3.3/1.8-V switching I/O (type 3)	Pull up or pull down
SD1DAT0 to 3	Input / Output	1.8/3.3	VDD1833_SD1	Hi-Z	3.3/1.8-V switching I/O (type 3)	Pull up or pull down
VDD1833_SD1	—	1.8/3.3	—	—	—	Open*6
VDD1833_SD2	—	1.8/3.3	—	—	—	Open
VDD1833_PRE18_SD2	—	1.8	—	—	—	Open
USB20_DP	Input / Output	3.3	USB20_USVDD33	Low	USB2 PHY	Open
USB20_DM	Input / Output	3.3	USB20_USVDD33	Low	USB2 PHY	Open

Table 2.2-1 List of External Pins (3/12)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
USB20_OTGID	Input	1.8	USB20_USVDD18	Hi-Z	USB2 PHY	Open
USB20_VUBUSIN*11	Input	3.3*4	USB20_USVDD33	Hi-Z	USB2 PHY	Open
USB20_OTGEXICEN	Output	3.3	VDD33_OTHERS	High	3.3-V I/O	Open
USB20_TXRTUNE	—	—	—	—	USB2 PHY	Open
USB20_USVDD33	—	3.3	—	—	—	V_{SS}
USB20_USVDD18	—	1.8	—	—	—	V_{SS}
USB20_USDVDD*10	—	0.8	—	—	—	V_{SS}
USB30_DP	Input / Output	3.3	USB30_USVDD33	Low	USB2 PHY	Open
USB30_DM	Input / Output	3.3	USB30_USVDD33	Low	USB2 PHY	Open
USB30_RX0M	Input	0.8	USB30_USVPTX	—	USB3 PHY	Open
USB30_RX0P	Input	0.8	USB30_USVPTX	—	USB3 PHY	Open
USB30_TX0M	Output	0.8	USB30_USVPTX	Hi-Z	USB3 PHY	Open
USB30_TX0P	Output	0.8	USB30_USVPTX	Hi-Z	USB3 PHY	Open
USB3_USRESREF	—	—	—	—	USB3 PHY	Open
USB30_TXRTUNE	—	—	—	—	USB2 PHY	Open
USB30_USVPH	—	1.8	—	—	—	V_{SS}
USB30_USVPTX	—	0.8	—	—	—	V_{SS}
USB30_USVDD33	—	3.3	—	—	—	V_{SS}
USB30_USVDD18	—	1.8	—	—	—	V_{SS}
USB30_USDVDD*10	—	0.8	—	—	—	V_{SS}
PCIE_TXDPL0	Output	1.8	PCIE_VCC18AL01	Hi-Z	PCIE PHY	Open*9
PCIE_TXDNL0	Output	1.8	PCIE_VCC18AL01	Hi-Z	PCIE PHY	Open*9
PCIE_TXDPL1	Output	1.8	PCIE_VCC18AL01	Hi-Z	PCIE PHY	Open*9
PCIE_TXDNL1	Output	1.8	PCIE_VCC18AL01	Hi-Z	PCIE PHY	Open*9
PCIE_RXDPL0	Input	1.8	PCIE_VCC18AL01	—	PCIE PHY	Open
PCIE_RXDNL0	Input	1.8	PCIE_VCC18AL01	—	PCIE PHY	Open
PCIE_RXDPL1	Input	1.8	PCIE_VCC18AL01	—	PCIE PHY	Open
PCIE_RXDNL1	Input	1.8	PCIE_VCC18AL01	—	PCIE PHY	Open
PCIE_REFCLKP0	Input	1.8	PCIE_VCC18AL01	—	PCIE PHY	Open
PCIE_REFCLKN0	Input	1.8	PCIE_VCC18AL01	—	PCIE PHY	Open
PCIE0_RSTOUTB	Output	3.3	VDD33_OTHERS	High	3.3-V I/O	Open
PCIE_VCC18ACMN	—	1.8	—	—	—	V_{SS}
PCIE_VCC18AL01	—	1.8	—	—	—	V_{SS}
PCIE_VCC08AL01	—	0.8	—	—	—	V_{SS}
ET0_MDIO	Input / Output	1.8/3.3	VDD1833_ET0	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
ET0_MDC	Output	1.8/3.3	VDD1833_ET0	Low	3.3/1.8-V switching I/O (type 3)	Open
ET0_RXCTL_RXDV	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_TXCTL_TXEN	Output	1.8/3.3	VDD1833_ET0	Low	3.3/1.8-V switching I/O (type 3)	Open
ET0_TXER	Output	1.8/3.3	VDD1833_ET0	Low	3.3/1.8-V switching I/O (type 3)	Open
ET0_RXER	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_RXC_RXCLK	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_TXC_TXCLK	Input / Output	1.8/3.3	VDD1833_ET0	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open

Table 2.2-1 List of External Pins (4/12)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
ET0_CRS	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_COL	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_TXD0	Output	1.8/3.3	VDD1833_ET0	Low	3.3/1.8-V switching I/O (type 3)	Open
ET0_TXD1	Output	1.8/3.3	VDD1833_ET0	Low	3.3/1.8-V switching I/O (type 3)	Open
ET0_TXD2	Output	1.8/3.3	VDD1833_ET0	Low	3.3/1.8-V switching I/O (type 3)	Open
ET0_TXD3	Output	1.8/3.3	VDD1833_ET0	Low	3.3/1.8-V switching I/O (type 3)	Open
ET0_RXD0	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_RXD1	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_RXD2	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_RXD3	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET0_PHYINTR	Input	1.8/3.3	VDD1833_ET0	—	3.3/1.8-V switching I/O (type 3)	Pull down
VDD1833_ET0	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_ET	—	1.8	—	—	—	Open*6
ET1_MDIO	Input / Output	1.8/3.3	VDD1833_ET1	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
ET1_MDC	Output	1.8/3.3	VDD1833_ET1	Low	3.3/1.8-V switching I/O (type 3)	Open
ET1_RXCTL_RXDV	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_TXCTL_TXEN	Output	1.8/3.3	VDD1833_ET1	Low	3.3/1.8-V switching I/O (type 3)	Open
ET1_TXER	Output	1.8/3.3	VDD1833_ET1	Low	3.3/1.8-V switching I/O (type 3)	Open
ET1_RXER	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_RXC_RXCLK	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_TXC_TXCLK	Input / Output	1.8/3.3	VDD1833_ET1	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
ET1_CRS	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_COL	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_TXD0	Output	1.8/3.3	VDD1833_ET1	Low	3.3/1.8-V switching I/O (type 3)	Open

Table 2.2-1 List of External Pins (5/12)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
ET1_TXD1	Output	1.8/3.3	VDD1833_ET1	Low	3.3/1.8-V switching I/O (type 3)	Open
ET1_TXD2	Output	1.8/3.3	VDD1833_ET1	Low	3.3/1.8-V switching I/O (type 3)	Open
ET1_TXD3	Output	1.8/3.3	VDD1833_ET1	Low	3.3/1.8-V switching I/O (type 3)	Open
ET1_RXD0	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_RXD1	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_RXD2	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_RXD3	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
ET1_PHYINTR	Input	1.8/3.3	VDD1833_ET1	—	3.3/1.8-V switching I/O (type 3)	Pull down
VDD1833_ET1	—	1.8/3.3	—	—	—	Open*6
DSI_DPCLK	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DNCLK	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DPDATA0	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DNDATA0	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DPDATA1	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DNDATA1	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DPDATA2	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DNDATA2	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DPDATA3	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_DNDATA3	Output	1.2*1	DSI_VDD12	Low	DSI PHY	Open
DSI_VREG0P4V	—	—	—	—	—	Open
DSI_VDD0P8	—	0.8	—	—	—	Always in use
DSI_VDD18	—	1.8	—	—	—	Open
DSI_VDD12	—	1.2	—	—	—	Open
CSI0_CLKP	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_CLKN	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA0P	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA0N	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA1P	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA1N	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA2P	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA2N	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA3P	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_DATA3N	Input	1.8*1	CSI0_MSVDD18	—	CSI PHY	Open
CSI0_MSVDD18	—	1.8	—	—	—	Open
CSI0_MSVDD0P8	—	0.8	—	—	—	Always in use
CSI1_CLKP	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_CLKN	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA0P	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA0N	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA1P	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA1N	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA2P	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open

Table 2.2-1 List of External Pins (6/12)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
CSI1_DATA2N	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA3P	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_DATA3N	Input	1.8*1	CSI1_MSVDD18	—	CSI PHY	Open
CSI1_MSVDD18	—	1.8	—	—	—	Open
CSI1_MSVDD0P8	—	0.8	—	—	—	Always in use
DDR0_DQA0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA2	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA3	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA4	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA5	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA6	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA7	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DMIA0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQSAT0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQSAC0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA8	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA9	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA10	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA11	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA12	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA13	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA14	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQA15	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DMIA1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQSAT1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQSAC1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB2	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB3	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB4	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB5	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB6	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB7	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DMIB0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQSBT0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQSBC0	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB8	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB9	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB10	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB11	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB12	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB13	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB14	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQB15	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DMIB1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQSBT1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_DQSBC1	Input / Output	0.6/1.1	DDR0_VDDQLP	Low	DDR PHY	Open
DDR0_CKEA0	Input / Output	1.1	DDR0_VDDQ	Low	DDR PHY	Open
DDR0_CKEA1	Input / Output	1.1	DDR0_VDDQ	Low	DDR PHY	Open
DDR0_CAA0	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open

Table 2.2-1 List of External Pins (7/12)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
DDR0_CAA1	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CKAT	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CKAC	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CSA0	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CSA1	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAA2	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAA3	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAA4	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAA5	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CKEB0	Input / Output	1.1	DDR0_VDDQ	Low	DDR PHY	Open
DDR0_CKEB1	Input / Output	1.1	DDR0_VDDQ	Low	DDR PHY	Open
DDR0_CAB0	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAB1	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CKBT	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CKBC	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CSB0	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CSB1	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAB2	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAB3	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAB4	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_CAB5	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_RESETN	Output	1.1	DDR0_VDDQ	Low	DDR PHY	Open
DDR0_DTEST	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_ATEST	Input / Output	0.6/1.1	DDR0_VDDQLP	Hi-Z	DDR PHY	Open
DDR0_ZN	—	—	—	—	DDR PHY	Open
DDR0_VDDQ	—	1.1	—	—	—	V_{SS}
DDR0_VDDQLP*6	—	0.6/1.1	—	—	—	V_{SS}
DDR0_VAA	—	1.8	—	—	—	V_{SS}
P00	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P01	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P02	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P03	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P04	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P05	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P06	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P07	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P10	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P11	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open

Table 2.2-1 List of External Pins (8/12)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
P12	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P13	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P14	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P15	Input / Output	1.8/3.3	VDD1833_AWO	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P20	Input / Output	1.2/1.8	VDD1218_I3C	Hi-Z	1.8/1.2-V switching I/O	Open
P21	Input / Output	1.2/1.8	VDD1218_I3C	Hi-Z	1.8/1.2-V switching I/O	Open
P30	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P31	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P32	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P33	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P34	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P35	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P36	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P37	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P40	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P41	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P42	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P43	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P44	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P45	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P46	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P47	Input / Output	1.8/3.3	VDD1833_OTHERS_A	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P50	Input / Output	1.8/3.3	VDD1833_OTHERS_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open

Table 2.2-1 List of External Pins (9/12)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
P51	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P52	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P53	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P54	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P55	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P56	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P57	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P60	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P61	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P62	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P63	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P64	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P65	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P66	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P67	Input / Output	1.8/3.3	VDD1833_OTHER S_B	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P70	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P71	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P72	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P73	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P74	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P75	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P76	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P77	Input / Output	1.8/3.3	VDD1833_OTHER S_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open

Table 2.2-1 List of External Pins (10/12)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
P80	Input / Output	1.8/3.3	VDD1833_OTHERS_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P81	Input / Output	1.8/3.3	VDD1833_OTHERS_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P82	Input / Output	1.8/3.3	VDD1833_OTHERS_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P83	Input / Output	1.8/3.3	VDD1833_OTHERS_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P84	Input / Output	1.8/3.3	VDD1833_OTHERS_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P85	Input / Output	1.8/3.3	VDD1833_OTHERS_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P86	Input / Output	1.8/3.3	VDD1833_OTHERS_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P87	Input / Output	1.8/3.3	VDD1833_OTHERS_C	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P90	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
P91	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
P92	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
P93	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P94	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P95	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P96	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
P97	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA0	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA1	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA2	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA3	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA4	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA5	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PA6	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open

Table 2.2-1 List of External Pins (11/12)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
PA7	Input / Output	1.8/3.3	VDD1833_OTHERS_D	Hi-Z	3.3/1.8-V switching I/O (type 2)	Open
PB0	Input / Output	1.8/3.3	VDD1833_SD2	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
PB1	Input / Output	1.8/3.3	VDD1833_SD2	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
PB2	Input / Output	1.8/3.3	VDD1833_SD2	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
PB3	Input / Output	1.8/3.3	VDD1833_SD2	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
PB4	Input / Output	1.8/3.3	VDD1833_SD2	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
PB5	Input / Output	1.8/3.3	VDD1833_SD2	Hi-Z	3.3/1.8-V switching I/O (type 3)	Open
TS0AVDD18	—	1.8	—	—	—	Always in use
TS0DVDD08A	—	0.8	—	—	—	Always in use
TS1AVDD18	—	1.8	—	—	—	Always in use
TS1DVDD08A	—	0.8	—	—	—	Always in use
OTPVDD18	—	1.8	—	—	—	Always in use
PLVDD_PLLCM33	—	1.8	—	—	—	Always in use
PLVSS_PLLCM33	—	—	—	—	—	Always in use
PLVDD_PLLCLN_DTY_DRP	—	1.8	—	—	—	Always in use
PLVSS_PLLCLN_DTY_DRP	—	—	—	—	—	Always in use
PLVDD_PLLCA55	—	1.8	—	—	—	Always in use
PLVSS_PLLCA55	—	—	—	—	—	Always in use
PLVDD_PLLVDO_DSI	—	1.8	—	—	—	Always in use
PLVSS_PLLVDO_DSI	—	—	—	—	—	Always in use
PLVDD_PLLDDR0	—	1.8	—	—	—	Always in use
PLVSS_PLLDDR0	—	—	—	—	—	Always in use
PLVDD_PLLETH_GPU	—	1.8	—	—	—	Always in use
PLVSS_PLLETH_GPU	—	—	—	—	—	Always in use
PLDVDD08_PLLCM33	—	0.8	—	—	—	Always in use
PLDVDD08_PLLCLN_DTY_DRP	—	0.8	—	—	—	Always in use
PLDVDD09_PLLCA55	—	0.8/0.9*5	—	—	—	Always in use
PLDVDD08_PLLVDO_DSI	—	0.8	—	—	—	Always in use
PLDVDD08_PLLDDR0	—	0.8	—	—	—	Always in use
PLDVDD08_PLLETH_GPU	—	0.8	—	—	—	Always in use
VDD09_CA55	—	0.8/0.9*5	—	—	—	Always in use
VDD08_AWO	—	0.8	—	—	—	Always in use
VDD08_DDR	—	0.8	—	—	—	Always in use
VDD18_AWO	—	1.8	—	—	—	Always in use
VDD1833_AWO	—	1.8/3.3	—	—	—	Open*6
VDD1833_PRE18_AWO	—	1.8	—	—	—	Open*6
VDD33_OTHERS	—	3.3	—	—	—	Open*6
VDD33_PRE18_OTHERS	—	1.8	—	—	—	Open*6
VDD08_OTHERS	—	0.8	—	—	—	Always in use
VDD1833_OTHERS_A	—	1.8/3.3	—	—	—	Open*6
VDD1833_OTHERS_B	—	1.8/3.3	—	—	—	Open*6
VDD1833_OTHERS_C	—	1.8/3.3	—	—	—	Open*6
VDD1833_OTHERS_D	—	1.8/3.3	—	—	—	Open*6

Table 2.2-1 List of External Pins (12/12)

Pin Name	Input / Output	Voltage (V)	I/O Power Group	Initial Value*7	I/O Type	Pin State when not in Use
VDD1218_I3C	—	1.2/1.8	—	—	—	Open*6
VDD18_PWC	—	1.8	—	—	—	Always in use
V_{SS}	—	—	—	—	—	Always in use

Note 1. This voltage is the IO buffer voltage. The amplitude is different between LP (low power) mode and HS (high speed) mode. For details, refer to the *MIPI Alliance Specification for D-PHY Version 1.2*.

Note 2. Pull-up or pull-down resistors are integrated in the IO buffers. For the resistance values, refer to the DC characteristics in **Section 3 Electrical Characteristics.**

Note 3. This pin is compliant with the JTAG specification.

Note 4. See **Figure 2.3-1** for how to connect the USBVBUS.

Note 5. VDD09_CA55 and PLDVDD09_PLLCA55 should be at the same voltage.

Note 6. When these power supplies are open, the corresponding signal pins should be open. When supplying power, follow the instructions in the table.

Note 7. The initial value indicates the status during a reset (QRESN = 0) and immediately after release from the reset state (QRESN = 1).

Note 8. When using these pins at 1.1 V, DDRx_VDDQLP should be connected to DDRx_VDDQ. (x = 0)

Note 9. All unconnected lanes must be terminated during compliance test.

Note 10. Connect an external resistor (6.2kΩ). For details, refer to the *RZ/V2N Group PCB Design Guidelines*.

Note 11. A load switch or similar component should be added so that voltage is applied to the USB20_VUBUSIN pin after power is supplied for USB20.

2.2.2 List of Multiplexed Functional Pins

For details on pin functions, reter to *RZ/V2N Group User's Manual: Hardware*.

Table 2.2-2 List of Multiplexed Functional Pins (1/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
P00	GPIO/TINT_GP00	—	PDMDAT00	—	—	—	—	—	—
		—	GTETRGA	GTETRGE	—	—	IRQ0	—	—
P01	GPIO/TINT_GP01	—	PDMCLK00	—	—	—	—	—	—
		—	GTETRGB	GTETRGF	—	—	IRQ1	—	—
P02	GPIO/TINT_GP02	—	PDMDAT01	—	—	—	—	—	—
		—	GTETRGC	GTETRGG	—	—	IRQ2	DACK0	DREQ0
P03	GPIO/TINT_GP03	—	PDMCLK01	—	—	—	—	—	—
		—	GTETRGD	GTETRGH	—	—	IRQ3	TEND0	DREQ0
P04	GPIO/TINT_GP04	—	PDMDAT02	SSLA0	SSLB2	ADC0_ADTRG	ADC1_ADTRG	ADC2_ADTRG	SSI3_SDATA
		SPDIF1_OUT	TOC20	TIC20	GTETRGE	—	IRQ8	—	XSPI0_WP0N
P05	GPIO/TINT_GP05	—	PDMCLK02	SSLA1	SSLC2	ADC0_ADTRG	TOC31	TIC31	SSI4_SCK
		SPDIF1_IN	TOC21	TIC21	GTETRGF	ADC1_ADTRG	IRQ9	DACK0	XSPI0_ECS1N
P06	GPIO/TINT_GP06	—	SDA8	—	—	—	—	—	—
		—	—	—	—	—	IRQ12	—	—
P07	GPIO/TINT_GP07	—	SCL8	—	—	—	—	—	—
		—	—	—	—	—	IRQ13	—	—
P10	GPIO/TINT_GP10	—	PDMDAT10	—	—	—	—	—	AUDIO_CLKB
		—	TOC00	TIC00	GTETRGA	—	IRQ4	DACK0	XSPI0_CS1N
P11	GPIO/TINT_GP11	—	PDMCLK10	—	—	—	—	—	AUDIO_CLKC
		—	TOC01	TIC01	GTETRGB	—	IRQ5	—	XSPI0_RESET1N
P12	GPIO/TINT_GP12	—	PDMDAT11	—	—	—	—	—	SSI3_SCK
		SPDIF0_OUT	TOC10	TIC10	GTETRGC	—	IRQ6	—	XSPI0_RSTO1N
P13	GPIO/TINT_GP13	—	PDMCLK11	—	—	—	—	—	SSI3_WS
		SPDIF0_IN	TOC11	TIC11	GTETRGD	—	IRQ7	TEND0	XSPI0_INT1N
P14	GPIO/TINT_GP14	—	PDMDAT12	SSLA2	SSLB3	ADC0_ADTRG	TOC20	TIC20	SSI4_WS
		SPDIF2_OUT	TOC30	TIC30	GTETRGG	ADC2_ADTRG	IRQ10	TEND0	XSPI0_WP1N

Table 2.2-2 List of Multiplexed Functional Pins (2/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
P15	GPIO/TINT_GP15	—	PDMCLK12	SSLA3	SSLC3	ADC0_ADTRG	ADC1_ADTRG	ADC2_ADTRG	SSI4_SDATA
		SPDIF2_IN	TOC31	TIC31	GTETRGH	—	IRQ11	TEND0	DREQ0
P20	GPIO/TINT_GP20	—	SDA30	—	—	SDA2	—	—	—
		—	GTETRGC	GTETRGG	—	—	IRQ14	DACK3	DREQ1
P21	GPIO/TINT_GP21	—	SCL30	—	—	SCL2	—	—	—
		—	GTETRGD	GTETRGH	—	—	IRQ15	TEND3	DREQ2
P30	GPIO/TINT_GP30	—	SDA0	—	—	—	—	—	—
		—	GTIOC4A	GTIOC4AN	GTIOC12A	GTIOC12AN	IRQ0	DACK1	—
P31	GPIO/TINT_GP31	—	SCL0	—	—	—	—	—	—
		—	GTIOC4B	GTIOC4BN	GTIOC12B	GTIOC12BN	IRQ1	TEND1	—
P32	GPIO/TINT_GP32	—	SDA1	—	—	—	—	—	—
		—	GTIOC5A	GTIOC5AN	GTIOC13A	GTIOC13AN	IRQ2	DACK2	—
P33	GPIO/TINT_GP33	—	SCL1	—	—	—	—	—	—
		—	GTIOC5B	GTIOC5BN	GTIOC13B	GTIOC13BN	IRQ3	TEND2	—
P34	GPIO/TINT_GP34	—	SDA2	TXD3_MOSI3_SDA3	—	—	SSLA0	SSLB0	—
		—	GTIOC6A	GTIOC6NA	GTIOC14A	GTIOC14AN	IRQ4	DACK3	—
P35	GPIO/TINT_GP35	—	SCL2	RXD3_MISO3_SCL3	—	—	SSLA1	SSLC0	—
		—	GTIOC6B	GTIOC6BN	GTIOC14B	GTIOC14BN	IRQ5	TEND3	—
P36	GPIO/TINT_GP36	—	SDA3	SCK3	DE3	CTS3N	SSLA2	SSLB1	—
		—	GTIOC7A	GTIOC7AN	GTIOC15A	GTIOC15AN	IRQ6	DACK4	—
P37	GPIO/TINT_GP37	—	SCL3	SS3_CTS3N_RTS3N	DE3	—	SSLA3	SSLC1	—
		—	GTIOC7B	GTIOC7BN	GTIOC15B	GTIOC15BN	IRQ7	TEND4	—
P40	GPIO/TINT_GP40	—	SDA4	TXD4_MOSI4_SDA4	—	—	CTXDP4	—	SSI0_SCK
		—	GTIOC0A	GTIOC0AN	—	—	IRQ8	DACK1	DREQ3
P41	GPIO/TINT_GP41	—	SCL4	RXD4_MISO4_SCL4	—	—	CRXDP4	—	SSI0_WS
		—	GTIOC0B	GTIOC0BN	—	—	IRQ9	TEND1	DREQ4

Table 2.2-2 List of Multiplexed Functional Pins (3/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
P42	GPIO/TINT_GP42	—	SDA5	SCK4	DE4	CTS4N	CTX4	—	SSI0_SDATA
		—	GTIOC1A	GTIOC1AN	—	—	IRQ10	—	USB20_VBUSEN
P43	GPIO/TINT_GP43	—	SCL5	SS4_CTS4N_RTS4N	DE4	—	CRX4	—	SSI9_SDATA
		—	GTIOC1B	GTIOC1BN	—	—	IRQ11	—	USB20_OVRCURN
P44	GPIO/TINT_GP44	—	SDA6	TXD5_MOSI5_SDA5	—	—	CTXDP5	—	SSI1_SCK
		—	GTIOC2A	GTIOC2AN	—	—	IRQ12	DACK4	DREQ1
P45	GPIO/TINT_GP45	—	SCL6	RXD5_MISO5_SCL5	—	—	CRXDP5	—	SSI1_WS
		—	GTIOC2B	GTIOC2BN	—	—	IRQ13	TEND4	DREQ2
P46	GPIO/TINT_GP46	—	SDA7	SCK5	DE5	CTS5N	CTX5	—	SSI1_SDATA
		—	GTIOC3A	GTIOC3AN	—	—	IRQ14	DACK2	DREQ3
P47	GPIO/TINT_GP47	—	SCL7	SS5_CTS5N_RTS5N	DE5	—	CRX5	—	SSI2_SDATA
		—	GTIOC3B	GTIOC3BN	—	—	IRQ15	TEND2	DREQ4
P50	GPIO/TINT_GP50	—	TXD0_MOSI0_SDA0	—	—	—	—	—	—
		—	—	—	GTIOC8A	GTIOC8AN	IRQ0	—	—
P51	GPIO/TINT_GP51	—	RXD0_MISO0_SCL0	—	—	—	—	—	—
		—	—	—	GTIOC8B	GTIOC8BN	IRQ1	—	—
P52	GPIO/TINT_GP52	—	TXD1_MOSI1_SDA1	SCK0	DE0	CTS0N	—	—	—
		—	—	—	GTIOC10A	GTIOC10AN	IRQ4	—	—
P53	GPIO/TINT_GP53	—	RXD1_MISO1_SCL1	SS0_CTS0N_RTS0N	DE0	—	—	—	—
		—	—	—	GTIOC10B	GTIOC10BN	IRQ5	—	—
P54	GPIO/TINT_GP54	—	TXD2_MOSI2_SDA2	—	—	—	—	—	—
		—	—	—	GTIOC12A	GTIOC12AN	IRQ8	—	—

Table 2.2-2 List of Multiplexed Functional Pins (4/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
P55	GPIO/TINT_GP55	—	RXD2_MISO2_SCL2	—	—	—	—	—	—
		—	—	—	GTIOC12B	GTIOC12BN	IRQ9	—	—
P56	GPIO/TINT_GP56	—	TXD3_MOSI3_SDA3	SCK2	DE2	CTS2N	—	—	—
		—	GTETRGA	GTETRGE	GTIOC14A	GTIOC14AN	IRQ12	—	—
P57	GPIO/TINT_GP57	—	RXD3_MISO3_SCL3	SS2_CTS2N_RTS2N	DE2	—	—	—	—
		—	GTETRGB	GTETRGF	GTIOC14B	GTIOC14BN	IRQ13	—	—
P60	GPIO/TINT_GP60	—	SCK0	DE0	CTS0N	SDA4	—	TXD2_MOSI2_SDA2	AUDIO_CLKB
		SPDIF0_OUT	GTETRGA	GTETRGE	GTIOC9A	GTIOC9AN	IRQ2	USB30_VBUSEN	USB20_VBUSEN
P61	GPIO/TINT_GP61	—	SS0_CTS0N_RTS0N	DE0	—	SCL4	—	RXD2_MISO2_SCL2	AUDIO_CLKOUT
		SPDIF0_IN	GTETRGB	GTETRGF	GTIOC9B	GTIOC9BN	IRQ3	USB30_OVRCURN	USB20_OVRCURN
P62	GPIO/TINT_GP62	—	SCK1	DE1	CTS1N	SDA5	—	TXD3_MOSI3_SDA3	AUDIO_CLKC
		SPDIF1_OUT	GTETRGG	GTETRGC	GTIOC11A	GTIOC11AN	IRQ6	—	USB20_VBUSEN
P63	GPIO/TINT_GP63	—	SS1_CTS1N_RTS1N	DE1	—	SCL5	—	RXD3_MISO3_SCL3	AUDIO_CLKOUT
		SPDIF1_IN	GTETRGH	GTETRGD	GTIOC11B	GTIOC11BN	IRQ7	—	USB20_OVRCURN
P64	GPIO/TINT_GP64	—	SCK2	DE2	CTS2N	SDA6	—	TXD6_MOSI6_SDA6	AUDIO_CLKB
		SPDIF2_OUT	GTETRGE	GTETRGA	GTIOC13A	GTIOC13AN	IRQ10	USB20_VBUSEN	USB30_VBUSEN
P65	GPIO/TINT_GP65	—	SS2_CTS2N_RTS2N	DE2	—	SCL6	—	RXD6_MISO6_SCL6	AUDIO_CLKC
		SPDIF2_IN	GTETRGF	GTETRGB	GTIOC13B	GTIOC13BN	IRQ11	USB20_OVRCURN	USB30_OVRCURN
P66	GPIO/TINT_GP66	—	SCK3	DE3	CTS3N	SDA7	—	TXD7_MOSI7_SDA7	SSI6_SCK
		—	GTETRGC	GTETRGG	GTIOC15A	GTIOC15AN	IRQ14	—	USB30_VBUSEN

Table 2.2-2 List of Multiplexed Functional Pins (5/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
P67	GPIO/TINT_GP67	—	SS3_CTS3N_RTS3N	DE3	—	SCL7	—	RXD7_MISO7_SCL7	SSI6_WS
		—	GTETRGD	GTETRGH	GTIOC15B	GTIOC15BN	IRQ15	—	USB30_OVRCURN
P70	GPIO/TINT_GP70	—	TXD4_MOSI4_SDA4	—	—	—	CTXDP0	—	SSI6_SDATA
		AUDIO_CLKB	GTIOC0A	GTIOC0AN	—	—	IRQ0	DACK1	—
P71	GPIO/TINT_GP71	—	RXD4_MISO4_SCL4	—	—	—	CRXDP0	—	SSI5_SCK
		AUDIO_CLKC	GTIOC0B	GTIOC0BN	—	—	IRQ1	TEND1	—
P72	GPIO/TINT_GP72	—	TXD5_MOSI5_SDA5	—	—	—	CTXDP1	—	SSI5_SDATA
		SPDIF1_OUT	GTIOC2A	GTIOC2AN	—	—	IRQ4	DACK3	—
P73	GPIO/TINT_GP73	—	RXD5_MISO5_SCL5	—	—	—	CRXDP1	—	SSI7_SCK
		SPDIF1_IN	GTIOC2B	GTIOC2BN	—	—	IRQ5	TEND3	—
P74	GPIO/TINT_GP74	—	TXD6_MOSI6_SDA6	—	—	—	CTXDP2	—	SSI3_SCK
		—	GTIOC4A	GTIOC4AN	—	—	IRQ8	DACK3	DREQ1
P75	GPIO/TINT_GP75	—	RXD6_MISO6_SCL6	—	—	—	CRXDP2	—	SSI3_WS
		—	GTIOC4B	GTIOC4BN	—	—	IRQ9	TEND3	DREQ2
P76	GPIO/TINT_GP76	—	TXD7_MOSI7_SDA7	—	—	—	CTXDP3	—	SSI5_SCK
		SSI6_SCK	GTIOC6A	GTIOC6AN	—	—	IRQ12	DACK1	DREQ3
P77	GPIO/TINT_GP77	—	RXD7_MISO7_SCL7	—	—	—	CRXDP3	—	SSI5_WS
		SSI6_WS	GTIOC6B	GTIOC6BN	—	—	IRQ13	TEND1	DREQ4
P80	GPIO/TINT_GP80	—	SCK4	DE4	CTS4N	—	CTX0	TXD8_MOSI8_SDA8	SSI5_WS
		SPDIF0_OUT	GTIOC1A	GTIOC1AN	—	—	IRQ2	DACK2	—

Table 2.2-2 List of Multiplexed Functional Pins (6/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
P81	GPIO/TINT_GP81	—	SS4_CTS4N_RTS4N	DE4	—	—	CRX0	RXD8_MISO8_SCL8	SSI8_SDATA
		SPDIF0_IN	GTIOC1B	GTIOC1BN	—	—	IRQ3	TEND2	—
P82	GPIO/TINT_GP82	—	SCK5	DE5	CTS5N	—	CTX1	TXD9_MOSI9_SDA9	SSI7_WS
		SPDIF2_OUT	GTIOC3A	GTIOC3AN	—	—	IRQ6	DACK4	—
P83	GPIO/TINT_GP83	—	SS5_CTS5N_RTS5N	DE5	—	—	CRX1	RXD9_MISO9_SCL9	SSI7_SDATA
		SPDIF2_IN	GTIOC3B	GTIOC3BN	—	—	IRQ7	TEND4	—
P84	GPIO/TINT_GP84	—	SCK6	DE6	CTS6N	—	CTX2	TXD4_MOSI4_SDA4	SSI3_SDATA
		—	GTIOC5A	GTIOC5AN	—	—	IRQ10	USB30_VBUSEN	USB20_VBUSEN
P85	GPIO/TINT_GP85	—	SS6_CTS6N_RTS6N	DE6	—	—	CRX2	RXD4_MISO4_SCL4	SSI4_SDATA
		—	GTIOC5B	GTIOC5BN	—	—	IRQ11	USB30_OVRCURN	USB20_OVRCURN
P86	GPIO/TINT_GP86	—	SCK7	DE7	CTS7N	—	CTX3	TXD5_MOSI5_SDA5	SSI5_SDATA
		—	GTIOC7A	GTIOC7AN	—	—	IRQ14	—	USB30_VBUSEN
P87	GPIO/TINT_GP87	—	SS7_CTS7N_RTS7N	DE7	—	—	CRX3	RXD5_MISO5_SCL5	SSI6_SDATA
		—	GTIOC7B	GTIOC7BN	—	—	IRQ15	—	USB30_OVRCURN
P90	GPIO/TINT_GP90	—	MOSIA	TXD6_MOSI6_SDA6	—	—	—	—	—
		—	—	—	—	—	IRQ0	—	—
P91	GPIO/TINT_GP91	—	MISOA	RXD6_MISO6_SCL6	—	—	—	—	—
		—	—	—	—	—	IRQ1	—	—
P92	GPIO/TINT_GP92	—	RSPCKA	SCK6	DE6	CTS6N	—	TXD0_MOSI0_SDA0	—
		—	—	—	—	—	IRQ2	—	—
P93	GPIO/TINT_GP93	—	SSLA0	SS6_CTS6N_RTS6N	DE6	—	—	RXD0_MISO0_SCL0	AUDIO_CLKB
		—	—	—	—	—	IRQ3	SD1WP	SD0WP

Table 2.2-2 List of Multiplexed Functional Pins (7/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
P94	GPIO/TINT_GP94	—	SSLA1	TXD7_MOSI7_SDA7	—	—	—	—	AUDIO_CLKC
		SPDIF0_OUT	GTIOC8A	GTIOC8AN	GTIOC4A	GTIOC4AN	IRQ4	SD1CD	SD0CD
P95	GPIO/TINT_GP95	—	SSLA2	RXD7_MISO7_SCL7	—	—	—	—	SSI0_SCK
		SPDIF0_IN	GTIOC8B	GTIOC8BN	GTIOC4B	GTIOC4BN	IRQ5	USB20_VBUSEN	USB30_VBUSEN
P96	GPIO/TINT_GP96	—	SSLA3	SCK7	DE7	CTS7N	—	TXD1_MOSI1_SDA1	SSI0_WS
		AUDIO_CLKOUT	GTIOC9A	GTIOC9AN	GTIOC5A	GTIOC5AN	IRQ6	USB20_OVRCURN	USB30_OVRCURN
P97	GPIO/TINT_GP97	—	ADC0_ADTRG	SS7_CTS7N_RTS7N	DE7	ADC1_ADTRG	ADC2_ADTRG	RXD1_MISO1_SCL1	SSI0_SDATA
		AUDIO_CLKOUT	GTIOC9B	GTIOC9BN	GTIOC5B	GTIOC5BN	IRQ7	—	—
PA0	GPIO/TINT_GPA0	—	SD0IOVS	—	ADC0_ADTRG	ADC1_ADTRG	ADC2_ADTRG	—	—
		—	—	—	—	—	IRQ8	SD1WP	SD2WP
PA1	GPIO/TINT_GPA1	—	SD0PWEN	—	ADC0_ADTRG	ADC1_ADTRG	ADC2_ADTRG	—	—
		—	—	—	—	—	IRQ9	SD1CD	SD2CD
PA2	GPIO/TINT_GPA2	—	SD1IOVS	—	—	—	—	—	—
		—	—	—	—	—	IRQ10	—	SD2WP
PA3	GPIO/TINT_GPA3	—	SD1PWEN	—	—	—	—	—	—
		—	—	—	—	—	IRQ11	—	SD2CD
PA4	GPIO/TINT_GPA4	—	SD2IOVS	SS8_CTS8N_RTS8N	DE8	SSLB0	SSLC3	—	AUDIO_CLKOUT
		SPDIF1_OUT	GTIOC10A	GTIOC10AN	GTIOC6A	GTIOC6AN	IRQ12	DACK1	SD0WP
PA5	GPIO/TINT_GPA5	–	SD2PWEN	CTS8N	DE8	SSLB1	SSLC2	—	SSI9_WS
		SPDIF1_IN	GTIOC10B	GTIOC10BN	GTIOC6B	GTIOC6BN	IRQ13	TEND1	SD0CD
PA6	GPIO/TINT_GPA6	–	SD2WP	CTS9N	DE9	SSLB2	SSLC1	—	SSI9_SDATA
		SPDIF2_OUT	GTIOC11A	GTIOC11AN	GTIOC7A	GTIOC7AN	IRQ14	DACK3	SD1WP
PA7	GPIO/TINT_GPA7	–	SD2CD	SS9_CTS9N_RTS9N	DE9	SSLB3	SSLC0	—	SSI9_SCK
		SPDIF2_IN	GTIOC11B	GTIOC11BN	GTIOC7B	GTIOC7BN	IRQ15	TEND3	SD1CD
PB0	GPIO/TINT_GPB0	–	SD2CLK	SCK8	DE8	RSPCKB	—	—	SSI1_SCK
		–	—	—	—	—	IRQ0	USB30_VBUSEN	—

Table 2.2-2 List of Multiplexed Functional Pins (8/8)

Pin Name	GPIO	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7
		Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15
PB1	GPIO/TINT_GPB1	—	SD2DAT0	TXD8_MOSI8_SDA8	—	MOSIB	—	—	SSI1_WS
		—	—	—	—	—	IRQ1	USB30_OVRCURN	—
PB2	GPIO/TINT_GPB2	—	SD2DAT1	RXD8_MISO8_SCL8	—	MISOB	—	—	SSI1_SDATA
		—	—	—	—	—	IRQ2	TEND4	DREQ2
PB3	GPIO/TINT_GPB3	—	SD2DAT2	RXD9_MISO9_SCL9	—	—	MISOC	—	SSI2_SCK
		—	—	—	—	—	IRQ3	DACK4	DREQ1
PB4	GPIO/TINT_GPB4	—	SD2DAT3	TXD9_MOSI9_SDA9	—	—	MOSIC	—	SSI2_WS
		—	—	—	—	—	IRQ4	DACK2	DREQ3
PB5	GPIO/TINT_GPB5	—	SD2CMD	SCK9	DE9	—	RSPCKC	—	SSI2_SDATA
		—	—	—	—	—	IRQ5	TEND2	DREQ4

Note: —: Reserved functions

2.3 Pin Functions of Functional Blocks

Table 2.3-1 List of Pin Functions (1/7)

Classification	Pin Name	I/O	Function
Clock	QXTAL	Out	24-MHz main clocks. These pins are to connect a 24-MHz crystal oscillator. When an external clock signal is used, the QXTAL pin should be open.
	QEXTAL	In	
	EMXTAL	Out	Reserved pins. The EMXTAL pin should be open. The EMEXTAL pin should be connected to V_{ss}.
	EMEXTAL	In	
	RTXOUT	Out	32.768-kHz real-time clocks. These pins are to connect a 32.768-kHz crystal oscillator. When an external clock signal is used, the RTXOUT pin should be open.
	RTXIN	In	
	AUDIO_XTAL	Out	4- to 48-MHz audio clocks. These pins are to connect a crystal oscillator. When an external clock signal is used, the clock frequency is allowed 50-MHz max. and the Audio_XTAL pin should be open.
	AUDIO_EXTAL	In	
	AUDIO_CLKB	In	Max. 50-MHz audio clock B
	AUDIO_CLKC	In	Max. 50-MHz audio clock C
	AUDIO_CLKOUT	Out	Max. 25-MHz audio clock out
Boot mode control	BOOTSELCPU	In	Select the cold boot CPU. Low: CM33, High: CA55
	BOOTPLLCA_1	In	Input the CA55 frequency at the CA55 cold boot. BOOTPLLCA_[1:0] = [Low:Low]:1.1 GHz BOOTPLLCA_[1:0] = [Low:High]: 1.5 GHz*1 BOOTPLLCA_[1:0] = [High:Low]: 1.6 GHz*1 BOOTPLLCA_[1:0] = [High:High]: 1.7 GHz*1 *Note 1.* Enabled when VDD09_CA55 is at 0.9 V.
	BOOTPLLCA_0	In	
	MD_BOOT4	In	Select the boot mode [4] (reserved) Fix the pin to the low level.
	MD_BOOT3	In	Select the operation mode [3] Low: Normal mode, High: Debug mode
	MD_BOOT2	In	Select the boot device IO voltage Low: 3.3 V, High: 1.8 V *Note*: Enabled in boot mode 1 and boot mode 2 only
	MD_BOOT1	In	Input the boot mode select signal. MD_BOOT[1:0] = [Low:Low]: eSD*1 (boot mode 0) MD_BOOT[1:0] = [Low:High]: eMMC*1 (boot mode 1) MD_BOOT[1:0] = [High:Low]: xSPI (boot mode 2) MD_BOOT[1:0] = [High:High]: SCIF download (boot mode 3) *Note 1.* Enable CA55 cold boot only
	MD_BOOT0	In	
	MD_CLKS	In	Select SSCG OFF or ON Low: OFF, High: ON
System controller	QRESN	In	Input the reset signal. The reset state is entered when this signal goes low.
	QBYPASS	In	Select Main CLK oscillation mode Low: Crystal, High: External clock
	BSCANP	In	Select boundary scan mode Low: Not selected, High: Selected
Interrupt	NMI	In	Input interrupt trigger signal to all CPUs
	IRQ0 to 15	In	Input the external interrupt request signals
	TINT0 to 31	In	Input the external interrupt request signals

Table 2.3-1 List of Pin Functions (2/7)

Classification	Pin Name	I/O	Function
Power controller	QRESNSEL	In	Select the internal reset signal to be generated Low: Generated by the PWC High: Generated by the QRESN
	PWEN0	Out	Power enable for 1.8-V power supply to OTP and ADC (active high)*2
	PWEN1	Out	Power enable for 1.8-V power supply to MIPI-DSI and MIPI-CSI2 (active high)*2
	PWEN2	Out	Power enable for 1.2-V power supply to MIPI-DSI (active high)*2
Debugger interface	TMS_SWDIO	I/O	Test mode select pin. Functions as the SWDIO pin in serial wire debug (SWD) mode.
	TCK_SWCLK	In	Test clock pin. Functions as the SWCLK pin in serial wire debug (SWD) mode.
	TDO	Out	Test data output pin.
	TDI	In	Test data input pin.
	TRSTN	In	Test reset pin.
Direct memory access controller (DMAC)	DREQ0 to 4	In	Input DMAC request signal from the external device
	DACK0 to 4	Out	Output the acknowledge signal which indicates acceptance of DMAC request to the external device
	TEND0 to 4	Out	Output DMAC end signal
Watchdog timer (WDT)	WDTUDFCM	Out	Output the CM33_WDT underflow error signal with active low. This pin sets Nch open drain mode. (Register setting is possible.)
	WDTUDFCA	Out	Output the CA55_WDT underflow error signal with active low. This pin sets Nch open drain mode. (Register setting is possible.)
SCIF download interface	SCIF_RXD	In	UART receive pin for SCIF
	SCIF_TXD	Out	UART transfer pin for SCIF
12-bit A/D converter interface	ANIn00 to ANIn07	In	Input the ADC signals (n = 0 to 2)
	ADCn_ADTRG	In	Input the ADC trigger signal (n = 0 to 2)
Expanded serial peripheral interface (xSPI)	XSPI0_CKP	Out	Clock output pins. CKP and CKN waves have opposite phase.
	XSPI0_CKN	Out	
	XSPI0_DS	I/O	Read data strobe / Write data mask
	XSPI0_IO0 to 7	I/O	Input/output data 0 to data 7
	XSPI0_CS0N	Out	Output the chip select signal for the channel 0. Low: Selected, High: Not selected
	XSPI0_RESET0N	Out	Output the reset status signal for the channel 0. Low: reset status
	XSPI0_RSTO0N	In	Input the reset status signal from the channel 0
	XSPI0_INT0N	In	Input the interrupt signal from the channel 0
	XSPI0_ECS0N	In	Input the error correction status from the channel 0
	XSPI0_WP0N	Out	Output the write-protection signal for the channel 0
	XSPI0_CS1N	Out	Output the chip select signal for the channel 1 Low: Selected, High: Not selected
	XSPI0_RESET1N	Out	Output the reset status signal for the channel 1 Low: reset status
	XSPI0_RSTO1N	In	Input the reset status signal from the channel 1
	XSPI0_INT1N	In	Input the interrupt signal from the channel 1
	XSPI0_ECS1N	In	Input the error correction status from the channel 1
	XSPI0_WP1N	Out	Output the write-protection signal for the channel 1

Table 2.3-1 List of Pin Functions (3/7)

Classification	Pin Name	I/O	Function
DDR memory interface channel 0	DDRn_DQA0 to 15, DDRn_DQB0 to 15	I/O	DRAM data bits and strobes
	DDRn_DMIA0 to 1, DDRn_DMIB0 to 1	I/O	DRAM data bits and strobes
	DDRn_DQSAT0 to 1, DDRn_DQSBT0 to 1	I/O	DRAM data bits and strobes
	DDRn_DQSAC0 to 1, DDRn_DQSBC0 to 1	I/O	DRAM data bits and strobes
	DDRn_CKEA0 to 1, DDRn_CKEB0 to 1	I/O	DRAM address bits and command bits
	DDRn_CAA0 to 5, DDRn_CAB0 to 5	I/O	DRAM address bits and command bits
	DDRn_CSA0 to 1, DDRn_CSB0 to 1	I/O	DRAM address bits and command bits
	DDRn_CKAT, DDRn_CKBT	I/O	DRAM address bits and command bits
	DDRn_CKAC, DDRn_CKBC	I/O	DRAM address bits and command bits
	DDRn_RESETN	Out	Output DRAM reset signal
	DDRn_DTEST	I/O	Digital observation pin
	DDRn_ATEST	I/O	Voltage reference for receivers and analog test point for debug
	DDRn_ZN	—	Connect calibration external reference resistor (120Ω ± 1%)
SD/eMMC interface	SD0CLK	Out	Output the clock signal to external SD/eMMC device
	SD0CMD	I/O	Input/output the command code from/to external SD/eMMC device
	SD0DAT0 to 7	I/O	Input/output data 0 to data 7
	SD0RSTN	Out	Output the reset signal to external eMMC device
	SD0WP	In	Input the write-protection signal from external SD device
	SD0CD	In	Input the card-detect signal from external SD slot
	SD0PWEN	Out	Output the power-enable signal to power supply IC for SD device Low: Disabled, High: Enabled
	SD0IOVS	Out	Output the IO voltage level signal to SD device Low: 3.3 V, High: 1.8 V
SD interface	SD1CLK, SD2CLK	Out	Output the clock signals to external SD device
	SD1CMD, SD2CMD	Out	Input/output the command code from/to external SD device
	SD1DAT0 to 3, SD2DAT0 to 3	I/O	Input/output data 0 to data 3
	SD1WP, SD2WP	In	Input the write-protection signals from external SD device
	SD1CD, SD2CD	In	Input the card-detect signals from external SD slot
	SD1PWEN, SD2PWEN	Out	Output the power-enable signals to the power supply IC for SD device Low: Disabled, High: Enabled
	SD1IOVS, SD2IOVS	Out	Output the IO voltage level signals to SD device Low: 3.3 V, High: 1.8 V

Table 2.3-1 List of Pin Functions (4/7)

Classification	Pin Name	I/O	Function
USB2.0 channel 0	USB20_DP	I/O	USB2.0 D+ signal
	USB20_DM	I/O	USB2.0 D− signal
	USB20_OTGID	In	Input OTG ID (pulled up by the internal resistor) Low: Host, High: Peripheral
	USB20_VUBUSIN	In	Input USB VBUS detect signal*1
	USB20_OTGEXICEN	Out	OTG power supply IC control pin
	USB20_VBUSEN	Out	VBUS control signal (active high)
	USB20_OVRCURN	In	Overcurrent detection (active low)
	USB20_TXRTUNE	In	USB transmitter tune pin. This analog signal connects to an external resistor (200Ω ±1%) that adjusts the USB PHY's high-speed source impedance.
USB3.2 channel 0	USB30_DP	I/O	USB2.0 D+ signals
	USB30_DM	I/O	USB2.0 D− signals
	USB30_RX0M	In	USB3.2 super-speed plus differential receive pair (negative)
	USB30_RX0P	In	USB3.2 super-speed plus differential receive pair (positive)
	USB30_TX0M	Out	USB3.2 super-speed plus differential transfer pair (negative)
	USB30_TX0P	Out	USB3.2 super-speed plus differential transfer pair (positive)
	USB30_VBUSEN	Out	VBUS control signals (active high)
	USB30_OVRCURN	In	Overcurrent detection (active low)
	USB3_USRESREF	—	USB3 reference resistor with 200Ω (1%, 100 ppm/°C) to V_{SS}
	USB30_TXRTUNE	—	USB transmitter tune pin. This analog signal connects to an external resistor (200Ω ±1%) that adjusts the USB PHY's high-speed source impedance.
PCIe Gen3	PCIE_TXDPL0	Out	PCIe TX data (positive) of Lane 0
	PCIE_TXDNL0	Out	PCIe TX data (negative) of Lane 0
	PCIE_TXDPL1	Out	PCIe TX data (positive) of Lane 1
	PCIE_TXDNL1	Out	PCIe TX data (negative) of Lane 1
	PCIE_RXDPL0	In	PCIe RX data (positive) of Lane 0
	PCIE_RXDNL0	In	PCIe RX data (negative) of Lane 0
	PCIE_RXDPL1	In	PCIe RX data (positive) of Lane 1
	PCIE_RXDNL1	In	PCIe RX data (negative) of Lane 1
	PCIE_REFCLKP0	In	Differential reference clock (positive)
	PCIE_REFCLKN0	In	Differential reference clock (negative)
	PCIE0_RSTOUTB	Out	Output the reset signal

Table 2.3-1 List of Pin Functions (5/7)

Classification	Pin Name	I/O	Function
Gb Ethernet channel 0, 1	ET0_MDIO, ET1_MDIO	I/O	Management data I/O
	ET0_MDC, ET1_MDC	Out	Management data clocks
	ET0_RXCTL_RXDV, ET1_RXCTL_RXDV	In	RX control/data valid
	ET0_TXCTL_TXEN, ET1_TXCTL_TXEN	Out	TX control/data enable
	ET0_TXER, ET1_TXER	Out	TX data error (MII mode)
	ET0_RXER, ET1_RXER	In	RX data error (MII mode)
	ET0_RXC_RXCLK, ET1_RXC_RXCLK	In	RX clocks
	ET0_TXC_TXCLK, ET1_TXC_TXCLK	I/O	TX clocks
	ET0_CRS, ET1_CRS	In	Carrier sense (MII mode)
	ET0_COL, ET1_COL	In	Collision detection (MII mode)
	ET0_TXD0, ET1_TXD0	Out	TX data 0
	ET0_TXD1, ET1_TXD1	Out	TX data 1
	ET0_TXD2, ET1_TXD2	Out	TX data 2
	ET0_TXD3, ET1_TXD3	Out	TX data 3
	ET0_RXD0, ET1_RXD0	In	RX data 0
	ET0_RXD1, ET1_RXD1	In	RX data 1
	ET0_RXD2, ET1_RXD2	In	RX data 2
	ET0_RXD3, ET1_RXD3	In	RX data 3
	ET0_PHYINTR, ET1_PHYINTR	In	PHY interrupt signals
MIPI-DSI	DSI_DPCLK	Out	Output clocks (positive)
	DSI_DNCLK	Out	Output clocks (negative)
	DSI_DPDATA0 to 3	Out	TX data 0 to TX data 3 (positive)
	DSI_DNDATA0 to 3	Out	TX data 0 to TX data 3 (negative)
	DSI_VREG0P4V	—	Connect this pin to V_{SS} via a 2.2-nF capacitor
MIPI-CSI2 channel n (n = 0 to 1)	CSIn_CLKP	In	Input clocks (positive)
	CSIn_CLKN	In	Input clocks (negative)
	CSIn_DATA0P to CSIn_DATA3P	In	RX data 0 to RX data 3 (positive)
	CSIn_DATA0N to CSIn_DATA3N	In	RX data 0 to RX data 3 (negative)

Table 2.3-1 List of Pin Functions (6/7)

Classification	Pin Name	I/O	Function
CANFD interface channel n (n = 0 to 5)	CRXn	In	RX data 0 to RX data 5
	CTXn	Out	TX data 0 to TX data 5
	CRXDPn	Out	RX data 0 to RX data 5 phase signal
	CTXDPn	Out	TX data 0 to TX data 5 phase signal
Serial peripheral interface (RSPI) channel x (x = A, B, C)	RSPCKx	I/O	Synchronous clock signal
	MOSIx	I/O	Data of Main-Out / Sub-In
	MISOx	I/O	Data of Main-In / Sub-Out
	SSLx0 to 3	I/O*3	Chip select pins
Serial communication interface (RSCI) channel n (n = 0 to 9)	RXDn	In	Input the receive data (asynchronous mode / clock synchronous mode / simple SPI mode / smart card mode)
	TXDn	Out	Output the transmission data (asynchronous mode / clock synchronous mode / simple SPI mode / smart card mode)
	SCKn	I/O	Clock pins (clock synchronous mode / simple SPI mode / smart card mode)
	CTSnN	In	Input the start of transmission as the hardware flow control signals (asynchronous mode / clock synchronous mode)
	RTSnN	Out	Output the reception as the hardware flow control signals (asynchronous mode / clock synchronous mode)
	MOSIn	I/O	Data of Main-Out / Sub-In (simple SPI mode)
	MISOn	I/O	Data of Main-In / Sub-Out (simple SPI mode)
	SCLn	I/O	I2C clocks (simple I2C mode)
	SDAn	I/O	I2C data (simple I2C mode)
	SSn	In	Input chip selector (simple SPI mode)
	DEn	Out	Output driver enable signal for half duplex (asynchronous mode)
I2C bus interface (RIIC) channel n (n = 0 to 8)	SCLn	I/O	Clock pins with Nch open drain
	SDAn	I/O	Data pins with Nch open drain
I3C bus interface (I3C)	SCL30	I/O	Clock pin
	SDA30	I/O	Data pin
General purpose timer (GPT)	GTIOC0A to 15A, GTIOC0B to 15B, GTIOC0AN to 15AN, GTIOC0BN to 15BN	I/O	Input capture for pulse width, output timer compare, and output PWM signals “nX” and “nXN” are anti-phase signals (X = A or B, n = 0 to 15).
	GTETRGA to GTETRGH	In	Input disable-output request signals for GPT outputs
Compare match timer (CMTW) channel n (n = 0 to 3)	TICn0, TICn1	In	Input capture signals
	TOCn0, TOCn1	Out	Output compare signals
Pulse density modulation interface (PDM) channel n (n = 0 to 6)	PDMDAT00 to 02, PDMDAT10 to 12	In	Input PDM data
	PDMCLK00 to 02, PDMCLK10 to 12	Out	Output PDM sampling clocks
Serial sound interface (SSIU) channel n	SSIn_SDATA	I/O	Serial sound data (TDM supported) (n = 0 to 9)*4
	SSIn_SCK	I/O	Serial clock (n = 0 to 7, 9)*4
	SSIn_WS	I/O	Word select (n = 0 to 7, 9)*4
SPDIF channel n (n = 0 to 2)	SPDIFn_OUT	Out	Output SPDIF data
	SPDIFn_IN	In	Input SPDIF data

Table 2.3-1 List of Pin Functions (7/7)

Classification	Pin Name	I/O	Function
I/O ports	P00 to P15	I/O	General purpose input/output pins with 3.3-V tolerance.
	P20 and P21	I/O	General purpose input/output pins included with I3C functions with 1.8-V tolerance.
	P30 to P47	I/O	General purpose input/output pins with 3.3-V tolerance.
	P50 to P57	I/O	General purpose input/output pins with 3.3-V tolerance.
	P60 to P67	I/O	General purpose input/output pins with 3.3-V tolerance. Selectable to use ELC function pins/groups.
	P70 to P77	I/O	General purpose input/output pins with 3.3-V tolerance.
	P80 to P87	I/O	General purpose input/output pins with 3.3-V tolerance. Selectable to use ELC function pins/groups.
	P90 to P92	I/O	General purpose input/output pins without 3.3-V tolerance.
	P93 to PA7	I/O	General purpose input/output pins with 3.3-V tolerance.
	PB0 to PB5	I/O	General purpose input/output pins without 3.3-V tolerance.

Note 1. Since this LSI has a resistor mounted between the USB20_VUBUSIN pin and V_{SS}, connect the pin to the USVBUS pin via a 30-kΩ (±1%) resistor. The schematic diagram is shown in **Figure 2.3-1.**

Note 2. QRESNSEL should be at the low level.

Note 3. SSLx1 to SSLx3 are output only.

Note 4. Half duplex: Ch. 0 to 9
Full duplex: Pairing ch. 0&9, 1&2, 3&4, 5&6, and 7&8

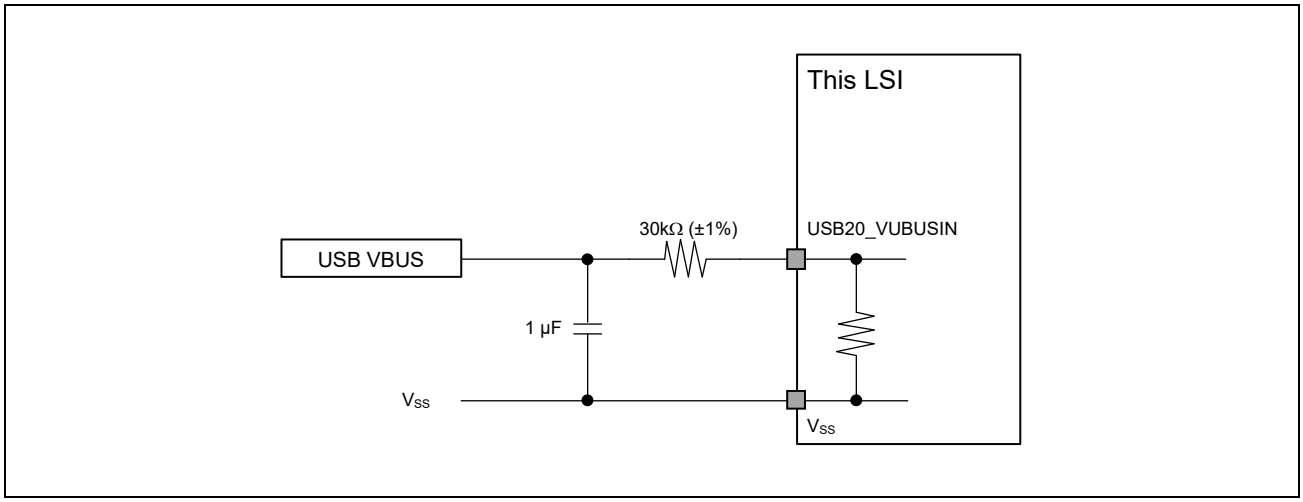


Figure 2.3-1 Connection Diagram of Resistor to USB20_VUBUSIN

Section 3 Electrical Characteristics

This section describes the electrical characteristics of this LSI.

3.1 Absolute Maximum Ratings

Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Table 3.1-1 Absolute Maximum Ratings (1/3)

Unit Name	Item	Symbol	Min.	Max.	Unit
CA55	VDD09_CA55	CA55_V_{DD09}	−0.4	1.2	V
PD_OTHERS	VDD08_OTHERS	OTHERS_V_{DD08}	−0.4	1.2	V
	VDD33_OTHERS	OTHERS_V_{DD33}	−0.4	3.8	V
	VDD33_PRE18_OTHERS	OTHERS_PRE18V_{DD33}	−0.4	2.5	V
	VDD1833_OTHERS_A	OTHERSA_V_{DD1833}	−0.4	3.8	V
	VDD1833_OTHERS_B	OTHERSB_V_{DD1833}	−0.4	3.8	V
	VDD1833_OTHERS_C	OTHERSC_V_{DD1833}	−0.4	3.8	V
	VDD1833_OTHERS_D	OTHERSD_V_{DD1833}	−0.4	3.8	V
PD_AWO	VDD08_AWO	AWO_V_{DD08}	−0.4	1.2	V
	VDD18_AWO	AWO_V_{DD18}	−0.4	2.5	V
	VDD1833_AWO	AWO_V_{DD1833}	−0.4	3.8	V
	VDD1833_PRE18_AWO	AWO_PRE18V_{DD1833}	−0.4	2.5	V
USB30	USB30_USVPH	USB30_USV_{PH}	−0.4	2.5	V
	USB30_USVPTX	USB30_USV_{PTX}	−0.4	1.2	V
	USB30_USVDD33	USB30_USV_{DD33}	−0.4	3.8	V
	USB30_USVDD18	USB30_USV_{DD18}	−0.4	2.5	V
	USB30_USDVDD	USB30_$USDV_{DD}$	−0.4	1.2	V
USB20	USB20_USVDD33	USB20_USV_{DD33}	−0.4	3.8	V
	USB20_USVDD18	USB20_USV_{DD18}	−0.4	2.5	V
	USB20_USDVDD	USB20_$USDV_{DD}$	−0.4	1.2	V
TSU0	TS0AVDD18	TS0AV_{DD18}	−0.4	2.5	V
	TS0DVDD08A	TS0DV_{DD08A}	−0.4	1.2	V
TSU1	TS1AVDD18	TS1AV_{DD18}	−0.4	2.5	V
	TS1DVDD08A	TS1DV_{DD08A}	−0.4	1.2	V
xSPI	VDD1833_XSPI	XSPI_V_{DD1833}	−0.4	3.8	V
SD0	VDD1833_SD0	SD0_V_{DD1833}	−0.4	3.8	V
	VDD1833_PRE18_SD	SD_PRE18V_{DD1833}	−0.4	2.5	V
SD1	VDD1833_SD1	SD1_V_{DD1833}	−0.4	3.8	V
	VDD1833_PRE18_SD	SD_PRE18V_{DD1833}	−0.4	2.5	V
SD2	VDD1833_SD2	SD2_V_{DD1833}	−0.4	3.8	V
	VDD1833_PRE18_SD2	SD2_PRE18V_{DD1833}	−0.4	2.5	V

Table 3.1-1 Absolute Maximum Ratings (2/3)

Unit Name	Item	Symbol	Min.	Max.	Unit
OTP	OTPVDD18	OTP_V_{DD18}	−0.4	2.5	V
DDR0	VDD08_DDR	DDR_V_{DD08}	−0.4	1.2	V
	DDR0_VDDQ	DDR0_V_{DDQ}	−0.4	1.5	V
	DDR0_VDDQLP	DDR0_V_{DDQLP}	−0.4	1.5	V
	DDR0_VAA	DDR0_V_{AA}	−0.4	2.5	V
GBETH0	VDD1833_ET0	ET0_V_{DD1833}	−0.4	3.8	V
	VDD1833_PRE18_ET0	ET0_PRE18V_{DD1833}	−0.4	2.5	V
GBETH1	VDD1833_ET1	ET1_V_{DD1833}	−0.4	3.8	V
	VDD1833_PRE18_ET1	ET1_PRE18V_{DD1833}	−0.4	2.5	V
CRU0	CSI0_MSVDD18	CSI0_MSV$_{DD18}$	−0.4	2.5	V
	CSI0_MSVDD0P8	CSI0_MSV$_{DD0P8}$	−0.4	1.2	V
CRU1	CSI1_MSVDD18	CSI1_MSV$_{DD18}$	−0.4	2.5	V
	CSI1_MSVDD0P8	CSI1_MSV$_{DD0P8}$	−0.4	1.2	V
DSI	DSI_VDD0P8	DSI_V_{DD0P8}	−0.4	1.2	V
	DSI_VDD12	DSI_V_{DD12}	−0.4	2.5	V
	DSI_VDD18	DSI_V_{DD18}	−0.4	2.5	V
PCIE	PCIE_VCC18ACMN	PCIE_$V_{CC18ACMN}$	−0.4	2.5	V
	PCIE_VCC18AL01	PCIE_$V_{CC18AL01}$	−0.4	2.5	V
	PCIE_VCC08AL01	PCIE_$V_{CC08AL01}$	−0.4	1.2	V
I3C	VDD1218_I3C	I3C_V_{DD1218}	−0.4	2.5	V
ADC	ADC0_ADAVDD18	ADC0_ADAV$_{DD18}$	−0.4	2.5	V
	ADC1_ADAVDD18	ADC1_ADAV$_{DD18}$	−0.4	2.5	V
	ADC2_ADAVDD18	ADC2_ADAV$_{DD18}$	−0.4	2.5	V
CPG	PLVDD_PLLCM33	PLLCM33_PLV$_{DD}$	−0.4	2.5	V
	PLVDD_PLLCLN_DTY_DRP	PLLCLN_DTY_DRP_PLV$_{DD}$	−0.4	2.5	V
	PLVDD_PLLCA55	PLLCA55_PLV$_{DD}$	−0.4	2.5	V
	PLVDD_PLLVDO_DSI	PLLVDO_DSI_PLV$_{DD}$	−0.4	2.5	V
	PLVDD_PLLDDR0	PLLDDR0_PLV$_{DD}$	−0.4	2.5	V
	PLVDD_PLLETH_GPU	PLLETH_GPU_PLV$_{DD}$	−0.4	2.5	V
	PLDVDD08_PLLCM33	PLLCM33_PLDV$_{DD08}$	−0.4	1.2	V
	PLDVDD08_PLLCLN_DTY_DRP	PLLCLN_DTY_DRP_PLDV$_{DD08}$	−0.4	1.2	V
	PLDVDD09_PLLCA55	PLLCA55_PLDV$_{DD09}$	−0.4	1.2	V
	PLDVDD08_PLLVDO_DSI	PLLVDO_DSI_PLDV$_{DD08}$	−0.4	1.2	V
	PLDVDD08_PLLDDR0	PLLDDR0_PLDV$_{DD08}$	−0.4	1.2	V
	PLDVDD08_PLLETH_GPU	PLLETH_GPU_PLDV$_{DD08}$	−0.4	1.2	V
CST	VDD1833_JTAG	JTAG_V_{DD1833}	−0.4	3.8	V
	VDD1833_PRE18_JTAG	JTAG_PRE18V_{DD1833}	−0.4	2.5	V
PWC	VDD18_PWC	PWC_V_{DD18}	−0.4	2.5	V
—	Input voltage (0.6-V I/O)	V_{in06}	−0.4	DDRn_V_{DDQLP} + 0.3*1	V
—	Input voltage (1.1-V I/O)	V_{in11}	−0.4	DDRn_V_{DDQ} + 0.3*1	V
—	Input voltage (1.2-V I/O)	V_{in12}	−0.4	V_{12} + 0.3*2	V
—	Input voltage (1.8-V I/O)	V_{in18}	−0.4	V_{18} + 0.3*3	V
—	Input voltage (1.8-V I/O (3.3-V tolerant))*4	V_{in18_tol}	−0.4	3.6	V

Table 3.1-1 Absolute Maximum Ratings (3/3)

Unit Name	Item	Symbol	Min.	Max.	Unit
—	Input voltage (3.3-V I/O)	V_{in33}	−0.4	V_{33} + 0.3*5	V
—	Analog input voltage (ADC I/O)	V_{ain18}	0	$ADAV_{DD18}$	V
—	Junction temperature	T_j	−40	125	°C
—	Storage temperature	T_{stg}	−40	150	°C

Note 1. n = 0, 1. The voltage to be applied must be within the absolute maximum rating (1.5 V).

Note 2. The voltage to be applied must be within the absolute maximum rating (2.5 V). V_{12} indicates the power supply voltage for 1.2-V I/O pins.

Note 3. The voltage to be applied must be within the absolute maximum rating (2.5 V). V_{18} indicates the power supply voltage for 1.8-V I/O pins. When 1.8-V is used for the 3.3/1.8-V switching I/O, this specification is applied.

Note 4. Pxx pins (with the exceptions of P2x, P90, P91, P92, and PBx)

Note 5. The voltage to be applied must be within the absolute maximum rating (3.8 V). V_{33} indicates the power supply voltage for 3.3-V I/O pins. When 1.8-V is used for the 3.3/1.8-V switching I/O, this specification is applied.

3.2 Recommended Operating Range

Table 3.2-1 Recommended Operating Range (1/2)

Unit Name	Item	Symbol	Min.	Typ.	Max.	Unit	Note
CA55	VDD09_CA55	CA55_V_{DD09}	0.86	0.9	0.94	V	0.9 V: OD*1
			0.76	0.8	0.84	V	0.8 V: ND*1
PD_OTHERS	VDD08_OTHERS	OTHERS_V_{DD08}	0.76	0.8	0.84	V	*2
	VDD33_OTHERS	OTHERS_V_{DD33}	3.135	3.3	3.465	V	
	VDD33_PRE18_OTHERS	OTHERS_PRE18V_{DD33}	1.71	1.8	1.89	V	
	VDD1833_OTHERS_A	OTHERSA_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_OTHERS_B	OTHERSB_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_OTHERS_C	OTHERSC_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_OTHERS_D	OTHERSD_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
PD_AWO	VDD08_AWO	AWO_V_{DD08}	0.76	0.8	0.84	V	
	VDD18_AWO	AWO_V_{DD18}	1.71	1.8	1.89	V	
	VDD1833_AWO	AWO_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_AWO	AWO_PRE18V_{DD1833}	1.71	1.8	1.89	V	
USB30	USB30_USVPH	USB30_USV_{PH}	1.71	1.8	1.89	V	
	USB30_USVPTX	USB30_USV_{PTX}	0.76	0.8	0.84	V	
	USB30_USVDD33	USB30_USV_{DD33}	3.14	3.3	3.46	V	
	USB30_USVDD18	USB30_USV_{DD18}	1.71	1.8	1.89	V	
	USB30_USDVDD	USB30_$USDV_{DD}$	0.76	0.8	0.84	V	
USB20	USB20_USVDD33	USB20_USV_{DD33}	3.14	3.3	3.46	V	
	USB20_USVDD18	USB20_USV_{DD18}	1.71	1.8	1.89	V	
	USB20_USDVDD	USB20_$USDV_{DD}$	0.76	0.8	0.84	V	
TSU0	TS0AVDD18	TS0AV_{DD18}	1.71	1.8	1.89	V	
	TS0DVDD08A	TS0DV_{DD08A}	0.76	0.8	0.84	V	
TSU1	TS1AVDD18	TS1AV_{DD18}	1.71	1.8	1.89	V	
	TS1DVDD08A	TS1DV_{DD08A}	0.76	0.8	0.84	V	
xSPI	VDD1833_XSPI	XSPI_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
SD0	VDD1833_SD0	SD0_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_SD	SD_PRE18V_{DD1833}	1.71	1.8	1.89	V	
SD1	VDD1833_SD1	SD1_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_SD	SD_PRE18V_{DD1833}	1.71	1.8	1.89	V	
SD2	VDD1833_SD2	SD2_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_SD2	SD2_PRE18V_{DD1833}	1.71	1.8	1.89	V	
OTP	OTPVDD18	OTP_V_{DD18}	1.71	1.8	1.89	V	

Table 3.2-1 Recommended Operating Range (2/2)

Unit Name	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DDR0	VDD08_DDR	DDR_V_{DD08}	0.76	0.8	0.84	V	*2
	DDR0_VDDQ	DDR0_V_{DDQ}	1.06	1.1	1.17	V	
	DDR0_VDDQLP	DDR0_V_{DDQLP}	0.57	0.6	0.65	V	0.6 V: LPDDR4X
			1.06	1.1	1.17	V	1.1 V: LPDDR4
	DDR0_VAA	DDR0_V_{AA}	1.71	1.8	1.89	V	
GBETH0	VDD1833_ET0	ET0_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_ET0	ET0_PRE18V_{DD1833}	1.71	1.8	1.89	V	
GBETH1	VDD1833_ET1	ET1_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_ET1	ET1_PRE18V_{DD1833}	1.71	1.8	1.89	V	
CRU0	CSI0_MSVDD18	CSI0_MSV$_{DD18}$	1.71	1.8	1.89	V	
	CSI0_MSVDD0P8	CSI0_MSV$_{DD0P8}$	0.76	0.8	0.84	V	
CRU1	CSI1_MSVDD18	CSI1_MSV$_{DD18}$	1.71	1.8	1.89	V	
	CSI1_MSVDD0P8	CSI1_MSV$_{DD0P8}$	0.76	0.8	0.84	V	
DSI	DSI_VDD0P8	DSI_V_{DD0P8}	0.76	0.8	0.84	V	
	DSI_VDD12	DSI_V_{DD12}	1.14	1.2	1.26	V	
	DSI_VDD18	DSI_V_{DD18}	1.71	1.8	1.89	V	
PCIE	PCIE_VCC18ACMN	PCIE_$V_{CC18ACMN}$	1.71	1.8	1.89	V	
	PCIE_VCC18AL01	PCIE_$V_{CC18AL01}$	1.71	1.8	1.89	V	
	PCIE_VCC08AL01	PCIE_$V_{CC08AL01}$	0.76	0.8	0.84	V	
I3C	VDD1218_I3C	I3C_V_{DD1218}	1.71	1.8	1.89	V	
			1.14	1.2	1.26	V	
ADC	ADC0_ADAVDD18	ADC0_ADAV$_{DD18}$	1.71	1.8	1.89	V	
	ADC1_ADAVDD18	ADC1_ADAV$_{DD18}$	1.71	1.8	1.89	V	
	ADC2_ADAVDD18	ADC2_ADAV$_{DD18}$	1.71	1.8	1.89	V	
CPG	PLVDD_PLLCM33	PLLCM33_PLV$_{DD}$	1.71	1.8	1.89	V	
	PLVDD_PLLCLN_DTY_DRP	PLLCLN_DTY_DRP_ PLV$_{DD}$	1.71	1.8	1.89	V	
	PLVDD_PLLCA55	PLLCA55_PLV$_{DD}$	1.71	1.8	1.89	V	
	PLVDD_PLLVDO_DSI	PLLVDO_DSI_PLV$_{DD}$	1.71	1.8	1.89	V	
	PLVDD_PLLDDR0	PLLDDR0_PLV$_{DD}$	1.71	1.8	1.89	V	
	PLVDD_PLLETH_GPU	PLLETH_GPU_PLV$_{DD}$	1.71	1.8	1.89	V	
	PLDVDD08_PLLCM33	PLLCM33_PLDV$_{DD08}$	0.76	0.8	0.84	V	
	PLDVDD08_PLLCLN_DTY_DRP	PLLCLN_DTY_DRP_PLD V_{DD08}	0.76	0.8	0.84	V	
	PLDVDD09_PLLCA55	PLLCA55_PLDV$_{DD09}$	0.86	0.9	0.94	V	0.9 V: OD*1
			0.76	0.8	0.84	V	0.8 V: ND*1
	PLDVDD08_PLLVDO_DSI	PLLVDO_DSI_PLDV$_{DD08}$	0.76	0.8	0.84	V	
	PLDVDD08_PLLDDR0	PLLDDR0_PLDV$_{DD08}$	0.76	0.8	0.84	V	
	PLDVDD08_PLLETH_GPU	PLLETH_GPU_PLDV$_{DD08}$	0.76	0.8	0.84	V	
CST	VDD1833_JTAG	JTAG_V_{DD1833}	3.14	3.3	3.46	V	
			1.71	1.8	1.89	V	
	VDD1833_PRE18_JTAG	JTAG_PRE18V_{DD1833}	1.71	1.8	1.89	V	
PWC	VDD18_PWC	PWC_V_{DD18}	1.71	1.8	1.89	V	

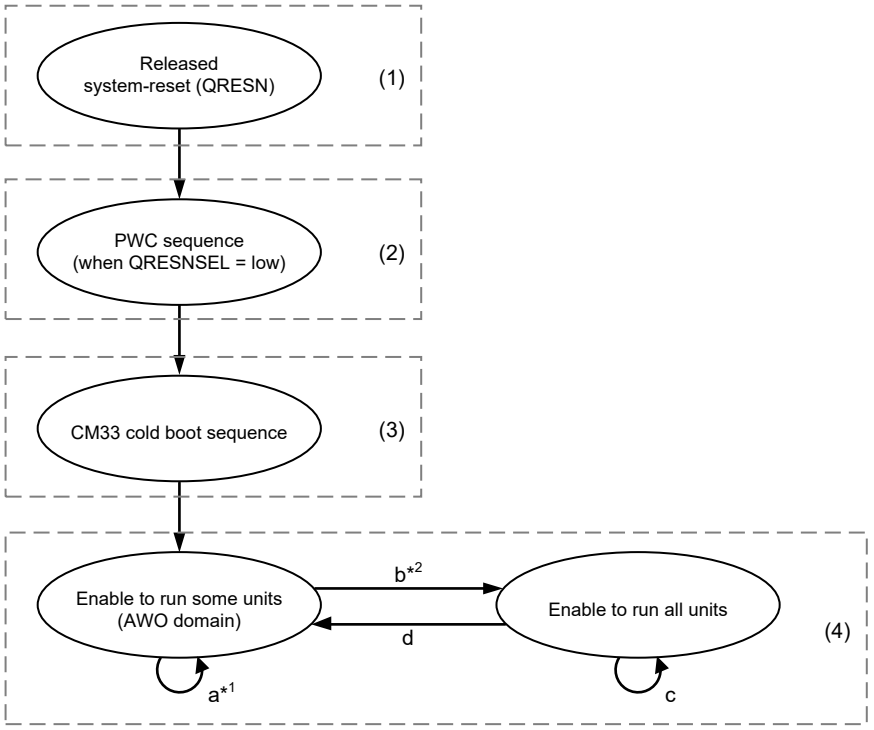
Note 1. OD: Over drive (up to 1.8-GHz operation frequency)
ND: Normal drive (up to 1.1-GHz operation frequency)

Note 2. To avoid the possibility of noise, separating this power supply from other power supply terminals is recommended.

3.3 Power-On/Off Sequence

3.3.1 CM33 Boot Mode (PWC Enabled)

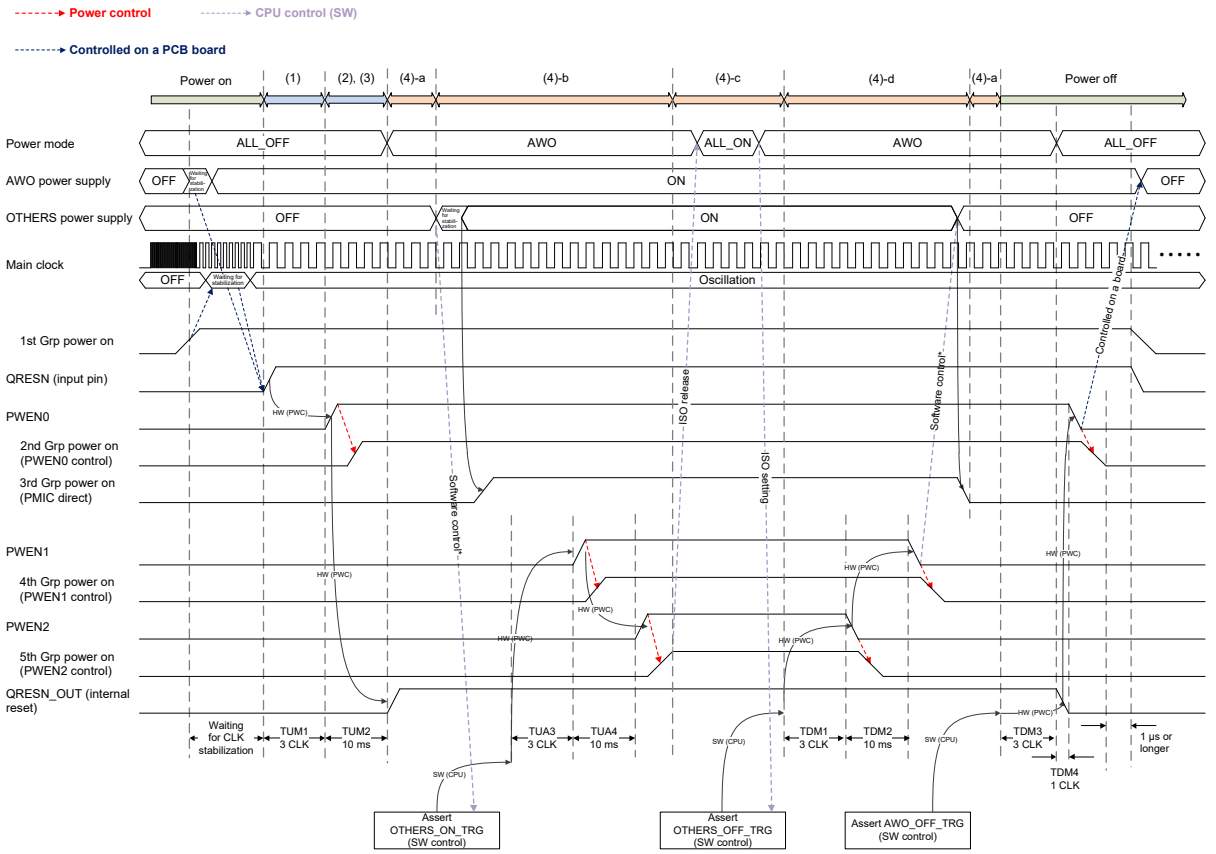
The state diagram of CM33 cold boot is shown in **Figure 3.3-1**. The boot mode states (1) to (4) refer to the sequence of (1) to (4) in **Figure 3.3-2**.



Note 1. CM33 operates the system managements.

Note 2. When the power mode switches from AWO to ALL_ON depending on the user system, CM33 sets the LSI registers and PMIC registers to supply power to the OTHERS domain.

Figure 3.3-1 CM33 Boot State Diagram



1st Grp power supply

0.8 V
VDD08_AWO
TS0DVDD08A
PLDVDD08_PLLCM33

1.8 V
VDD18_AWO
VDD1833_PRE18_AWO
VDD1833_PRE18_JTAG
VDD1833_PRE18_SD2
PLVDD_PLLCM33
TS0AVDD18
VDD18_PWC

1.2/1.8 V
VDD1218_I3C

(When used as 1.8 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

2nd Grp power supply

(When used as 3.3 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

1.8 V
ADCn_ADAVDD18 (n=0 to 2)
OTPVDD18

3rd Grp power supply

0.8 V
VDD08_DDR*1
VDD08_OTHERS*1
USB20_USDVDD
USB30_USVPTX
USB30_USDVDD
PCIE_VCC08AL01
DSI_VDD0P8
CSI0_MSVDD0P8
CSI1_MSVDD0P8
TS1DVDD08A
PLDVDD08_PLLCLN_DTY_DRP
PLDVDD08_PLLVDO_DSI
PLDVDD08_PLLDDR0
PLDVDD08_PLLETH_GPU

0.8 V / 0.9 V
VDD09_CA55
PLDVDD09_PLLCA55

1.1 V
DDR0_VDDQ*2

0.6 V / 1.1 V
DDR0_VDDQLP*2

1.8 V
VDD1833_PRE18_SD
USB20_USVDD18
USB30_USVPH
USB30_USVDD18
PCIE_VCC18ACMN
PCIE_VCC18AL01
VDD1833_PRE18_ET
TS1AVDD18
PLVDD_PLLCLN_DTY_DRP
PLVDD_PLLCA55
PLVDD_PLLVDO_DSI
PLVDD_PLLDDR0
PLVDD_PLLETH_GPU
VDD33_PRE18_OTHERS
DDR0_VAA

3.3 V
USB20_USVDD33
USB30_USVDD33

(When used as 1.8 V)
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

4th Grp power supply

1.8 V
DSI_VDD18
CSI0_MSVDD18
CSI1_MSVDD18

3.3 V
(or 3rd Grp)
VDD33_OTHERS

(When used as 3.3 V)
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

5th Grp power supply

1.2 V
DSI_VDD12

Note 1. Power supplies for VDD08_DDR and VDD08_OTHERS should be controlled simultaneously (within ±5 ms).
Note 2. When using DDR IO Retention mode, keep the power supply ON.

(Continued on next page)

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Software control: RIIC or PFC (GPIO) control

Note: The clock stabilization time depends on the board design. Make the setting according to the results of evaluation.

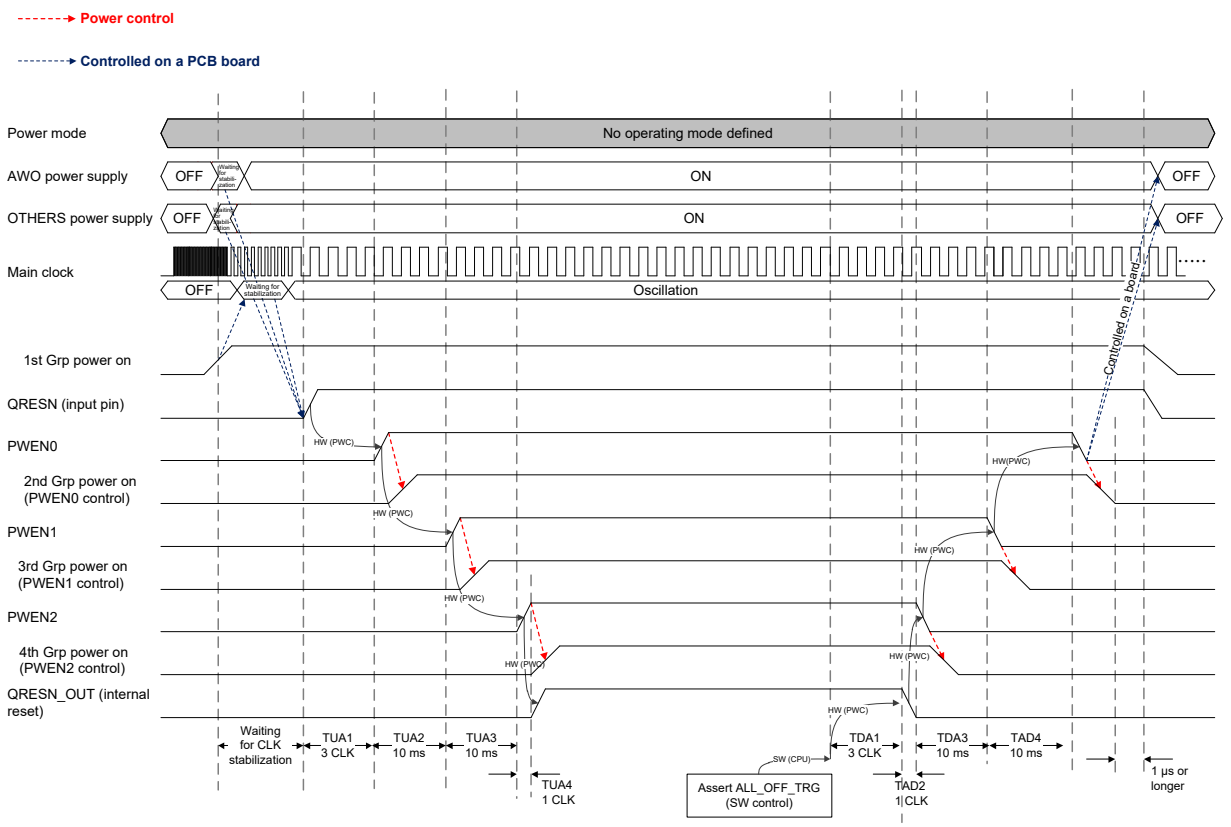
Note: Refer to the notes in **3.3.3** and **3.3.4** for details on the restrictions on the rise time and fall time of each power supply.

Note: When the QRESN pin becomes low, the PWEN0 to PWEN2 pins become low simultaneously.

Note: When using the PWC, set QRESN to the low level at the same time as or after the 1st Grp power off.

Figure 3.3-2 Power-On/Power-Off Sequence (CM33 Boot)

3.3.2 CA55 Boot Mode (PWC Enabled)



1st Grp power supply (1)

0.8 V
VDD08_AWO
TS0DVDD08A
PLDVDD08_PLLCM33

1.8 V
VDD18_AWO
VDD1833_PRE18_AWO
VDD1833_PRE18_JTAG
VDD1833_PRE18_SD2
PLVDD_PLLCM33
TS0AVDD18
VDD18_PWC

1.2/1.8 V
VDD1218_I3C

(When used as 1.8 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

1st Grp power supply (2)

0.8 V
VDD08_DDR*1
VDD08_OTHERS*1
USB20_USDVDD
USB30_USVPTX
USB30_USDVDD
PCIE_VCC08AL01
DSI_VDD0P8
CSI0_MSVDD0P8
CSI1_MSVDD0P8
TS1DVDD08A
PLDVDD08_PLLCLN_DTY_DRP
PLDVDD08_PLLVDO_DSI
PLDVDD08_PLLDDR0
PLDVDD08_PLLETH_GPU

0.8 V / 0.9 V
VDD09_CA55
PLDVDD09_PLLCA55

1.1 V
DDR0_VDDQ

0.6 V / 1.1 V
DDR0_VDDQLP

1.8 V
VDD1833_PRE18_SD
USB20_USVDD18
USB30_USVPH
USB30_USVDD18
PCIE_VCC18ACMN
PCIE_VCC18AL01
VDD1833_PRE18_ET
TS1AVDD18
PLVDD_PLLCLN_DTY_DRP
PLVDD_PLLCA55
PLVDD_PLLVDO_DSI
PLVDD_PLLDDR0
PLVDD_PLLETH_GPU
VDD33_PRE18_OTHERS
DDR0_VAA

3.3 V
USB20_USVDD33
USB30_USVDD33

(When used as 1.8 V)
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

2nd Grp power supply

(When used as 3.3 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

(or 3rd Grp)
1.8 V / 3.3 V
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

(or 1st Grp or 3rd Grp)
3.3 V
VDD33_OTHERS

1.8 V
ADCn_ADAVDD18(n=0 to 2)
OTPVDD18

3rd Grp power supply

1.8 V
DSI_VDD18
CSI0_MSVDD18
CSI1_MSVDD18

4th Grp power supply

1.2 V
DSI_VDD12

Note 1. Power supplies for VDD08_DDR and VDD08_OTHERS should be controlled simultaneously (within ±5 ms).

(Continued on next page)

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Note: The clock stabilization time depends on the board design. Make the setting according to the results of evaluation.

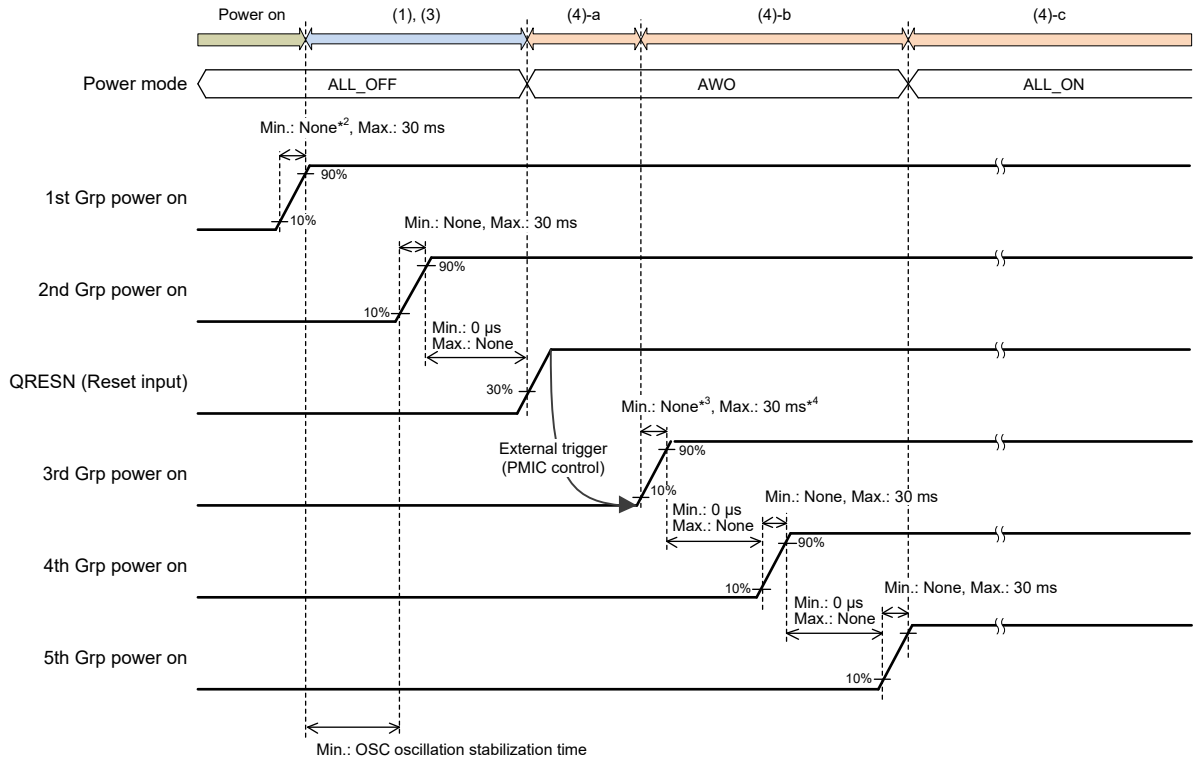
Note: Refer to the notes in **3.3.5** and **3.3.6** for details on the restrictions on the rise time and fall time of each power supply.

Note: When the QRESN pin becomes low, the PWEN0 to PWEN2 pins become low simultaneously.

Note: When using the PWC, set QRESN to the low level at the same time as or after the 1st Grp power off.

Figure 3.3-3 Power-On/Power-Off Sequence (CA55 Boot)

3.3.3 Power-On Sequence – CM33 Boot Mode (PWC Disabled)



1st Grp power supply

0.8 V
VDD08_AWO
TS0DVDD08A
PLDVDD08_PLLCM33

1.8 V
VDD18_AWO
VDD1833_PRE18_AWO
VDD1833_PRE18_JTAG
VDD1833_PRE18_SD2
PLVDD_PLLCM33
TS0AVDD18
VDD18_PWC

1.2/1.8 V
VDD1218_I3C

(When used as 1.8 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

2nd Grp power supply

(When used as 3.3 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

1.8 V
ADCn_ADAVDD18(n=0 to 2)
OTPVDD18

3rd Grp power supply

0.8 V
VDD08_DDR*1
VDD08_OTHERS*1
USB20_USDVDD
USB30_USVPTX
USB30_USDVDD
PCIE_VCC08AL01
DSI_VDD0P8
CSI0_MSVDD0P8
CSI1_MSVDD0P8
TS1DVDD08A
PLDVDD08_PLLCLN_DTY_DRP
PLDVDD08_PLLVDO_DSI
PLDVDD08_PLLDDR0
PLDVDD08_PLLETH_GPU

0.8 V / 0.9 V
VDD09_CA55
PLDVDD09_PLLCA55

1.1 V
DDR0_VDDQ*5

0.6 V / 1.1 V
DDR0_VDDQLP*5

1.8 V
VDD1833_PRE18_SD
USB20_USVDD18
USB30_USVPH
USB30_USVDD18
PCIE_VCC18ACMN
PCIE_VCC18AL01
VDD1833_PRE18_ET
TS1AVDD18
PLVDD_PLLCLN_DTY_DRP
PLVDD_PLLCA55
PLVDD_PLLVDO_DSI
PLVDD_PLLDDR0
PLVDD_PLLETH_GPU
VDD33_PRE18_OTHERS
DDR0_VAA

3.3 V
USB20_USVDD33
USB30_USVDD33

(When used as 1.8 V)
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

4th Grp power supply

1.8 V
DSI_VDD18
CSI0_MSVDD18
CSI1_MSVDD18

3.3 V
(or 3rd Grp)
VDD33_OTHERS

(When used as 3.3 V)
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

5th Grp power supply

1.2 V
DSI_VDD12

(Continued on next page)

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Note 1. Power supplies for VDD08_DDR and VDD08_OTHERS should be controlled simultaneously (within ±5 ms).

Note 2. TS0DVDD08A, TS0AVDD18: Min. 10 µs

Note 3.
- DDR0_VDDQ, DDR0_VDDQLP (1.1 V): Min. 180 µs
- DDR0_VDDQLP (0.6 V): Min. 100 µs
- DDR0_VAA: Min. 290 µs
- VDD08_DDR: Min. 5 µs
- USB30_USVPTX, USB30_USVPH: Min. 10 µs
- USB20_USDVDD, USB30_USDVDD: Min. 10 µs
- USB20_USVDD18, USB30_USVDD18: Min. 20 µs
- USB20_USVDD33, USB30_USVDD33: Min. 30 µs
- TS1DVDD08A, TS1AVDD18: Min. 10 µs

Note 4. USB20_USDVDD, USB20_USVDD18, USB20_USVDD33, USB30_USDVDD, USB30_USVDD18, USB30_USVDD33: Max. 10 ms

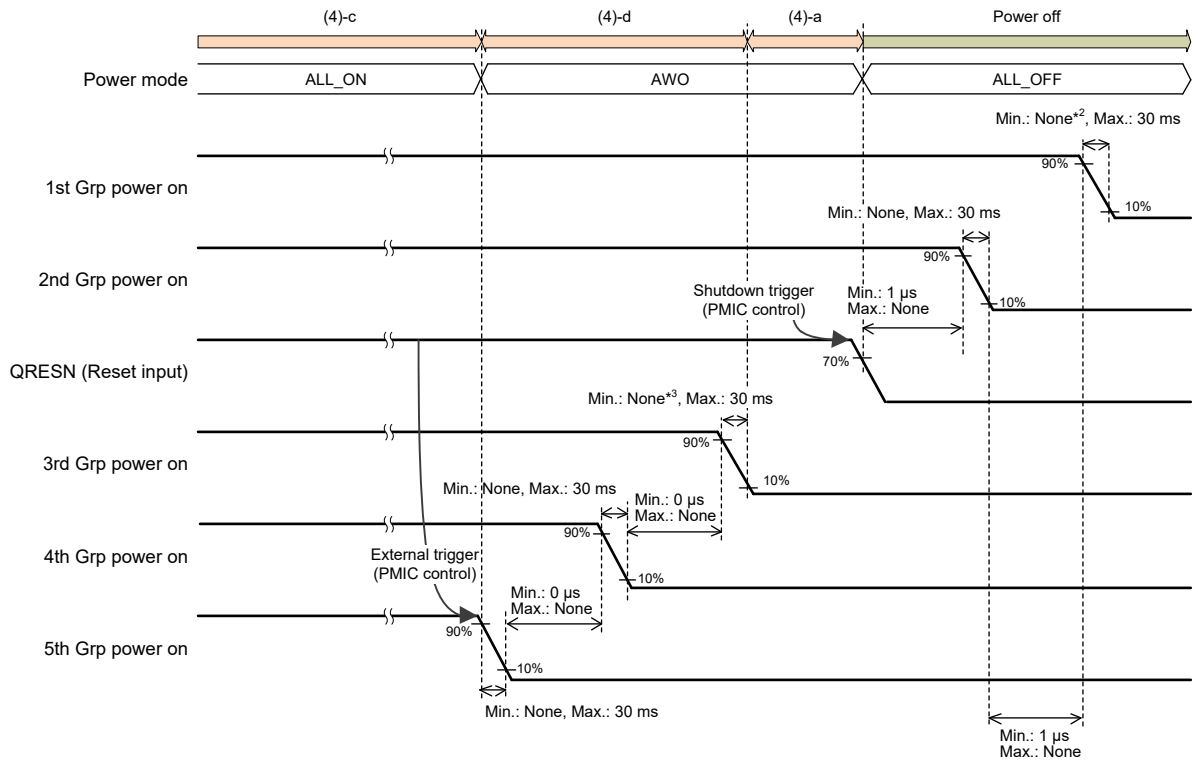
Note 5. When using DDR IO Retention mode, keep the power supply ON.

Note: The clock stabilization time depends on the board design. Make the setting according to the results of evaluation.

Note: The rise time of each power supply must be compliant with the maximum 30 ms regulation.

Figure 3.3-4 Power-On Sequence (CM33 Boot Mode)

3.3.4 Power-Off Sequence – CM33 Boot Mode (PWC Disabled)



1st Grp power supply

0.8 V
VDD08_AWO
TS0DVDD08A
PLDVDD08_PLLCM33

1.8 V
VDD18_AWO
VDD1833_PRE18_AWO
VDD1833_PRE18_JTAG
VDD1833_PRE18_SD2
PLVDD_PLLCM33
TS0AVDD18
VDD18_PWC

1.2/1.8 V
VDD1218_I3C

(When used as 1.8 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

2nd Grp power supply

(When used as 3.3 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

1.8 V
ADCn_ADAVDD18(n=0 to 2)
OTPVDD18

3rd Grp power supply

0.8 V
VDD08_DDR*1
VDD08_OTHERS*1
USB20_USDVDD
USB30_USVPTX
USB30_USDVDD
PCIE_VCC08AL01
DSI_VDD0P8
CSI0_MSVDD0P8
CSI1_MSVDD0P8
TS1DVDD08A
PLDVDD08_PLLCLN_DTY_DRP
PLDVDD08_PLLVDO_DSI
PLDVDD08_PLLDDR0
PLDVDD08_PLLETH_GPU

0.8 V / 0.9 V
VDD09_CA55
PLDVDD09_PLLCA55

1.1 V
DDR0_VDDQ*4

0.6 V / 1.1 V
DDR0_VDDQLP*4

1.8 V
VDD1833_PRE18_SD
USB20_USVDD18
USB30_USVPH
USB30_USVDD18
PCIE_VCC18ACMN
PCIE_VCC18AL01
VDD1833_PRE18_ET
TS1AVDD18
PLVDD_PLLCLN_DTY_DRP
PLVDD_PLLCA55
PLVDD_PLLVDO_DSI
PLVDD_PLLDDR0
PLVDD_PLLETH_GPU
VDD33_PRE18_OTHERS
DDR0_VAA

3.3 V
USB20_USVDD33
USB30_USVDD33

(When used as 1.8 V)
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

4th Grp power supply

1.8 V
DSI_VDD18
CSI0_MSVDD18
CSI1_MSVDD18

3.3 V
(or 3rd Grp)
VDD33_OTHERS

(When used as 3.3 V)
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

5th Grp power supply

1.2 V
DSI_VDD12

(Continued on next page)

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Note 1. Power supplies for VDD08_DDR and VDD08_OTHERS should be controlled simultaneously (within ±5 ms).

Note 2. TS0DVDD08A, TS0AVDD18: Min. 10 µs

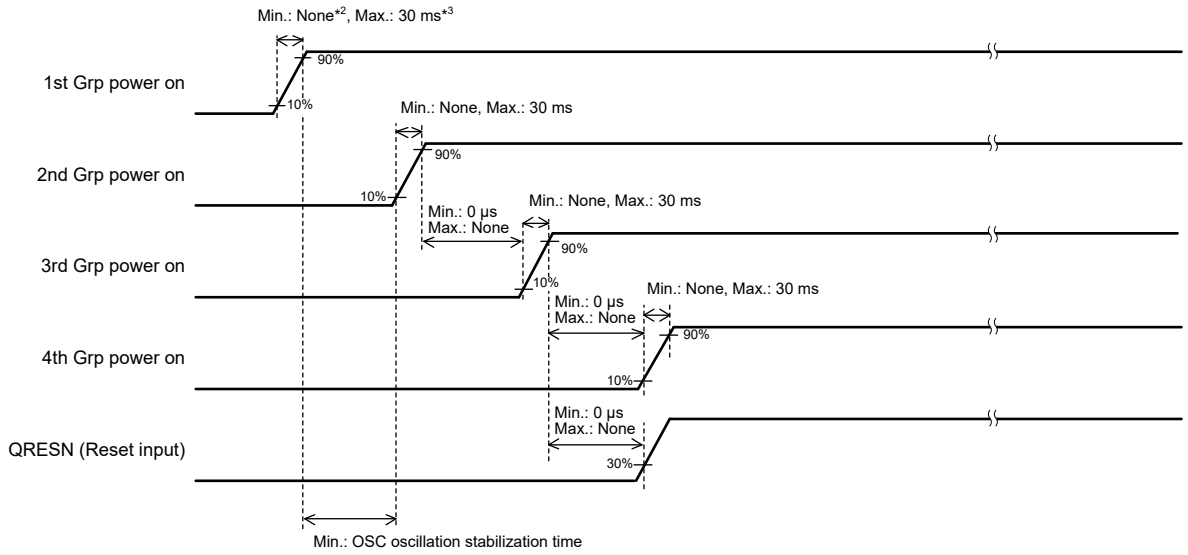
Note 3. TS1DVDD08A, TS1AVDD18: Min. 10 µs

Note 4. When using DDR IO Retention mode, keep the power supply ON.

Note: The fall time of each power supply must be compliant with the maximum 30 ms regulation.

Figure 3.3-5 Power-Off Sequence (CM33 Boot Mode)

3.3.5 Power-On Sequence – CA55 Boot Mode (PWC Disabled)



1st Grp power supply (1)

0.8 V
VDD08_AWO
TS0DVDD08A
PLDVDD08_PLLCM33

1.8 V
VDD18_AWO
VDD1833_PRE18_AWO
VDD1833_PRE18_JTAG
VDD1833_PRE18_SD2
PLVDD_PLLCM33
TS0AVDD18
VDD18_PWC

1.2/1.8 V
VDD1218_I3C

(When used as 1.8 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

1st Grp power supply (2)

0.8 V
VDD08_DDR*1
VDD08_OTHERS*1
USB20_USDVDD
USB30_USVPTX
USB30_USDVDD
PCIE_VCC08AL01
DSI_VDD0P8
CSI0_MSVDD0P8
CSI1_MSVDD0P8
TS1DVDD08A
PLDVDD08_PLLCLN_DTY_DRP
PLDVDD08_PLLVDO_DSI
PLDVDD08_PLLDDR0
PLDVDD08_PLLETH_GPU

0.8 V / 0.9 V
VDD09_CA55
PLDVDD09_PLLCA55

1.1 V
DDR0_VDDQ

0.6 V / 1.1 V
DDR0_VDDQLP

1.8 V
VDD1833_PRE18_SD
USB20_USVDD18
USB30_USVPH
USB30_USVDD18
PCIE_VCC18ACMN
PCIE_VCC18AL01
VDD1833_PRE18_ET
TS1AVDD18
PLVDD_PLLCLN_DTY_DRP
PLVDD_PLLCA55
PLVDD_PLLVDO_DSI
PLVDD_PLLDDR0
PLVDD_PLLETH_GPU
VDD33_PRE18_OTHERS
DDR0_VAA

3.3 V
USB20_USVDD33
USB30_USVDD33

(When used as 1.8 V)
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

2nd Grp power supply

(When used as 3.3 V)
VDD1833_JTAG
VDD1833_XSPI
VDD1833_SD2
VDD1833_AWO
VDD1833_OTHERS_A
VDD1833_OTHERS_B
VDD1833_OTHERS_C
VDD1833_OTHERS_D

(or 3rd Grp)
1.8 V / 3.3 V
VDD1833_SD0
VDD1833_SD1
VDD1833_ET0
VDD1833_ET1

(or 1st Grp or 3rd Grp)
3.3 V
VDD33_OTHERS

1.8 V
ADCn_ADAVDD18(n=0 to 2)
OTPVDD18

3rd Grp power supply

1.8 V
DSI_VDD18
CSI0_MSVDD18
CSI1_MSVDD18

4th Grp power supply

1.2 V
DSI_VDD12

(Continued on next page)

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Note 1. Power supplies for VDD08_DDR and VDD08_OTHERS should be controlled simultaneously (within ±5 ms).

Note 2.
- TS0DVDD08A, TS0AVDD18: Min. 10 µs
- DDR0_VDDQ, DDR0_VDDQLP (1.1 V): Min. 180 µs
- DDR0_VDDQLP (0.6 V): Min. 100 µs
- DDR0_VAA: Min. 290 µs
- VDD08_DDR: Min. 5 µs
- USB30_USVPTX, USB30_USVPH: Min. 10 µs
- USB20_USDVDD, USB30_USDVDD: Min. 10 µs
- USB20_USVDD18, USB30_USVDD18: Min. 20 µs
- USB20_USVDD33, USB30_USVDD33: Min. 30 µs
- TS1DVDD08A, TS1AVDD18: Min. 10 µs

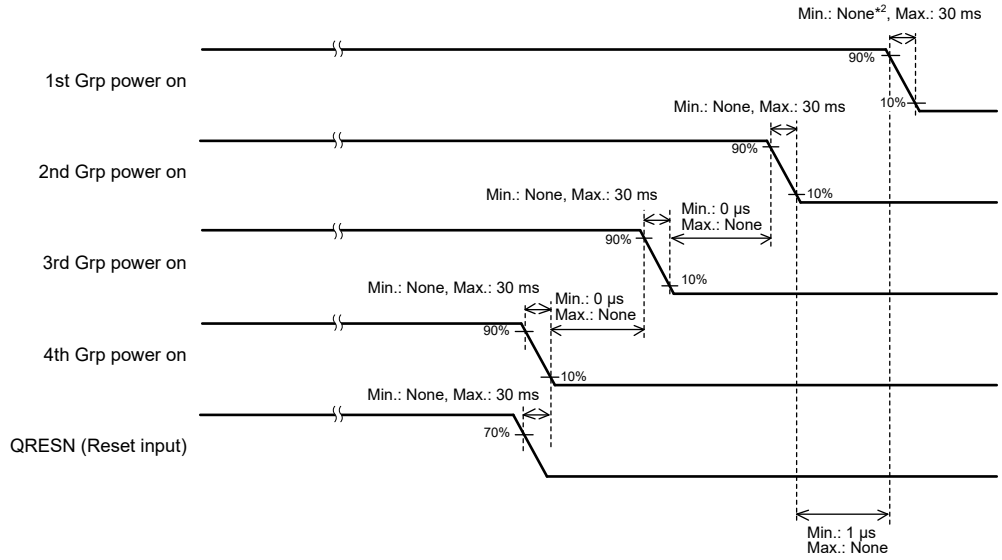
Note 3. USB20_USDVDD, USB20_USVDD18, USB20_USVDD33, USB30_USDVDD, USB30_USVDD18, USB30_USVDD33: Max. 10 ms

Note: The clock stabilization time depends on the board design. Make the setting according to the results of evaluation.

Note: The rise time of each power supply must be compliant with the maximum 30 ms regulation.

Figure 3.3-6 Power-On Sequence (CA55 Boot Mode)

3.3.6 Power-Off Sequence – CA55 Boot Mode (PWC Disabled)



1st Grp power supply (1)
0.8 V VDD08_AWO TS0DVDD08A PLDVDD08_PLLCM33
1.8 V VDD18_AWO VDD1833_PRE18_AWO VDD1833_PRE18_JTAG VDD1833_PRE18_SD2 PLVDD_PLLCM33 TS0AVDD18 VDD18_PWC
1.2/1.8 V VDD1218_I3C
(When used as 1.8 V) VDD1833_JTAG VDD1833_XSPI VDD1833_SD2 VDD1833_AWO VDD1833_OTHERS_A VDD1833_OTHERS_B VDD1833_OTHERS_C VDD1833_OTHERS_D

1st Grp power supply (2)	
0.8 V VDD08_DDR*1 VDD08_OTHERS*1 USB20_USDVDD USB30_USVPTX USB30_USDVDD PCIE_VCC08AL01 DSI_VDD0P8 CSI0_MSVDD0P8 CSI1_MSVDD0P8 TS1DVDD08A PLDVDD08_PLLCLN_DTY_DRP PLDVDD08_PLLVDO_DSI PLDVDD08_PLLDDR0 PLDVDD08_PLLETH_GPU	1.8 V VDD1833_PRE18_SD USB20_USVDD18 USB30_USVPH USB30_USVDD18 PCIE_VCC18ACMN PCIE_VCC18AL01 VDD1833_PRE18_ET TS1AVDD18 PLVDD_PLLCLN_DTY_DRP PLVDD_PLLCA55 PLVDD_PLLVDO_DSI PLVDD_PLLDDR0 PLVDD_PLLETH_GPU VDD33_PRE18_OTHERS DDR0_VAA
0.8 V / 0.9 V VDD09_CA55 PLDVDD09_PLLCA55	3.3 V USB20_USVDD33 USB30_USVDD33
1.1 V DDR0_VDDQ	(When used as 1.8 V) VDD1833_SD0 VDD1833_SD1 VDD1833_ET0 VDD1833_ET1
0.6 V / 1.1 V DDR0_VDDQLP	

2nd Grp power supply
(When used as 3.3 V) VDD1833_JTAG VDD1833_XSPI VDD1833_SD2 VDD1833_AWO VDD1833_OTHERS_A VDD1833_OTHERS_B VDD1833_OTHERS_C VDD1833_OTHERS_D
(or 3rd Grp) 1.8 V / 3.3 V VDD1833_SD0 VDD1833_SD1 VDD1833_ET0 VDD1833_ET1
(or 1st Grp or 3rd Grp) 3.3 V VDD33_OTHERS
1.8 V ADCn_ADAVDD18(n=0 to 2) OTPVDD18

3rd Grp power supply
1.8 V DSI_VDD18 CSI0_MSVDD18 CSI1_MSVDD18

4th Grp power supply
1.2 V DSI_VDD12

Note 1. Power supplies for VDD08_DDR and VDD08_OTHERS should be controlled simultaneously (within ±5 ms).

Note 2. – TS0DVDD08A, TS0AVDD18: Min. 10 µs
– TS1DVDD08A, TS1AVDD18: Min. 10 µs

Note: The fall time of each power supply must be compliant with the maximum 30 ms regulation.

Figure 3.3-7 Power-Off Sequence (CA55 Boot Mode)

3.4 DC Characteristics

3.4.1 Maximum Supply Current

Conditions for the supply current: Power supply voltage = Max. value, Tj = −40 to 125ºC

Table 3.4-1 Max. Supply Currents during Operation (1/2)

Unit Name	Item	Symbol	Max.	Unit	Note
CA55	0.8-V (or 0.9-V) power supply current	I_{DD09_CA55}	3031	mA	VDD09_CA55
PD_OTHERS	0.8-V core power supply current	I_{DD08_OTHERS}	7489	mA	VDD08_OTHERS
	3.3-V core power supply current	I_{DD33_OTHERS}	1	mA	VDD33_OTHERS
	Pre-driver power supply current	$I_{DD33PRE18\_OTHERS}$	1	mA	VDD33_PRE18_OTHERS
	Group A I/O power supply current	$I_{DD1833\_OTHERSA}$	25	mA	VDD1833_OTHERS_A
	Group B I/O power supply current	$I_{DD1833\_OTHERSB}$	25	mA	VDD1833_OTHERS_B
	Group C I/O power supply current	$I_{DD1833\_OTHERSC}$	25	mA	VDD1833_OTHERS_C
	Group D I/O power supply current	$I_{DD1833\_OTHERSD}$	13	mA	VDD1833_OTHERS_D
PD_AWO	0.8-V core power supply current	I_{DD08_AWO}	315	mA	VDD08_AWO
	1.8-V core power supply current	I_{DD18_AWO}	3	mA	VDD18_AWO
	I/O power supply current	I_{DD1833_AWO}	8	mA	VDD1833_AWO
	Pre-driver power supply current	$I_{DD1833PRE18\_AWO}$	14	mA	VDD1833_PRE18_AWO
USB30	1.8-V PHY power supply current	$I_{DDUSB30\_USVPH}$	31	mA	USB30_USVPH
	0.8-V PHY power supply current	$I_{DDUSB30\_USVPTX}$	53	mA	USB30_USVPTX
	3.3-V PHY power supply current	$I_{DDUSB30\_USVDD33}$	12	mA	USB30_USVDD33
	1.8-V PHY power supply current	$I_{DDUSB30\_USVDD18}$	56	mA	USB30_USVDD18
	0.8-V PHY power supply current	$I_{DDUSB30\_USDVDD}$	16	mA	USB30_USDVDD
USB20	3.3-V PHY power supply current	$I_{DDUSB20\_USVDD33}$	12	mA	USB20_USVDD33
	1.8-V PHY power supply current	$I_{DDUSB20\_USVDD18}$	56	mA	USB20_USVDD18
	0.8-V PHY power supply current	$I_{DDUSB20\_USDVDD}$	16	mA	USB20_USDVDD
TSU0	1.8-V power supply current	$I_{DDTS0AVDD18}$	1	mA	TS0AVDD18
	0.8-V power supply current	$I_{DDTS0DVDD08A}$	1	mA	TS0DVDD08A
TSU1	1.8-V power supply current	$I_{DDTS1AVDD18}$	1	mA	TS1AVDD18
	0.8-V power supply current	$I_{DDTS1DVDD08A}$	1	mA	TS1DVDD08A
xSPI	I/O power supply current	I_{DD1833_XSPI}	16	mA	VDD1833_XSPI
SD0	I/O power supply current	I_{DD1833_SD0}	16	mA	VDD1833_SD0
	Pre-driver power supply current	$I_{DD1833PRE18\_SD}$	2	mA	VDD1833_PRE18_SD
SD1	I/O power supply current	I_{DD1833_SD1}	9	mA	VDD1833_SD1
SD2	I/O power supply current	I_{DD1833_SD2}	9	mA	VDD1833_SD2
	Pre-driver power supply current	$I_{DD1833PRE18\_SD2}$	2	mA	VDD1833_PRE18_SD2
OTP	1.8-V power supply current	$I_{DDOTPVDD18}$	6	mA	OTPVDD18
DDR0	0.8-V core power supply current	I_{DD08_DDR}	934	mA	VDD08_DDR
	1.1-V PHY power supply current	I_{DDQ_DDR0}	760	mA	DDR0_VDDQ
	PHY power supply current	I_{DDQLP_DDR0}	242	mA	DDR0_VDDQLP
	1.8-V PLL power supply current	I_{DDVAA_DDR0}	5	mA	DDR0_VAA
GBETH0	I/O power supply current	I_{DD1833_ET0}	11	mA	VDD1833_ET0
	Pre-driver power supply current	$I_{DD1833PRE18\_ET0}$	4	mA	VDD1833_PRE18_ET
GBETH1	I/O power supply current	I_{DD1833_ET1}	11	mA	VDD1833_ET1

Table 3.4-1 Max. Supply Currents during Operation (2/2)

Unit Name	Item	Symbol	Max.	Unit	Note
CRU0	1.8-V PHY power supply current	$I_{DDMSVDD18\_CSI0}$	8	mA	CSI0_MSVDD18
	0.8-V core power supply current	$I_{DDMSVDD0P8\_CSI0}$	25	mA	CSI0_MSVDD0P8
CRU1	1.8-V PHY power supply current	$I_{DDMSVDD18\_CSI1}$	8	mA	CSI1_MSVDD18
	0.8-V core power supply current	$I_{DDMSVDD0P8\_CSI1}$	25	mA	CSI1_MSVDD0P8
DSI	0.8-V core power supply current	I_{DD0P8_DSI}	43	mA	DSI_VDD0P8
	1.2-V PHY power supply current	I_{DD12_DSI}	1	mA	DSI_VDD12
	1.8-V PHY power supply current	I_{DD18_DSI}	8	mA	DSI_VDD18
PCIE	1.8-V power supply current	$I_{DDPCIEVCC18ACMN}$	19	mA	PCIE_VCC18ACMN
	1.8-V PHY power supply current	$I_{DDPCIEVCC18AL01}$	53	mA	PCIE_VCC18AL01
	0.8-V PHY power supply current	$I_{DDPCIEVCC08AL01}$	112	mA	PCIE_VCC08AL01
I3C	I/O power supply current	I_{DD1218_I3C}	1	mA	VDD1218_I3C
ADC	1.8-V analog power supply current	$I_{DDADC0\_ADAVDD18}$	1	mA	ADC0_ADAVDD18
	1.8-V analog power supply current	$I_{DDADC1\_ADAVDD18}$	1	mA	ADC1_ADAVDD18
	1.8-V analog power supply current	$I_{DDADC2\_ADAVDD18}$	1	mA	ADC2_ADAVDD18
CPG	PLLCM33 1.8-V power supply current	$I_{DDPLVDD\_PLLCM33}$	2	mA	PLVDD_PLLCM33
	PLLCLN_DTY_DRP 1.8-V power supply current	$I_{DDPLVDD\_PLLCLNDTYDRP}$	6	mA	PLVDD_PLLCLN_DTY_DRP
	PLLCA55 1.8-V power supply current	$I_{DDPLVDD\_PLLCA55}$	2	mA	PLVDD_PLLCA55
	PLLVDO_DSI 1.8-V power supply current	$I_{DDPLVDD\_PLLVCDDSI}$	4	mA	PLVDD_PLLVDO_DSI
	PLLDDR0 1.8-V power supply current	$I_{DDPLVDD\_PLLDDR0}$	2	mA	PLVDD_PLLDDR0
	PLLETH_GPU 1.8-V power supply current	$I_{DDPLVDD\_PLLETHGPU}$	4	mA	PLVDD_PLLETH_GPU
	PLLCM33 0.8-V power supply current	$I_{DDPLVDD08\_PLLCM33}$	3	mA	PLDVDD08_PLLCM33
	PLLCLN_DTY_DRP 0.8-V power supply current	$I_{DDPLVDD08\_PLLCLNDTYDRP}$	8	mA	PLDVDD08_PLLCLN_DTY_DRP
	PLLCA55 0.8-V (or 0.9-V) power supply current	$I_{DDPLVDD08\_PLLCA55}$	3	mA	PLDVDD09_PLLCA55
	PLLVDO_DSI 0.8-V power supply current	$I_{DDPLVDD08\_PLLVCDDSI}$	5	mA	PLDVDD08_PLLVDO_DSI
	PLLDDR0 0.8-V power supply current	$I_{DDPLVDD08\_PLLDDR0}$	3	mA	PLDVDD08_PLLDDR0
	PLLETH_GPU 0.8-V power supply current	$I_{DDPLVDD08\_PLLETHGPU}$	5	mA	PLDVDD08_PLLETH_GPU
CST	I/O power supply current	I_{DD1833_JTAG}	2	mA	VDD1833_JTAG
	Pre-driver power supply current	$I_{DD1833PRE18\_JTAG}$	1	mA	VDD1833_PRE18_JTAG
PWC	1.8-V I/O power supply current	I_{DD18_PWC}	1	mA	VDD18_PWC

3.4.2 Standard I/O Characteristics

For the I/O types, refer to the external pin list in **2.2.1 List of External Pins**.

Table 3.4-2 DC Characteristics

V_{DD} = 1.11 V to 1.95 V (1.8/1.2-V switching I/O type), V_{DD} = 1.65 V to 1.95 V (1.8-V I/O type and 1.8-V OSC I/O type), V_{DD} = 1.65 V to 3.60 V (3.3/1.8-V switching I/O types 1, 2 and 3), V_{DD} = 3.00 V to 3.60 V (3.3-V I/O type) (1/4)

Item	I/O Type	Symbol	Min.	Typ.	Max.	Unit	Condition
External voltage tolerance	3.3/1.8-V switching I/O type 2	V_{TOL}	—	—	3.6	V	V_{DD} power-off & on
High-level input voltage	1.8/1.2-V switching I/O type (1.2 V)	V_{IH}	0.8 × V_{DD}	—	V_{DD} + 0.3	V	—
	1.8/1.2-V switching I/O type (1.8 V)	V_{IH}	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
	1.8-V I/O type 1.8-V OSC I/O type 3.3/1.8-V switching I/O type 1 3.3/1.8-V switching I/O type 2 3.3/1.8-V switching I/O type 3 3.3-V I/O type	V_{IH}	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
Low-level input voltage	1.8/1.2-V switching I/O type (1.2 V)	V_{IL}	−0.3	—	0.2 × V_{DD}	V	—
	1.8/1.2-V switching I/O type (1.8 V)	V_{IL}	−0.3	—	0.3 × V_{DD}	V	—
	1.8-V I/O type 1.8-V OSC I/O type 3.3/1.8-V switching I/O type 1 3.3/1.8-V switching I/O type 2 3.3/1.8-V switching I/O type 3 3.3-V I/O type	V_{IL}	−0.3	—	0.3 × V_{DD}	V	—
Hysteresis voltage	1.8/1.2-V switching I/O type 1.8-V I/O type	ΔV	0.1 × V_{DD}	—	—	V	—
	3.3/1.8-V switching I/O type 1*1 3.3/1.8-V switching I/O type 2*2	ΔV	0.08 × V_{DD}	—	—	V	—
	3.3/1.8-V switching I/O type 3*13	ΔV	0.1	—	—	V	—

Table 3.4-2 DC Characteristics

V_{DD} = 1.11 V to 1.95 V (1.8/1.2-V switching I/O type), V_{DD} = 1.65 V to 1.95 V (1.8-V I/O type and 1.8-V OSC I/O type), V_{DD} = 1.65 V to 3.60 V (3.3/1.8-V switching I/O types 1, 2 and 3), V_{DD} = 3.00 V to 3.60 V (3.3-V I/O type) (2/4)

Item	I/O Type	Symbol	Min.	Typ.	Max.	Unit	Condition
Input leakage current	1.8/1.2-V switching I/O type (1.2 V)	I_I	−10	—	10	µA	V_{in} = V_{SS} or V_{DD} max & V_{DD} power-on
			−10	—	10	µA	V_{in} = V_{SS} or V_{DD} max & V_{DD} power-off
	1.8/1.2-V switching I/O type (1.8 V)	I_I	−15	—	15	µA	V_{in} = V_{DD} max & V_{DD} power-on
			−18	—	18	µA	V_{in} = V_{SS} or V_{DD} max & V_{DD} power-off
	1.8-V I/O type 1.8-V OSC I/O type 3.3/1.8-V switching I/O type 1	I_I	−12	—	12	µA	V_{in} = V_{DD} max & V_{DD} power-on
	3.3/1.8-V switching I/O type 2	I_I	−12	—	12	µA	V_{in} = V_{DD} max & V_{DD} power-on
			−18	—	18	µA	V_{in} = V_{SS} or V_{DD} max & V_{DD} power-off
	3.3/1.8-V switching I/O type 3 3.3-V I/O type	I_I	−12	—	12	µA	V_{in} = V_{DD} max & V_{DD} power-on
Input pull-down resistor current	1.8/1.2-V switching I/O type*3 (1.2 V)	I_{RPU}	10	—	100	µA	V_{in} = V_{DD} max
	1.8/1.2-V switching I/O type*3 (1.8 V)	I_{RPU}	25	—	130	µA	V_{in} = V_{DD} max
	1.8-V I/O type*5	I_{RPU}	25	—	130	µA	V_{in} = V_{DD} max
	3.3/1.8-V switching I/O type 1*7 3.3/1.8-V switching I/O type 2*9	I_{RPU}	25	—	200	µA	V_{in} = V_{DD} max
	3.3/1.8-V switching I/O type 3*11	I_{RPU}	18	—	148	µA	V_{in} = V_{DD} max
Input pull-up resistor current	1.8/1.2-V switching I/O type*4 (1.2 V)	I_{RPD}	−10	—	−100	µA	V_{in} = V_{SS}
	1.8/1.2-V switching I/O type*4 (1.8 V)	I_{RPD}	−35	—	−185	µA	V_{in} = V_{SS}
	1.8-V I/O type*6	I_{RPD}	−35	—	−185	µA	V_{in} = V_{SS}
	3.3/1.8-V switching I/O type 1*8 3.3/1.8-V switching I/O type 2*10	I_{RPD}	−25	—	−200	µA	V_{in} = V_{SS}
	3.3/1.8-V switching I/O type 3*12	I_{RPD}	−18	—	−192	µA	V_{in} = V_{SS}

Table 3.4-2 DC Characteristics

V_{DD} = 1.11 V to 1.95 V (1.8/1.2-V switching I/O type), V_{DD} = 1.65 V to 1.95 V (1.8-V I/O type and 1.8-V OSC I/O type), V_{DD} = 1.65 V to 3.60 V (3.3/1.8-V switching I/O types 1, 2 and 3), V_{DD} = 3.00 V to 3.60 V (3.3-V I/O type) (3/4)

Item	I/O Type	Symbol	Min.	Typ.	Max.	Unit	Condition
High-level output voltage	1.8/1.2-V switching I/O type (1.2 V)	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −1/−2/−4/−6 mA (drive strength X1/X2/X4/X6)
	1.8/1.2-V switching I/O type (1.8 V)	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −2/−4/−8/−12 mA (drive strength X1/X2/X4/X6)
	1.8-V I/O type 1.8-V OSC I/O type	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −2/−4/−8/−12 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 1 (1.8 V) 3.3/1.8-V switching I/O type 2 (1.8V)	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −1.6/−3.2/−6.4/−9.6 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 1 (3.3 V) 3.3/1.8-V switching I/O type 2 (3.3V)	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −2/−4/−8/−12 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 3 (1.8 V)	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −5/−6/−7/−10 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 3 (3.3 V)	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −9/−11/−13/−18 mA (drive strength X1/X2/X4/X6)
	3.3-V I/O type	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −2/−4/−8/−12 mA (drive strength X1/X2/X4/X6)
Low-level output voltage	1.8/1.2-V switching I/O type (1.2 V)	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 1/2/4/6 mA (drive strength X1/X2/X4/X6)
	1.8/1.2-V switching I/O type (1.8 V)	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 2/4/8/12 mA (drive strength X1/X2/X4/X6)
	1.8-V I/O type 1.8-V OSC I/O type	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 2/4/8/12 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 1 (1.8 V) 3.3/1.8-V switching I/O type 2 (1.8V)	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 1.6/3.2/6.4/9.6 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 1 (3.3 V) 3.3/1.8-V switching I/O type 2 (3.3V)	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 2/4/8/12 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 3 (1.8 V)	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 5/6/7/10 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O type 3 (3.3 V)	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 9/11/13/18 mA (drive strength X1/X2/X4/X6)
	3.3-V I/O type	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 2/4/8/12 mA (drive strength X1/X2/X4/X6)

Table 3.4-2 DC Characteristics

V_{DD} = 1.11 V to 1.95 V (1.8/1.2-V switching I/O type), V_{DD} = 1.65 V to 1.95 V (1.8-V I/O type and 1.8-V OSC I/O type), V_{DD} = 1.65 V to 3.60 V (3.3/1.8-V switching I/O types 1, 2 and 3), V_{DD} = 3.00 V to 3.60 V (3.3-V I/O type) (4/4)

Item	I/O Type	Symbol	Min.	Typ.	Max.	Unit	Condition
Pull-up resistance	1.8/1.2-V switching I/O type*4 (1.2 V)	R_{PU}	15	—	160	kΩ	—
	1.8/1.2-V switching I/O type*4 (1.8 V)	R_{PU}	10	—	50	kΩ	—
	1.8-V I/O type*6	R_{PU}	10	—	50	kΩ	—
	3.3/1.8-V switching I/O type 1*8 (1.8 V) 3.3/1.8-V switching I/O type 2*10 (1.8 V)	R_{PU}	10	—	50	kΩ	—
	3.3/1.8-V switching I/O type 1*8 (3.3 V) 3.3/1.8-V switching I/O type 2*10 (3.3 V)	R_{PU}	10	—	100	kΩ	—
	3.3/1.8-V switching I/O type 3*12	R_{PU}	12	—	92	kΩ	—
Pull-down resistance	1.8/1.2-V switching I/O type*3 (1.2 V)	R_{PD}	15	—	160	kΩ	—
	1.8/1.2-V switching I/O type*3 (1.8 V)	R_{PD}	15	—	60	kΩ	—
	1.8-V I/O type*5	R_{PD}	15	—	60	kΩ	—
	3.3/1.8-V switching I/O type 1*7 (1.8 V) 3.3/1.8-V switching I/O type 2*9 (1.8 V)	R_{PD}	10	—	50	kΩ	—
	3.3/1.8-V switching I/O type 1*7 (3.3 V) 3.3/1.8-V switching I/O type 2*9 (3.3 V)	R_{PD}	10	—	100	kΩ	—
	3.3/1.8-V switching I/O type 3*11	R_{PD}	13	—	92	kΩ	—
Input capacitance	—	C_{in}	—	—	10	pF	

Note 1. Only for the TRSTN pin

Note 2. When the RIIC function is in use or the schmitt control is on

Note 3. Only for the P20 and P21 pins (when the internal pull-down is enabled)

Note 4. Only for the P20 and P21 pins (when the internal pull-up is enabled)

Note 5. Only for the QBYPASS, BSCANP, MD_BOOT0, MD_BOOT3, MD_BOOT4, BOOTSELCPU, and BOOTPLLCA_0 pins

Note 6. Only for the MD_BOOT1, MD_BOOT2, BOOTPLLCA_1, and MD_CLKS pins

Note 7. Only for the WDTUDFCA, WDTUDFCM, and SCIF_RXD, SCIF_TXD, XSPI0_CS0N, XSPI0_RESET0N, XSPI0_RSTO0N, XSPI0_INT0N, and XSPI0_ECS0N pins (when the internal pull-down is enabled)

Note 8. Only for the WDTUDFCA, WDTUDFCM, and SCIF_RXD, SCIF_TXD, XSPI0_CS0N, XSPI0_RESET0N, XSPI0_RSTO0N, XSPI0_INT0N, and XSPI0_ECS0N pins (when the internal pull-up is enabled)

Note 9. When the internal pull-down is enabled

Note 10. When the internal pull-up is enabled

Note 11. Only for the pins other than SD0CLK, SD0RSTN, SD1CLK, ET0_PHYINTR, and ET1_PHYINTR (when the internal pull-down is enabled)

Note 12. Only for the pins other than SD0CLK, SD0RSTN, SD1CLK, ET0_PHYINTR, and ET1_PHYINTR (when the internal pull-up is enabled)

Note 13. Only for the P90, P91, P92, PB0, PB1, PB2, PB3, PB4, and PB5 pins (when the RIIC function is in use or the schmitt control is on)

3.5 AC Characteristics

Conditions:

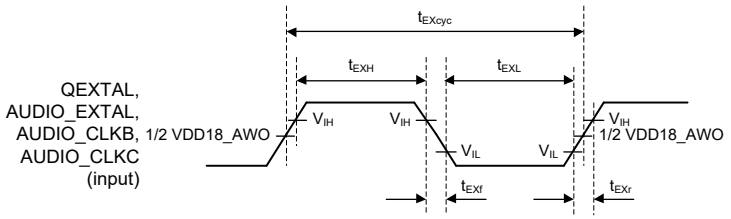
VDD18 = VDD18_AWO = VDD1833_* (1.8 V mode)

VDD33 = VDD1833_* (3.3 V mode)

3.5.1 Clock Timing

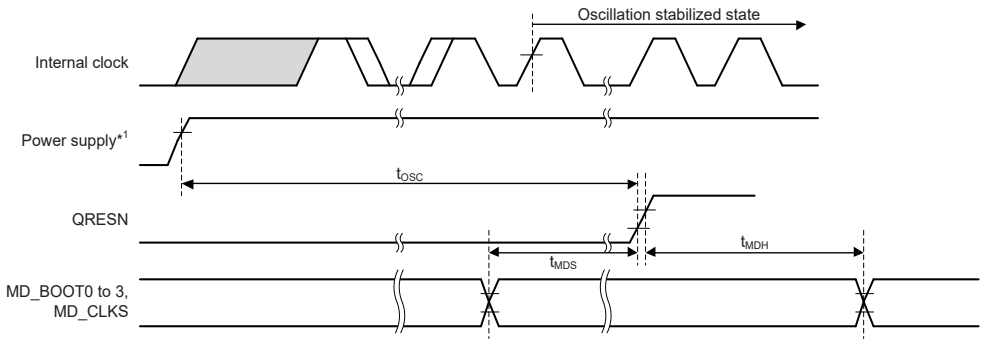
Table 3.5-1 Clock Timing Table

Item	Symbol	Min.	Max.	Unit	Figures
QEXTAL clock input frequency	f_{EX}	24 −50 ppm	24 +50 ppm	MHz	**Figure 3.5-1**
QEXTAL clock input cycle time	t_{EXcyc}	41.67	41.67	ns	
AUDIO_EXTAL clock input frequency	f_{EX}	4	48	MHz	
AUDIO_EXTAL clock input cycle time	t_{EXcyc}	20.83	250	ns	
AUDIO_CLKB, AUDIO_CLKC clock input frequency (external clock is input)	f_{EX}	4	50	MHz	
AUDIO_CLKB, AUDIO_CLKC clock input cycle time (external clock is input)	t_{EXcyc}	20	250	ns	
QEXTAL clock input low-level pulse width	t_{EXL}	0.4	0.6	t_{EXcyc}	
QEXTAL clock input high-level pulse width	t_{EXH}	0.4	0.6	t_{EXcyc}	
AUDIO_EXTAL, AUDIO_CLKB, AUDIO_CLKC clock input low-level pulse width	t_{EXL}	0.45	0.55	t_{EXcyc}	
AUDIO_EXTAL, AUDIO_CLKB, AUDIO_CLKC clock input high-level pulse width	t_{EXH}	0.45	0.55	t_{EXcyc}	
QEXTAL, AUDIO_EXTAL, AUDIO_CLKB, AUDIO_CLKC clock input rise time	t_{EXr}	—	4	ns	
QEXTAL, AUDIO_EXTAL, AUDIO_CLKB, AUDIO_CLKC clock input fall time	t_{EXf}	—	4	ns	
Mode hold time	t_{MDH}	—	100	ns	**Figure 3.5-2**
Mode setup time	t_{MDS}	—	100	ns	



Note: When the clock is input on the QEXTAL, AUDIO_EXTAL, AUDIO_CLKB, or AUDIO_CLKC

Figure 3.5-1 Clock Input Timing



Note 1. 1st Grp power supply (refer to **3.3 Power-On/Off Sequence**)

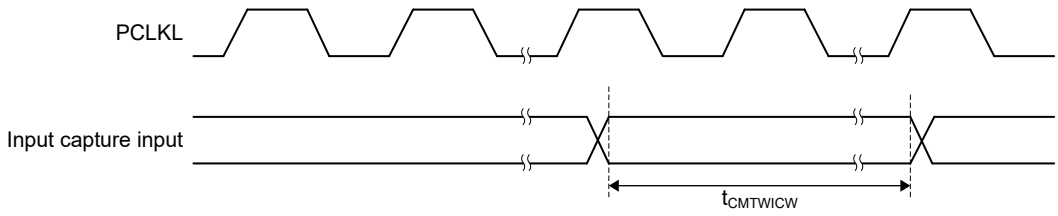
Figure 3.5-2 Power-On Oscillation Settling Time

3.5.2 CMTW Timing

Table 3.5-2 CMTW Timing

Parameter			Symbol	Min.	Max.	Unit	Figure
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWICW}$	1.5	—	t_{PLcyc}*1	**Figure 3.5-3**
		Both-edge setting		2.5	—		

Note 1. t_{PLcyc}: PCLKL cycle



Note: PCLKL: CMTWn internal clock (n = 0 to 7)

Figure 3.5-3 CMTW Input Capture Input Timing

3.5.3 POEG and GPT Trigger Timings

GPT Conditions: High-drive output is selected in the PFC register.

Table 3.5-3 POEG and GPT Trigger Timings

Parameter			Symbol	Min.	Max.	Unit	Figure
POEG	POEG input trigger pulse width		t_{POEW}	1.5	—	t_{Pcyc}*1	**Figure 3.5-4**
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}*2	**Figure 3.5-5**
		Dual edge		2.5	—		

Note 1. t_{Pcyc}: POEGnx internal clock cycle (x = A to D, n = 0, 1)

Note 2. t_{PDcyc}: GPTn internal clock cycle (n = 0, 1)

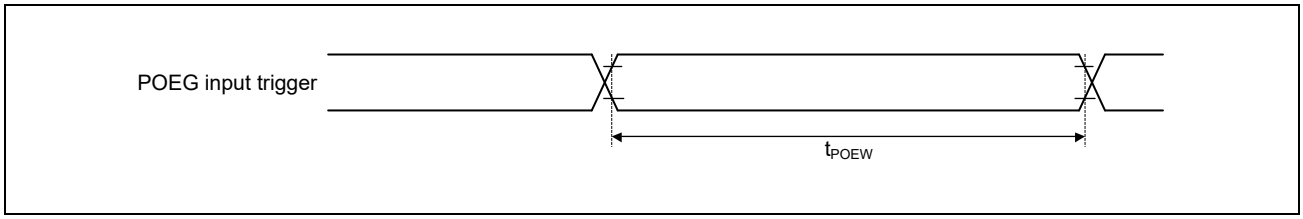


Figure 3.5-4 POEG Input Trigger Timing

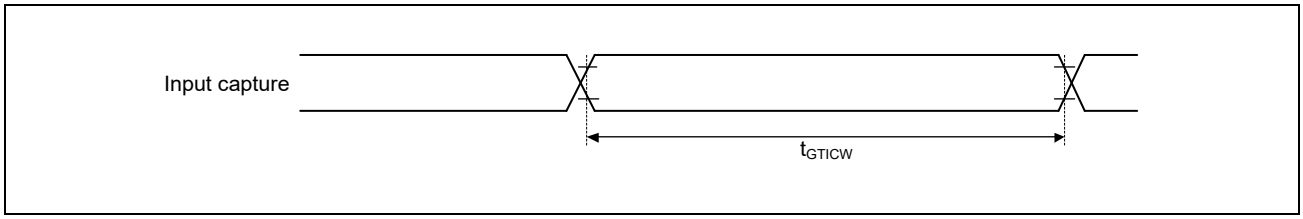


Figure 3.5-5 GPT Input Capture Timing

3.5.4 Watchdog Timer Access Timing

Table 3.5-4 Watchdog Timer Timing

Item	Symbol	Min.	Max.	Unit	Figures
WDTUDFCM / WDTUDFCA output time	t_L	64	64	t_{P1cyc}*1	**Figure 3.5-6**

Note 1. t_{P1cyc} indicates WDTn loco clock (n = 0 to 3).

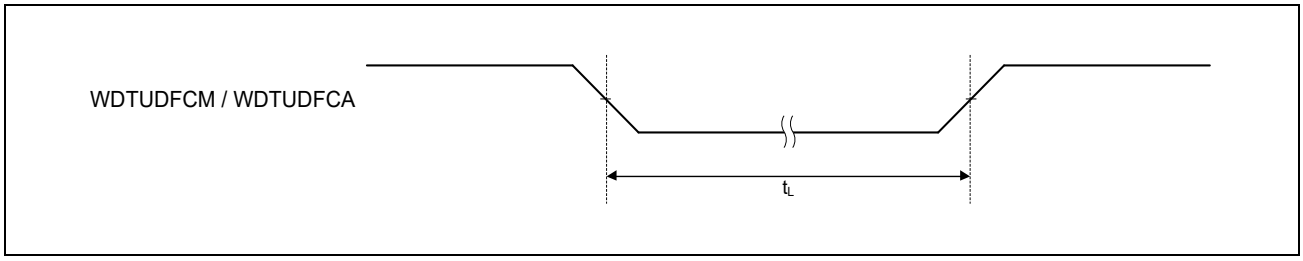


Figure 3.5-6 Watchdog Timer Output Timing

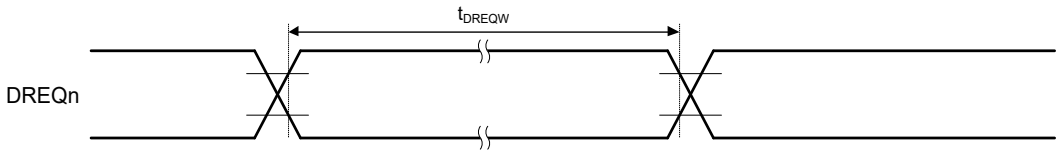
3.5.5 DMAC Timing

Table 3.5-5 DMAC Timing

Item	Symbol	Min.	Max.	Unit	Figures
DREQn pulse width	t_{DREQW}	20	—	t_{cyc}*1	Figure 3.5-7
TENDn pulse width	t_{TENDW}	16	16	$t_{PCLKcyc}$*2	Figure 3.5-8

Note 1. t_{cyc} = 41.666 ns (24 MHz)

Note 2. $t_{PCLKcyc}$ = 10 ns (100 MHz)



Note: This specification “(Min. 20 t_{cyc})” is the min. pulse width when the digital noise filter is off.

Figure 3.5-7 DMAC DREQn Timing

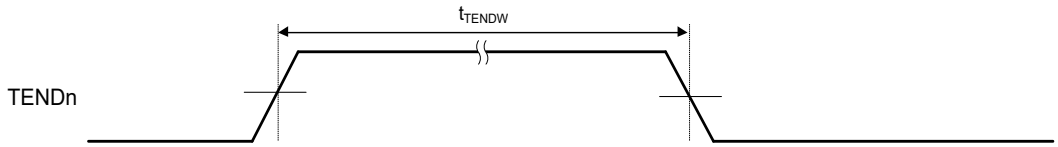


Figure 3.5-8 DMAC TENDn Timing

3.5.6 LPDDR4 PHY Characteristics

The LPDDR4 PHY of this LSI is compliant with the JEDEC 209-4D / JEDEC 209-4-1A standard.

3.5.7 SD Access Timing

Conditions:

V_{OH} = VDD33 × 0.7

V_{OL} = VDD33 × 0.3

C = 40 pF (3.3 V)

Drive strength: ×6

3.5.7.1 SD Access Timing (SDR 3.3-V)

Table 3.5-6 SD AC Access Timing (SDR at 3.3-V Operation)

Item	Symbol	Default Speed Mode (25 MHz)		High Speed Mode (50 MHz)		Unit	Figures
		Min.	Max.	Min.	Max.		
SDnCLK clock cycle	t_{SDCYC}	40.0	—	20.0	—	ns	**Figure 3.5-9**
SDnCLK clock high level width	t_{SDWH}	10	—	7	—	ns	
SDnCLK clock low level width	t_{SDWL}	10	—	7	—	ns	
SDnCLK clock rise time	t_{SDLH}	—	10	—	3	ns	
SDnCLK clock fall time	t_{SDHL}	—	10	—	3	ns	
SDnCMD,SDnDATm output delay	t_{SDODLY}	−7.5	2.5	−6.2	2.5	ns	
SDnCMD,SDnDATm input set up time	t_{SDIS}	4.0	—	4.0	—	ns	
SDnCMD,SDnDATm input hold time	t_{SDIH}	2.0	—	2.0	—	ns	
SDnCMD,SDnDATm input data width	t_{SDIDW}	—	—	—	—	ns	

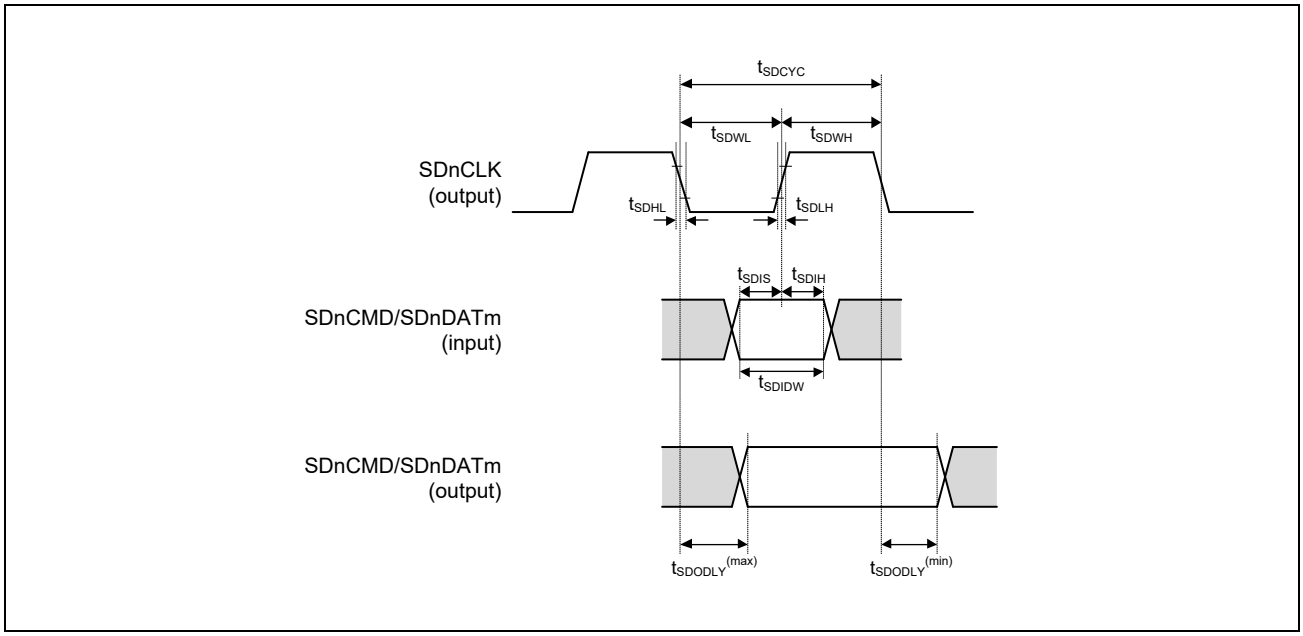


Figure 3.5-9 SDHC Interface Timing (SDR 3.3-V Power Supply)

NOTE

The disclosure of other characteristics of the SD interface needs the conclusion of the following agreement.

- SD Host/Ancillary Product License Agreement (SD HALA)

For details, contact Renesas sales representatives.

3.5.8 eMMC Access Timing

Conditions:

V_{OH} = VDD18 × 0.7, V_{OL} = VDD18 × 0.3, C = 15 pF (1.8 V)

V_{OH} = VDD33 × 0.7, V_{OL} = VDD33 × 0.3, C = 30 pF (3.3 V)

Drive strength: ×6

3.5.8.1 eMMC host interface timing (default)

Table 3.5-7 eMMC Host Interface Timing (MMC Default 3.3-V Power Supply)

Item	Symbol	Min.	Max.	Unit	Figures
SDnCLK clock cycle	t_{MMCPP}	20.0	—	ns	**Figure 3.5-10**
SDnCLK clock high level width	t_{MMCWH}	7	—	ns	
SDnCLK clock low level width	t_{MMCWL}	7	—	ns	
SDnCLK clock rise time	t_{MMCLH}	—	3	ns	
SDnCLK clock fall time	t_{MMCHL}	—	3	ns	
SDnCMD/SDnDATm output delay	$t_{MMCODLY}$	−6.2	2.5	ns	
SDnCMD/SDnDATm input setup time	t_{MMCISU}	4.0	—	ns	
SDnCMD/SDnDATm input hold time	t_{MMCIH}	2.0	—	ns	
SDnCMD/SDnDATm input data width	t_{MMCIDW}	—	—	ns	

Table 3.5-8 eMMC Host Interface Timing (MMC Default 1.8-V Power Supply)

Item	Symbol	Min.	Max.	Unit	Figures
SDnCLK clock cycle	t_{MMCPP}	20.0	—	ns	**Figure 3.5-10**
SDnCLK clock high level width	t_{MMCWH}	7	—	ns	
SDnCLK clock low level width	t_{MMCWL}	7	—	ns	
SDnCLK clock rise time	t_{MMCLH}	—	3	ns	
SDnCLK clock fall time	t_{MMCHL}	—	3	ns	
SDnCMD/SDnDATm output delay	$t_{MMCODLY}$	−4.2	1.6	ns	
SDnCMD/SDnDATm input setup time	t_{MMCISU}	1.3	—	ns	
SDnCMD/SDnDATm input hold time	t_{MMCIH}	1.878	—	ns	
SDnCMD/SDnDATm input data width	t_{MMCIDW}	—	—	ns	

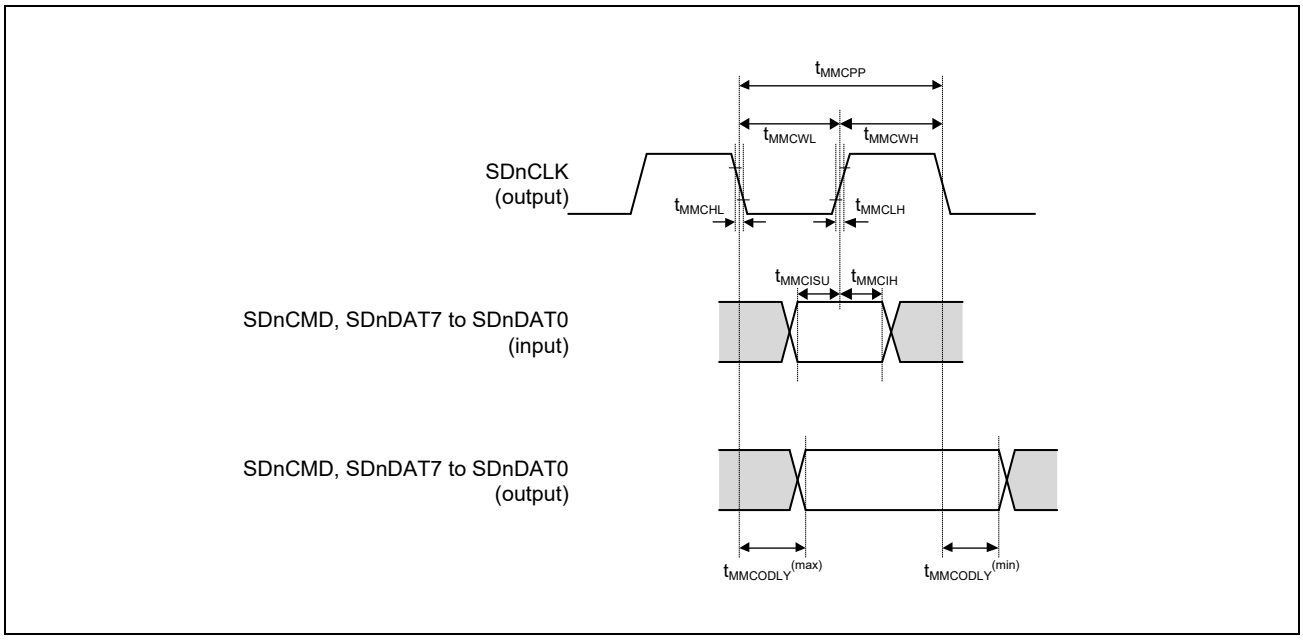


Figure 3.5-10 eMMC Host Interface Timing (MMC Default 1.8-V/3.3-V Power Supply)

3.5.8.2 eMMC host interface timing (HS-SDR)

NOTES

1. The spec of eMMC host interface timing (HS-SDR 3.3-V power supply) is the same as **Table 3.5-7 eMMC Host Interface Timing (MMC Default 3.3-V Power Supply)**.
2. The spec of eMMC host interface timing (HS-SDR 1.8V power supply) is the same as **Table 3.5-8 eMMC Host Interface Timing (MMC Default 1.8-V Power Supply)**.

3.5.8.3 eMMC host interface timing (HS-DDR)

Table 3.5-9 eMMC Host Interface Timing (HS-DDR 3.3-V Power Supply Operation)

Item	Symbol	High Speed Mode (50 MHz)		Unit	Figures
		Min.	Max.		
SDnCLK clock cycle	t_{SDCYC}	20.0	—	ns	**Figure 3.5-11**
SDnCLK clock high level width	t_{SDWH}	9.0	11.0	ns	
SDnCLK clock low level width	t_{SDWL}	9.0	11.0	ns	
SDnCLK clock rise time	t_{SDLH}	—	3.0	ns	
SDnCLK clock fall time	t_{SDHL}	—	3.0	ns	
SDnCMD output delay	t_{SDODLY}	−6.0	6.0	ns	
SDnCMD input set up time	t_{SDIS}	4.8	—	ns	
SDnCMD input hold time	t_{SDIH}	2.5	—	ns	
SDnDATm output delay	t_{SDODLY_DDR}	2.5	6.5	ns	
SDnDATm input set up time	t_{SDIS_DDR}	1.768	—	ns	
SDnDATm input hold time	t_{SDIH_DDR}	1.5	—	ns	

Table 3.5-10 eMMC Host Interface Timing (HS-DDR 1.8-V Power Supply Operation)

Item	Symbol	High Speed Mode (50 MHz)		Unit	Figures
		Min.	Max.		
SDnCLK clock cycle	t_{MMCCYC}	20.0	—	ns	**Figure 3.5-11**
SDnCLK clock high level width	t_{MMCWH}	9.0	11.0	ns	
SDnCLK clock low level width	t_{MMCWL}	9.0	11.0	ns	
SDnCLK clock rise time	t_{MMCLH}	—	3.0	ns	
SDnCLK clock fall time	t_{MMCHL}	—	3.0	ns	
SDnCMD output delay	$t_{MMCODLY}$	−6.0	3.0	ns	
SDnCMD input set up time	t_{MMCIS}	4.8	—	ns	
SDnCMD input hold time	t_{MMCIH}	2.5	—	ns	
SDnDATm output delay	$t_{MMCODLY\_DDR}$	2.5	6.5	ns	
SDnDATm input set up time	t_{MMCIS_DDR}	1.768	—	ns	
SDnDATm input hold time	t_{SMMCIH_DDR}	1.5	—	ns	

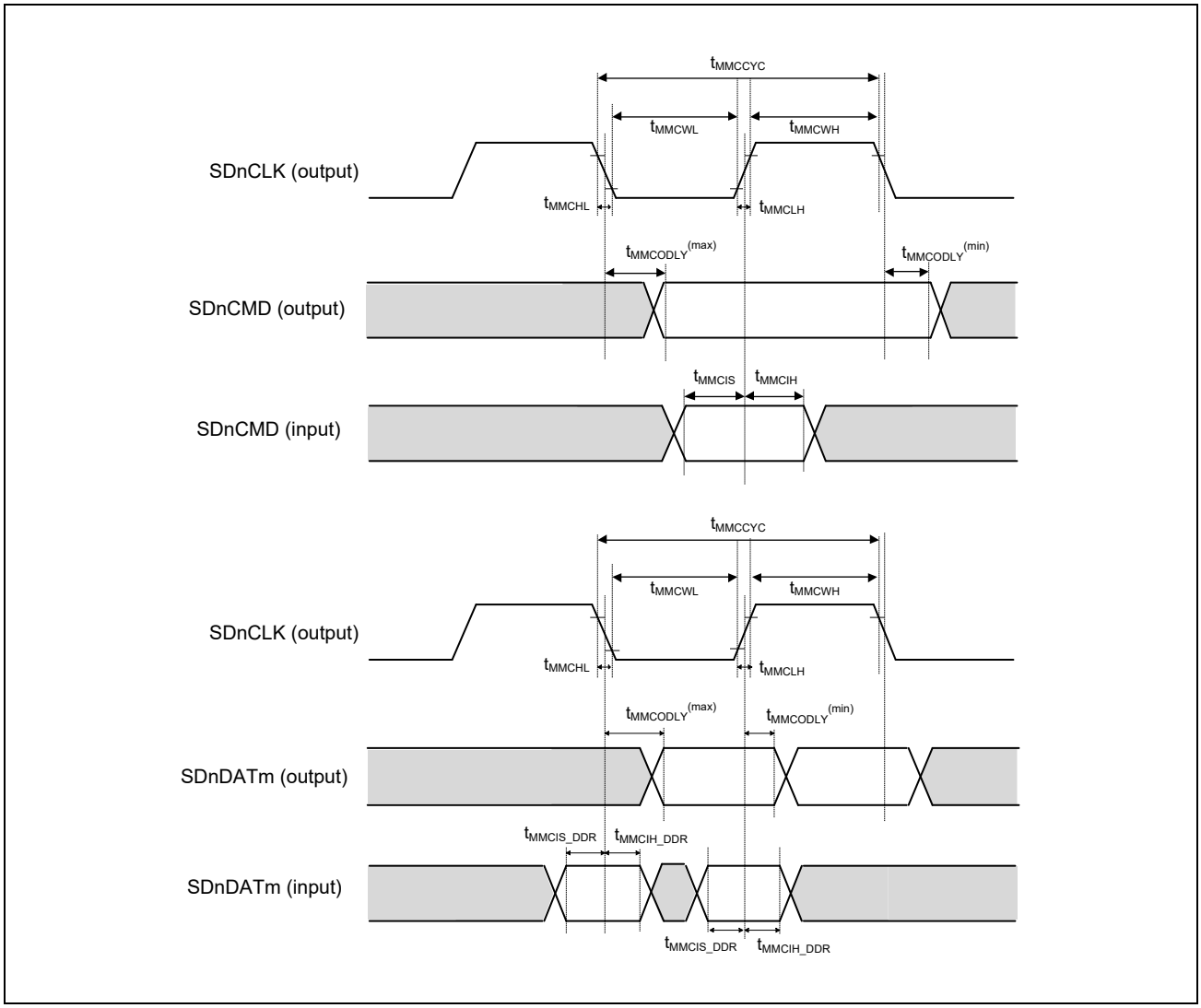


Figure 3.5-11 eMMC Host Interface (MMC Interface HS-DDR Mode 1.8/3.3-V Power Supply Selection)

3.5.8.4 eMMC host interface timing (HS200)

Table 3.5-11 eMMC Host Interface Timing (HS200 1.8-V Power Supply Operation, Output Load 15 pF)

Item	Symbol	Min.	Max.	Unit	Figures
SDnCLK clock cycle	t_{MMCPP}	5.0	10.0	ns	**Figure 3.5-12**
SDnCLK clock high level width	t_{MMCWH}	1.5	—	ns	
SDnCLK clock low level width	t_{MMCWL}	1.5	—	ns	
SDnCLK clock rise time	t_{MMCLH}	—	1.0	ns	
SDnCLK clock fall time	t_{MMCHL}	—	1.0	ns	
SDnCMD/SDnDATm output delay	$t_{MMCODLY}$	−1.7	0.9	ns	
SDnCMD/SDnDATm input setup time	t_{MMCISU}	—	—	ns	
SDnCMD/SDnDATm input hold time	t_{MMCIH}	—	—	ns	
SDnCMD/SDnDATm input data width	t_{MMCIDW}	2.88	—	ns	

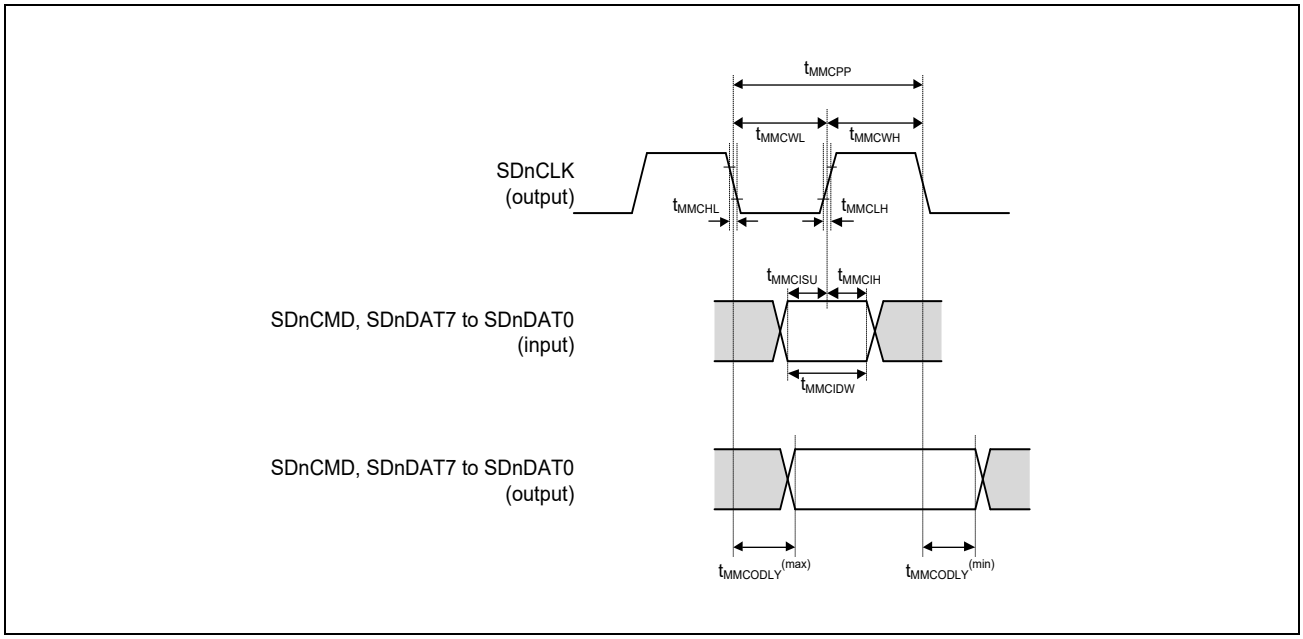


Figure 3.5-12 eMMC Host Interface (MMC Interface HS200 Mode 1.8-V Power Supply Selection)

3.5.9 Ethernet Interface Timing

Conditions:

V_{OH} = VDD18 × 0.5, V_{OL} = VDD18 × 0.5

V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5

C = 15 pF (RGMII), 30 pF (MII)

Drive strength: ×2, ×4

Table 3.5-12 Ethernet Interface Timing (n = 0, 1)

Parameter			Symbol	Min.	Max.	Unit	Figure
Ethernet (RGMII)	ETn_TXC_TXCLK, ETn_RXC_RXCLK cycle time duration	1 Gbps	$t_{RGMIIck}$	7.2	8.8	ns	**Figure 3.5-13**
		100 Mbps		36	44	ns	
		10 Mbps		360	440	ns	
	ETn_TXC_TXCLK, ETn_RXC_RXCLK frequency	1 Gbps	—	125 − 50 ppm	125 + 50 ppm	MHz	
		100 Mbps		25 − 50 ppm	25 + 50 ppm	MHz	
		10 Mbps		2.5 − 50 ppm	2.5 + 50 ppm	MHz	
	ETn_TXC_TXCLK, ETn_RXC_RXCLK duty cycle	1 Gbps	—	45	55	%	
		100 Mbps 10 Mbps		40	60	%	
	ETn_TXC_TXCLK, ETn_TXD0 to ETn_TXD3, ETn_TXCTL_TXEN, ETn_RXC_RXCLK, ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV rise/fall time		t_{RGMIIr}, t_{RGMIIf}	—	0.75*1	ns	
	ETn_TXD0 to ETn_TXD3, ETn_TXCTL_TXEN, ETn_TXC_TXCLK output skew		$t_{RGMIIos}$	−0.5	0.5	ns	
	ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV setup time		t_{RGMIIs}	1	—	ns	
	ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV hold time		t_{RGMIIh}	1	—	ns	
Ethernet (MII)	ETn_TXC_TXCLK, ETn_RXC_RXCLK cycle time	100 Mbps	t_{MIIck}	40	—	ns	**Figure 3.5-14**
		10 Mbps		400	—	ns	
	ETn_TXC_TXCLK, ETn_RXC_RXCLK frequency	100 Mbps	—	25 − 50 ppm	25 + 50 ppm	MHz	
		10 Mbps		2.5 − 50 ppm	2.5 + 50 ppm	MHz	
	ETn_TXD0 to ETn_TXD3, ETn_TXCTL_TXEN, ETn_TXER output delay time		t_{MIId}	1	20	ns	
	ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV, ETn_RXER setup time		t_{MIIs}	10	—	ns	
	ETn_RXD0 to ETn_RXD3, ETn_RXCTL_RXDV, ETn_RXER hold time		t_{MIIh}	10	—	ns	

Note 1. The measurement condition of t_{RGMIIr} and t_{RGMIIf} is in FIGURE 3 in Reduced Gigabit Media Independent Interface (RGMII) 12/10/2000 Version 1.3.

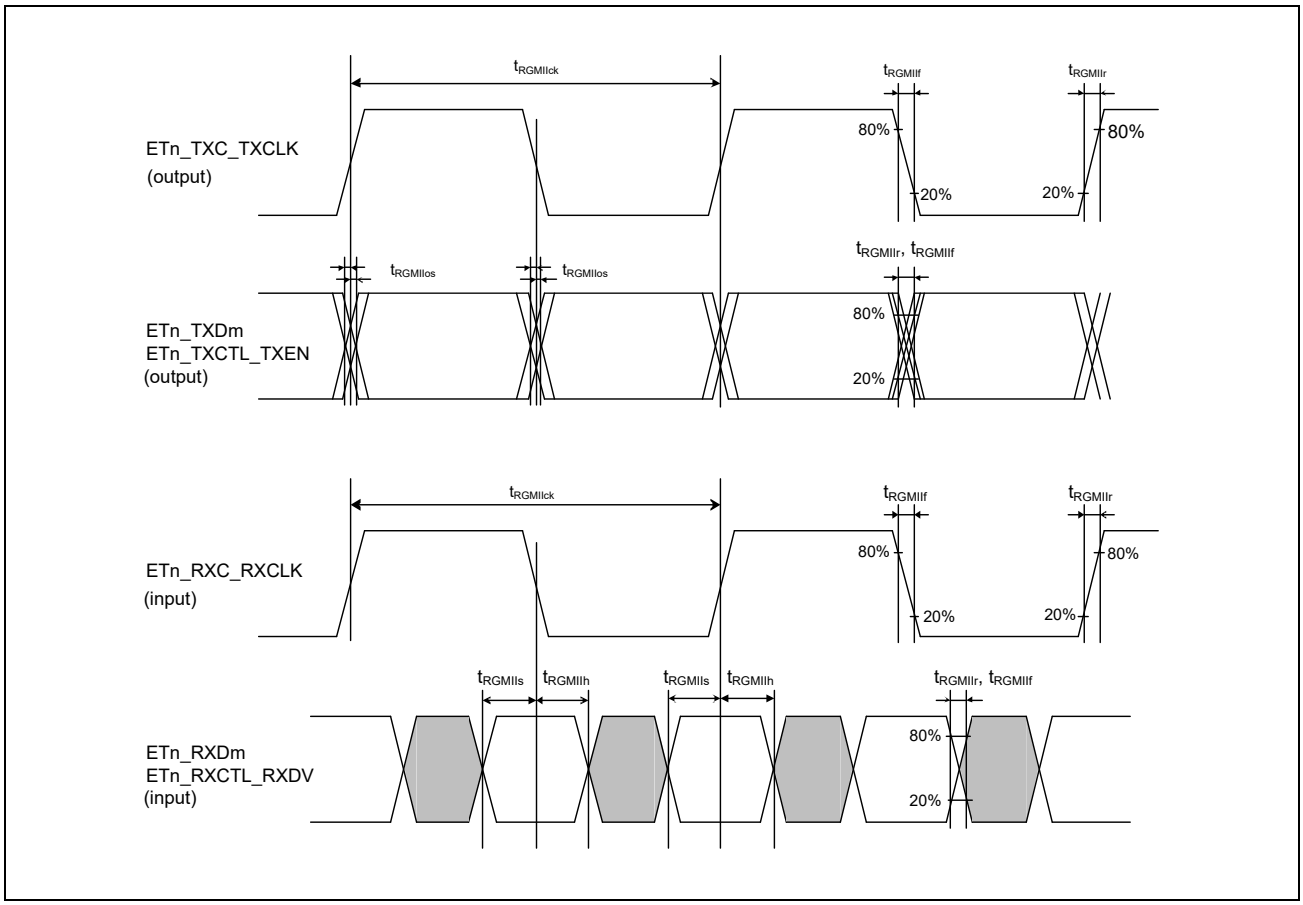


Figure 3.5-13 RGMII Transmission and Reception Timing (n = 0, 1)

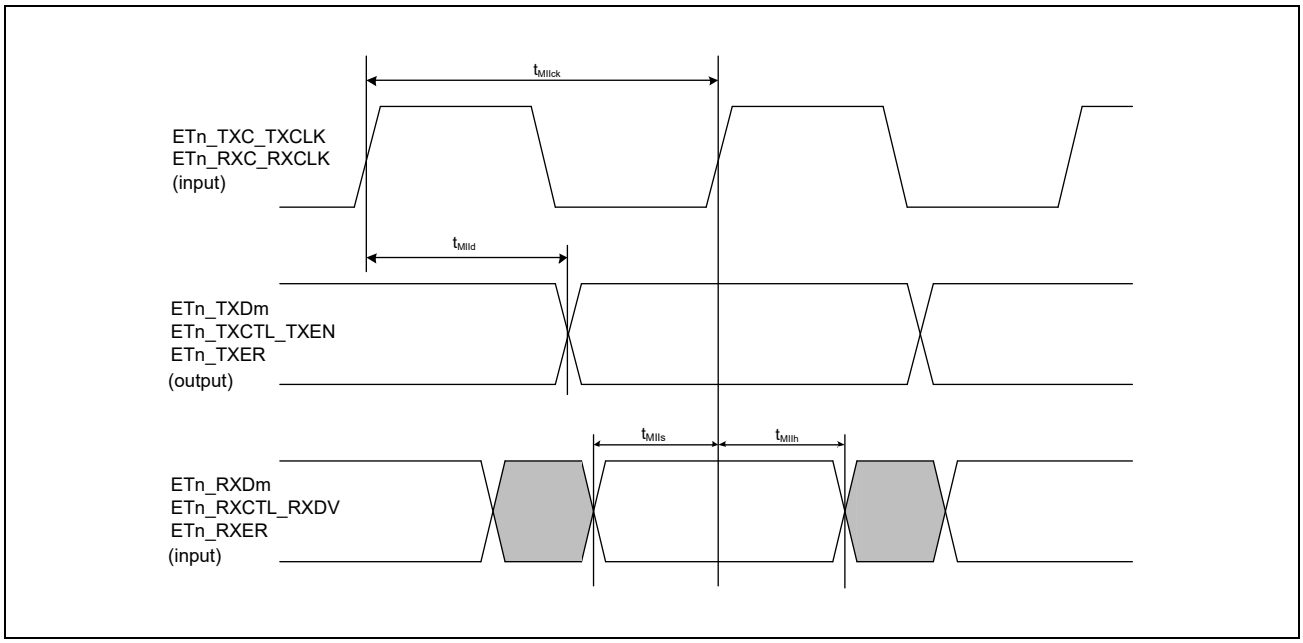


Figure 3.5-14 MII Transmission and Reception Timing (n = 0, 1)

3.5.10 USB 3.2 PHY Characteristics

The USB3 PHY of this LSI is compliant with the following USB 3.2 Gen2x1 standard:

Universal Serial Bus 3.2 Specification

3.5.11 USB 2.0 PHY Characteristics

The USB2 PHY of this LSI is compliant with the following USB 2.0 standard:

Universal Serial Bus 2.0 Specification

3.5.12 PCI Express PHY Characteristics

The PCI Express PHY of this LSI is compliant with the following PCIe standard:

Revision 4.0 of the PCI Express® Base Specification for Gen1/Gen 2/Gen 3

3.5.13 xSPI Timing

Conditions:

- Single-end clock

  V_{OH} = VDD18 × 0.8, V_{OL} = VDD18 × 0.2, C = 15 pF (1.8 V)
  V_{OH} = VDD33 × 0.8, V_{OL} = VDD33 × 0.2, C = 15 pF (3.3 V)

- Data

  V_{OH} = VDD18 × 0.8, V_{OL} = VDD18 × 0.2, C = 15 pF (1.8 V)
  V_{OH} = VDD33 × 0.8, V_{OL} = VDD33 × 0.2, C = 15 pF (3.3 V)

Drive strength: ×6

Table 3.5-13 xSPI Timing (1/2)

Parameter		Symbol	1.8V		3.3V		Unit	Figure
			Min.	Max.	Min.	Max.		
Cycle time	SDR	t_{PERIOD}	7.5	—	12.5	—	ns	**Figure 3.5-15**
	DDR		7.5	—	12.5	—	ns	
Clock output slew rate		t_{SRck}	0.75 / 0.56*1	—	1.03	—	V/ns	
Clock duty cycle distortion		t_{CKDCD}	0.0	t_{PERIOD} × 0.05	0.0	t_{PERIOD} × 0.05	ns	
Clock minimum pulse width		t_{CKMPW}	t_{PERIOD} × 0.45	—	t_{PERIOD} × 0.45	—	ns	
Differential clock crossing voltage		$V_{OX(AC)}$	0.4 × VDD18	0.6 × VDD18	—	—	V	
DS duty cycle distortion		t_{DSDCD}	0.0	t_{PERIOD} × 0.04	0.0	t_{PERIOD} × 0.04	ns	
DS minimum pulse width		t_{DSMPW}	t_{PERIOD} × 0.41	—	t_{PERIOD} × 0.41	—	ns	
Data input/output slew rate		t_{SR}	0.75 / 0.56*1	—	1.03	—	V/ns	
Data input setup time (to CK)	SDR	t_{SU}	2.0	—	2.4	—	ns	**Figure 3.5-16**
Data input hold time (to CK)		t_{H}	1.0	—	1.0	—	ns	
Data output delay time		t_{OD}	—	1.6*2	—	1.8*2	ns	
Data output hold time		t_{OH}	−1.5	—	−2.3	—	ns	
Data output buffer off time		t_{BOFF}	−1.5	—	−2.3	—	ns	
Data input setup time (to DS)	DDR*2	t_{SU}	−0.6 / −0.8*1	—	−0.6 / −0.8*1	—	ns	**Figure 3.5-17**, **Figure 3.5-18**
Data input hold time (to DS)		t_{H}	t_{PERIOD} × 0.41 − 0.6 / t_{PERIOD} × 0.41 − 0.8*1	—	t_{PERIOD} × 0.41 − 0.6 / t_{PERIOD} × 0.41 − 0.8*1	—	ns	
Data output setup time (to CK)		t_{SUO}	0.6 / 1.0*1,*4	—	1.0	—	ns	
Data output hold time (to CK)		t_{HO}	0.6 / 1.0*1,*4	—	1.0	—	ns	
CS low to clock high		t_{CSLCKH}	6.0 / 8.0*1,*3	6.0 / 8.0*1 *3	—	8.0*3	—	**Figure 3.5-16** to **Figure 3.5-18**
Clock low to CS high		t_{CKLCSH}	6.0 / 8.0*1	6.0 / 8.0*1	—	8.0	—	
CS high time		t_{CSTD}	1	16	1	16	t_{PERIOD}	

Table 3.5-12 xSPI Timing (2/2)

Parameter	Symbol	1.8V		3.3V		Unit	Figure
		Min.	Max.	Min.	Max.		
DS low to CS high	t_{DSLCSH}	6.0 / 8.0*1	—	10.6	—	ns	**Figure 3.5-19**
CS high to DS Tri-state	t_{CSHDST}	0.0	t_{PERIOD}	0.0	t_{PERIOD}	ns	
CS low to DS low*5	t_{CSLDSL}	0.0	12.5*6	0.0	17.4*6	ns	
DS Tri-state to CS low	t_{DSTCSL}	0.0	—	0.0	—	ns	

Note: CK: XSPI0_CKP (XSPI0_CKN)
DS: XSPI0_DS
CS: XSPI0_CS0N, XSPI0_CS1N

Note 1. Specification at 133 MHz / Specification at 100 MHz

Note 2. These are values when the OEN assertion is extended.

Note 3. These are the values when the CS assertion is extended.

Note 4. The standard value for xSPI266 is 0.8 ns.

Note 5. If the DS is high during the command & modifier phase when using JESD251 Profile 2.0 memory, the time from CS low to DS high must also meet this specification.

Note 6. When using JESD251 Profile 1.0 memory or JESD251 Profile 2.0 memory with Latency mode set to 0, this constraint does not apply if the internal pull-down resistor of the DS pin is enabled.

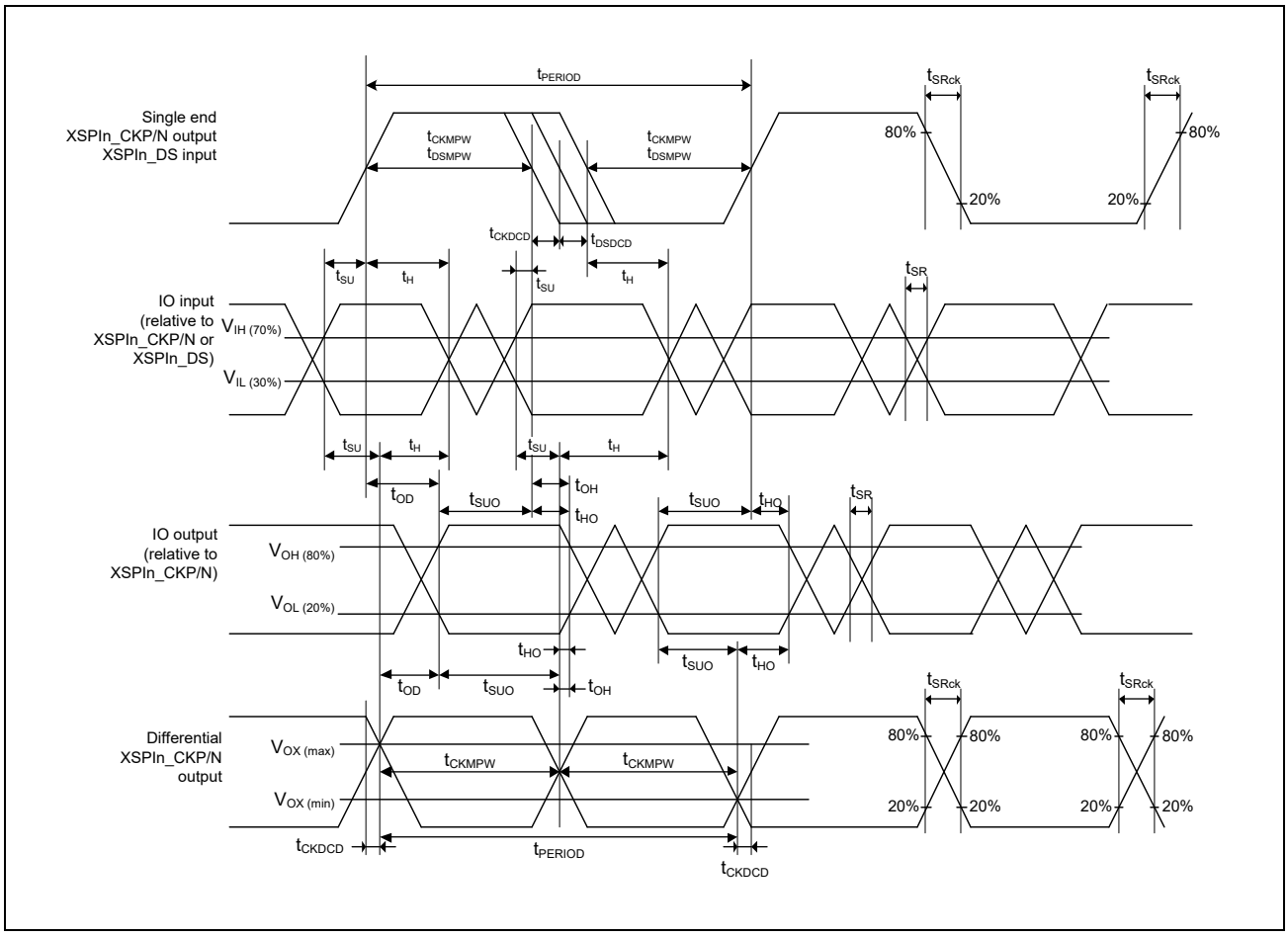


Figure 3.5-15 xSPI Clock / DS Timing

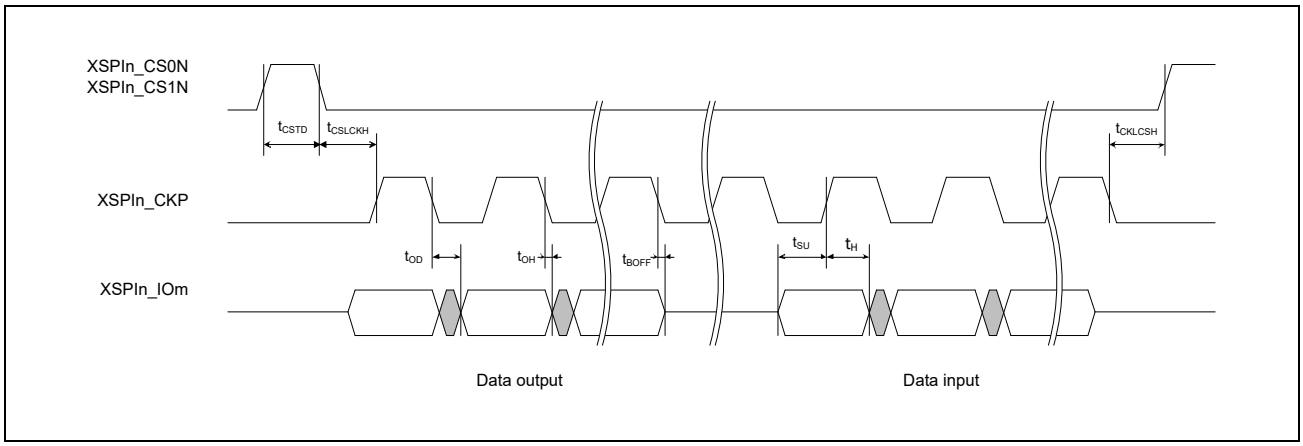


Figure 3.5-16 SDR Transmission and Reception Timing (1S-1S-1S, 1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S)

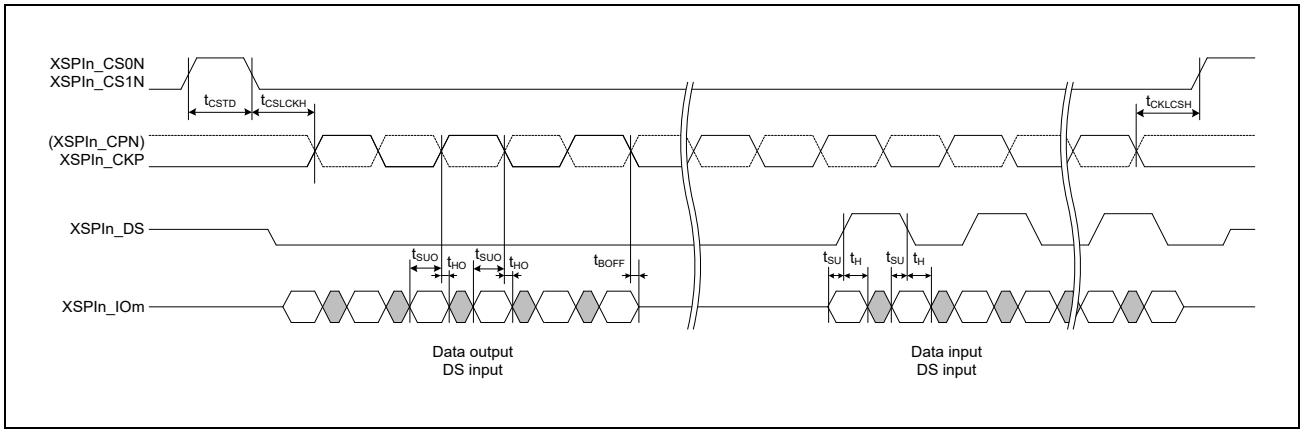


Figure 3.5-17 DDR Transmission and Reception Timing (4S-4D-4D, 8D-8D-8D)

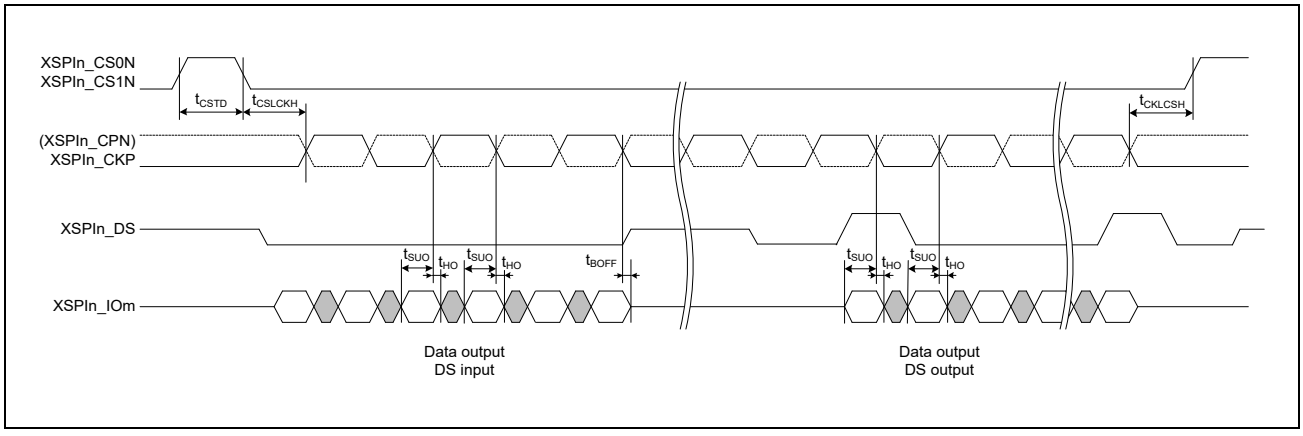


Figure 3.5-18 DDR Transmission and Reception Timing (HyperRAM write)

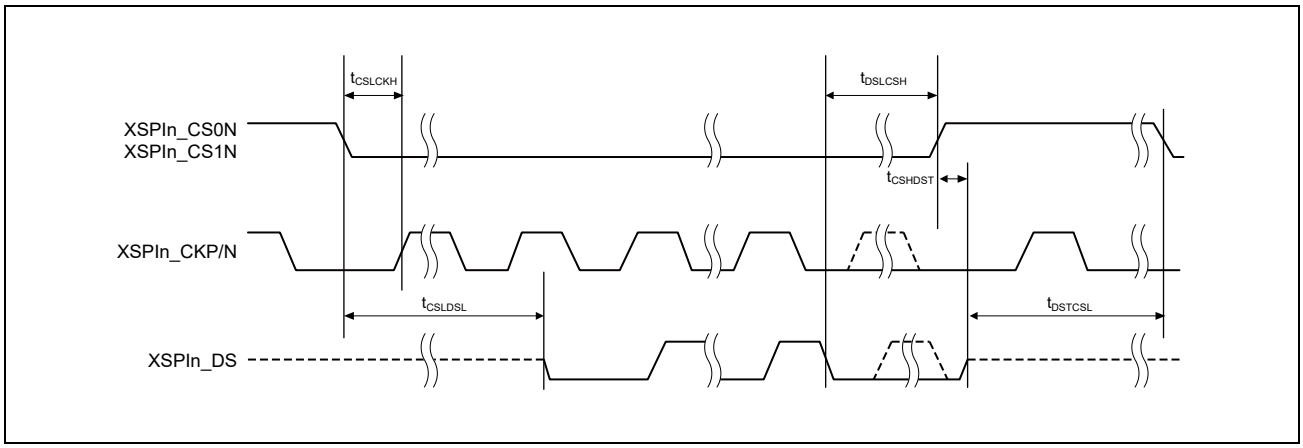


Figure 3.5-19 DS to CS Signal Timing

3.5.14 Serial Communications Interface (RSCI) Access Timing

Conditions:

V_{OH} = VDD18 × 0.5, V_{OL} = VDD18 × 0.5, C = 30 pF (1.8 V)

V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF (3.3 V)

Drive strength: ×2, ×4 (However, ×6 only for SCL (P93) and SDA (P92) of RSCI0 in simple I2C mode)

Table 3.5-14 RSCI Timing (1/2)

Parameter			Symbol	Min.	Max.	Unit	Figure
RSCI (Asynchronous)	Input clock cycle		t_{Scyc}	4	—	$t_{PSCIcyc}$	**Figure 3.5-20**
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	3	ns	
	Input clock fall time		t_{SCKf}	—	3	ns	
	Output clock cycle		t_{Scyc}	6	—	$t_{PSCIcyc}$	
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time	V_{DD1833} = 1.8 V	t_{SCKr}	—	6.18*2	ns	
		V_{DD1833} = 3.3 V		—	7.9*2	ns	
	Output clock fall time	V_{DD1833} = 1.8 V	t_{SCKf}	—	6.18*2	ns	
		V_{DD1833} = 3.3 V		—	7.9*2	ns	
RSCI (Simple I2C, Standard mode)	SDA input rise time		t_{Sr}	—	1000	ns	**Figure 3.5-21**
	SDA input fall time		t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time		t_{SP}	0	2 × NFcyc*1	ns	
	Data input setup time		t_{SDAS}	250	—	ns	
	Data input hold time		t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load		C_b	—	400	pF	
RSCI (Simple I2C, Fast mode)	SDA input rise time		t_{Sr}	—	300	ns	**Figure 3.5-21**
	SDA input fall time		t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time		t_{SP}	0	2 × NFcyc*1	ns	
	Data input setup time		t_{SDAS}	100	—	ns	
	Data input hold time		t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load		C_b	—	400	pF	

Table 3.5-13 RSCI Timing (2/2)

Parameter			Symbol	Min.	Max.	Unit	Figure
RSCI (Clock sync, Simple SPI)	SCK output clock cycle (master)		t_{SPcyc}	4	65536	$t_{PSCIcyc}$	**Figure 3.5-22** to **Figure 3.5-27**
	SCK input clock cycle (slave)			4	65536	$t_{PSCIcyc}$	
	SCK clock high-level pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low-level pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	Input clock rise time		t_{SPCKR}	—	3	ns	
	Input clock fall time		t_{SPCKF}	—	3	ns	
	Output clock rise time	V_{DD1833} = 1.8 V	t_{SPCKR}	—	6.18*2	ns	
		V_{DD1833} = 3.3 V		—	7.9*2	ns	
	Output clock fall time	V_{DD1833} = 1.8 V	t_{SPCKF}	—	6.18*2	ns	
		V_{DD1833} = 3.3 V		—	7.9*2	ns	
	Data input setup time	Internal clock	t_{SU}	7	—	ns	
		External clock		3	—	ns	
	Data input hold time	Internal clock	t_H	3	—	ns	
		External clock		3	—	ns	
	Data output delay time	Internal clock	t_{OD}	—	3	ns	
		External clock		—	12	ns	
	Data output hold time	Internal clock	t_{OH}	−3	—	ns	
		External clock		0	—	ns	
	Data rise/fall time	V_{DD1833} = 1.8 V	t_{DR}, t_{DF}	—	6.18*2	ns	
		V_{DD1833} = 3.3 V		—	7.9*2	ns	
	Slave access time	Internal clock	t_{SA}	—	3 × $t_{PSCIcyc}$ + 12	ns	
		External clock		—	3 × $t_{PSCIcyc}$ + 12	ns	
	Slave output release time	Internal clock	t_{REL}	—	3 × $t_{PSCIcyc}$ + 12	ns	
		External clock		—	3 × $t_{PSCIcyc}$ + 12	ns	
RSCI (Simple SPI)	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	**Figure 3.5-22** to **Figure 3.5-27**
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	SS input rise/fall time		t_{SSR}, t_{SSF}	—	3	ns	

Note: $t_{PSCIcyc}$: RSCIn operating clock cycle (n = 0 to 9)

Note 1. NFcyc = 4p × 2q − 1 × $t_{PSCIcyc}$
p: Common Control Register 2 set value (p = 0, 1, 2, 3)
q: Common Control Register 1 set value (q = 1, 2, 3, 4)

Note 2. Output transition time from 20% to 80%

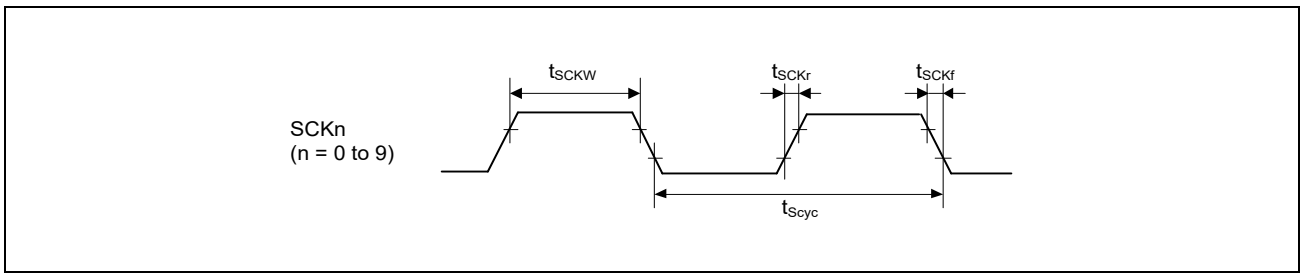
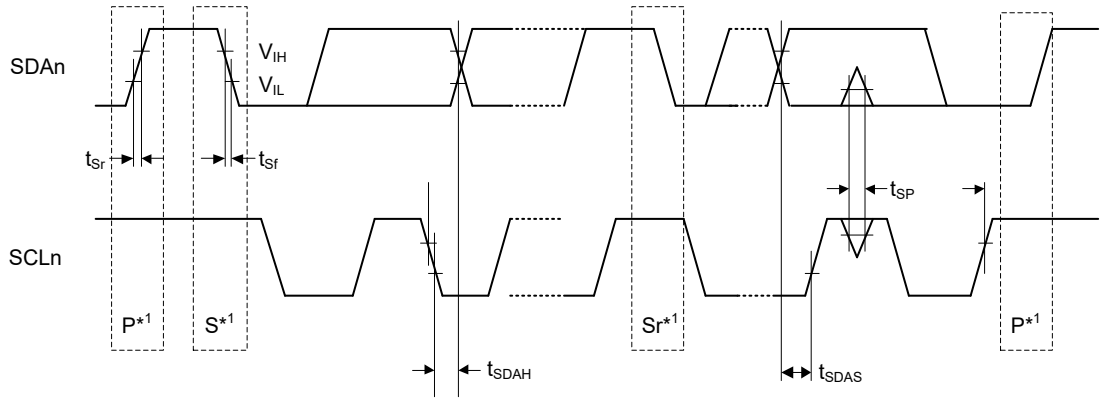


Figure 3.5-20 SCK Clock Input/Output Timing



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 3.5-21 RSCI Simple I2C Mode Timing

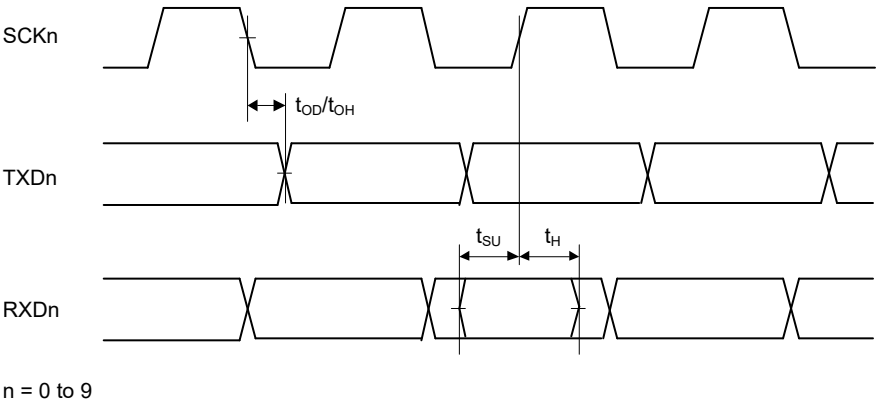


Figure 3.5-22 RSCI Input/Output Timing in Clock Synchronous Mode

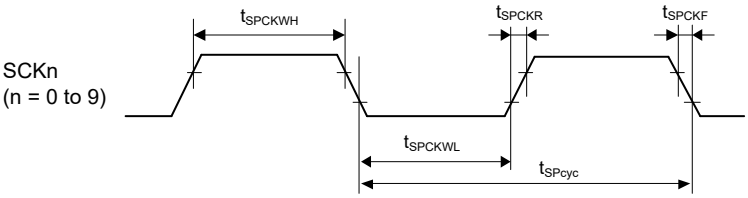


Figure 3.5-23 RSCI Simple SPI Mode Clock Timing

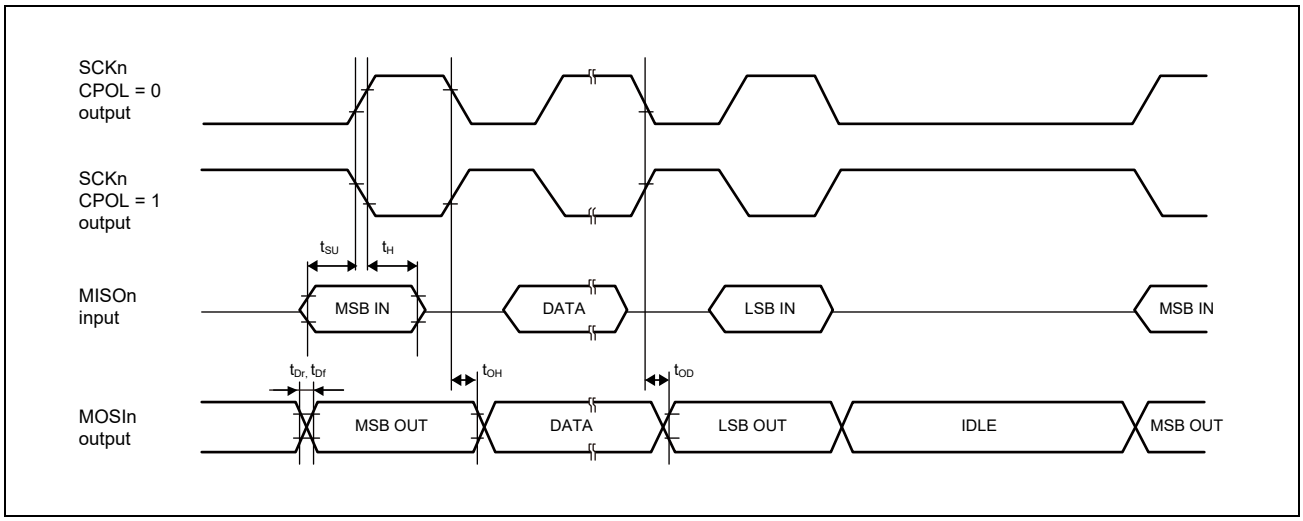


Figure 3.5-24 RSCI Simple SPI Mode Timing for Master when CPHA = 0

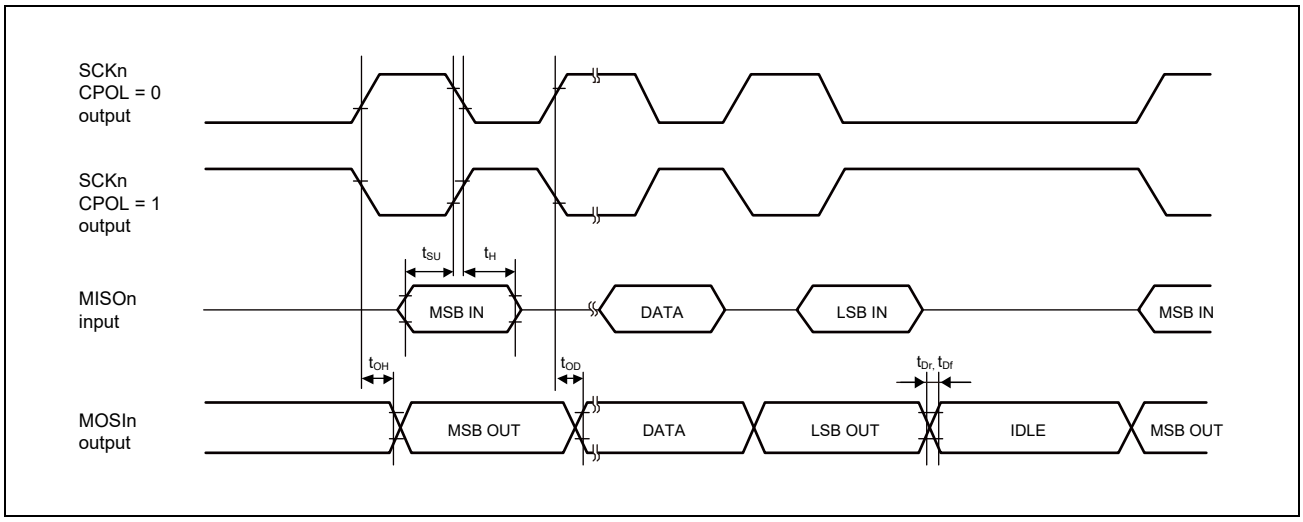


Figure 3.5-25 RSCI Simple SPI Mode Timing for Master when CPHA = 1

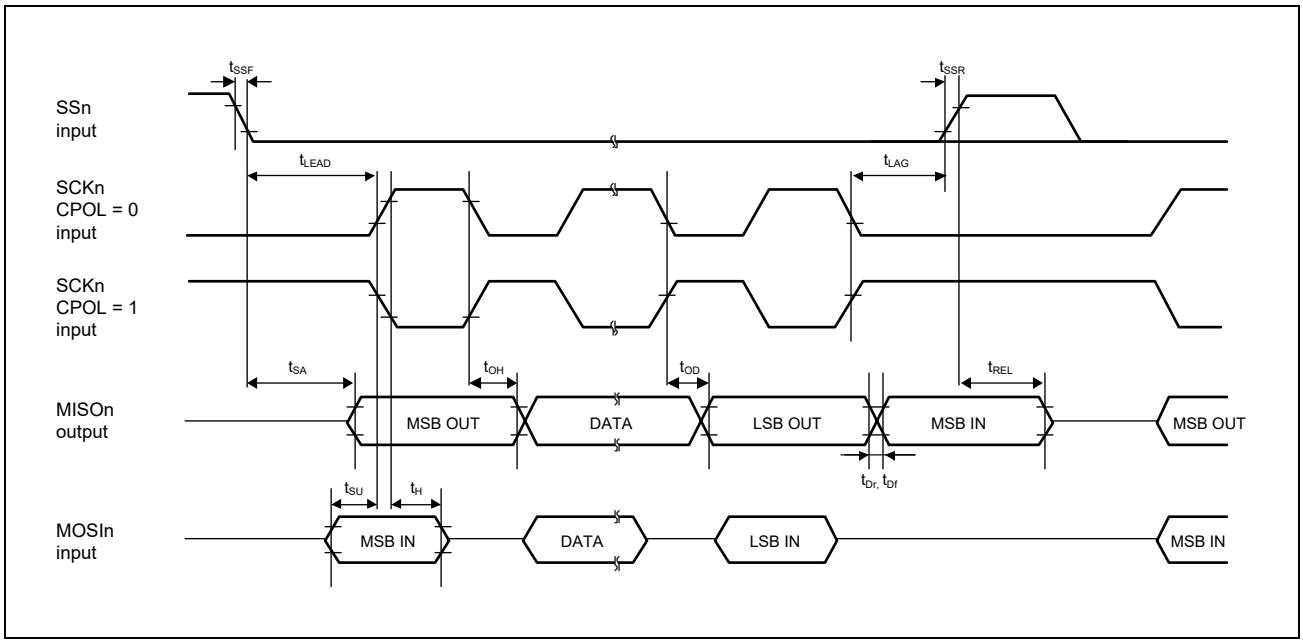


Figure 3.5-26 RSCI Simple SPI Mode Timing for Slave when CPHA = 0

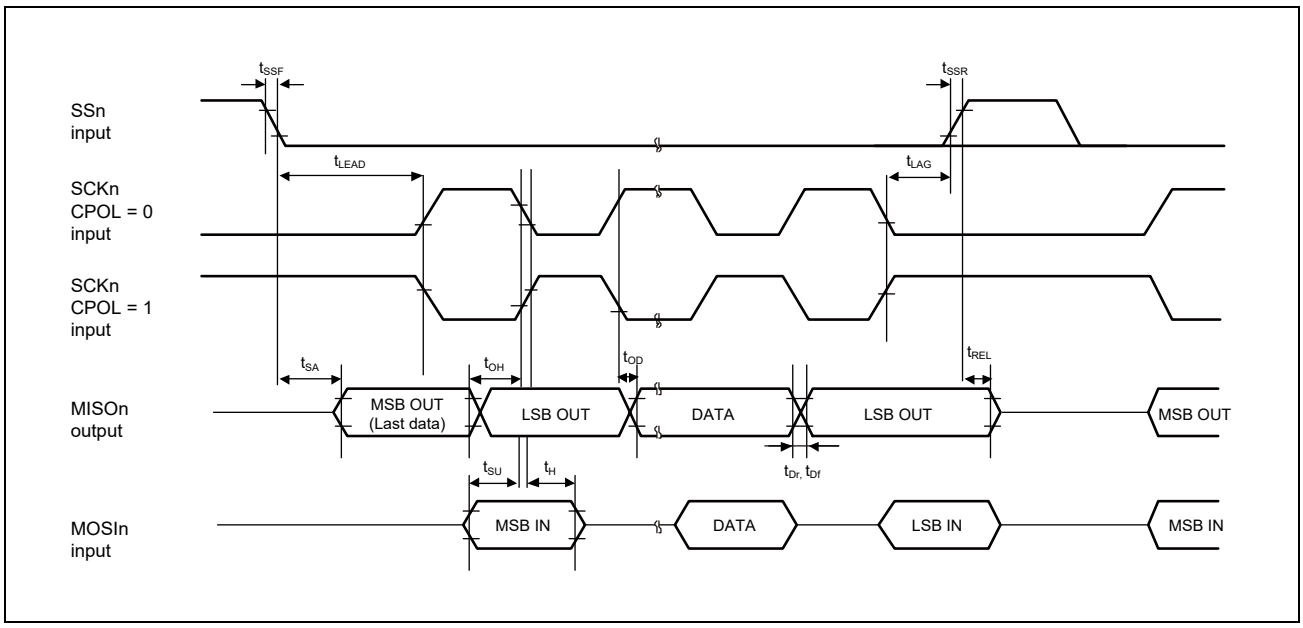


Figure 3.5-27 RSCI Simple SPI Mode Timing for Slave when CPHA = 1

3.5.15 Renesas Serial Peripheral Interface (RSPI) Access Timing

Conditions:

V_{OH} = VDD18 × 0.5, V_{OL} = VDD18 × 0.5, C = 30 pF (1.8 V)

V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF (3.3 V)

Drive strength: ×6

Table 3.5-15 RSPI Timing (1/2)

Parameter		Symbol	Min.*1	Max.*1	Unit	Figure
RSPCK clock cycle	Master	t_{SPcyc}	4	4096	t_{SPIcyc}	**Figure 3.5-28**
	Slave		4	4096	t_{SPIcyc}	
RSPCK clock high-level pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 2.5$	—	ns	
	Slave		1	—	t_{SPIcyc}	
RSPCK clock low-level pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 2.5$	—	ns	
	Slave		1	—	t_{SPIcyc}	
RSPCK clock rise/fall time	Output	t_{SPCKr}, t_{SPCKf}	—	3*5	ns	
	Input		—	3*5	ns	
Data input setup time	Master	t_{SU}	5.3	—	ns	**Figure 3.5-29** to **Figure 3.5-35**
	Slave		3	—	ns	
Data input hold time	Master	t_H	3	—	ns	
	Slave		3	—	ns	
SSL setup time	Master	t_{LEAD}	$N \times t_{SPcyc} - 3$*2	$N \times t_{SPcyc} + 3$*2	ns	**Figure 3.5-29** to **Figure 3.5-32**
	Slave		5	—	t_{SPIcyc}	
SSL hold time	Master	t_{LAG}	$N \times t_{SPcyc} - 3$*3	$N \times t_{SPcyc} + 3$*3	ns	
	Slave		5	—	t_{SPIcyc}	
Continuous transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{SPIcyc}$	$8 \times t_{SPcyc} + 2 \times t_{SPIcyc}$	ns	
	Slave		$t_{SPcyc} + 5 \times t_{SPIcyc}$	—	ns	
TI-SSP SS input setup time		t_{TISS}	3.1	—	ns	**Figure 3.5-33** to **Figure 3.5-35**
TI-SSP SS input hold time		t_{TISH}	3	—	ns	
TI-SSP next access time		t_{TIND}	M*4	—	t_{SPIcyc}	
TI-SSP Master SS output delay		t_{TISSOD}	−3	3	ns	
TI-SSP Master OE delay 1		$t_{TIMOED1}$	—	2	ns	
TI-SSP Master OE delay 2		$t_{TIMOED2}$	—	2	ns	
TI-SSP Slave OE delay 1		$t_{TISOED1}$	—	7.5	ns	
TI-SSP Slave OE delay 2		$t_{TISOED2}$	—	7.5	ns	
SSL Activation to Data Output Delay		t_{OD1}	—	3	ns	**Figure 3.5-29**
Data output delay time	Master	t_{OD}	—	3	ns	**Figure 3.5-29** to **Figure 3.5-35**
	Slave		—	7.5	ns	
Data output hold time	Master	t_{OH}	−3	—	ns	
	Slave		3	—	ns	
MOSI, MISO rise/fall time	Output	t_{Dr}, t_{Df}	—	3*5	ns	
	Input		—	1	µs	
SSL rise/fall time	Output	t_{SSLr}, t_{SSLf}	—	3*5	ns	**Figure 3.5-29**, **Figure 3.5-30**
	Input		—	1	µs	

Table 3.5-15 RSPI Timing (2/2)

Parameter	Symbol	Min.*1	Max.*1	Unit	Figure
Slave access time	t_{SA}	—	8	ns	**Figure 3.5-31**, **Figure 3.5-32**
Slave output release time	t_{REL}	—	8	ns	

Note 1. t_{SPIcyc}: RSPIn peripheral clock cycle

Note 2. SPI Clock Delay Register set value + 1 (1 to 8)

Note 3. SPI Slave Select Negation Delay Register set value + 1 (1 to 8)

Note 4. SPI Slave Select Negation Delay Register set value + 2 (2 to 9)

Note 5. Output transition time from 20% to 80%

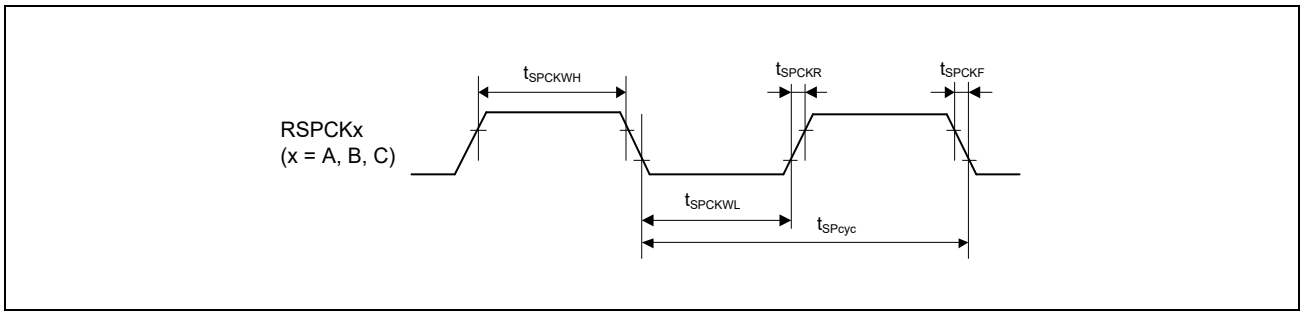


Figure 3.5-28 RSPI Clock Timing

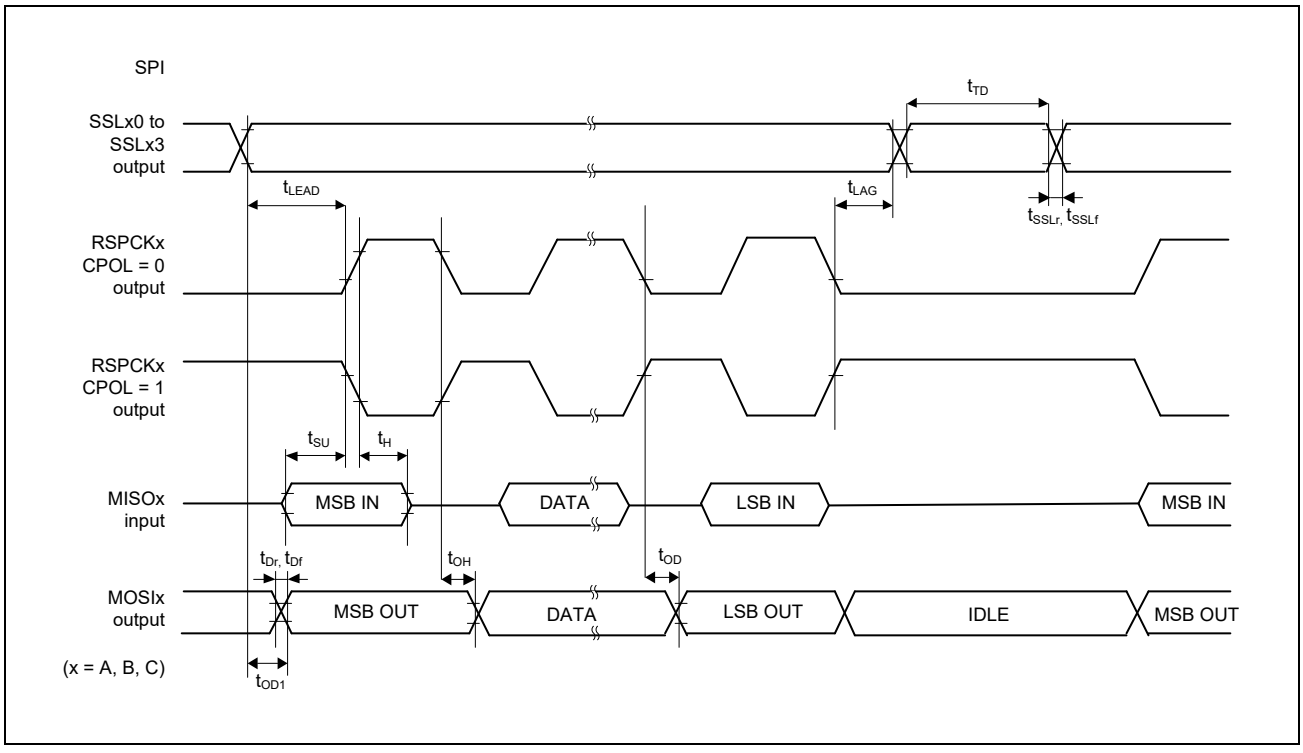


Figure 3.5-29 RSPI Timing (Master, Motorola RSPI, CPHA = 0)

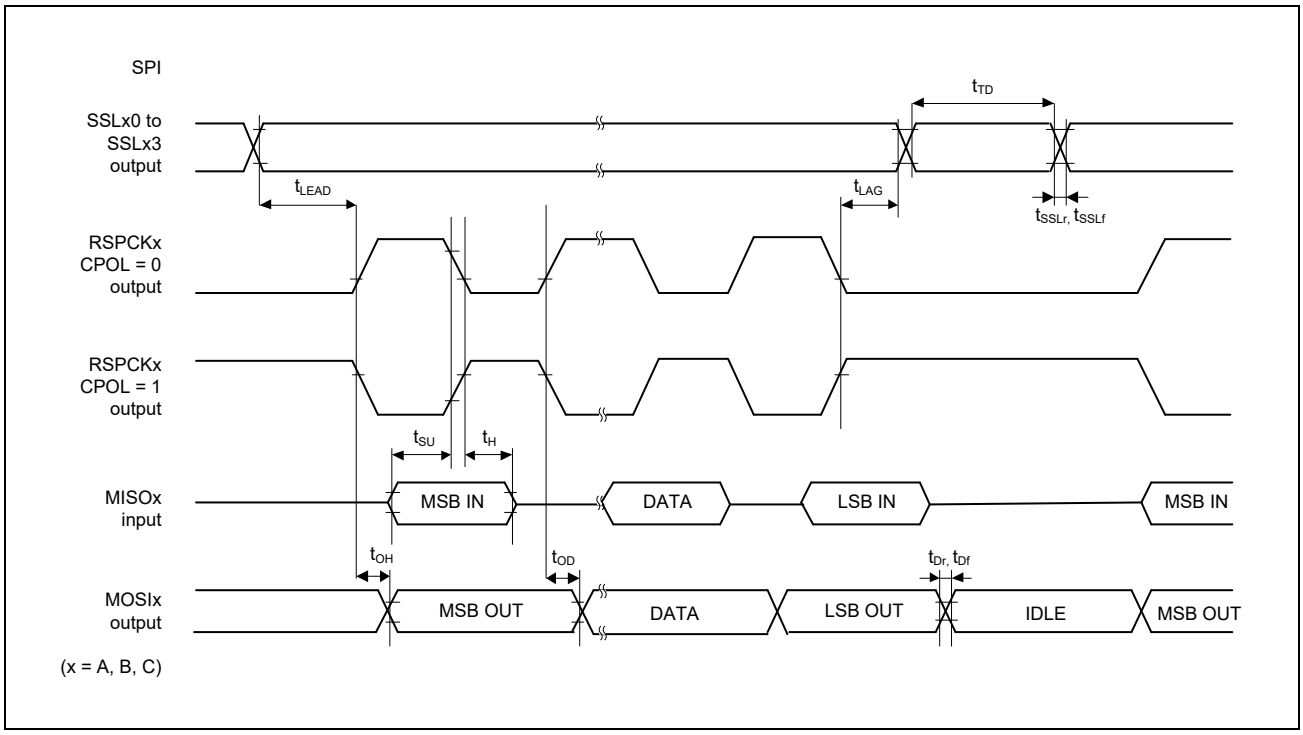


Figure 3.5-30 RSPI Timing (Master, Motorola RSPI, CPHA = 1)

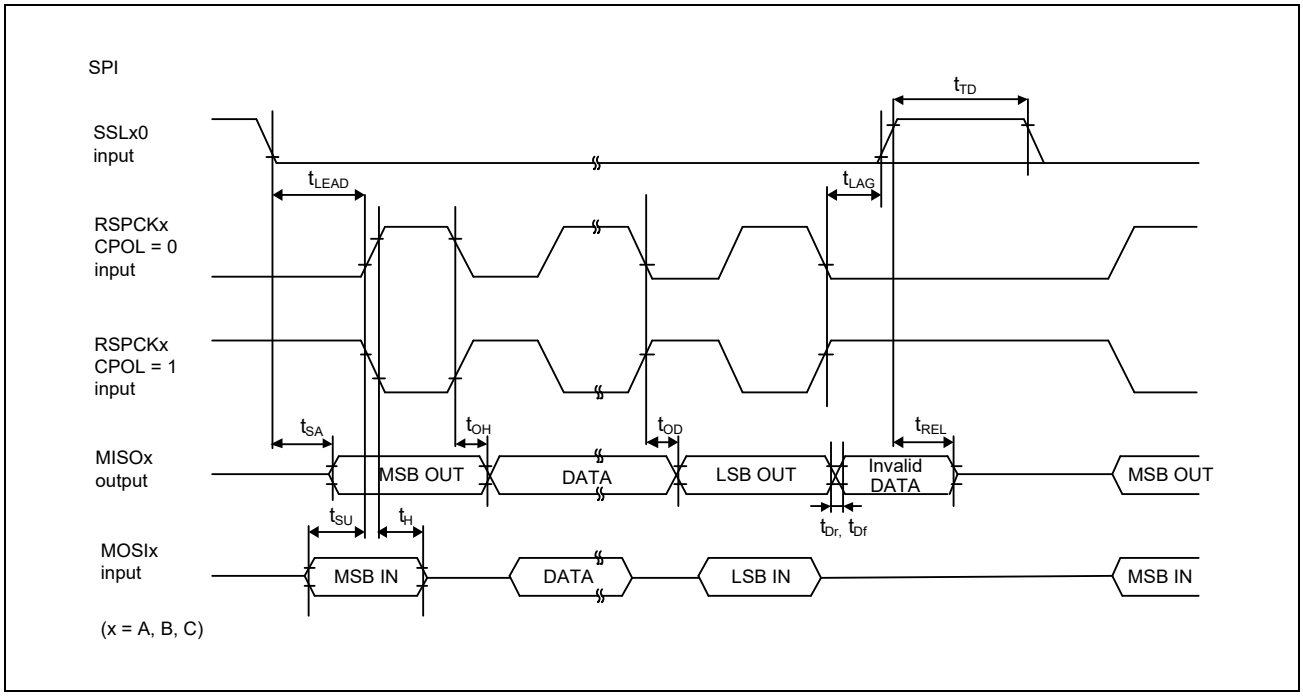


Figure 3.5-31 RSPI Timing (Slave, Motorola RSPI, CPHA = 0)

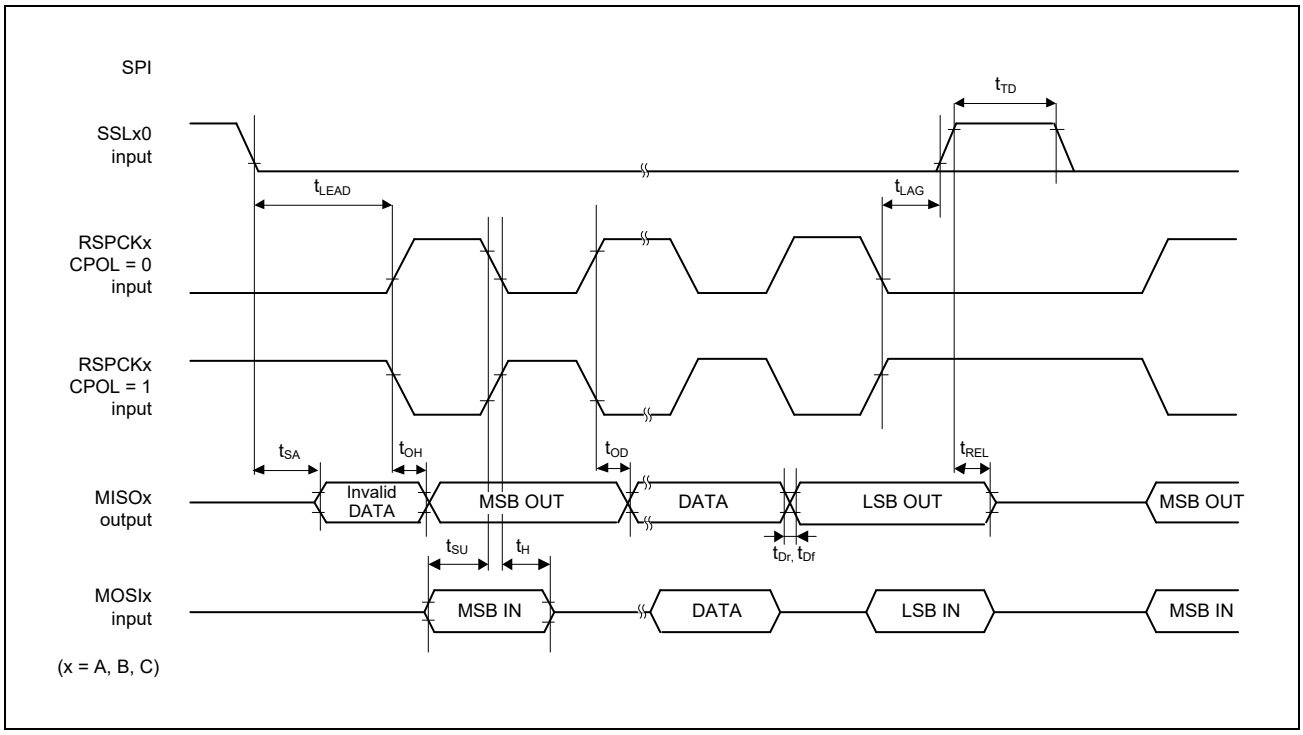


Figure 3.5-32 RSPI Timing (Slave, Motorola RSPI, CPHA = 1)

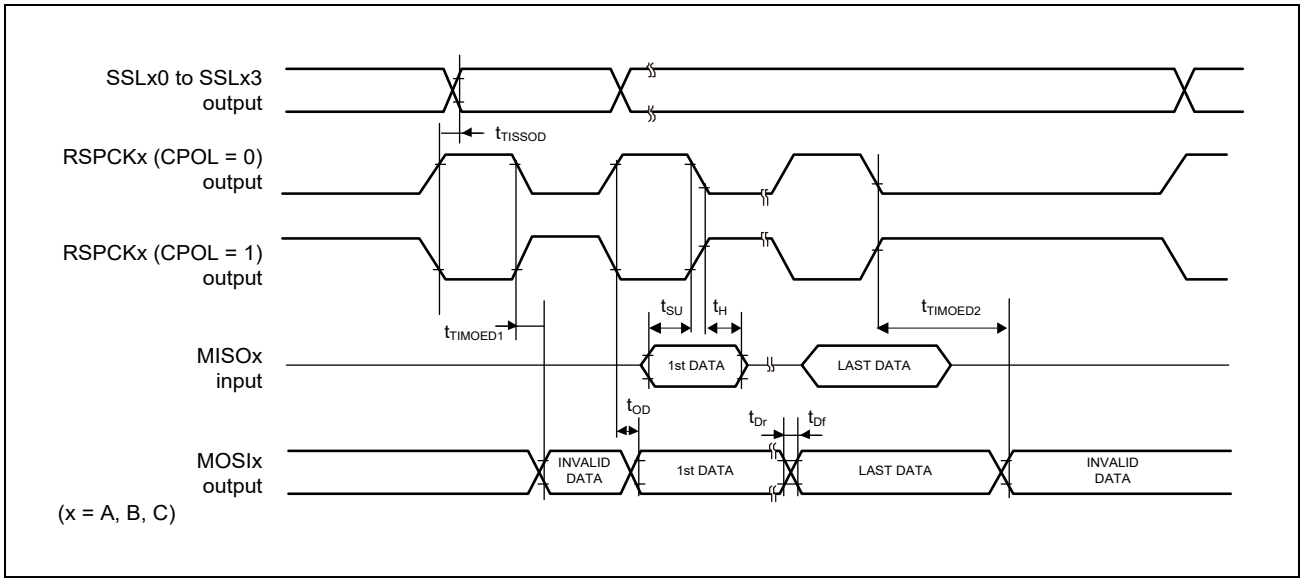


Figure 3.5-33 RSPI Timing (Master, TI SSP)

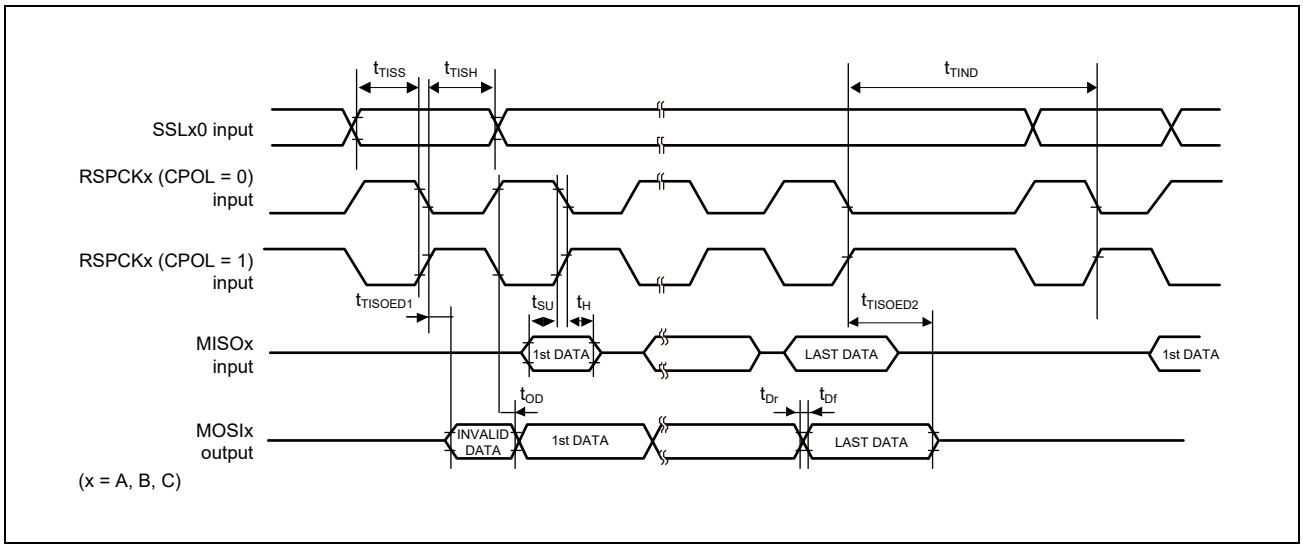


Figure 3.5-34 RSPI Timing (Slave, TI-SSP, with delay in burst transfer)

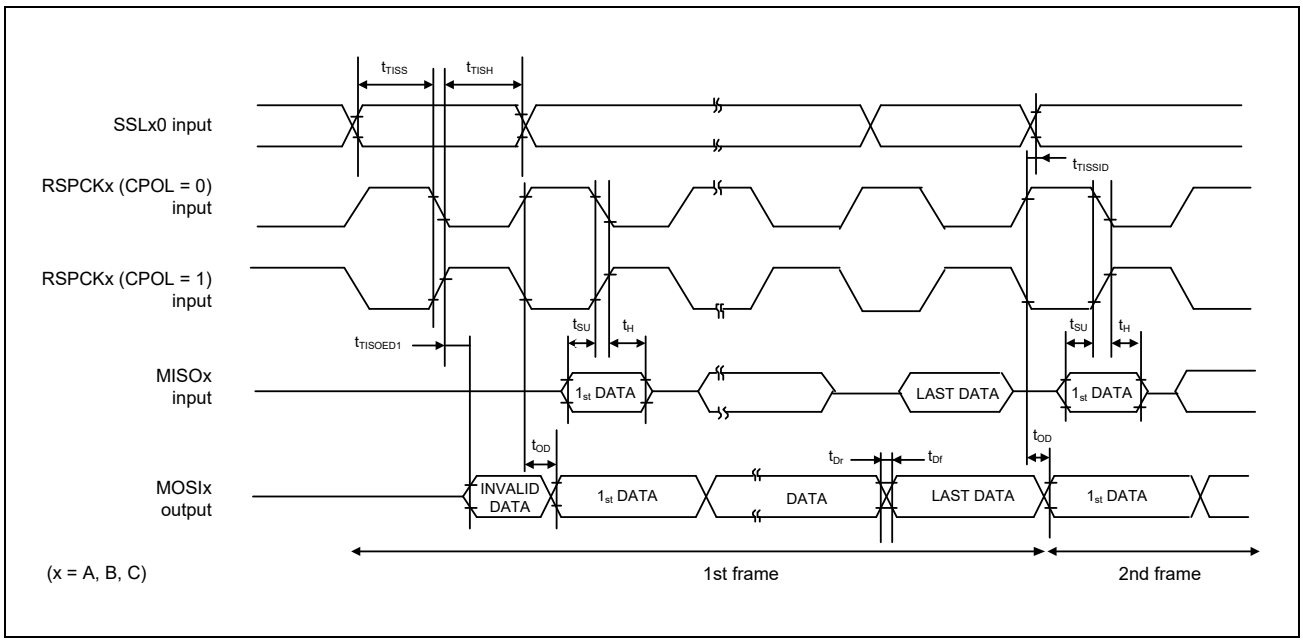


Figure 3.5-35 RSPI Timing (Slave, TI-SSP, without delay in burst transfer)

3.5.16 Renesas IIC Bus Interface (RIIC) Access Timing

Conditions: V_{OL} = 0.4 V

Drive strength: ×6

Table 3.5-16 RIIC Timing

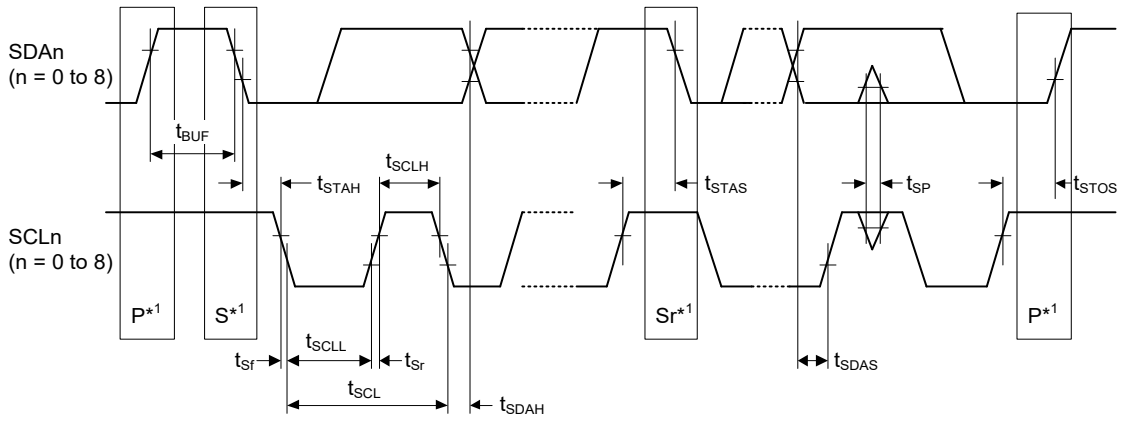
Parameter		Symbol	Min.*1,*2	Max.*1,*2	Unit	Figure
RIIC (Standard-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	**Figure 3.5-36**
	SCL input high-level pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low-level pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{sr}	—	1000	ns	
	SCL, SDA input fall time	t_{sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	**Figure 3.5-36**
	SCL input high-level pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low-level pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{sr}	—*4	300	ns	
	SCL, SDA input fall time	t_{sf}	—*4	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load*3	C_b	—	400	pF	
RIIC (Fast-mode Plus)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 240	—	ns	**Figure 3.5-36**
	SCL input high-level pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL input low-level pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL, SDA input rise time	t_{sr}	—*4	120	ns	
	SCL, SDA input fall time	t_{sf}	—*4	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 120	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load*3	C_b	—	550	pF	

Note 1. t_{IICcyc}: RIIC internal reference clock (IICϕ) cycle

Note 2. The values outside parentheses apply when the digital noise filter stage is 1 clock cycle while the digital filter is enabled. The values within parentheses apply when the digital noise filter stage is 4 clock cycle while the digital filter is enabled.

Note 3. C_b is the total capacitance of the bus lines.

Note 4. The minimum values are not specified for t_{sr} and t_{sf} in Fast-mode or Fast-mode Plus.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 3.5-36 RIIC Bus Interface Input/Output Timing

3.5.17 I3C Timing

Conditions: V_{OH} = VDD1218_I3C × 0.5, V_{OL} = VDD1218_I3C × 0.5, C = 30 pF (1.2 V or 1.8 V)

Drive strength: ×6

Table 3.5-17 I3C Timing

Parameter		Symbol	Min.*1	Max.	Unit	Figure
IIC (Standard mode, SMBus)	SCL3n cycle time	t_{SCL}	4(36) × t_{IICcyc} + 4 × t_{Pcyc} + 1300	—	ns	**Figure 3.5-37**
	SCL3n high-level pulse width	t_{SCLH}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL3n low-level pulse width	t_{SCLL}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 800	—	ns	
	SCL3n, SDA3n rise time	t_{Sr}	—	1000	ns	
	SCL3n, SDA3n fall time	t_{Sf}	—	300	ns	
	SCL3n, SDA3n spike pulse removal time	t_{SP}	0	1(16) × t_{IICcyc}	ns	
	SDA3n bus free time	t_{BUF}	3(20) × t_{IICcyc} + 300	—	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Setup time for repeated START condition	t_{STAS}	1000	—	ns	
	Setup time for STOP condition	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL3n, SDA3n capacitive load	C_b	—	400	pF	
IIC (Fast mode)	SCL3n cycle time	t_{SCL}	4(36) × t_{IICcyc} + 4 × t_{Pcyc} + 600	—	ns	**Figure 3.5-37**
	SCL3n high-level pulse width	t_{SCLH}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL3n low-level pulse width	t_{SCLL}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 300	—	ns	
	SCL3n, SDA3n rise time	t_{Sr}	—	300	ns	
	SCL3n, SDA3n fall time	t_{Sf}	—	300	ns	
	SCL3n, SDA3n spike pulse removal time	t_{SP}	0	1(16) × t_{IICcyc}	ns	
	SDA3n bus free time	t_{BUF}	3(20) × t_{IICcyc} + 300	—	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Setup time for repeated START condition	t_{STAS}	300	—	ns	
	Setup time for STOP condition	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL3n, SDA3n capacitive load	C_b	—	400	pF	

Note 1. t_{IICcyc}: I3C internal reference clock (I3Cϕ) cycle, t_{Pcyc}: I3C core clock cycle
Values in parentheses apply when the digital noise filter stage is 16 clock cycle while the digital filter is enabled.

Table 3.5-18 IIC Timing (Fast-mode+)

Parameter		Symbol	Min.*1	Max.	Unit	Figure
IIC (Fast-mode+)	SCL3n cycle time	t_{SCL}	4(26) × t_{IICcyc} + 4 × t_{Pcyc} + 240	—	ns	**Figure 3.5-37**
	SCL3n high-level pulse width	t_{SCLH}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	ns	
	SCL3n low-level pulse width	t_{SCLL}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	ns	
	SCL3n, SDA3n rise time	t_{Sr}	—	120	ns	
	SCL3n, SDA3n fall time	t_{Sf}	—	120	ns	
	SCL3n, SDA3n spike pulse removal time	t_{SP}	—	1(16) × t_{IICcyc}	ns	
	SDA3n bus free time	t_{BUF}	3(20) × t_{IICcyc} + 120	—	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 135	—	ns	
	Setup time for repeated START condition	t_{STAS}	260	—	ns	
	Setup time for STOP condition	t_{STOS}	260	—	ns	
	Data setup time	t_{SDAS}	50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL3n, SDA3n capacitive load	C_b	—	550	pF	

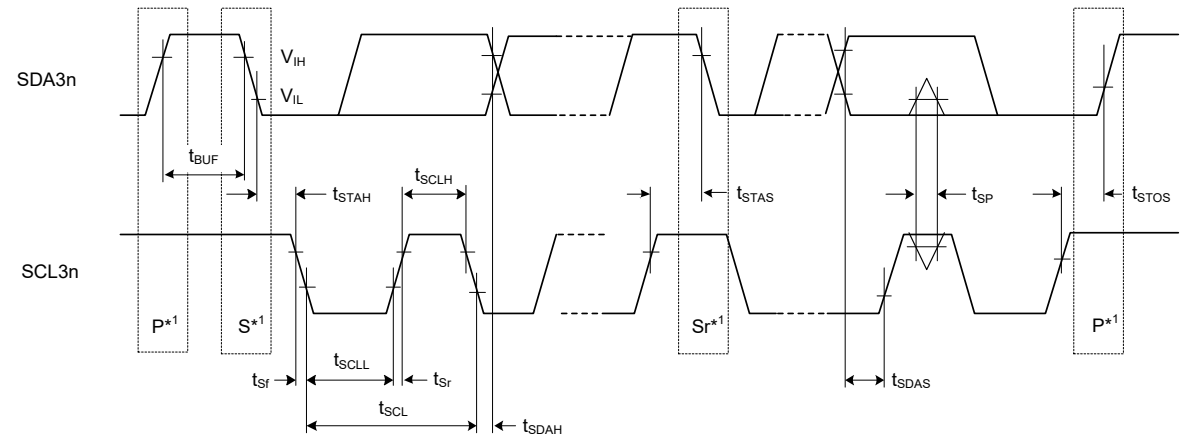
Note 1. t_{IICcyc}: I3C internal reference clock (I3Cϕ) cycle, t_{Pcyc}: I3C core clock cycle.
Values in parentheses apply when the digital noise filter stage is 16 clock cycle while the digital filter is enabled.

Table 3.5-19 IIC Timing (HS mode)

Parameter		Symbol	Cb = 100 pF		Cb = 400 pF		Unit	Figure
			Min.*1	Max.	Min.*1	Max.		
IIC (HS mode)	SCL3n cycle time	t_{SCL}	3(36) × t_{IICcyc} + 4 × t_{Pcyc} + 240	—	3(36) × t_{IICcyc} + 4 × t_{Pcyc} + 240	—	ns	**Figure 3.5-37**
	SCL3n high-level pulse width	t_{SCLH}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	ns	
	SCL3n low-level pulse width	t_{SCLL}	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	2(18) × t_{IICcyc} + 2 × t_{Pcyc} + 120	—	ns	
	SCL3n rise time	t_{Sr}	—	40	—	80	ns	
	SCL3n rise time after a repeated START condition and after an acknowledge bit	t_{Sr}	—	80	—	160	ns	
	SDA3n rise time	t_{Sr}	—	80	—	160	ns	
	SCL3n fall time	t_{Sf}	—	40	—	80	ns	
	SDA3n fall time	t_{Sf}	—	80	—	160	ns	
	SCL3n, SDA3n spike pulse removal time	t_{SP}	0	1(16) × t_{IICcyc}	0	1(16) × t_{IICcyc}	ns	
	Hold time for START condition	t_{STAH}	t_{IICcyc} + 135	—	t_{IICcyc} + 135	—	ns	
	Setup time for repeated START condition	t_{STAS}	160	—	160	—	ns	
	Setup time for STOP condition	t_{STOS}	160	—	160	—	ns	
	Data setup time	t_{SDAS}	10	—	10	—	ns	
	Data hold time	t_{SDAH}	0	80	0	150	ns	
	SCL3n, SDA3n capacitive load	C_b	—	100	—	400	pF	

Note 1. t_{IICcyc}: I3C internal reference clock (I3Cϕ) cycle, t_{Pcyc}: I3C core clock cycle.
Values in parentheses apply when the digital noise filter stage is 16 clock cycle while the digital filter is enabled.

Note 2. The maximum SCL clock frequency is 1.7 MHz.



Note: n = 0

Note 1. S, P, and Sr indicate the following conditions
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 3.5-37 I3C Bus Interface Input/Output Timing

Table 3.5-20 I3C Timing (Open Drain Timing Parameters)

Parameter		Symbol	Min.*1	Max.	Unit	Figure	Notes
SCL3n clock Low period		t_{LOW_OD}	200	—	ns	**Figure 3.5-40**	1, 2
		$t_{DIG\_OD\_L}$	t_{LOW_ODmin} + t_{fDA_ODmin}	—		**Figure 3.5-40**	—
SCL3n clock High period		t_{HIGH}	—	41	ns	**Figure 3.5-40**	3, 4
		t_{DIG_H}	36 (when 1.8 V) 40 (when 1.2 V)	t_{HIGH} + t_{CF}	ns	**Figure 3.5-40**	—
SDA3n signal fall time		t_{fDA_OD}	t_{CF}	33	ns	**Figure 3.5-40**	—
SDA3n data setup time open drain mode	V_{DD1218} = 1.8 V	t_{SU_OD}	12	—	ns	**Figure 3.5-39**, **Figure 3.5-40**	1
	V_{DD1218} = 1.2 V		13.9	—	ns	**Figure 3.5-39**, **Figure 3.5-40**	
Clock after START (S) condition		t_{CAS}	38.4	For ENTAS0: 1 µ	seconds	**Figure 3.5-40**	5, 6
				For ENTAS1: 100 µ			
				For ENTAS2: 2 m			
				For ENTAS3: 50 m			
Clock before STOP (P) condition		t_{CBP}	t_{CASmin}/2	—	seconds	**Figure 3.5-41**	—
Current master to secondary master overlap time during handoff		$t_{MMOverlap}$	$t_{DIG\_OD\_Lmin}$	—	ns	**Figure 3.5-46**	—
Bus available condition		t_{AVAL}	1	—	us	—	7
Bus idle condition		t_{IDLE}	1	—	ms	—	—
Time internal where new master not driving SDA3n low		t_{MMLock}	$t_{AVALmin}$	—	us	**Figure 3.5-46**	—

Note 1. This is approximately equal to t_{LOWmin} + t_{DS_ODmin} + t_{rDA_ODtyp} + t_{SU_ODmin}.

Note 2. The Master may use a shorter Low period if it knows that this is safe, i.e., that SDA is already above VIH.

Note 3. This is based on t_{SPIKE}, rise and fall times, and interconnect.

Note 4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I^2C Devices, and/or in consideration of the interconnect (e.g., a short bus).

Note 5. On a Legacy Bus where I2C Devices need to see Start.

Note 6. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3

Note 7. On a Mixed Bus with Fm Legacy I2C Devices, t_{AVAL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF})

Table 3.5-21 I3C Timing (Push-Pull Timing Parameters for SDR)

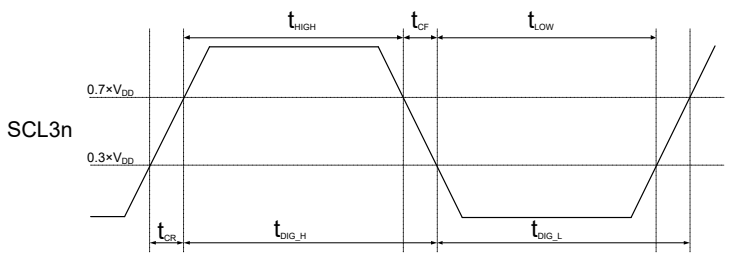
Parameter		Symbol	Min.*1	Max.	Unit	Figure	Notes
SCL3n clock frequency	V_{DD1218} = 1.8 V	t_{SCL}	0.01	12.5	MHz	—	1
	V_{DD1218} = 1.2 V		0.01	12.39	MHz	—	
SCL3n clock Low period		t_{LOW}	24	—	ns	**Figure 3.5-38**	—
		t_{DIG_L}	32	—	ns	**Figure 3.5-38**	2, 4
SCL3n clock High period for Mixed Bus		t_{HIGH}	24	—	ns	**Figure 3.5-38**	—
		t_{DIG_H}	32	45	ns	**Figure 3.5-38**	2, 3
SCL3n clock High period		t_{HIGH}	24	—	ns	**Figure 3.5-38**	—
		t_{DIG_H}	32	45	ns	**Figure 3.5-38**	2
Clock in to data out for a slave	V_{DD1218} = 1.8 V	t_{SCO}	—	12	ns	**Figure 3.5-43**	—
	V_{DD1218} = 1.2 V		—	12.7	ns		
SCL3n clock rise time		t_{CR}	—	150 × 1/f_{SCL} (capped at 60)	ns	**Figure 3.5-38**	—
SCL3n clock fall time		t_{CF}	—	150 × 1/f_{SCL} (capped at 60)	ns	**Figure 3.5-38**	—
SDA3n signal data hold in push-pull mode	Master	t_{HD_PP}	t_{CR} + 3 and t_{CF} + 3	—	—	**Figure 3.5-42**	4
	Slave		0	—	—	**Figure 3.5-44**	—
SDA3n signal data setup in push-pull mode	V_{DD1218} = 1.8 V	t_{SU_PP}	12	N/A	ns	**Figure 3.5-42**, **Figure 3.5-43**, **Figure 3.5-44**	—
	V_{DD1218} = 1.2 V		13.9	N/A	ns		
Clock after repeated START (Sr)		t_{CASr}	t_{CASmin}	N/A	ns	**Figure 3.5-45**	—
Clock before repeated START (Sr)		t_{CBSr}	t_{CASmin}/2	N/A	ns	**Figure 3.5-45**	—
Capacitive load per bus line (SDA3n / SCL3n)		C_b	—	50	pF	—	—

Note 1. FSCL = 1/(t_{DIG_L} + t_{DIG_H})

Note 2. t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using VIL and VIH (see **Figure 3.5-38**)

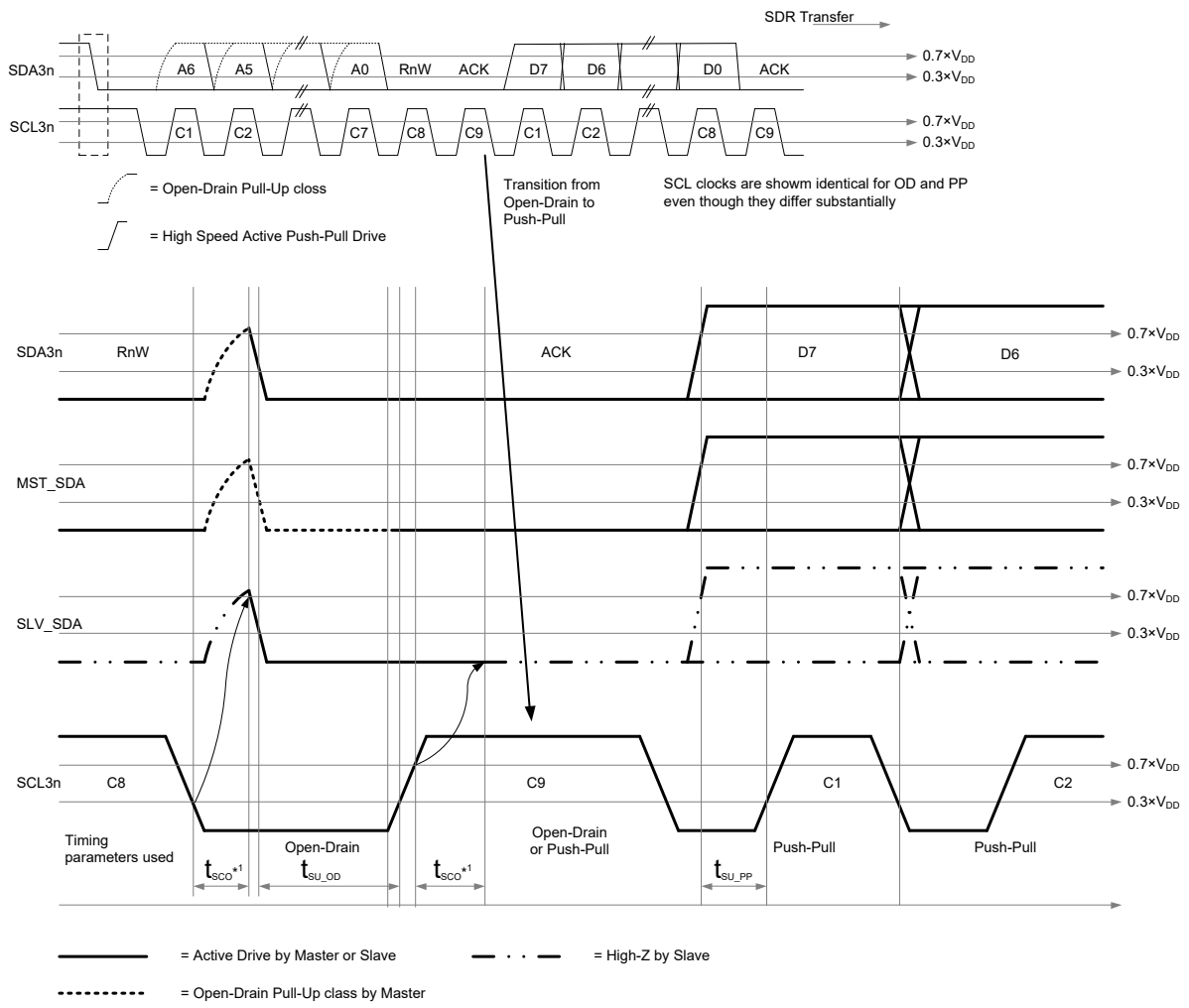
Note 3. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I^2C Devices do not interpret I3C signaling as valid I^2C signaling.

Note 4. As both edges are used, the hold time must be satisfied for the respective edges, for example, t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.



Note: V_{DD}: VDD1218_I3C

Figure 3.5-38 t_{DIG_H} and t_{DIG_L}

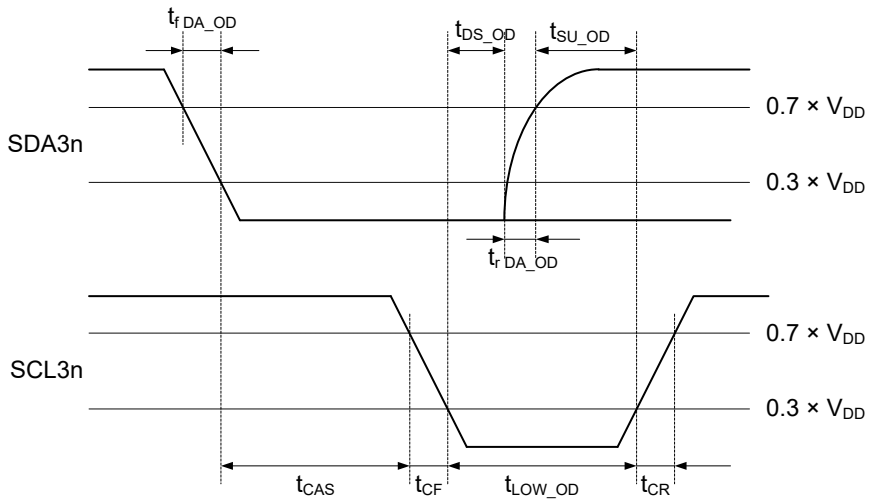


Note: V_{DD}: VDD1218_I3C

Note: Open-Drain: Master releases SDA after a suitable delay from SCL edges
Push-Pull: Master drives SDA after a suitable delay from SCL edges

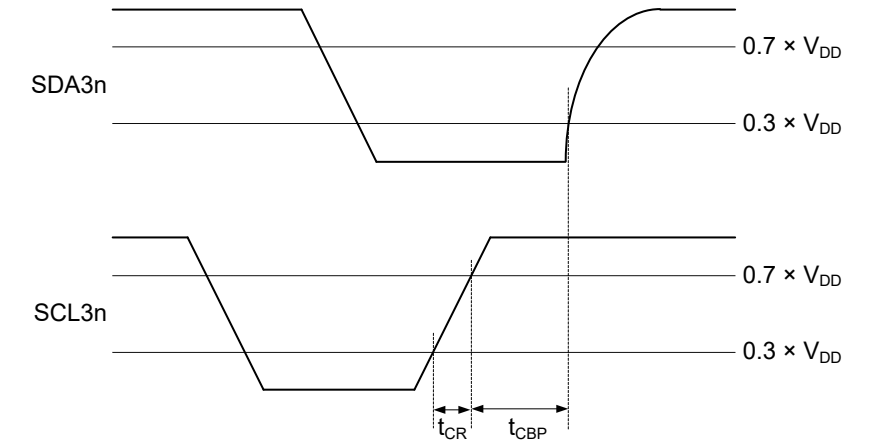
Note 1. t_{SCO} is depicted for informative purposes only

Figure 3.5-39 I3C Data Transfer – ACK by Slave



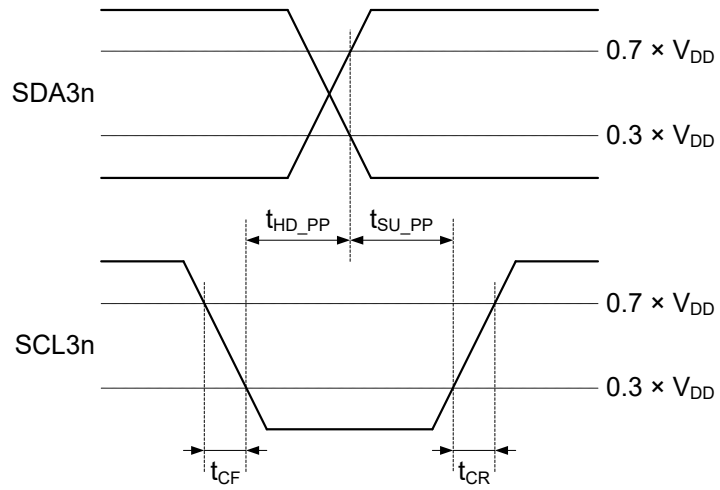
Note: V_{DD}: VDD1218_I3C

Figure 3.5-40 I3C START Condition Timing



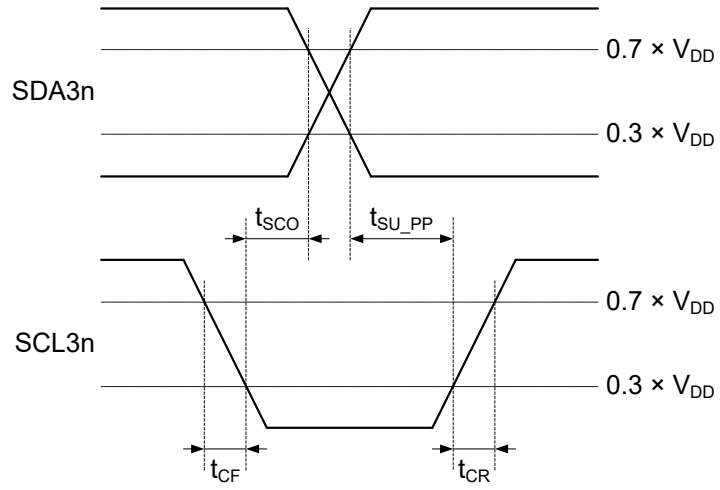
Note: V_{DD}: VDD1218_I3C

Figure 3.5-41 I3C STOP Condition Timing



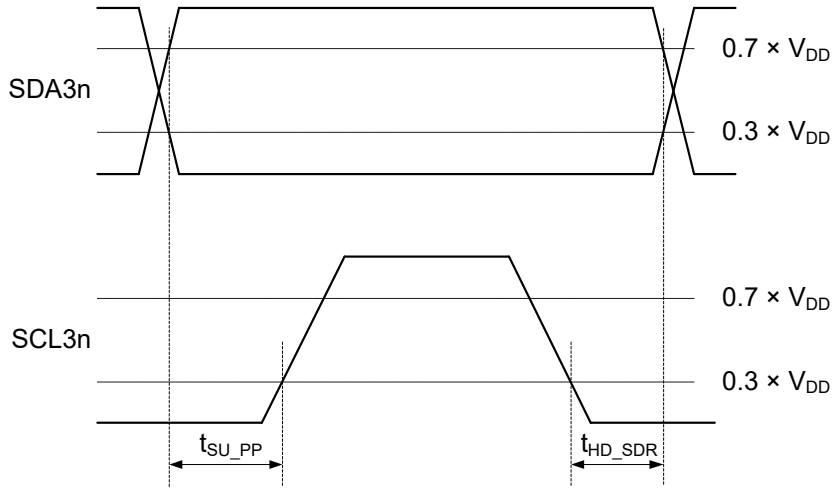
Note: V_{DD}: VDD1218_I3C

Figure 3.5-42 I3C Master Out Timing



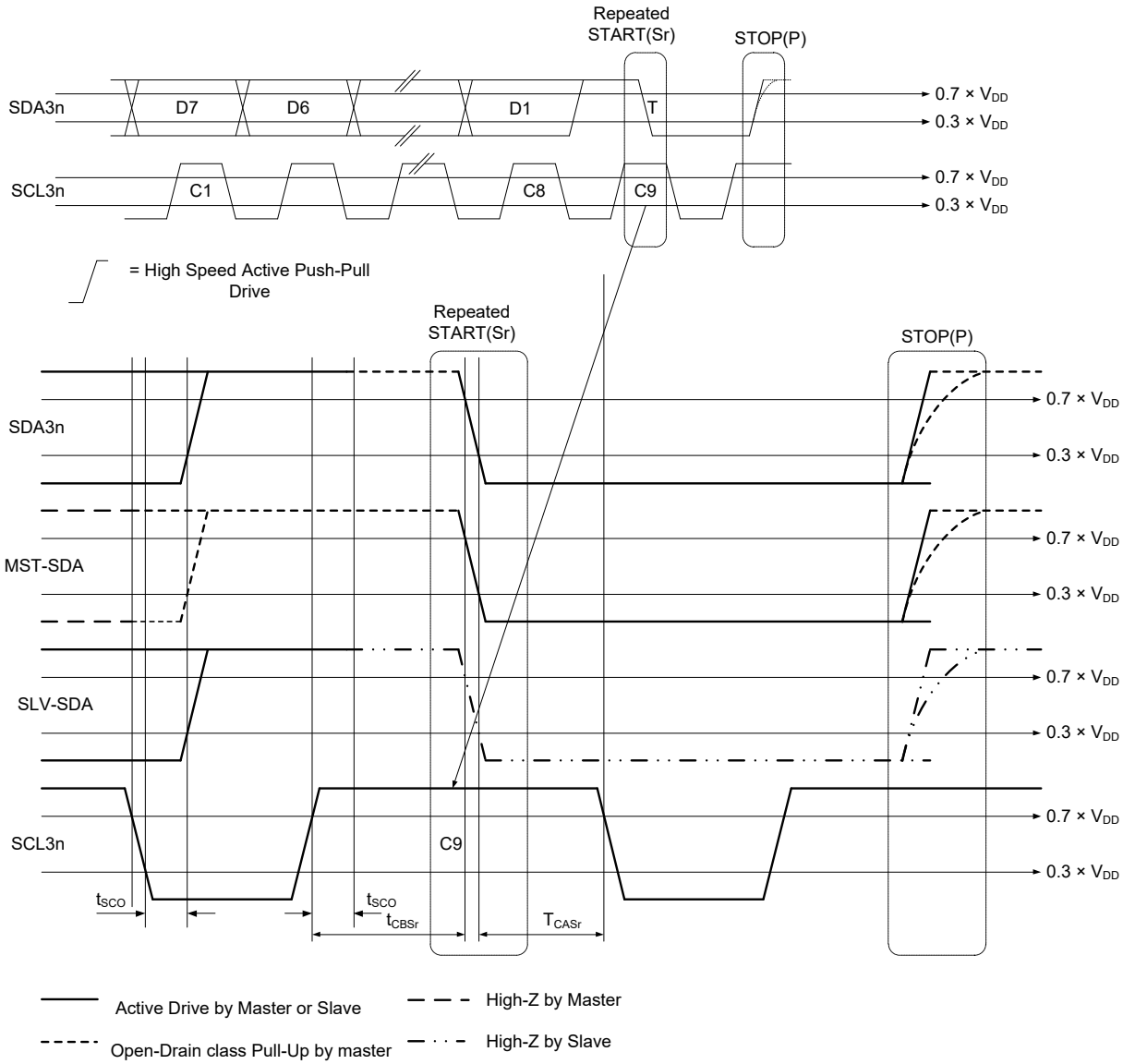
Note: V_{DD}: VDD1218_I3C

Figure 3.5-43 I3C Slave Out Timing



Note: V_{DD}: VDD1218_I3C

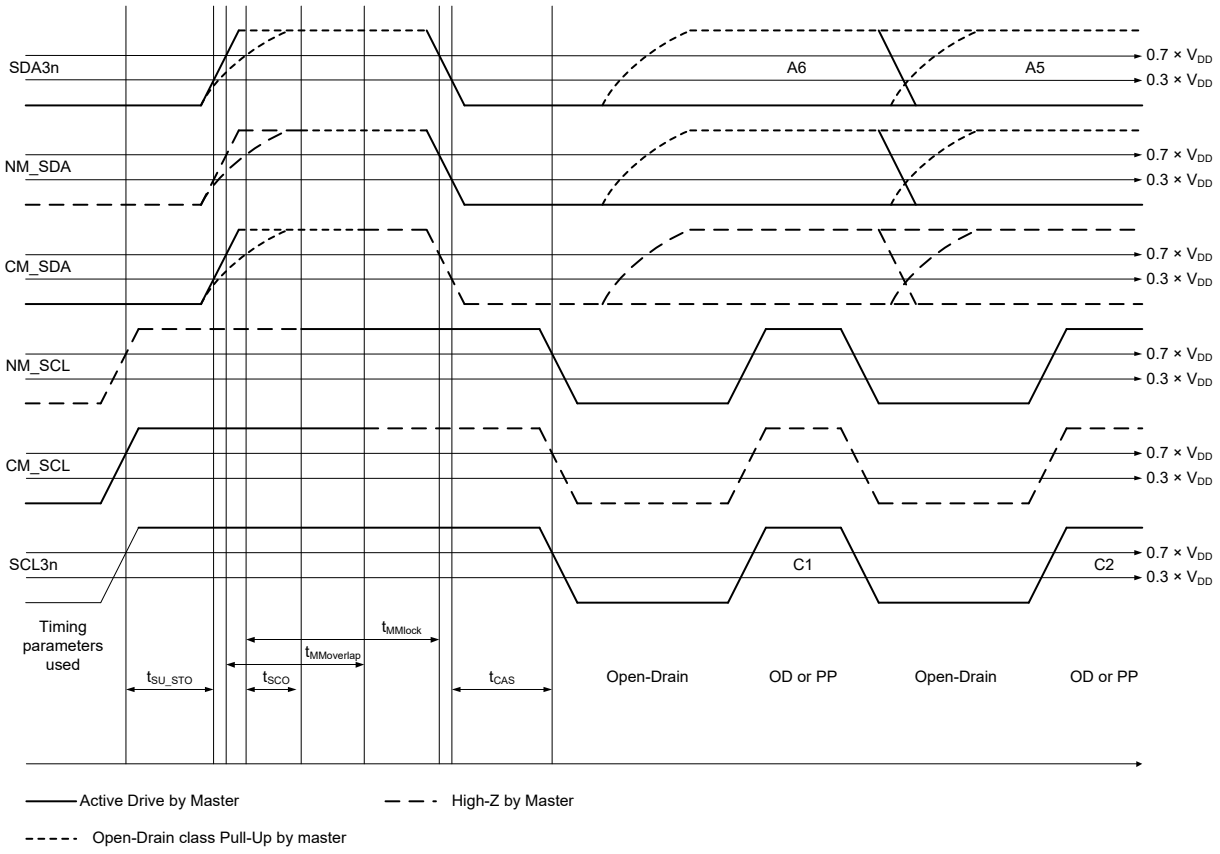
Figure 3.5-44 Master SDR Timing



Note: V_{DD}: VDD1218_I3C

Note: Sr immediately followed by P is illegal for I2C devices; however, many devices are not adversely affected by it. The condition is not illegal for I3C devices.

Figure 3.5-45 T-Bit When Master Ends Read with Repeated START and STOP



Note: V_{DD}: VDD1218_I3C

Note: Master releases or drives SDA after a suitable delay from SCL edges

Figure 3.5-46 I3C Timing

3.5.18 CANFD Interface Access Timing

Table 3.5-22 CANFD Interface Timing

Parameter		Symbol	CAN		CANFD		Unit	Figures
			Min.	Max.	Min.	Max.		
CANFD	Internal delay time	t_{node}*1	—	100	—	50	ns	**Figure 3.5-47**
	Transmission rate	—	—	1	—	8	Mbps	

Note 1. Internal delay time (t_{node}) = Internal transmission delay time (t_{output}) + Internal reception delay time (t_{input})

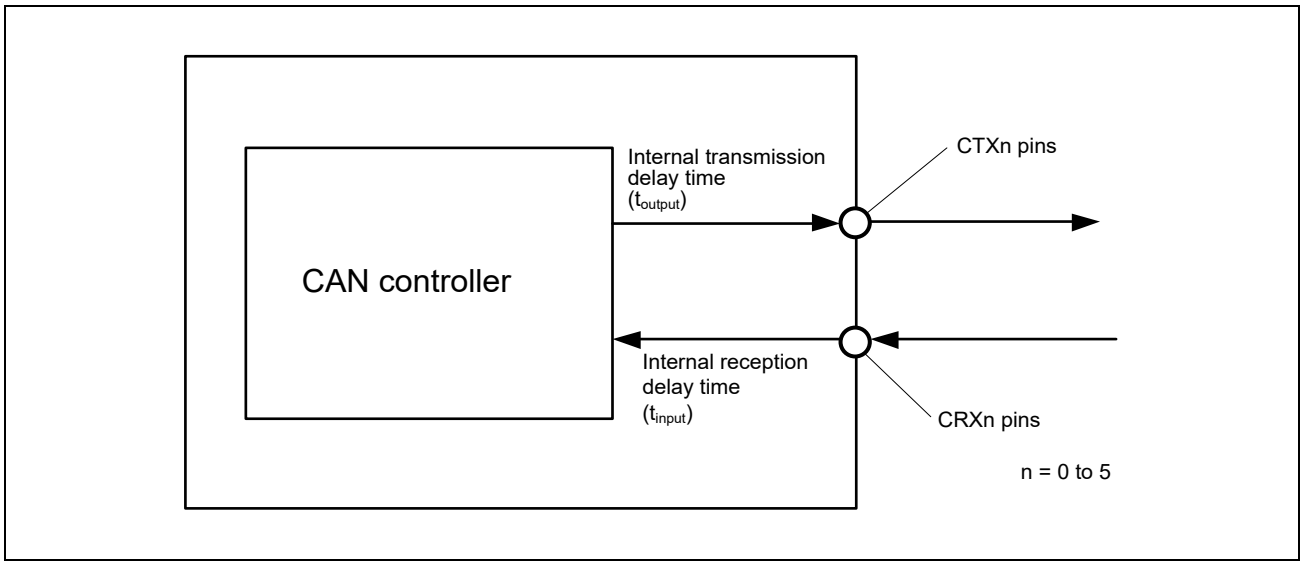


Figure 3.5-47 CANFD Interface Condition

3.5.19 A/D Converter Access Timing

Table 3.5-23 A/D Converter Trigger Timing

Parameter			Symbol	Min.	Max.	Unit*1	Figure
A/D converter	A/D converter trigger input pulse width	ADTRG	t_{TRGW}	1.5	—	$t_{PADCcyc}$	**Figure 3.5-48**

Note 1. $t_{PADCcyc}$: ADC internal clock cycle (ADC_0_PCLK)

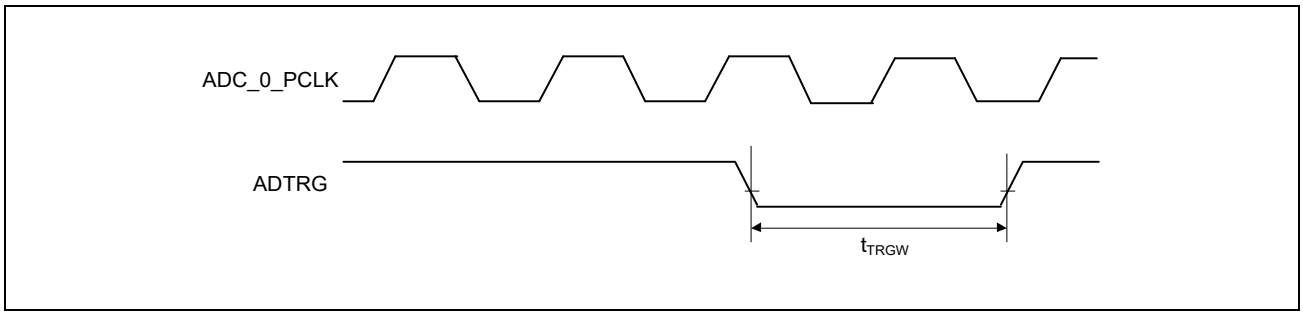


Figure 3.5-48 A/D Converter Trigger Input Timing (ADTRG)

3.5.20 SSIU Timing

Conditions:

V_{OH} = VDD18 × 0.5, V_{OL} = VDD18 × 0.5, C = 30 pF*1 (1.8 V)

V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF*1 (3.3 V)

Drive strength: ×1, ×2, ×4, ×6

Note 1. Other than t_{RC}: Rise-edge clock timing

Table 3.5-24 SSIU Signal Timing

Parameter	Symbol	Min.	Max.	Unit	Note	Figure
Output clock cycle	t_O	80	15625	ns	—	**Figure 3.5-49**
Input clock cycle	t_I	80	15625	ns	—	
Output clock high-cycle	t_{HC}	35*1	—	ns	—	
Output clock low-cycle	t_{LC}	35*1	—	ns	—	
Input clock high-cycle	t_{HC}	35	—	ns	—	
Input clock low-cycle	t_{LC}	35	—	ns	—	
Rise-edge clock timing	t_{RC}	—	20*2	ns	Output (100 pF)	
Output delay	t_D	-5	19	ns	—	**Figure 3.5-50** to **Figure 3.5-53**
Setup time	t_S	15	—	ns	—	
Hold time	t_H	5	—	ns	—	

Note 1. The width at high or low level of the clock signal when the input on AUDIO_CLKA, AUDIO_CLKB, or AUDIO_CLKC is output from SCK without frequency division in master mode is min. 30 ns.

Note 2. Output transition time from 20% to 80%

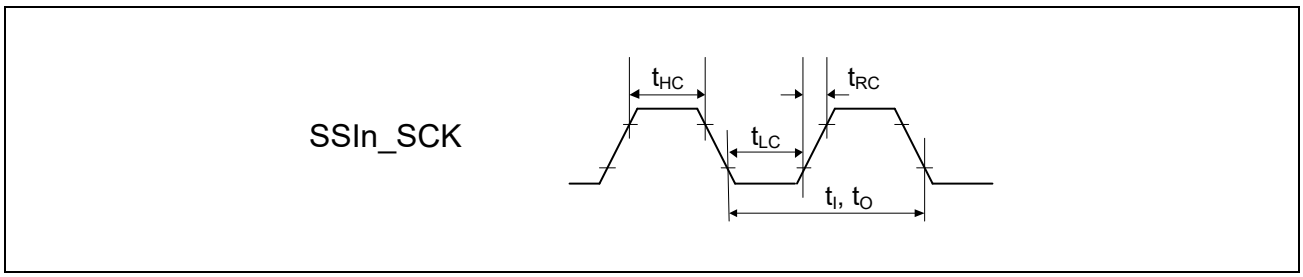


Figure 3.5-49 SCK Clock Input/Output Timing

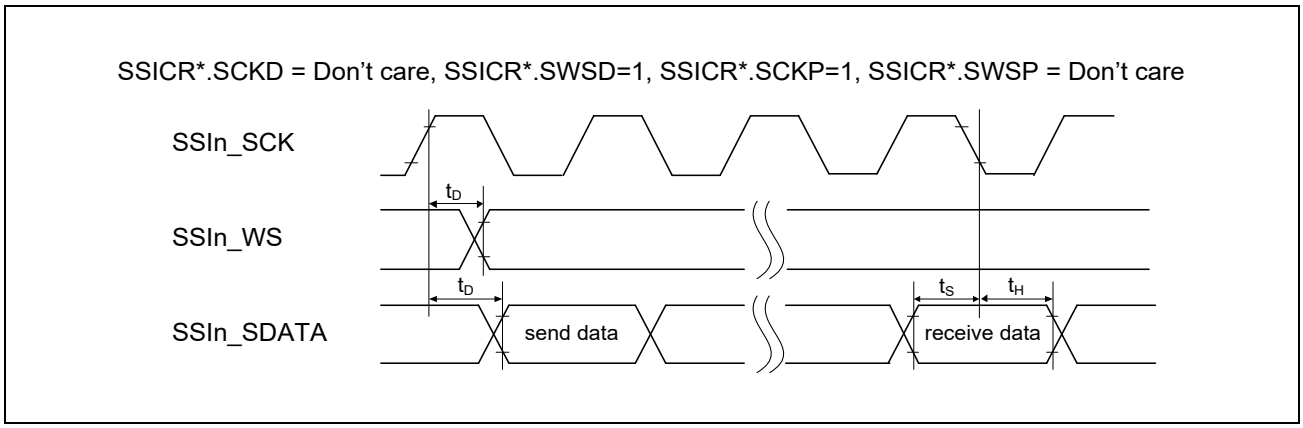


Figure 3.5-50 SSI Timing (1)

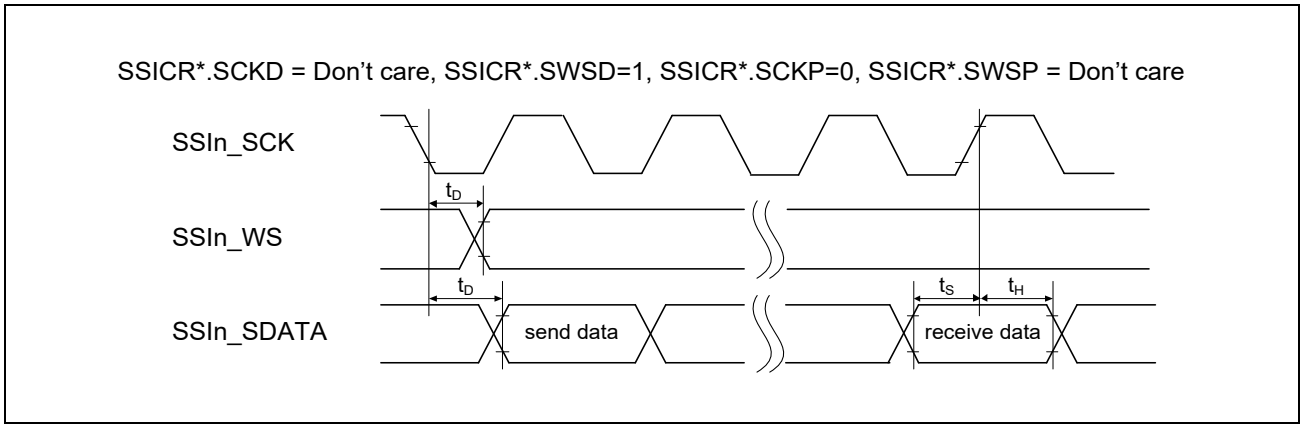


Figure 3.5-51 SSI Timing (2)

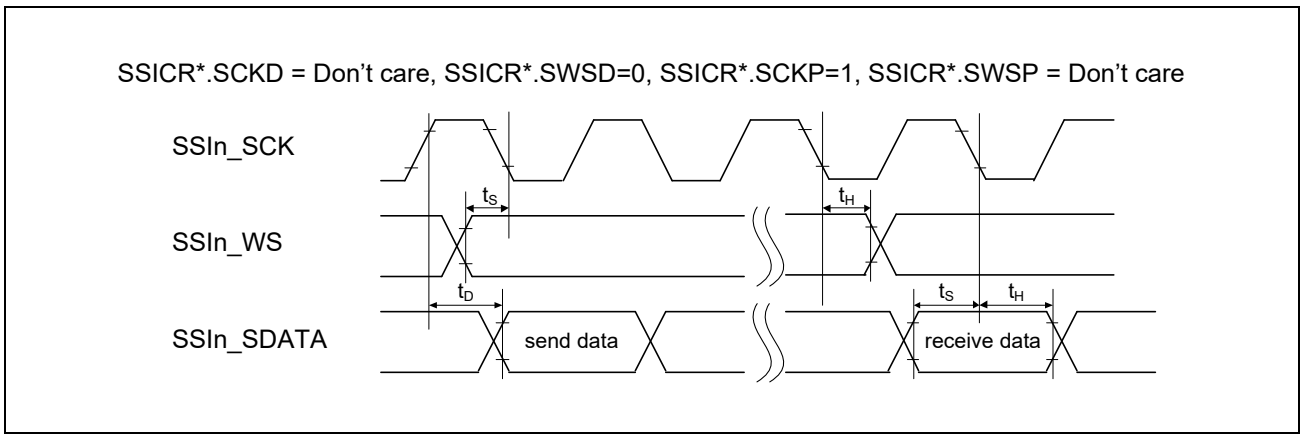


Figure 3.5-52 SSI Timing (3)

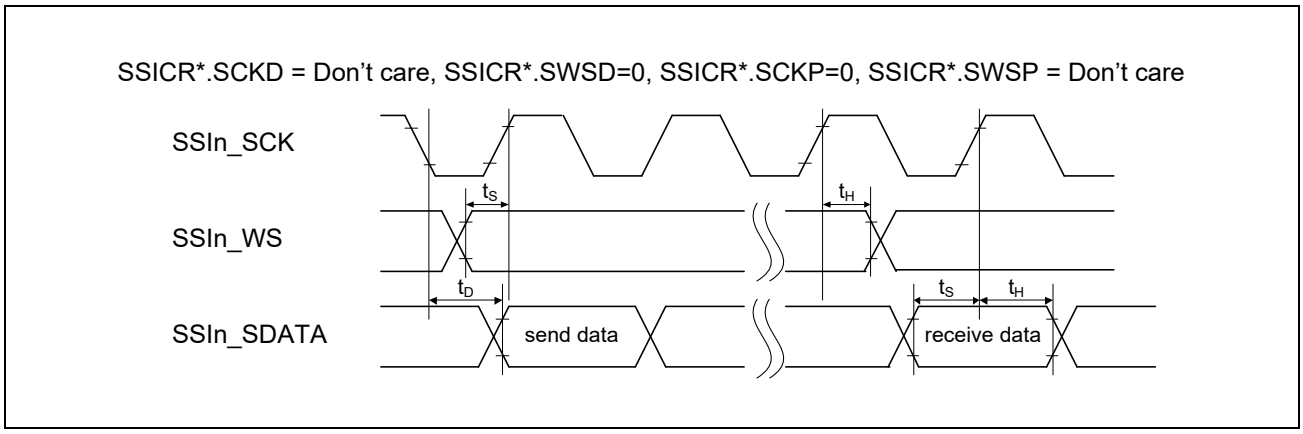


Figure 3.5-53 SSI Timing (4)

3.5.21 PDM Timing

Conditions:

V_{OH} = VDD18 × 0.5, V_{OL} = VDD18 × 0.5, C = 30 pF (1.8 V)

V_{OH} = VDD33 × 0.5, V_{OL} = VDD33 × 0.5, C = 30 pF (3.3 V)

Drive strength: ×1, ×2, ×4, ×6

Table 3.5-25 PDM Interface Timing

Parameter	Symbol	Min.	Max.	Unit	Figure
Clock period	t_{PSYNC}	2	32	t_{CCcyc} = 208.33 ns (4.8 MHz)*1	**Figure 3.5-54**
Clock high-level period	t_{PDCKWH}	t_{PSYNC} × 0.45	t_{PSYNC} × 0.55	ns	
Clock low-level period	t_{PDCKWL}	t_{PSYNC} × 0.45	t_{PSYNC} × 0.55	ns	
Clock rise time	t_{R-EDGE}	—	3*2	ns	
Clock fall time	t_{F-EDGE}	—	3*2	ns	
Setup time	t_{su}	15	—	ns	**Figure 3.5-55** , **Figure 3.5-56**
Hold time	t_h	0	—	ns	

Note 1. t_{CCcyc} is the period of PDMn core clock (n = 0, 1).

Note 2. Output transition time from 20% to 80%

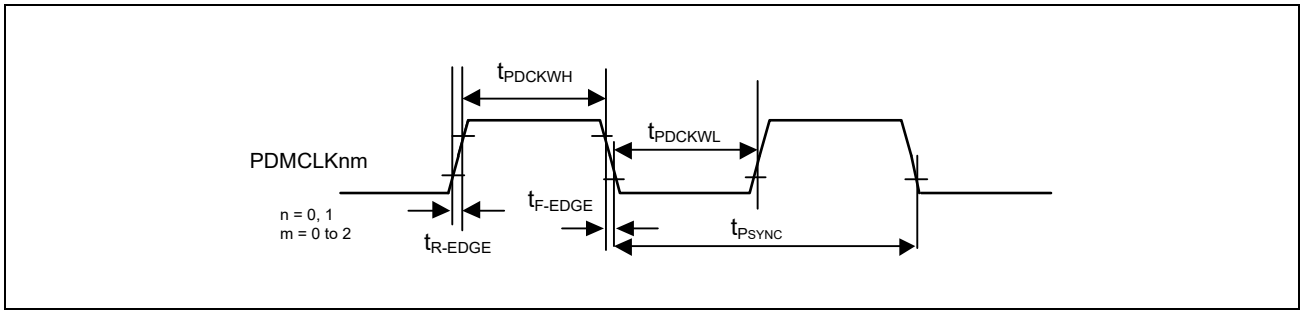


Figure 3.5-54 Timing of Clock Output (PDMCLKnm)

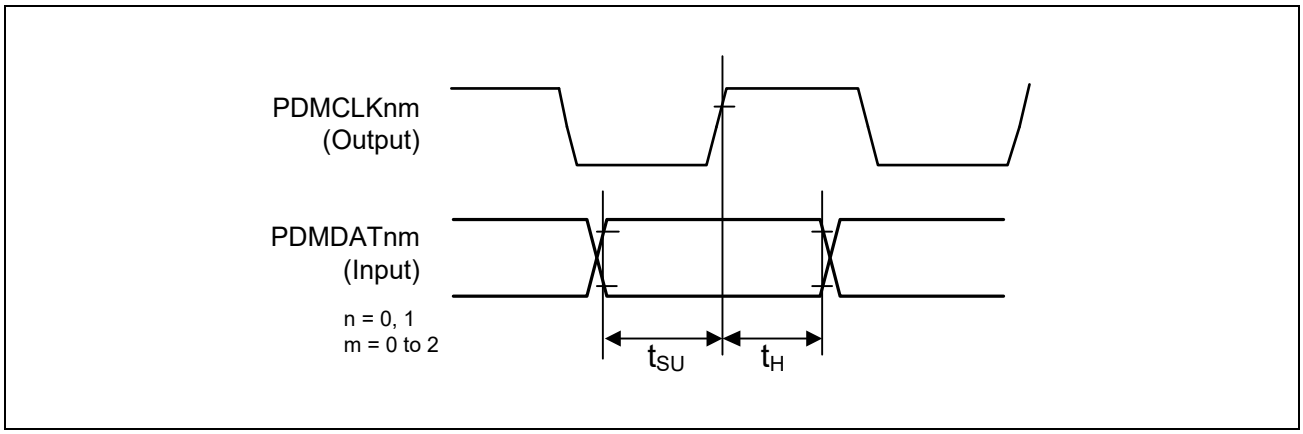


Figure 3.5-55 Timing of Clock Output (Synchronized with the rise of PDMCLKnm)

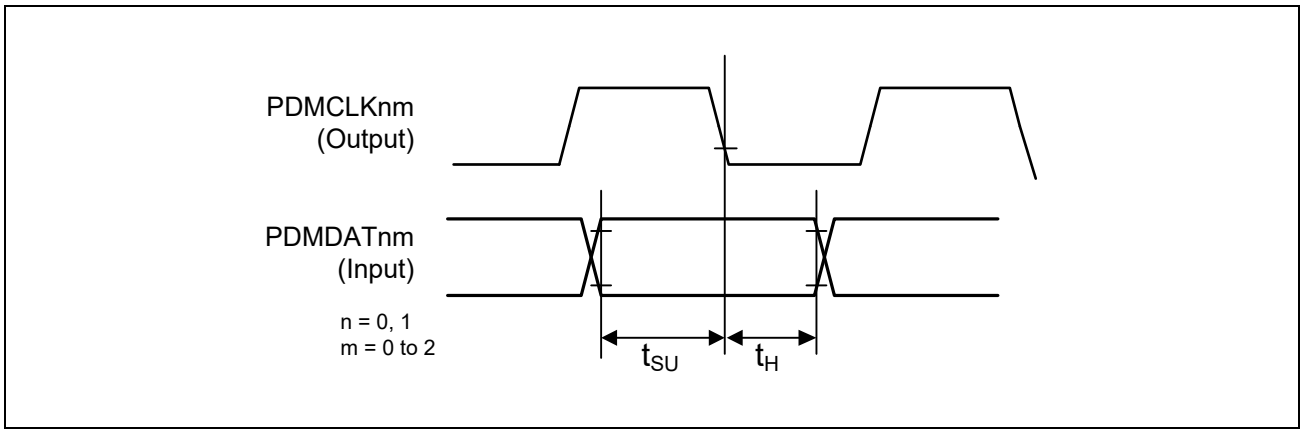


Figure 3.5-56 Timing of Clock Output (Synchronized with the fall of PDMCLKnm)

3.5.22 MIPI CSI-2 PHY Characteristics

The MIPI CSI-2 Rx D-PHY of this LSI is equivalent to the MIPI D-PHY Version 1.2.

For details, refer to the MIPI specification.

3.5.23 MIPI DSI Tx D-PHY Characteristics

The MIPI DSI Tx D-PHY of this LSI is compliant with the MIPI D-PHY Version 1.2.

For details, refer to the MIPI specification.

3.5.24 Control Signal Access Timing

Table 3.5-26 Control Signal Timing

Item	Symbol	Min.	Max.	Unit	Figures
QRESN pulse width	t_{RESW}	1	—	µs	**Figure 3.5-57**
TRSTN pulse width	t_{TRSW}	1	—	µs	
NMI pulse width	t_{NMIW}	20	—	t_{cyc}*1	**Figure 3.5-58**
IRQ pulse width	t_{IRQW}	20	—	t_{cyc}*1	
TINT pulse width	t_{TINTW}	20	—	t_{cyc}*1	

Note 1. t_{cyc} = 41.666 ns (24 MHz)

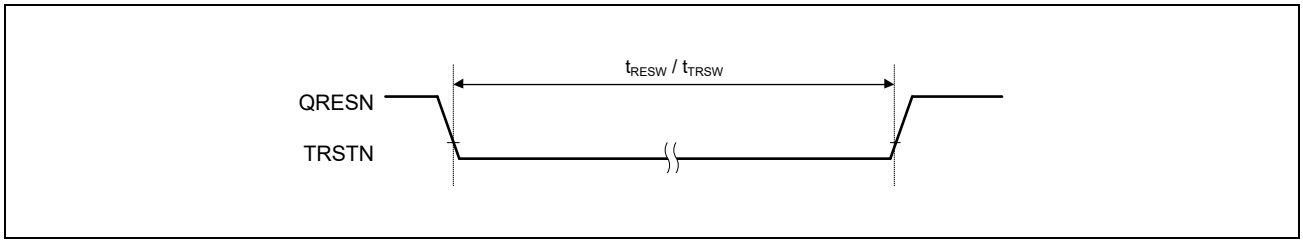
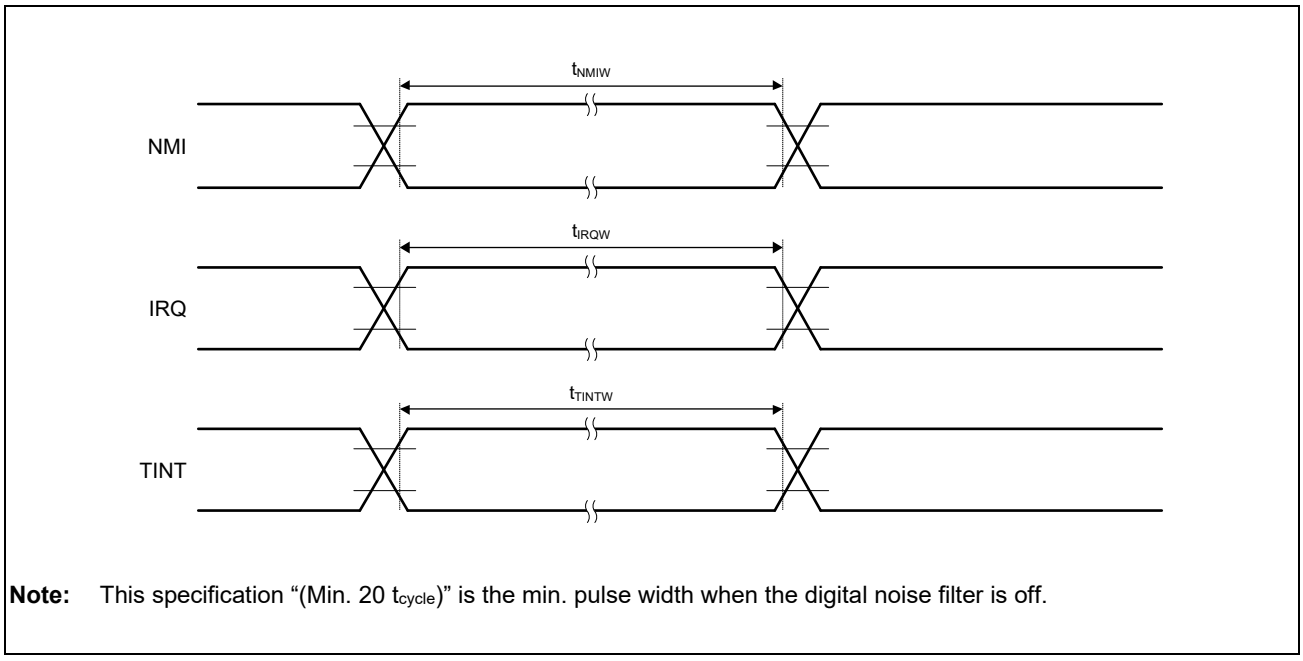


Figure 3.5-57 Reset Input Timing



Note: This specification “(Min. 20 t_{cycle})” is the min. pulse width when the digital noise filter is off.

Figure 3.5-58 Interrupt Signal Input Timing

3.5.25 JTAG Debugger Interface Access Timing

Table 3.5-27 Debugger IF Timing

Item	Symbol	Min.	Max.	Unit	Figures
TCK_SWCLK cycle time	t_{TCKcyc}	50	—	ns	**Figure 3.5-59**
TCK_SWCLK high-level pulse width	t_{TCKH}	20	—	ns	**Figure 3.5-60**
TCK_SWCLK low-level pulse width	t_{TCKL}	20	—	ns	
TDI setup time	t_{TDIS}	15	—	ns	
TDI hold time	t_{TDIH}	15	—	ns	
TMS_SWDIO setup time	t_{TMSS}	15	—	ns	
TMS_SWDIO hold time	t_{TMSH}	15	—	ns	
TMS_SWDIO delay time	t_{SWDO}	—	14	ns	
TDO delay time	t_{TDOD}	—	14	ns	
Capture register setup time	t_{CAPTS}	10	—	ns	**Figure 3.5-61**
Capture register hold time	t_{CAPTH}	10	—	ns	
Update register delay time	$t_{UPDATED}$	—	20	ns	

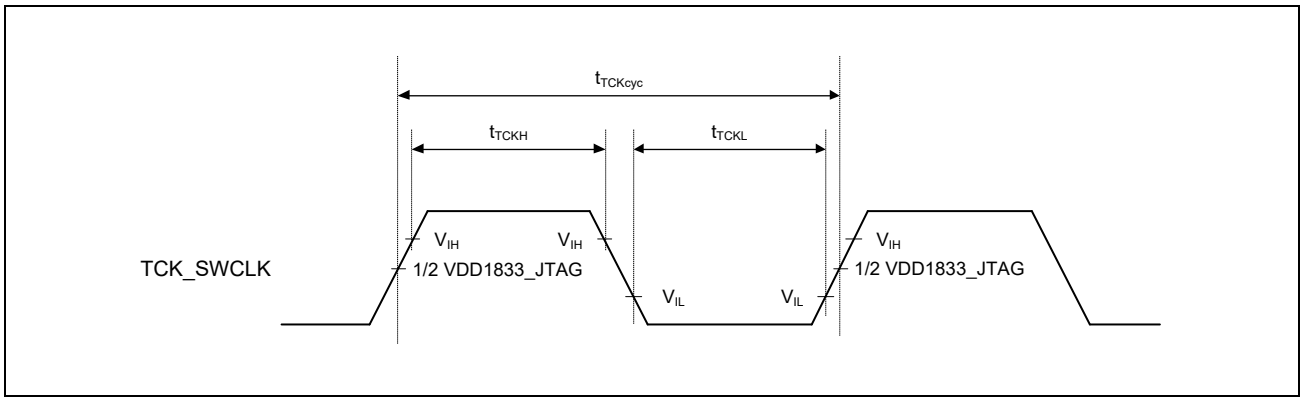


Figure 3.5-59 TCK_SWCLK Input Timing

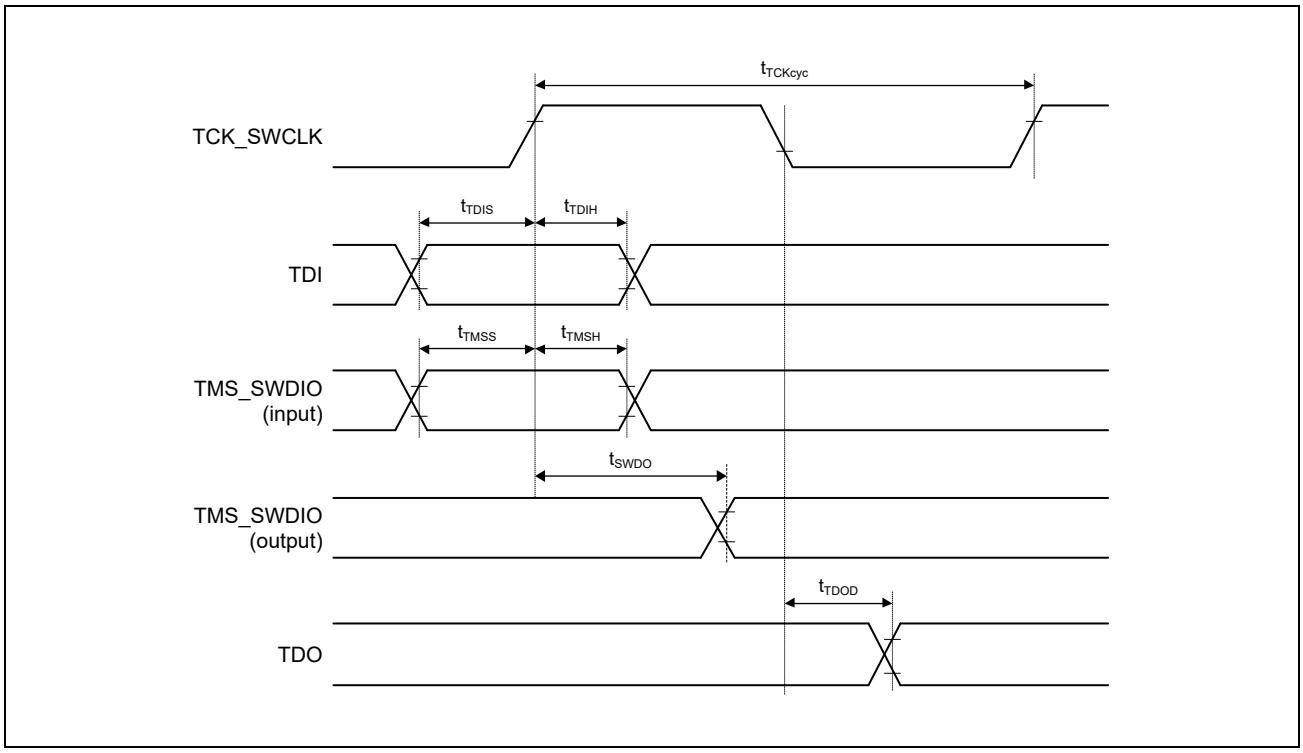


Figure 3.5-60 Data Transfer Timing

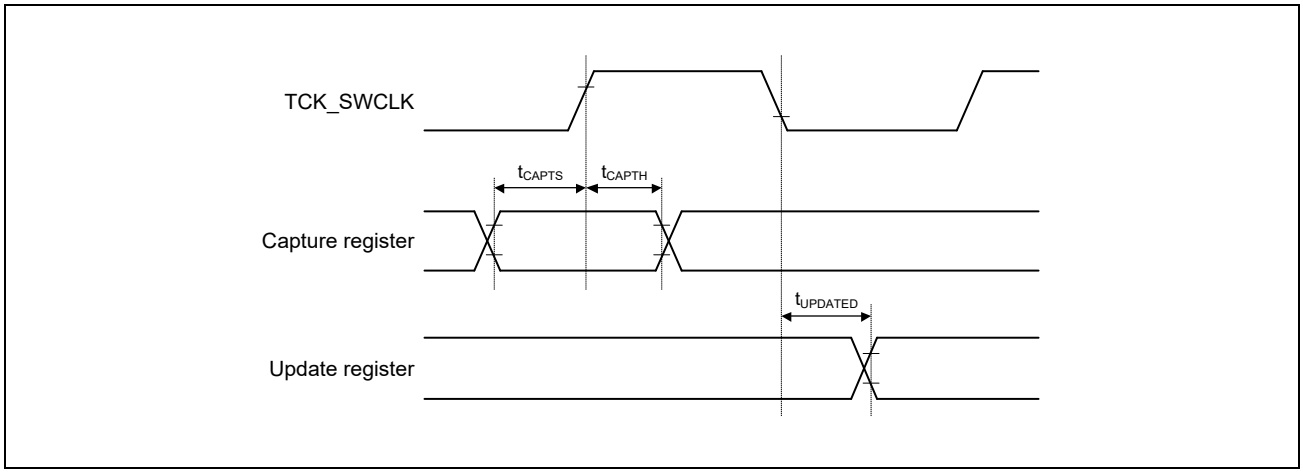


Figure 3.5-61 Boundary Scan Input/Output I/O Timing

3.6 Analog Characteristics

3.6.1 ADC Characteristics

Table 3.6-1 DC Characteristics

Item	Min.	Typ.	Max.	Unit
Resolution	—	12	—	Bit
Analog input capacitance	—	—	13	pF
Analog input range	0	—	ADCn_ADAVDD18*2	V
Conversion time*1 Permissible signal source impedance Max. = 1.0 kΩ	0.4	—	4.0	µs
Offset error	0	—	100	LSB
Full-scale error	-100	—	0	LSB
Quantization error	—	±0.5	—	LSB
DNL differential non-linearity error	—	—	±3.0	LSB
INL integral nonlinearity error	—	—	±6.0	LSB

Note 1. The conversion time is the total of the sampling time and the comparison time.

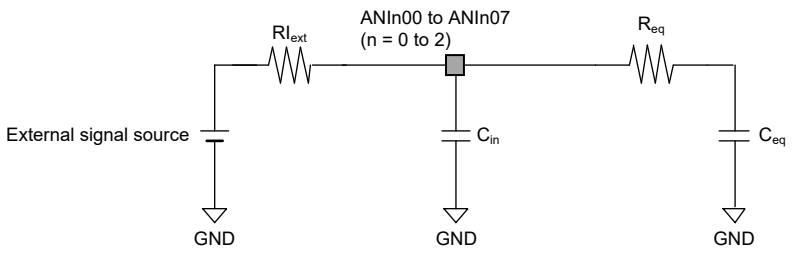
Note 2. n = 0 to 2

Table 3.6-2 Recommended External Input Resistance

Item	Symbol	Min.	Typ.	Max.	Unit
External input resistance*1 (ANIn00-ANIn07)*2	RI_{ext}	—	—	1	kΩ

Note 1. Output resistance of signal generator + Series parasitic resistance between signal source and ADC input.

Note 2. n = 0 to 2



Note: Analog input equivalent resistance (R_{eq}): 500 Ω
Analog input equivalent capacitance (C_{eq}): 10 pF
Analog input pin capacitance (C_{in}): 3 pF

Figure 3.6-1 A/D Converter Equivalent Circuit and Peripheral Configuration Diagram

3.6.2 Temperature Sensor Characteristics

Table 3.6-3 Temperature Sensor Characteristics

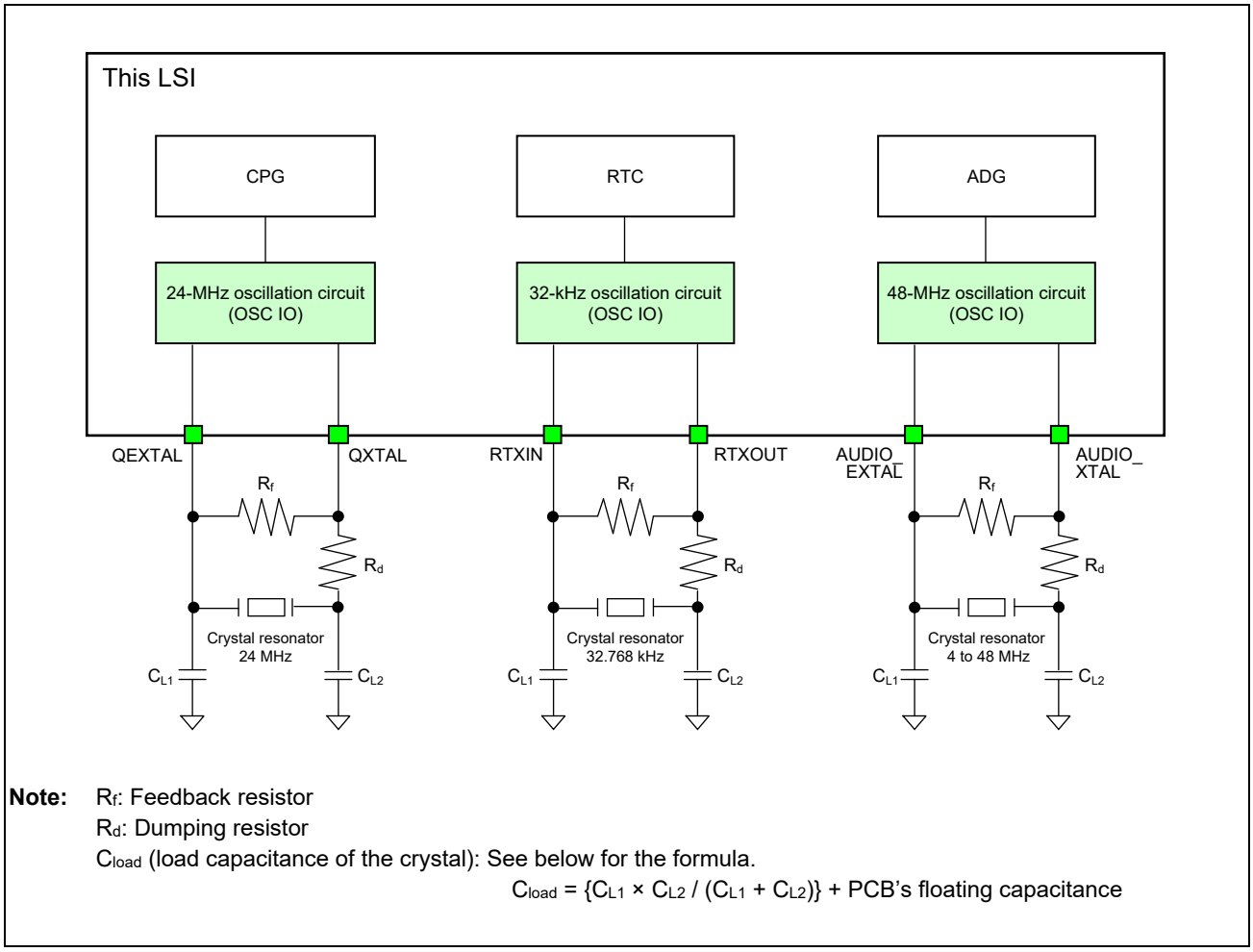
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Accuracy from −40°C to 125°C	Accm40_125	—	±3.0	±5.0	°C	—

3.7 Oscillation Circuits for Connecting Crystal Resonators (OSC)

This LSI chip includes two oscillation circuits (OSC) for connection to crystal resonators, specifically a 24-MHz crystal resonator for the system clock and a 32.768-kHz crystal resonator for the real-time clock. **Table 3.7-1** lists the pins for connecting the crystal resonators and the clock frequencies. **Figure 3.7-1** shows an example of the connections with crystal resonators.

Table 3.7-1 Pins for Connecting Crystal Resonators and Clock Frequency

External Pin Name	I/O	Clock Frequency
For the system clock		
QEXTAL	Input	24 MHz (frequency deviation: ±50 ppm)
QXTAL	Output	24 MHz
For the real-time clock		
RTXIN	Input	32.768 kHz (frequency deviation: ±50 ppm)
RTXOUT	Output	32.768 kHz
For the audio clocks		
AUDIO_EXTAL	Input	4 to 48 MHz
AUDIO_XTAL	Output	4 to 48 MHz



Note: R_f: Feedback resistor
R_d: Dumping resistor
C_{load} (load capacitance of the crystal): See below for the formula.

$$C_{load} = \{C_{L1} \times C_{L2} / (C_{L1} + C_{L2})\} + \text{PCB's floating capacitance}$$

Figure 3.7-1 Example of Connections with Crystal Resonators

Place the crystal resonators and the capacitors C_{L1} and C_{L2} as close as possible to the pins to connect crystal resonators. To avoid interference and to ensure correct oscillation, the grounding points of the capacitors appended to the crystal resonators should be shared, and no wiring patterns should be placed near these components.

The characteristics of the crystal resonators are closely related to the design of the user board. Therefore, the user should sufficiently evaluate them with reference to the example of connection of crystal resonators in **Figure 3.7-1**.

The circuit rating of a crystal resonator depends on the crystal resonator and the stray capacitance of the mounting circuit. Therefore, contact the manufacturer of the crystal resonator before deciding upon the circuit rating. The user should thoroughly evaluate and then set the parameters (resistor and capacitor values).

Table 3.7-2 is a list of recommended values for the crystal resonators.

Table 3.7-2 Recommended Model Values for the Crystal Resonators

	Model Values for the Crystal Resonators			
Clock Frequency	Max. ESR*1	Max. C_L*2	Max. C_0*3	Max. Drive Level
32.768 kHz	70 kΩ	12.5 pF	1.4 pF	1 µW
24 MHz	60 Ω	12 pF	7 pF	100 µW
48 MHz	50 Ω	10 pF	7 pF	100 µW

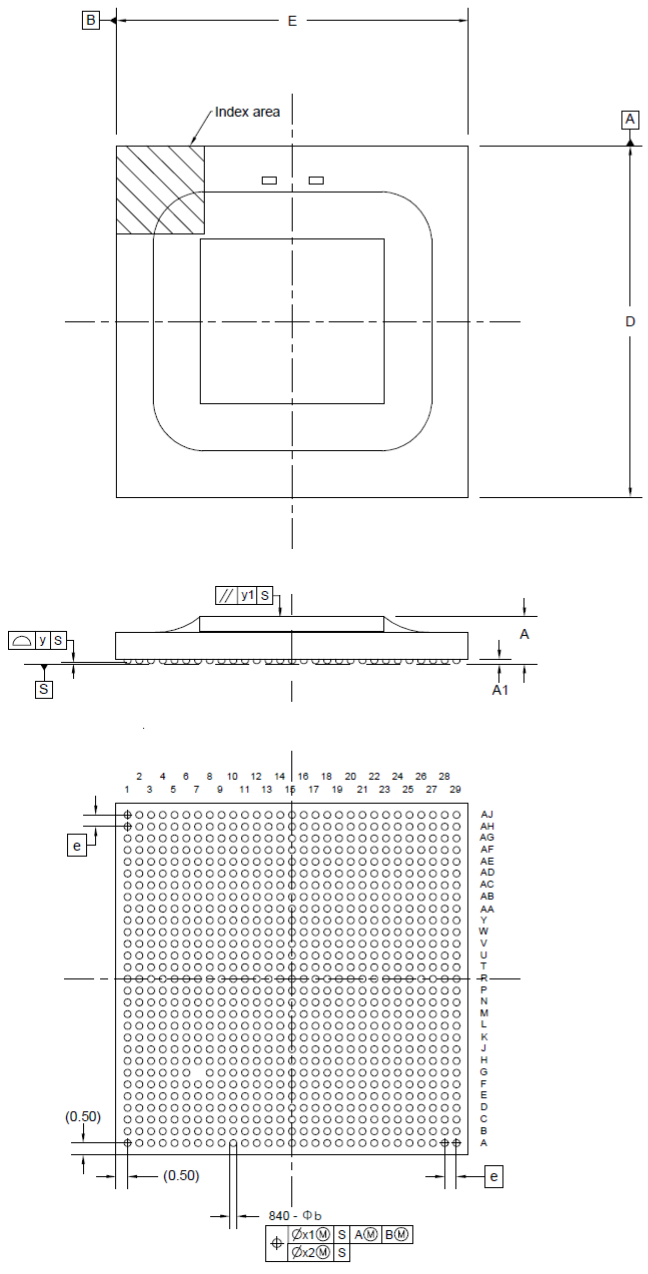
Note 1. ESR means the equivalent series resistor of the crystal resonator.

Note 2. C_L is the load capacitance of the crystal resonator.

Note 3. C_0 is the parallel capacitance of the crystal resonator.

Section 4 Package Dimensions

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-FBGA840-15x15-0.50	PRBG0840KA-A	0.87



Reference Symbol	Dimension in Millimeters		
	MIN.	NOM.	MAX.
D	14.85	15.00	15.15
E	14.85	15.00	15.15
e	—	0.50	—
A	(1.90)	(2.10)	2.30
A1	0.15	(0.25)	—
b	0.25	0.30	0.35
x1	—	—	0.20
x2	—	—	0.05
y	—	—	0.12
y1	—	—	0.20

Figure 3.7-1 Package Dimensions

REVISION HISTORY	RZ/V2N Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	July 31, 2024	—	First edition issued
1.10	Feb 28, 2025	Section 1 Overview	
		4	Table 1.3-2 Accelerator Engines Video Codec Unit: The description, modified
		5	Table 1.3-3 On-chip SRAM and External Memory Interfaces Note 1, added
		Section 2 Pin	
		37	Table 2.2-1 List of External Pins Note 11, added
		38	2.2.2 List of Multiplexed Functional Pins The main text, modified
		46	Table 2.3-1 List of Pin Functions (1/7) BOOTPLLCA_1, BOOTPLLCA_0: The function, modified (BOOTPLLCA[1:0] → BOOTPLLCA_[1:0])
		49	Table 2.3-1 List of Pin Functions (4/7) PCIE_TXDPL0, PCIE_TXDNL0, PCIE_TXDPL1, PCIE_TXDNL1, PCIE_RXDPL0, PCIE_RXDNL0, PCIE_RXDPL1, PCIE_RXDNL1, PCIE_REFCLKP0, PCIE_REFCLKN0, PCIE0_RSTOUTB: The function, modified
		Section 3 Electrical Characteristics	
		53	Table 3.1-1 Absolute Maximum Ratings Notes 3 and 5, modified
		60	Figure 3.3-2 Power-On/Power-Off Sequence (CM33 Boot) QRESN, modified Note, modified (The clock settling time → The clock stabilization time) Note, added
		63	Figure 3.3-3 Power-On/Power-Off Sequence (CA55 Boot) QRESN, modified Note, modified (The clock settling time → The clock stabilization time) Note, added
		65	Figure 3.3-4 Power-On Sequence (CM33 Boot Mode) Note, modified (The clock settling time → The clock stabilization time)
		69	Figure 3.3-6 Power-On Sequence (CA55 Boot Mode) Note, modified (The clock settling time → The clock stabilization time)
		76	Table 3.4-2 DC Characteristics Notes 2, 3, 4, 7, 8, 9, 10, 11, 12, and 13, modified
		77	3.5 AC Characteristics Conditions, modified
		79	Table 3.5-4 Watchdog Timer Timing Note 1, modified
		80	3.5.5 DMAC Timing, added
		86	3.5.9 Ethernet Interface Timing Conditions, modified Drive strength, added
		86	Table 3.5-12 Ethernet Interface Timing (n = 0, 1) ETn_TXD0 to ETn_TXD3, ETn_TXCTL_TXEN, ETn_TXER output delay time: The min. value, modified Note 1, added

Rev.	Date	Description	
		Page	Summary
1.10	Feb 28, 2025	89	Table 3.5-13 xSPI Timing (1/2) Data input setup time (to DS), Data input hold time (to DS), Data output setup time (to CK), and Data output hold time (to CK): The min. value, modified
		90	Table 3.5-13 xSPI Timing (2/2) CS low to DS low: The max. value, modified Notes 2, 3, and 4, modified Notes 5 and 6, added
		93	3.5.14 Serial Communications Interface (RSCI) Access Timing Drive strength, modified
		94	Table 3.5-14 RSCI Timing (2/2) RSCI (Clock sync, Simple SPI) and SCK clock rise/fall time, deleted RSCI (Clock sync, Simple SPI), Input clock rise time, Input clock fall time, Output clock rise time, and Output clock fall time, added Note, modified Notes 1 and 2, modified
		95	Figure 3.5-23 RSCI Simple SPI Mode Clock Timing, modified
		98	Table 3.5-15 RSPI Timing SSL Activation to Data Output Delay, added Notes 2, 3, and 4, modified
		99	Figure 3.5-28 RSPI Clock Timing, modified Figure 3.5-29 RSPI Timing (Master, Motorola RSPI, CPHA = 0), modified
		103	Table 3.5-16 RIIC Timing Note 2, modified
		105	Table 3.5-17 I3C Timing Note 1, modified
		106	Table 3.5-18 IIC Timing (Fast-mode+) Note 1, modified
		107	Table 3.5-19 IIC Timing (HS mode) SCL3n cycle time: The min. values under “Cb = 100 pF” and “Cb = 400 pF”, modified Note 1, modified
		109	Table 3.5-20 I3C Timing (Open Drain Timing Parameters) SCL3n clock High period: The min. value and note, modified Clock before STOP (P) condition: The min. value, modified Notes 3 and 4, added
		110	Table 3.5-21 I3C Timing (Push-Pull Timing Parameters for SDR) SCL3n clock High period for Mixed Bus, added Note 3, added
		118	Table 3.5-23 A/D Converter Trigger Timing Note 1, modified
		119	3.5.20 SSIU Timing Condition, modified Drive strength, added
		119	Table 3.5-24 SSIU Signal Timing Note 2, added
		122	3.5.21 PDM Timing Conditions, modified Output load conditions, deleted Drive strength, added
		122	Table 3.5-25 PDM Interface Timing Note 1, modified Note 2, added

Rev.	Date	Description	
		Page	Summary
1.10	Feb 28, 2025	127	Table 3.6-2 Recommended External Input Resistance Item, modified

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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